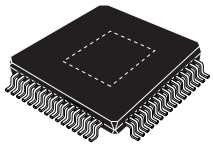
L9907

Automotive FET driver for 3 phase BLDC motor

Datasheet - production data



TQFP64 (exposed pad down)

GAPGPS00129

Features

- AEC-Q100 qualified
- Supply voltage from 4.2V to 54 V for working in single (12 V systems), double (24 V systems) and 48 V battery applications
- The device can withstand -7 V to 90 V at the FET high-side Driver pins
- Low standby current consumption
- 3.3 V internal regulator supplied by Vcc pin
- Boost regulator for full Rdson down to 6 V and over voltage protection
- 3 low-side + 3 high-side drivers
  - PWM operation up to 20 kHz
  - Gate driver current adjustable via SPI in 4 steps. Range set via external resistor. Maximum gate controlled current 600 mA
  - Source connection to each MOSFET
- Input pin for each gate driver
- 2-differential current sense amplifiers:
  - Output offset selectable via SPI (0.2*V_{cc} offset for ground shunt resistors connection, 0.5*V_{cc} offset for phase shunt resistors connection)
  - All the amplifier gain factors are programmable (10, 30, 50, 100)

8 MHz, 16-bit SPI

- Full diagnostic
- Programmable parameters:
  - Cross conduction dead time with a fixed minimum value
  - 4 current steps driving the PowerMOS gates (25%, 50%, 75%, 100%)
  - Phase or ground selection of current sense amplifier
  - Gain values for the current sense amplifiers
  - Zero current output voltage (offset) for the current sense amplifiers
  - Over voltage threshold selection for single or double battery operation
  - Short circuit detection thresholds for the low-side and the high-side MOSFETs (drain to source voltage monitor).

Protection and diagnostic

- FET driver:
  - FET driver supply Undervoltage (UV) diagnostic;
  - Gate to source output voltage limit;
  - Gate to source passive switch off.
- Power supply pins V_B and V_{CC}:
  - Overvoltage (OV), Undervoltage (UV) diagnostic and protection
- All logic pins withstand 35 V
- Power MOSFET drain to source voltage drop measurement for overcurrent protection
- Over-temperature diagnostic and shutdown
- Fault status flag output

Table 1. Device summary

Order code	Package	Packing
L9907	TQFP64 (10x10x1.0 mm)	Tray
L9907TR		Tape & reel

This is information on a product in full production. www.st.com

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1 Description

L9907 is a smart power device realized in STMicroelectronics advanced BCD-6s technology. It is able to drive all PowerMOS transistors for 3-phase BLDC motor applications. The circuit is suitable to operate in environments with high supply voltage such as double battery. Supply related pins are capable of withstanding up to 90 V.

Moreover, the device is able to control the six pre-driver channels independently. In this way it is possible to implement all kinds of electric motor control strategy.

The integrated boost regulator provides sufficient gate charge for all PowerMOS down to a battery voltage of 6 V. All pre-drivers have dedicated connections with the MOSFET sources. The device offers programmability for a base gate output current via an external resistor. Moreover, via SPI, it is possible to select among 4 gate output current levels even while the application is running. All channels are protected against short circuit and the device is protected against overtemperature conditions. Moreover, the boost converter implements an over voltage protection to allow safe functionality of pre-drivers in all battery voltage conditions. During over voltage conditions, BST_C voltage is limited by temporarily switching off the boost regulator and pre-drivers are allowed to operate. Boost will be self re-enabled as soon as the output voltage decreases to an acceptable value.

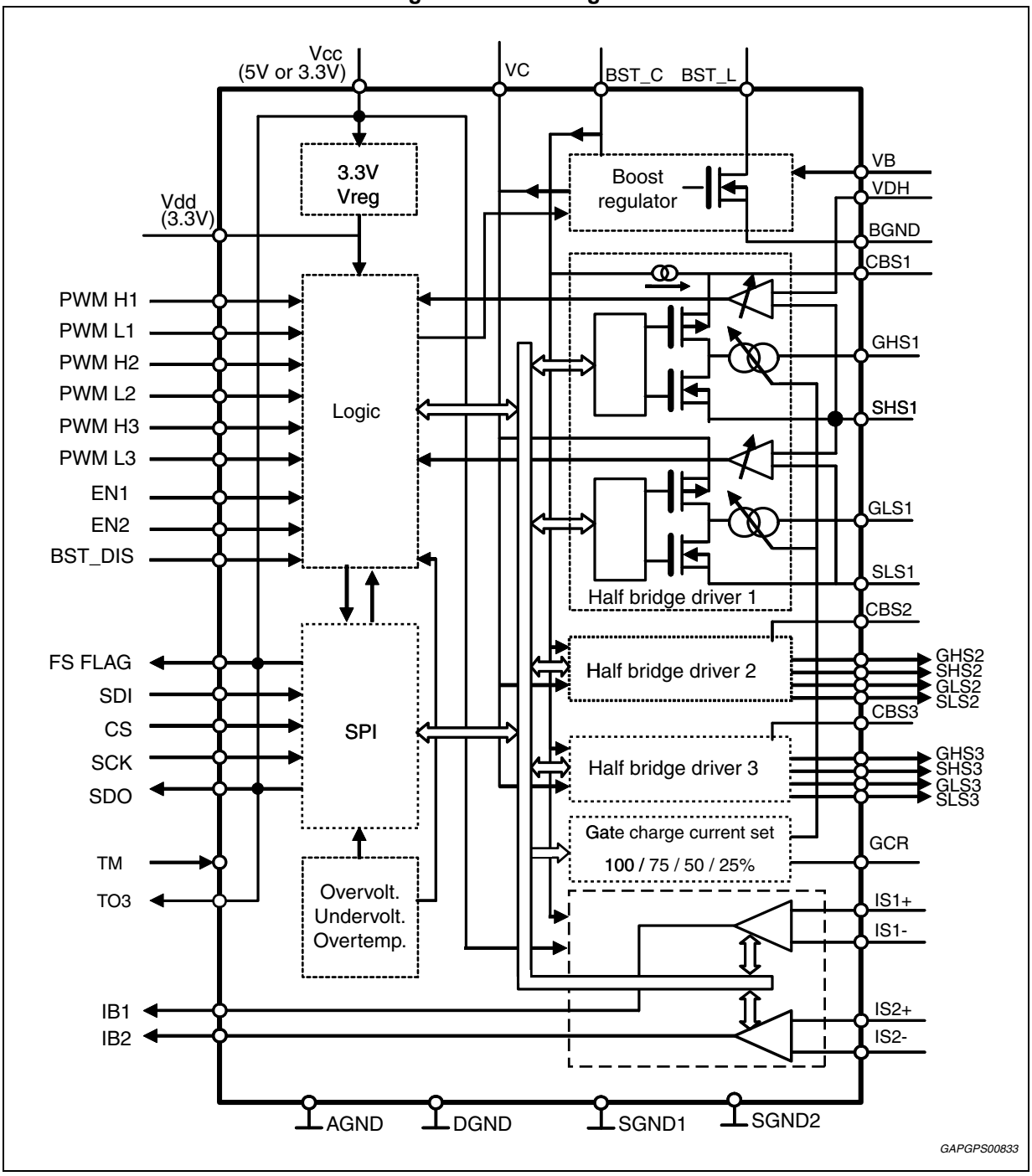
The device is equipped with 2 current sense amplifiers. Both have SPI selectable amplifier gain (10, 30, 50 and 100) and output offset voltage level in order to allow max flexibility for phase or ground current sense strategy. All I/O pins are 35 V compatible. Full diagnostic is available through SPI. The device is available in TQFP64.

The device is protected against Shoot Through events.

2 Block diagram and pin description

2.1 Block diagram

Figure 1. Block diagram



2.2 Pin description

Figure 2. Pin connection diagram

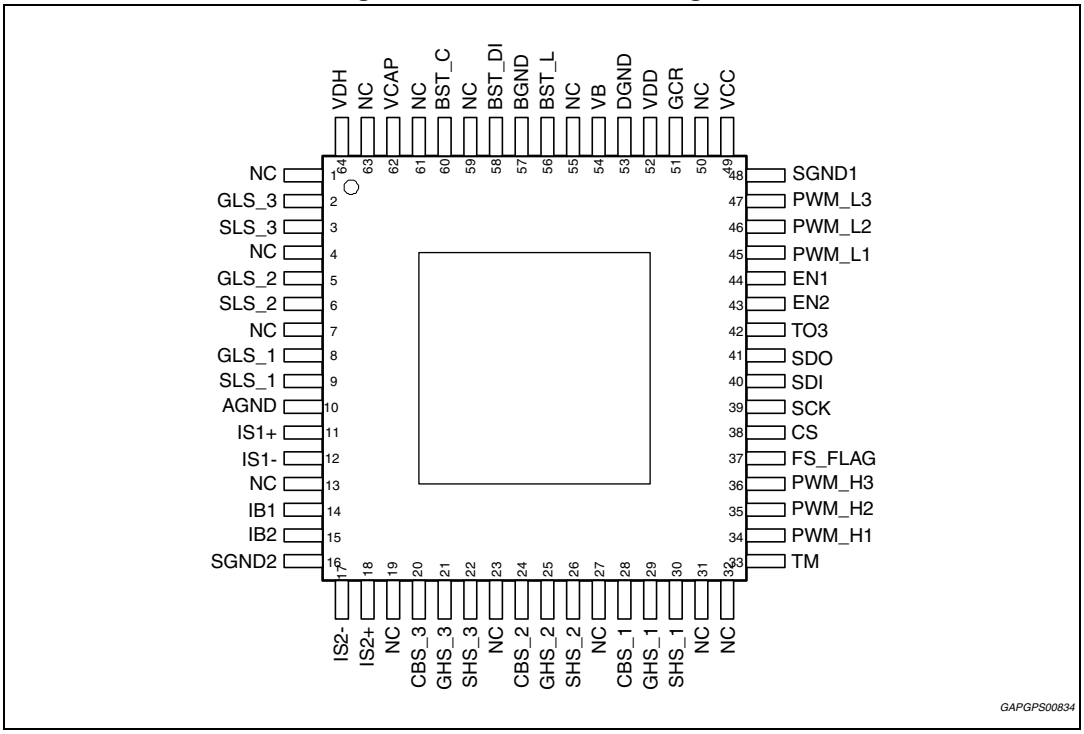


Table 2. Pin function

Pin #	Pin name	Description	I/O Type
1	NC	NC	-
2	GLS_3	Gate connection for low-side MOSFET, phase 3	O
3	SLS_3	Source connection for low-side MOSFET, phase 3	I
4	NC	NC	-
5	GLS_2	Gate connection for low-side MOSFET, phase 2	O
6	SLS_2	Source connection for low-side MOSFET, phase 2	I
7	NC	NC	-
8	GLS_1	Gate connection for low-side MOSFET, phase 1	O
9	SLS_1	Source connection for low-side MOSFET, phase 1	I
10	AGND	Analog ground	GND
11	IS1+	Positive input for current sense amplifier 1	I
12	IS1-	Negative input for current sense amplifier 1	I
13	NC	NC	-
14	IB1	Output for current sense amplifier 1 (Test mode digital output #1)	O
15	IB2	Output for current sense amplifier 2 (Test mode digital output #2)	O
16	SGND2	Substrate (and ESD_GND) connection 2	GND

Table 2. Pin function (continued)

Pin #	Pin name	Description	I/O Type
17	IS2-	Negative input for current sense amplifier 2	I
18	IS2+	Positive input for current sense amplifier 2	i
19	NC	NC	-
20	CBS_3	Bootstrap capacitor for high-side MOSFET, phase 3	I
21	GHS_3	Gate connection for high-side MOSFET, phase 3	O
22	SHS_3	Source connection for high-side MOSFET, phase 3	I
23	NC	NC	-
24	CBS_2	Bootstrap capacitor for high-side MOSFET, phase 2	I
25	GHS_2	Gate connection for high-side MOSFET, phase 2	O
26	SHS_2	Source connection for high-side MOSFET, phase 2	I
27	NC	NC	-
28	CBS_1	Bootstrap capacitor for high-side MOSFET, phase 1	I
29	GHS_1	Gate connection for high-side MOSFET, phase 1	O
30	SHS_1	Source connection for high-side MOSFET, phase 1	I
31	NC	NC	-
32	NC	NC	-
33	TM (1)	Test mode enable input	I
34	PWM_H1	PWM command input for high-side phase 1	I
35	PWM_H2	PWM command input for high-side phase 2	I
36	PWM_H3	PWM command input for high-side phase 3	I
37	FS_FLAG	Fault status flag output	O
38	CS	SPI chip select input	I
39	SCK	SPI serial clock input	I
40	SDI	SPI Serial data input	I
41	SDO	SPI serial data output	O
42	TO3	Test output	O
43	EN2	Enable Input 2 (ANDed with EN1 to enable any gate drive output).	I
44	EN1	Enable Input 1 (ANDed with EN2 to enable any gate drive output).	I
45	PWM_L1	PWM command input for low-side phase 1	I
46	PWM_L2	PWM command input for low-side phase 2	I
47	PWM_L3	PWM command input for low-side phase 3	I
48	SGND1	Substrate (and ESD_GND) connection 1	GND
49	Vcc	5 V / 3.3 V power supply input	I
50	NC	NC	-
51	GCR	Connection to resistor for current selection of gate driver	O

Table 2. Pin function (continued)

Pin #	Pin name	Description	I/O Type
52	Vdd	3.3 V power supply output (for IC internal purpose only)	O
53	DGND	Digital ground	GND
54	VB	Protected battery monitor	I
55	NC	NC	-
56	BST_L	Boost regulator inductance connection	O
57	BGND	Boost ground	GND
58	BST_DIS	Boost disable	I
59	NC	NC	-
60	BST_C	Boost regulator capacitance connection	I
61	NC	NC	-
62	VCAP	Decoupling capacitor for power supply of low-side drivers	I
63	NC	NC	-
64	VDH	High-side drain voltage sense	I

1. TM pin has to be connected to ground in the application.

3 Functional description

3.1 Power supply VB, VCC

Voltage present at VB and VCC pins is monitored in order to inhibit driver and/or boost functionality in case of under/over voltage detection. A VCC over voltage self test is embedded for safety integrity check: VCC over voltage threshold can be reduced on purpose to a level that is always triggered with nominal values on VCC rail. The device is self protected in case of ground disconnections versus both SGNDx pins. SGND1 and SGND2 pins are internally shorted and connected to substrate: at least one of these pins must be connected to board ground. In case of AGND loss, a dedicated comparator will lead to a POR state for logic, where boost regulator and MOSFET drivers are disabled. This fault doesn't set any SPI error bit. In case of DGND loss the device is automatically disabled: MOSFET drivers go in tri-state condition and external FETs are kept off using integrate passive pull down. In case of BGND ground loss the boost regulator cannot work properly: the effect is an undervoltage on HS and/or LS side gate voltage monitor.

The ground reference for all the voltages and thresholds available in the device is AGND. The Exposed Pad (EP) is mainly used for thermal dissipation. It should be grounded and connected together with SGNDx pins.

3.2 Voltage regulator VDD

The internal 3.3 V voltage regulator is used to supply the internal logic and all internal blocks. For stability reasons a 100 nF capacitor has to be connected to VDD pin. This regulator is to be intended for IC internal use only. Suggested limits for external capacitor are min = 100 nF -20% ma x= 220 nF +20%. All tests are performed with a 100 nF capacitor, unless otherwise specified.

3.3 EN1 and EN2 pins (ENABLE)

To enable the gate driver functionality EN1 and EN2 have to be pulled high. These pins are by default internally logically ANDed. In case REGOFF_EN bit in CMD4 SPI frame is set to 1 (refer to SPI mapping, *Table 20*), EN1 and EN2 have different meanings: EN2 stays the same as a gate driver functionality enabler, while EN1 will also become an enabler for all the regulators supplying the pre-driver circuitries. In this way, EN1 becomes a safety control pin that implements an additional switch-off path.

These pins are also used to enable the SPI write to CMD1 and CMD4. These registers contain gate driver sensitive to failure management bits which just can be written when at least one of the ENx pins is pulled low (gate driver disabled).

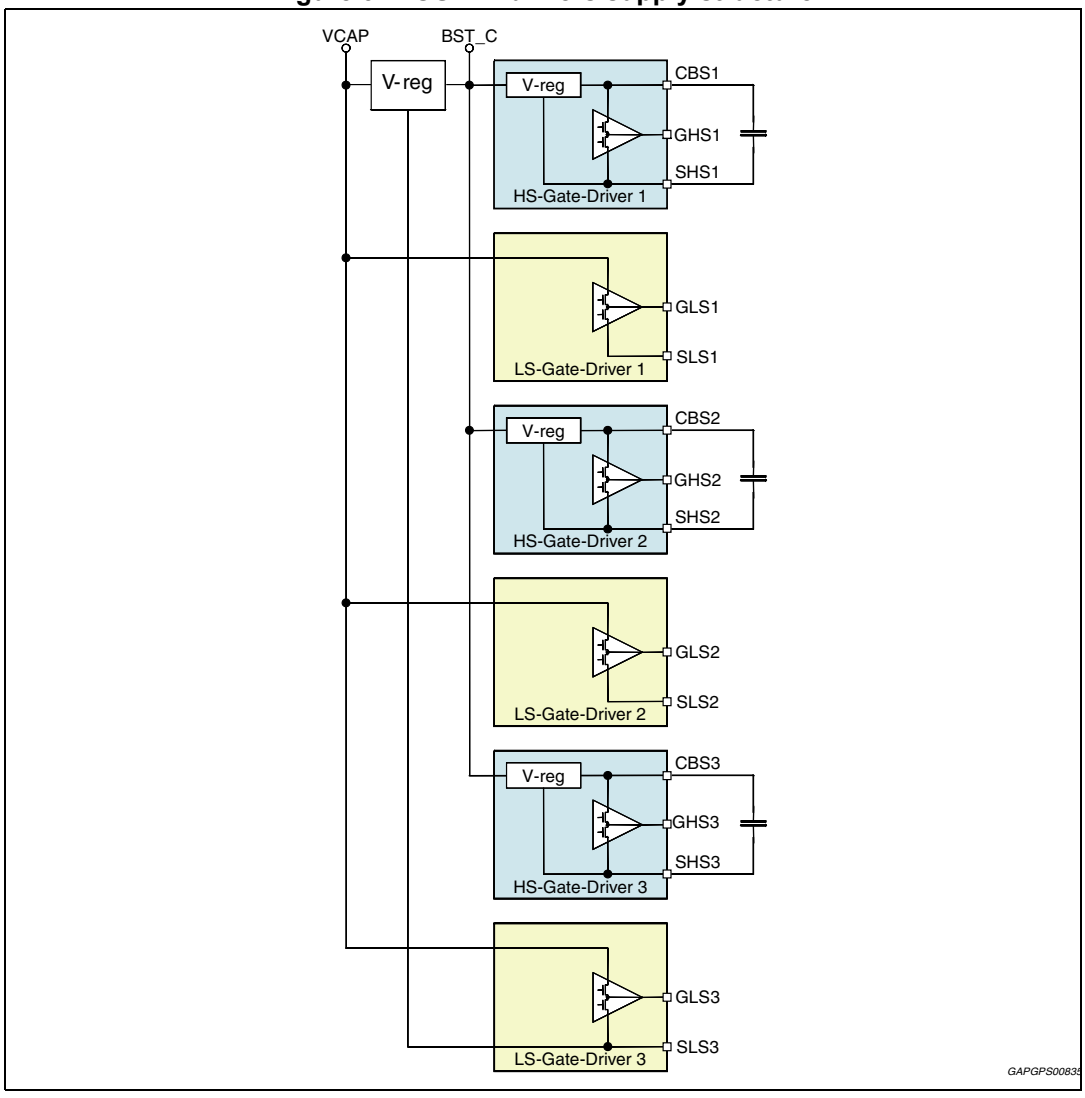
Nevertheless the pins are used as well to reactivate the gate driver in case of device internal switch off. Therefore a low cycle of at least 3µs has to be applied after fault condition is removed to one or both of the ENx pins.

On both pins internal pull down currents are implemented.

3.4 Boost converter

The purpose of the Boost converter is to generate a voltage around 10 V higher than the one present at VDH monitor pin. This voltage is used to supply HS drivers (through dedicated regulators) and LS drivers (through VCAP regulator). The regulated voltage is present at BST_C pin. BST_L pin is the drain of an integrated NDMOS switch. VCAP regulator is a current limited voltage regulator, fed by Boost and referred to SLS3 voltage, used to supply LS drivers. Each HS driver has a current limited voltage regulator that is fed by Boost, referred to SHSx pins and with regulated voltage present at CBSx pins. These regulators limit VGS of the external FETs. Overvoltage at BST_C pin (e.g. due to low current demand) is limited by skipping turn on pulses until over voltage condition is removed. A fixed voltage threshold on BST_C is implemented, in order to avoid the boost voltage exceeding a safety level in case of high voltage on VDH monitor pin. In case the user would not need this over voltage protection (e.g. for applications where high voltage is present on the VDH rail), L9907 provides a disabling bit in CMD3 SPI command (DIS_BST_{OV}). The Boost converter is disabled in case of validated Fault (see *Table 3*) and reactivated by fault removal and cleared after SPI reading.

Figure 3. MOSFET drivers supply structure



In case Boost converter is disabled, but voltage at BST_C pin is present, Current Sense Amplifiers are active but with degraded performances at least in common mode dynamic range. In order to improve EMC behaviour an external RC series snubber can be added between BST_L and BGND pins. RC~1/(6.28*fSW_BST).

3.4.1 BstDis (boost disable) function

In case noise-free CSA measuring is needed, a special functionality that temporarily disables Boost regulator is implemented, with the purpose to reduce PCB coupling between CSA output and boost PCB metal stripes that can act as antennas. Once BST_DIS pin is asserted, boost regulator is disabled starting from the next complete boost cycle (maximum delay T_BOOST_OFF_FILT).

Boost is re-enabled in two ways:

- internal timer expired (T_BOOST_OFF_MAX time is reached)
- BstDis pin deasserted

In both cases boost starts working again from the beginning of the next complete boost cycle.

T_BOOST_OFF_MAX = $6*T_{BOOS}T = 96*T_{CK}$

T_BOOST_OFF_FILT = $3*T_{CK}$ min, $21*T_{CK}$ max

Figure 4. Case of T_BOOST_OFF < T_BOOST_OFF_MAX

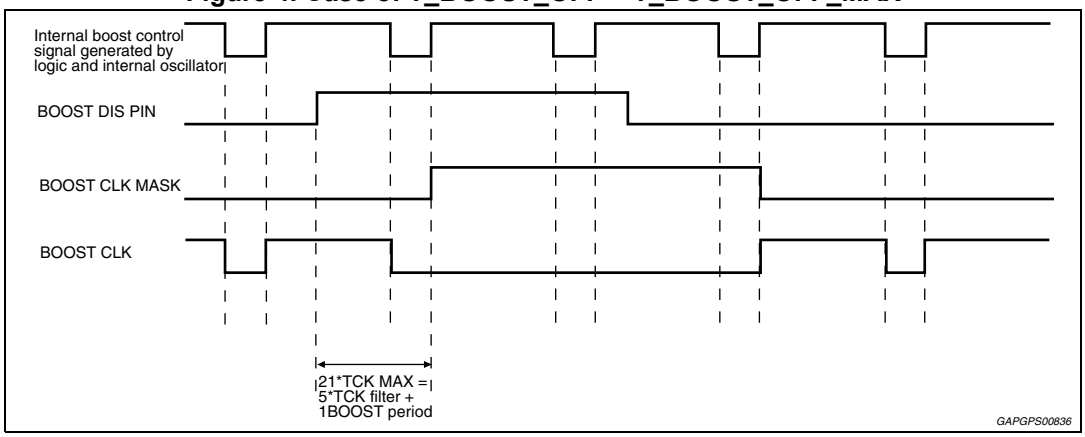
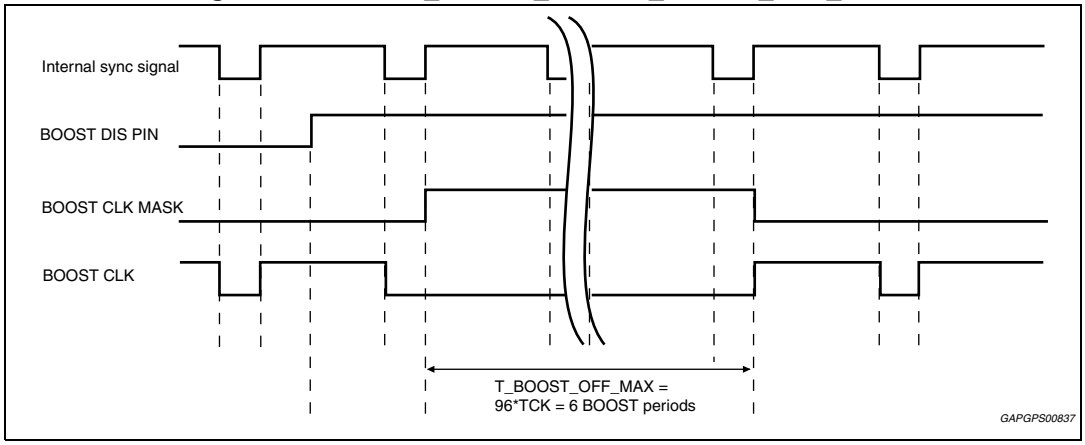


Figure 5. Case of T_BOOST_OFF > T_BOOST_OFF_MAX



When BST_DIS_EN bit of CMD2 SPI frame is set to 1 (refer to SPI mapping, *Table 20*), BST_DIS becomes a full-time control of the boost operation: the boost will be disabled as long as the BST_DIS pin is high. This implements a boost permanent disabler that can be used for different reasons, e.g. to allow more precise and less noisy measurements, to decrease power dissipation or current load on battery in all conditions when the boost is not strictly necessary.

3.5 MOSFET drivers

MOSFET drivers are programmable current mirrors used to limit gate charge/discharge current without gate series resistors (which can be used anyway). Programmability has got two degrees of freedom: SPI programmability (25, 50, 75, 100% of max. available current IG) for MOSFET gate current adjustment during running application and via external resistor at GCR pin to adjust the gate current among different applications. External MOSFETs are protected against over current in on-state monitoring their Vds voltage. Maximum Vgs of external MOSFETs is limited using VCAP regulator for LS drivers and dedicated floating regulators referred to sources for HS drivers.

3.5.1 GCR pin

At GCR pin a resistor has to be connected which defines in combination with the IGx SPI bits the gate current for charge and discharge.

Minimum value for GCR resistor is GCR(min) = 1 kΩ - 10% (maximum allowable gate current), maximum is GCR(max) = 22 kΩ +10% (minimum allowable gate current), but with degraded precision performances with GCR > 6 kΩ + 10%. Tested values are GCR = 1 kΩ and GCR = 6 kΩ

GCR pin circuitry implements a open/short protection in case of a too high/low resistive load connected to it. If one of the above conditions occurs, the device switches to an internally generated current, equivalent to approximately 15 kΩ. The current reference can be switched to the internal reference by using the GCR_INT_I bit of CMD2 frame (refer to SPI mapping, *Table 20*); this can be used when a reduced power dissipation is needed.

3.5.2 Shoot through protection

Shoot through protection's aim is to avoid destructive cross current conduction between high-side and low-side FETs of same phase in case of unwanted condition when PWM_Hx and PWM_Lx signals are set to logic '1' at the same time (e.g. because of a controller fault). With every activation of either PWM_Hx or PWM_Lx the cross current protection time is activated and switches off the corresponding half bridge for the programmed Dead time. The shoot through condition is validated via an up-down counter which is proportional to the programmed dead time. With this feature, continuous activation of HS and LS and also high frequency oscillations of the PWMx input signals (HS and LS) are detected and the shoot through failure state is set. If the fault condition is validated, all external FETs are switched OFF and FS_FLAG is asserted low. No SPI SDO diagnostic bit is set, since hypothesis is that the controller is not able to work properly. In case the SHT_PH bit of CMD2 SPI frame would be set to 1 (refer to SPI mapping, *Table 20*), the device allows the switching off of the only phase for which the shoot through occurred. The phase that experienced the fault is reported on DIAG2 SPI frame (SDO bits B<2:0>). In order to re-enable FET pre-drivers, at least one Enable signals EN1 or EN2 must be toggled. In order to unlatch also FS_FLAG status a SPI communication with diagnostic frame must be performed.

3.5.3 Drain source monitoring

To monitor the external MOSFET a Drain Source monitoring for all HS and LS is implemented. In case the drain source voltage exceeds a certain threshold (e.g. MOSFET short) during gate ON mode, all drivers will be disabled and the fail will be reported via FS_FLAG and SPI. In case the ShortPH bit of CMD2 SPI frame would be set to 1 (refer to SPI mapping, *Table 20*), the device allows the switching off of the only phase for which the drain-source short occurred.

3.6 Current sense amplifier (CSA)

Current Sense Amplifier converts and amplifies (with a 4-step programmable gain) current information through external shunt in a voltage signal. Each CSA can be configured for one side ("Ground") or both sides ("Phase") current flow through the shunt. Indeed the shunt can be referred to ground or floating. Current Sense Amplifier is active if IC is active (VCC and VDD present and within spec range), despite of EN status. In case Boost converter is disabled, but voltage at BST_C pin is present, Current Sense Amplifiers work but with degraded performances at least in common mode dynamic range.

3.7 General SPI usage

For device programmability a four-wire SPI is used. The device acts as SPI slave. Data will be latched on the negative clock edge and shifted out on the positive edge (µC setting: CPHA =1; CPOL = 0).

To perform an SPI write the WE bit has to be set and a correct ODD parity bit has to be written.

A data read out is always performed on the following SPI frame (after power-up CMD0 is read). That means sending data to a certain register will lead to shift out the content of the addressed register in the following SPI frame. In case of wrong SPI communication (e.g. due to stuck at 0 or at 1 of SDI) the current command is rejected and an error message (0xB001) is presented as SDO response at the following SPI cycle.

3.8 Device and FET fault handling

All internal fault events are filtered to achieve noise immunity. After filter-time they are latched in the corresponding SPI register and the FS_FLAG (active low) becomes low. In case the related driver-disable-bit (EN_x) is set, additionally the gate driver will be disabled and actively discharged (see: Fault Effect enabling; *Table 32* and *29*). In case EN_x is disabled the µC takes fully response to react on any errors immediately indicated by the FS_FLAG. Neither the boost nor the FET drivers will be disabled on deselected faults.

Table 3. Device and FET fault handling

Fault	Diagnosis	Device action when EN_x enabled	Exit from fault condition
Overtemperature	FS_FLAG = low; THSD SPI bit set	FET driver functionality disabled	– Remove fault => auto recovery – SPI read clears the Fault Flags and sets FS_FLAG to high
VB or VCC over- or undervoltage	FS_FLAG = low; VBOV or VBUV or VCCOV or VCCUV SPI bit set	FET driver functionality and Boost disabled	– Remove fault => auto recovery of Boost – EN cycling toggle reactivates the FET driver – SPI read clears the Fault Flags and sets FS_FLAG to high
Boost HS or LS undervoltage	FS_FLAG = low; UV_HS or UV_LS SPI bit set	FET driver functionality disabled	– Remove fault – EN cycling toggle reactivates the FET driver – SPI read clears the Fault Flags and sets FS_FLAG to high
VSC_HSx overcurrent	FS_FLAG = low; VSC_HSx SPI bit set	FET driver functionality disabled	– Remove fault – EN cycling toggle reactivates the FET driver – SPI read clears the Fault Flags and sets FS_FLAG to high
VSC_LSx overcurrent	FS_FLAG = low; VSC_LSx SPI bit set	FET driver functionality disabled	– Remove fault – EN cycling toggle reactivates the FET driver – SPI read clears the Fault Flags and sets FS_FLAG to high

3.8.1 SPI and PWM faults

Table 4. SPI and PWM faults

Fault	Diagnosis	Device Action	Exit from Fault Condition
SPI Error (wrong address access; parity error; SCK count error)	SPI_Error bit set and 0xB001 return frame	Faulty SPI frame is ignored	-
PWM_Hx and PWM_Lx shoot through protection	FS_FLAG = low;	FET driver functionality disabled	– Remove fault – EN cycling toggle reactivates the FET driver – SPI read sets FS_FLAG to high

4 Electrical specifications

4.1 Maximum operating ranges

The device may not operate properly if maximum operating condition is exceeded.

Table 5. Maximum operating conditions

Symbol	Parameter	Value	Unit
V_B	Protected battery monitor voltage	4.2 to 54(1)	V
V_{CC}	5 V / 3.3 V power supply	3 to 5.5	V
V_{DH}	High-side drain voltage sense	4.2 to 54(1) (2)	V
SHS_1 to 3	High-side source voltage	-7 to 54(1) (3)	V
ISxx	Current sense amplifier input pin voltage	-2 to V_{DH} +4(4)	V

1. Maximum operating voltage is 75 V in dynamic conditions.
2. V_{DH} maximum operating voltage range is limited by V(BST_C)-15 V.
3. SHS maximum operating voltage range is limited by V(CBSxmax)-15 V.
4. Maximum operating voltage is V_{DH} +20 V in dynamic conditions.

4.2 Absolute maximum ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

Table 6. Absolute maximum ratings

Parameter	Condition	Min	Max	Unit
Monitor supply pin	Pin VB	-0.3	75	V
		-10	+10	mA
Power supply pins	BST_C	-0.3	90	V
		-100	100	mA
	Pin: BST_L	-0.3	90	V
		-100	100	mA
	Pin Vcc	-0.3	35	V
		-10	25	mA
	Pin Vdd	-0.3	4.6	V
		-10	15	mA
	Pin VCAP	-0.3	20	V
		-100	100	mA
Miscellaneous Analog/Digital I/O pins	PWM_H1 to 3, PWM_L1 to 3, IB1, IB2, EN1, EN2, FS_FLAG, BST_DIS,TM, CS, SCK, SDI, SDO, TO3	-0.3	35(1)	V
		-10	10	mA

Table 6. Absolute maximum ratings (continued)

Parameter	Condition	Min	Max	Unit
Gate current selection pin	Pin GCR	-0.3	4.6	V
		-10	+10	mA
Current sense amplifier pins	IS1+,IS1-,IS2+,IS2-	-7	75	V
		-10	10	mA
Differential voltage between ISx +/-	Abs |ISx+ - ISx-|	-	15	V
High-side drain sense	Pin VDH	-4	75	V
		-10	10	mA
FET-driver pins	HS Bootstrap Cap pins: CBS_1 to 3	-0.3	90	V
	Differential gate to source HS pins: V(GHS_x) - V(SHS_x), x = 1 to 3(2)	-0.3	20	V
	Source HS pins: SHS_1 to 3	-7	75	V
	Source LS pins: SLS_1 to 3	-7	10	V
FET driver pins	Differential gate to source LS pins: V(GLS_x) - V(SLS_x), x = 1 to 3(2)	-0.3	20	V
Current sense amplifier differential voltage	BST_C-ISxx	-0.3	90	V
GND pins	Pins BGND and DGND	-0.3	4.6	V
	Pin AGND and EP	-0.3	0.3	V

1. In standard battery level application (12 V systems) the I/O pins and Vcc pin can stand a short to battery up to 35 V. A short to 35 V battery on any I/O pin also forces the Vcc to approximately 35 V. Care must be taken in order to avoid that under such conditions the Vcc pin is strongly pulled down to 5 V (or 3.3 V) with a current exceeding the absolute maximum ratings level.
2. Negative AMR is -0.3 V or -20 mA.

4.3 ESD protection

Table 7. ESD protection

Parameter	Condition	Min	Max	Unit
Logic and power pins	Human body model	-2	2	kV
FET driver pins	Human body model	-2	2	kV
All pins but corner pins	Charge device model	-250	250	V
Corner pins	Charge device model	-750	750	V

HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114_A. HBM with all unzapped pins grounded.

4.4 Temperature ranges and thermal data

Table 8. Temperature ranges and thermal data

Symbol	Parameter	Min	Max	Unit
T_j	Operating junction temperature	-40	150	°C
	100 hours over lifetime temperature (1)	-	175	°C
T_{stg}	Storage temperature	-55	150	°C
T_{ot}	Thermal shutdown temperature	175	205	°C
T_{hys}	Thermal shutdown temperature hysteresis(2)	10	-	°C
$R_{th\ j\text{-}amb}$	Thermal resistance junction-to-ambient (3)	-	23	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-to-case	-	3	°C/W

1. Functionality is guaranteed, the specified limits may be exceeded.
2. Guaranteed by design.
3. IC soldered on 2s2p PCB thermally enhanced.

4.5 Electrical characteristics

All voltages referred to ground (SGNDx ground) and currents are assumed to be positive when current flows into the pin.

4.5.1 Supply

The device is operated in the specified operating range, unless otherwise specified (V_{CC} = 3.20 V to 5.25 V, VB = 4.2 V to 54 V, T_j = -40 °C to 150 °C).

Table 9. Supply electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_B	Operating supply voltage range	-	4.2	-	54	V
VB OV_1	Overvoltage threshold for double battery applications (L9907)	VB_{OV2},VB_{OV1}= 01	36	-	42	V
VB OV_2	Overvoltage threshold for single battery application	VB_{OV2},VB_{OV1}= 10	27.5	31	34.5	V
Td VB	Overvoltage time delay for noise rejection	(guaranteed through scan)	30	-	80	µs
VB UV	Undervoltage disable threshold	-	4.2	4.6	5	V
Td $_{UV}$	Undervoltage time delay for noise rejection	(guaranteed through scan)	30	-	80	µs
$I_{VB(dis)}$	Supply current	VB= 13V, V_{cc} < 0.5 V, room temperature	-	1	10	µA

Table 9. Supply electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{VB}	VB supply current (1) (2)	VB= 13V, Vcc= 3.3V, open outputs, fPWM =0	-	-	10	mA
I_{BST_C}		VB = 13 V, drivers off, boost off	-	-	10	mA
V_{CC}	Operating supply voltage range	-	3.20	-	5.25	V
Icc	Vcc DC supply current	VB= 13 V, Vcc = 3.3 V	-	-	20	mA
		VB= 13 V, Vcc = 5 V	-	-	25	mA
Vcc UV	Vcc undervoltage monitor	-	2.9	3.05	3.2	V
VCC OV 3.3V	Vcc overvoltage monitor for 3.3V supply system	VCC_{OV2},VCC_{OV1}=10, Default on 3.3V	3.4	3.55	3.7	V
VCC OV 5V	Vcc overvoltage monitor for 5V supply system	VCC_{OV2},VCC_{OV1}=01	5.45	5.75	6.0	V
VCC OV test	Vcc overvoltage monitor for safety integrity check	VOV_{TST} = 1 (CMD2, B6)	2.6	2.8	3.0	V
Td Vcc	Overvoltage and undervoltage time delay for noise rejection	(guaranteed through scan)	30	-	80	µs
VDD UV	VDD undervoltage monitor and reset	-	2.5	2.7	2.8	V
AGNDloss	AGND loss threshold	Ramp AGND starting from 0 V	150	220	290	mV

1. The following is the estimated V_B supply current (I_{VB}) given power supply voltage level (V_B), PWM frequency (f_{PWM}) and gate charge (Q) for each MOSFET (It represents the current that flows through external inductor to recharge Clsd and high-side Cbs capacitors):

$$I_{VB} = 7.2\ Q\ f_{PWM}\left(1+\frac{V_{boost}-V_B}{V_B}\right) + 6\frac{2.81}{GCR}\left(1.5+\frac{V_{boost}}{0.85\ V_B}\right) + I_{BST\_C}$$

2. The following is the estimated VB Power Dissipation (P_{diss}, it cannot be calculated as VB times IVB) given power supply voltage level (VB), PWM frequency (f_{PWM}) and gate charge (Q) for each MOSFET:

$$Pdiss = 3.6\ Q\ f_{PWM}\ (V_B + 20V) + V_B\ \ 10mA\ (*)$$

(*) P_{diss} formula is valid in case VB = VDH. In case VDH and VB are different, please consider that VB + 20 V = V(BST_C,max). For the calculation, it is possible to change (VB + 20 V) in (VDH + 20 V) or BST_C voltage have to be measured directly.

4.5.2 Voltage regulator VDD

The device is operated in the specified operating range, unless otherwise specified (V_{CC} = 3.20 V to 5.25 V, VB = 4.2 V to 54 V, T_j = -40 °C to 150 °C).

Table 10. Voltage regulator VDD

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
VDD	-	No external current load	3.0	3.3	3.6	V
T_{wuae}	Wake up time (design info)	Time from V_{CC} to steady state to V_{dd} power on reset release (with 100 nF on V_{dd})	-	-	100	µs

4.5.3 Logic input pins (PWM_H1 to 3, PWM_L1 to 3, SCK, CS, SDI, BST_DIS, EN1 and EN2)

The device is operated in the specified operating range, unless otherwise specified (V_{CC} = 3.20 V to 5.25 V, VB = 4.2 V to 54 V, T_j = -40 °C to 150 °C).

Table 11. Logic I/O pins electrical characteristics

Symbol	Parameter	Test condition	Min	Max	Unit
Vin(HL)	High level input voltage	-	1.9	-	V
Vin(LL)	Low level input voltage	-	-	0.8	V
Vhin	Input voltage hysteresis	-	0.1	-	V
Twuae	Wake up time (design info)	Time from V_{CC} to steady state to V_{dd} power on reset release (with 100 nF on V_{dd})	-	100	µs
$I_{in(PD)}$(1)	PWM_H1 to 3, PWM_L1 to 3, SDI, BST_DIS, EN1 and EN2	V_{in} = 0.8 V	15	45	µA
$I_{in(PU)}$(1)	Input pins pull up current at CS pin	V_{in} = 2 V	-45	-15	µA
td_EN	EN1, EN2 falling edge deglitch time	Delay time from EN=(EN1 AND EN2) falling edge to gate drive switch off (guaranteed through scan)	1.36	3	µs

1. No PU/PD current at SCK pin.

4.5.4 Logic output pins (FS_FLAG, SDO, TO3)

The device is operated in the specified operating range, unless otherwise specified (V_{CC} = 3.20 V to 5.25 V, VB = 4.2 V to 54 V, T_j = -40 °C to 150 °C).

Table 12. Logic output pins (FS_FLAG, SDO, TO3) electrical characteristics

Symbol	Parameter	Test condition	Min	Max	Unit
Vout(HL)	High level output voltage	I_{sink} = -1 mA	Vcc-300mV	-	mV
Vout(LL)	Low level output voltage	I_{source} = 1 mA	-	300	mV

4.5.5 Boost converter

The device is operated in the specified operating range, unless otherwise specified (V_{CC} = 3.20 V to 5.25 V, VB = 4.2 V to 54 V, T_j = -40 °C to 150 °C).

Table 13. Boost converter electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{bst}	Boost regulator output voltage	I_{bst} = 50 mA	VDH+8.5	VDH+10	VDH+15	V
I_{bst}	Boost regulator output current	V_B = 14 V	-	50	70	mA

Table 13. Boost converter electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{LIM}	Boost switch current limit	-	250	-	500	mA
Lbst	Boost regulator inductance	-	-	47	-	µH
Cbst	Boost regulator capacitance	-	-	2	-	µF
f_{SW_BST}	Boost regulator switching frequency	-	280	350	420	kHz
BST_HOV	Boost over voltage threshold	-	63	-	73	V
BST_HOV _HYST	Boost over voltage hysteresis	-	8	-	10	V
T_{bst}	Boost regulator start-up time (design info)	C_{bst} = 2 µF	-	1	-	ms
VCAP	Supply voltage for the LS gate driver	I_{CAP} = 25 mA	V(SLS3) +8.5	-	V(SLS3) +15	V
I_{CAP}	Output current for the voltage regulator for the LS	V_B = 14 V	-65	-	-20	mA
V_{CBSX}	Bootstrap capacitor voltage V(CBSx)-V(SHSx)	V(SHSx) = 14 V, ICBSX = -6 mA	8.5	-	15	V
I_{CBSX}	Bootstrap capacitor charge current at pin CBSx	-	6	-	18	mA

4.5.6 MOSFET drivers

The device is operated in the specified operating range, unless otherwise specified (V_{CC} = 3.20 V to 5.25 V, VB = 4.2 V to 54 V, T_j = -40 °C to 150 °C).

Table 14. MOSFET drivers electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{GS}(L)	Low level output voltage	VGx-VSx @ I= 50 mA	-	100	250	mV
V_{GS}(H)	High level output voltage	VGx-VSx @ I= -5 mA	7.5	-	15	V
I_{Gxx_1}	Turn-on/off current with GCR = 1 kΩ (1)	IG_1,IG_0 = 11 100% Imax	450	600	750	mA
		IG_1,IG_0 = 10 75% Imax	337	450	563	mA
		IG_1,IG_0 = 01 50% Imax	225	300	375	mA
		IG_1,IG_0 = 00 25% Imax	112	150	188	mA
I_{Gxx_2}	Turn-on/off current with GCR = 6 kΩ	IG_1,IG_0 = 11 100% Imax	75	100	125	mA
		IG_1,IG_0 = 10 75% Imax	56	75	94	mA
		IG_1,IG_0 = 01 50% Imax	37	50	63	mA
		IG_1,IG_0 = 00 25% Imax	18	25	32	mA
I_{SLSx}(2)	Low-side driver SLS output current	GCR = 1 kΩ, PWM signals low	-	-	3.3	mA
I_{SHSx}(2)	High-side driver SHS output current	GCR = 1 kΩ, PWM signals low	-	-	3.3	mA
GCR_STG	Gate driver over current protection	-	-	-	880	Ω
GCR_OL	Gate driver under current protection	-	22	-	-	kΩ
RGxxON	ON-resistance of SINK stage	GCR = 1 kΩ, IG_1,IG_0=11, I = 25 mA injected into Gate pin	-	-	5	Ω

Table 14. MOSFET drivers electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
R_{Gxx}	Gate source passive discharge resistance	-	100	200	500	kΩ
t_{GHxlh}	Propagation delay time low to high	V_B = 13.5 V, C_g = 22 nF	-	-	300	ns
t_{GLxlh}	Propagation delay time low to high	V_B = 13.5 V, C_g = 22 nF	-	-	300	ns
t_{GHxhl}	Propagation delay time high to low	V_B = 13.5 V, C_g = 22 nF	-	-	300	ns
t_{GLxhl}	Propagation delay time high to low	V_B = 13.5 V, C_g = 22 nF	-	-	300	ns
f_{PWM}	PWM Switching frequency	-	-	-	20	kHz
Q	Drivable gate charge(3)	VGS = 10 V, 20 kHz	300	-	900	nC
t_{DT}	Dead time (adjustable in 4 steps via 2-bit SPI Register)	DT1, DT0 = 00 (default)	100	-	200	ns
		DT1, DT0 = 01	300	-	500	ns
		DT1, DT0 = 10	700	-	1000	ns
		DT1, DT0 = 11	1000	-	1500	ns

1. Only for turn-on currents with GCR = 1 kW: parameter is tested at hot temperature only; other temperatures are granted by design.
2. I = 400 µA + 2.81/GCR.
3. Design information. The IC does not provide any active internal Gate Charge limit.

Table 15. PowerMOS overcurrent drop voltage sense

Symbol	Parameter	Test condition(1)	Min	Typ	Max	Unit
V_{SC_LS}	Short circuit detection threshold low-side (adjustable in 4 steps via 2 bits SPI register)	SC_LS1, SC_LS0 = 00 (default)	0.4	0.5	0.6	V
		SC_LS1, SC_LS0 = 01	0.7	0.8	0.9	V
		SC_LS1, SC_LS0 = 10	0.9	1	1.1	V
		SC_LS1, SC_LS0 = 11	1.17	1.3	1.43	V
V_{SC_HS}	Short Circuit detection threshold high-side (adjustable in 4 steps via 2 bits SPI register)	SC_HS1, SC_HS0 = 00 (default)	0.4	0.5	0.6	V
		SC_HS1, SC_HS0 = 01	0.7	0.8	0.9	V
		SC_HS1, SC_HS0 = 10	0.9	1	1.1	V
		SC_HS1, SC_HS0 = 11	1.17	1.3	1.43	V
TSCoff	Short Circuit shut down delay (the circuit shuts down by short circuit longer than TSCoff; guaranteed through scan)	Masking time at switch ON	9	12	14(2)	µs
		Filter Time in normal operation	1	-	2	µs
$V_{SC\ TEST}$	Test functions for short circuit detection level (SCDL)(3)	VSC_{TST}=1 (CMD2, B7)	-0.7	-0.5	-0.3	V

1. The accuracy of SC detection thresholds for HS and LS is guaranteed for VB ≥ 6 V. In case VB < 6 V the accuracy for each configuration, both for HS and LS, is 22.5%.
2. The PWM ON time must be longer than this Short Circuit shutdown delay, else the short circuit condition cannot be detected.
3. Security Level test function. If this function is selected via SPI, the short circuit detection threshold is set to the specified negative level. In this way a short circuit is detected even if the current in the external MOSFET is zero, that is Vds=0.

Table 16. Gate voltage monitoring

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$V_{G\ UV\ HS}$	Undervoltage threshold for HS gate driver. It monitors the voltage difference between boost output pin BST_C and HS FET drain connection VDH	V(BST_C)-V(VDH)	4.6	-	6.8	V
$V_{G\ UV\ LS}$	Undervoltage threshold for LS gate driver. It monitors the voltage difference between low-side gate driver supply pin VCAP and LS FET 3 source connection SLS3	V(VCAP)-V(SLS3)	7.4	8.2	9.0	V
$t_{UV\ VG}$	Undervoltage filter time	(guaranteed through scan)	3.5	5	7	µs

4.5.7 Current sense amplifier

The device is operated in the specified operating range, unless otherwise specified (V_{CC} = 3.20 V to 5.25 V, VB = 4.2 V to 54 V, T_j = -40 °C to 150 °C).

Note: Table 17 is referred to bidirectional current measurement (shunt resistors on the phase of the motor).

Table 17. Phase current sense amplifier (SPI select: Offx=1, where x=1,2)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Vin_off	Differential input offset voltage	-	-5	-	5	mV
Vio_step	Calibration step of Differential input offset voltage(1)	-	0.5	1	1.5	mV
VICM	Common mode input voltage range	Operating	-2	-	VB+4	V
		Transient (t < 1 µs)	-7	-	VB+20	V
V_{obias}	Output bias voltage	V(Isx+) -V(Isx-) = 0	$0.5*V_{cc}$-0.5(2)	$0.5*V_{cc}$	$0.5*V_{cc}$+0.5(3)	V
IOD	Input offset drift (3)	Vcc = 5V	-	7	14	µV/°C
CMRR	Input common mode rejection ratio	-	70	86	-	dB
I_{SX+}(4)	Positive input pin current	Gain = 10 to 100, V_{CC} = 5 V	-200	-	-	µA
I_{SX-}(4)	Negative input pin current	Gain = 10 to 100, V_{CC} = 5 V	-1	-	-	mA
BST_C PSRR	Rejection ratio for Boost output power supply to amplifier Input	V(BST_C) / V(IBx) f=350KHz	40(5)	-	-	dB

Table 17. Phase current sense amplifier (SPI select: Offx=1, where x=1,2)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Gain	Gain	Gx1,Gx0 = 11 (x = 1,2)	-2%	100	+2%	-
		Gx1,Gx0 = 10 (x = 1,2)	-2%	50	+2%	-
		Gx1,Gx0 = 01 (x = 1,2)	-2%	30	+2%	-
		Gx1,Gx0 = 00 (x = 1,2) (default)	-2%	10	+2%	-
	Gain temperature drift (3)	-	-	-	100	ppm/ °C
V_{oh}	IBx output voltage high level	V(Isx+) -V(Isx-) > 500mV, I_{out} = 100 µA, V_{CC} = 3.3 V	V_{cc} - 0.12V	-	-	-
		V(Isx+) -V(Isx-) > 500mV, I_{out} = 100 µA, V_{CC} = 5V	V_{cc} - 0.15V	-	-	-
V_{ol}	IBx output voltage low level	V(Isx+) -V(Isx-) < -500mV, I_{out} = 100 µA	-	-	100	mV
SRCSO	CSO slew rate	RL = 1 kOhm, CL = 20 pF	0.5	2	-	V/µs
$t_{SETTLING}$	Output settling time	Gain = 10,30, 50 and 100, from 10% to 90% R_L = 1 kOhm, C_L = 20 pF	-	-	5.0	µs

1. 30 calibration steps (15 for positive and 15 for negative direction) are available through SPI command for offset calibration.
2. Worst case, if gain = 100 is selected.
3. Guaranteed by design.
4. $$I_{SxHI} = -\left(\frac{0.8 \cdot V_{CC}}{2000 \cdot Gnom} + I(trim, HI)\right) \cdot \frac{[2 + (3 \cdot Phase)]}{8} + 10\mu A$$

   $$I_{SxLO} = -\left(\frac{0.8 \cdot V_{CC}}{2000 \cdot Gnom} + I(trim, LO)\right) \cdot \frac{2}{8} + 10\mu A + I(rail)$$

   Where:
   I_{SxHI} is current flowing out from ISxHI pin
   I_{SxLO} is current flowing out from ISxLO pin
   Vcc = reference supply [5 V or 3.3 V]
   Gnom = nominal programmed gain [10, 30, 50, 100]
   I(trim,HI/LO) = offset trimming current (w.c. ±8 µA see expression below)
   Phase = programmed phase configuration [1 if selected, otherwise 0]
   I(rail) = current from auxiliary rail (used for floating OpAmp) [typ ~145 µA±35% T+Models]

   $$I(trim, HI) = \pm\frac{Vbg}{15} \cdot \frac{\left[\text{trimming bit}\frac{weight}{2}\right]}{10300 \cdot [5 + (3 \cdot Ground)]} \cdot \frac{[2 + (3 \cdot Phase)]}{8}$$

   $$I(trim, LO) = \pm\frac{Vbg}{15} \cdot \frac{\left[\text{trimming bit}\frac{weight}{2}\right]}{10300 \cdot [5 + (3 \cdot Ground)]} \cdot \frac{2}{8}$$

   Where:
   Vbg = band gap reference (1.2371 V nominal)
   Ground = programmed ground configuration [1 if selected, otherwise 0]
   Trimming bit weight= how many mV offset trimming are programmed.
   The ± depends on offset trim direction (+: bit7=1, -: bit7=0)
5. A 350 kHz, 100 mVpp, ripple at the boost regulator output, generates 1 mVpp noise at the amplifier input. It represents a 2 App current noise on a 0.5 mΩ current sense resistor.

Note: Table 18 is referred to current sense amplifier configuration for unidirectional current measurement (shunt resistors to ground). SPI select: Offx=0 (Power up default), where x=1,2 in CMD0 command frame.

Table 18. Ground current sense amplifier

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Vin_off	Differential input offset voltage	-	-5	-	5	mV
Vio_step	Calibration step of differential input offset voltage(1)	-	-	1	-	mV
VICM	Common Mode Input Voltage Range	Operating	-2	-	+2	V
		Transient (t<1µs)	-7	-	+7	V
V_{obias}	Output bias voltage	V(Isx+) -V(Isx-) = 0	$0.2*V_{cc}$-0.5(2)	$0.2*V_{cc}$	$0.2*V_{cc}$+0.5(3)	V
IOD	Input offset drift(3)	Vcc = 5V	-	7	14	µV/°C
CMRR	Input common mode rejection ratio	-	70	86	-	dB
I_{SX+}(4)	Positive input pin current	Gain = 10 to 100, V_{CC} = 5 V	-200	-	-	µA
I_{SX-}(4)	Negative input pin current	Gain = 10 to 100, V_{CC} = 5 V	-1	-	-	mA
BST_C PSRR	Rejection ratio for Boost output power supply to Amplifier Input	V(BST_C) / V(IBx) f=350KHz	40(5)	-	-	dB
Gain	Gain	Gx1,Gx0 = 11 (x=1,2)	-2%	100	+2%	-
		Gx1,Gx0 = 10 (x=1,2)	-2%	50	+2%	-
		Gx1,Gx0 = 01 (x=1,2)	-2%	30	+2%	-
		Gx1,Gx0 = 00 (x=1,2) (default)	-2%	10	+2%	-
	Gain temperature drift(3)	-	-	-	100	ppm/°C
V_{oh}	IBx output voltage high level	V(Isx+) -V(Isx-) > 500 mV, I_{out} = 100 µA, V_{CC} = 3.3 V	V_{cc} - 0.12V	-	-	V_{oh}
		V(Isx+) -V(Isx-) > 500 mV, I_{out} = 100 µA, V_{CC} = 5 V	V_{cc} - 0.15V	-	-	
V_{ol}	IBx output voltage low level	V(Isx+) -V(Isx-) < -500 mV, I_{out} = 100 µA	-	-	100	mV
SRCSO	CSO slew rate	R_L = 1 kΩ, C_L = 20 pF	1	2	-	V/µs
$t_{SETTLING}$	Output settling time	Gain = 10,30, 50 and 100, from 10% to 90% R_L = 1 kΩ, C_L = 20 pF	-	-	5	µs

1. 30 calibration steps (15 for positive and 15 for negative direction) are available through SPI command for offset calibration.
2. Worst case, if gain=100 is selected.

3. Guaranteed by design.
4. $$I_{SxHI} = -\left(\frac{0.8 \cdot V_{CC}}{2000 \cdot Gnom} + I(trim, HI)\right) \cdot \frac{[2 + (3 \cdot Phase)]}{8} + 10\mu A$$

   $$I_{SxLO} = -\left(\frac{0.8 \cdot V_{CC}}{2000 \cdot Gnom} + I(trim, LO)\right) \cdot \frac{2}{8} + 10\mu A + I(rail)$$

   Where:
   I_{SxHI} is current flowing out from ISxHI pin
   I_{SxLO} is current flowing out from ISxLO pin
   Vcc = reference supply [5 V or 3.3 V]
   Gnom = nominal programmed gain [10, 30, 50, 100]
   I(trim,HI/LO) = offset trimming current (w.c. ± 8 µA see expression below)
   Phase = programmed phase configuration [1 if selected, otherwise 0]
   I(rail) = current from auxiliary rail (used for floating OpAmp) [typ ~145 µA±35% T+Models]

   $$I(trim, HI) = \pm\frac{Vbg}{15} \cdot \frac{\left[\text{trimming bit}\frac{weight}{2}\right]}{10300 \cdot [5 + (3 \cdot Ground)]} \cdot \frac{[2 + (3 \cdot Phase)]}{8}$$

   $$I(trim, LO) = \pm\frac{Vbg}{15} \cdot \frac{\left[\text{trimming bit}\frac{weight}{2}\right]}{10300 \cdot [5 + (3 \cdot Ground)]} \cdot \frac{2}{8}$$

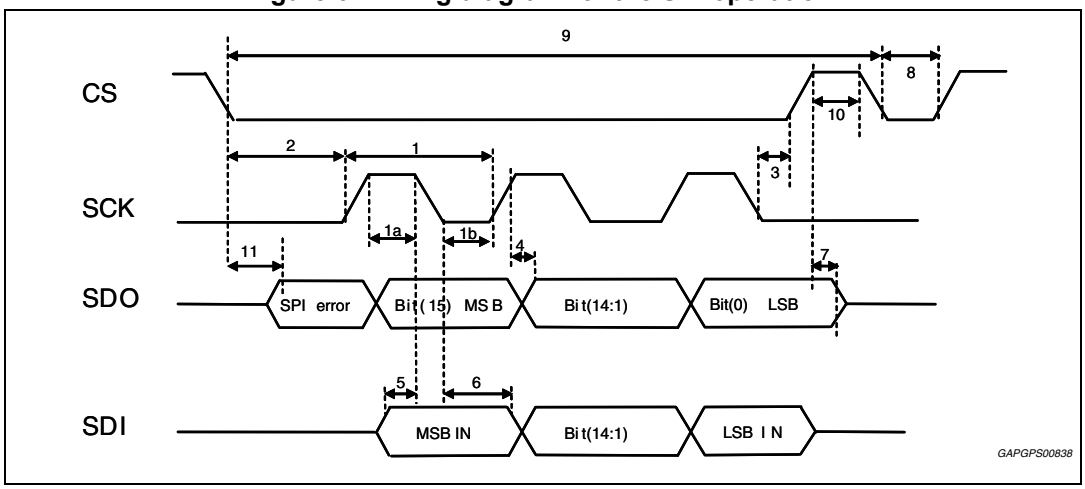
   Where:
   Vbg = band gap reference (1.2371 V nominal)
   Ground = programmed ground configuration [1 if selected, otherwise 0]
   Trimming bit weight= how many mV offset trimming are programmed.
   The ± depends on offset trim direction (+: bit7=1, -: bit7=0)
5. A 350 kHz, 100 mVpp, ripple at the boost regulator output, generates 1 mVpp noise at the amplifier input. It represents a 2 App current noise on a 0.5 mΩ current sense resistor.

5 SPI operation

The L9907 SPI is a standard 16-bit, four wire interface. By means of the SPI most device parameters can be internally set and the fault diagnostic can be read.

The timing diagram for the SPI operation is reported in *Figure 6* below. The IC reads the input data at SDI pin on the falling edge of the SPI clock (SCK). The IC outputs the SPI data at SDO pin on the rising edge of the SPI clock (SCK).

Figure 6. Timing diagram for the SPI operation.



The SPI protocol integrates an internal check to add robustness to the communication: a writing attempt of a not allowed register, an incorrect parity frame or a wrong number of bits (different than 16) results in a "SPI error bit", that is available at SDO immediately after asserting CS the next time and before starting the SCK toggling.

If the current SPI cycle is affected by a communication error, the current SDI command is rejected and a SPI error message (0xB001) is presented as SDO response at the following SPI cycle.

Table 19. SPI timing specifications

#	Parameter	Condition	Min.	Typ.	Max.	Unit
1	SCK Frequency ($f_{SC}K$)	1	-	-	8	MHz
2	SCK High/low time ($t_{SCK-high}$, $t_{-SCK-low}$)	1a, 1b	60	-	-	ns
3	Enable lead time (t_{lead})	2	740	-	-	ns
4	Enable lag time (t_{lag})	3	200	-	-	ns
5	Data valid time (t_{valid})	4 Cload<60pF @ fSCK=8MHz	-	-	50	ns
6	Data set up time (t_{SI-set}) Data hold time ($t_{SI-hold}$)	5 6	30 30	-	-	ns
7	Disable time ($t_{disable}$)	7			120	ns
8	SCK, SI rise/fall time (t_{rise}, t_{fall})	-	-	5	-	ns

Table 19. SPI timing specifications (continued)

#	Parameter	Condition	Min.	Typ.	Max.	Unit
9	SDO rise/fall time ($t_{SDO\text{-}rise}$, $t_{SDO\text{-}fall}$)	Cload < 60 pF @ fSCK =8 MHz	-	35	-	ns
10	CS $t_{CS\text{-}select}$ $t_{CS\text{-}access}$ $t_{CS\text{-}negated}$	 8 9 10	 50 3.58 640	-	-	 ns µs ns
11	SDO Access Time (t_a)	11	-	-	80	ns

5.1 SPI bits mapping

The L9907 provides the instructions to decide which kind of strategy to adopt for faults managing: the strategy can be selected by toggling the enable fault flags available in CMD4 and CMD1 registers.

When a fault has been validated, the corresponding diagnostic flag is set and FS_FLAG is asserted low. The device can perform shut-off or take no action depending on the value of the enable fault flag.

In the case where shut-off for a fault is disabled, micro becomes fully responsible for the shut-off management for the disabled fault.

As default value, all the enable fault flags are asserted high, so the device will take the actions described in the section related to each of them.

Table 20. SDI bit map definition

Item	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	AND (EN1, EN2)
CMD0	0	0	0	-	Par	WE	DT1	DT0	IG_1	IG_0	G21	G20	Off2	G11	G10	Off1	-
CMD1	0	0	1	EN_THSD	Par	WE	EN_VBov	EN_VBuv	SC_LS1	SC_LS0	SC_HS	SC_HS0	VBOV2	VBOV1	VccOV2	VccOV1	0
CMD2	0	1	0	GCR_INT_I(1)	Par	WE	BST_DIS_EN(1)	SHT_PH(1)	VSCTST	VOVTST	ShortPH(1)	-	-	-	-	-	-
CMD3	0	1	1	DIS_BSTov(1)	Par	WE	TRIM24	TRIM23	TRIM22	TRIM21	TRIM20	TRIM14	TRIM13	TRIM12	TRIM11	TRIM10	-
CMD4	1	0	0	REGOFF_EN	Par	WE	EN_Vccov	EN_Vccuv	EN_UV_HS	EN_UV_LS	EN_VSCHS1	EN_VSCHS2	EN_VSCHS3	EN_VSCLS1	EN_VSCLS2	EN_VSCLS3	0
DIAG	1	1	0	-	Par	-	-	-	-	-	-	-	-	-	-	-	-
DIAG2	1	1	1	-	Par	-	-	-	-	-	-	-	-	-	-	-	-

1. Writable only if AND(EN1,EN2) low else command ignored.

Table 21. SDI frame structure

Bit position	Description
B(15:13)	SDI command selection bits, used to select the SPI operation to be implemented
B11 (Par)	odd parity bit
B10 (WE)	Write Enable bit. A SPI cycle with WE=1 transfers the SDI data to the addressed CMDx register. A SPI cycle with WE=0 transfers the content of the addressed CMDx register to the SDO data of the following SPI cycle.
B(9:0)	the SDI setting bits to be internally stored for device operation in case of writing SPI cycle

1. CMD0 register - Driver settings: B(15:13) = 000

a) DT1 and DT0 (B9,B8) are used to select dead time (tDT) parameter: ('00' default condition at Power-On Reset)

Table 22. Dead time parameter

Dead time	B9 = DT1	B8 = DT0
100-200ns	0	0
300-500 ns	0	1
700-1000 ns	1	0
1000-1500 ns	1	1

b) IG_1 and IG_0 (B7,B6) are used to select turn on/off current value: ('00' default condition at Power-On Reset)

Table 23. Turn on/off current

Percentage	B7 = IG_1	B6 = IG_0
25%	0	0
50%	0	1
75%	1	0
100%	1	1

c) G21 and G20 (B5,B4) are used to select current sense amplifier 2 gain: ('00' default condition at power on reset)

Table 24. Current sense amplifier 2 gain

Gain	B5= G21	B4= G20
10	0	0
30	0	1
50	1	0
100	1	1

d) Off2 (B3) is used to select current sense amplifier 2 offset (for ground or phase connection): '0' (default value) means ground, '1' means phase.

e) G11 and G10 (B2,B1) are used to select Current sense amplifier 1 Gain:('00' default condition at Power-On Reset)

Table 25. Current sense amplifier 1 gain

Gain	B2 = G11	B1 = G10
10	0	0
30	0	1
50	1	0
100	1	1

f) Off1 (B0) is used to select current sense amplifier 1 offset (for ground or phase connection): '0' (default value) means ground, '1' means phase.

2. CMD1 register - Diagnostic settings: B(15:13) = 001

In order to avoid unsafe change of diagnostic settings, it is not possible to write the CMD1 register during normal Output Gate Drive operation. For this reason at least one Enable signal EN1 or EN2 must be deasserted in order to update the CMD1 register. If EN1 and EN2 are both asserted while a SPI cycle CMD1 with WE=1 is ongoing, then a SPI communication error is generated and the corresponding SPI command is ignored.

Since the Enable signals EN1 and EN2 also affect the output gate drives, a deglitch filter is implemented on both of them. This filter is active on either falling edge of EN1 or EN2 signal.

In order to avoid unsafe change of fault management settings, as for the CMD1 register, it is not possible to write CMD4 register during normal Output Gate Drive operation. For this reason at least one Enable signal EN1 or EN2 must be deasserted in order to update the register.

If EN1 and EN2 are both asserted while a SPI cycle CMD4 or CMD1 with WE=1 is ongoing, then a SPI communication error is generated and the corresponding SPI command is ignored.

a) SC_LS1 and SC_LS0 (B7,B6) are used to select short circuit detection threshold for low-side PowerMOS ('00' default condition at power up):

Table 26. Short circuit detection threshold for low-side PowerMOS

VSC_LS	B7 = SC_LS1	B6 = SC_LS0
0.4 – 0.6 V	0	0
0.7 – 0.9 V	0	1
0.9 – 1.1 V	1	0
1.17 – 1.43 V	1	1

Note: The accuracy in ranges in Table 26 are valid for VB > 6 V. For VB < 6 V the accuracy is 22.5% for each configuration.

b) SC_HS1 and SC_HS0 (B5-B4) are used to select short circuit detection threshold for high-side PowerMOS ('00' default condition at Power Up):

Table 27. Short circuit detection threshold for low-side PowerMOS

VSC_HS	B5 = SC_HS1	B4 = SC_HS0
0.4 – 0.6 V	0	0
0.7 – 0.9 V	0	1
0.9 – 1.1 V	1	0
1.17 – 1.43 V	1	1

Note: The accuracy in ranges in Table 27 are valid for VB > 6 V. For VB < 6 V the accuracy is 22.5% for each configuration.

c) VB_{OV2} and VB_{OV1} (B3-B2) are used to select over voltage threshold for single or double battery application

Table 28. VB over voltage threshold for single or double battery application

VB_{OV}	B3 = VB_{OV2}	B2 = VB_{OV1} (1)
27.5 – 34.5 V	1	0
36 – 42 V (Default)	0	1
Not Allowed	0	0
Not Allowed	1	1

1. For power supply configuration in 48 V domain, please refer to AN5124.

The power-up default value for this parameter is "01", corresponding to double battery applications.

A SPI command attempting to set a not allowed VB_{OV} configuration does not return any SPI error, and the VB_{OV} configuration register retains its previous value.

d) EN_THSD, EN_VBOV EN_VBUV (B12,B9,B8) are used to enable/disable effect of Thermal Shut Down, VB overvoltage, VB Under Voltage faults respectively. Default value is '1' for all of them, that means "fault effect is enabled".

Table 29. CMD1 SDI SPI bits vs. enabled fault

CMD1 SDI SPI BIT	Name	Description (Default value='1')
B12	EN_THSD	It enables Thermal shut down fault effect in case of THSD fault detection
B9	EN_VB_{OV}	It enables VB_{OV} fault effect in case of VB_{OV} fault detection
B8	EN_VB_{UV}	It enables VB_{UV} fault effect in case of VB_{UV} fault detection

e) VCC_{OV2} and VCC_{OV1} (B1-B0) are used to select the VCC over voltage thresholds:

Table 30. VCC over voltage threshold

VCC_{OV}	B1 = VCC_{OV2}	B0 = VCC_{OV1}
3.3 V (default)	1	0
5.0 V	0	1

Table 30. VCC over voltage threshold (continued)

VCC_{OV}	B1 = VCC_{OV2}	B0 = VCC_{OV1}
Not Allowed	0	0
Not Allowed	1	1

The Power Up default value for this parameter is "10", corresponding to Vcc = 3.3 V applications.

A SPI command attempting to set a not allowed VCC_{OV} configuration does not return any SPI error, and the VCC_{OV} configuration register retains its previous value.

3. CMD2 register - Test Mode Selections: B(15:13) = 010

a) SDI bit B12: GCR_INT_I

This bit is accessible for writing only if AND(EN1,EN2)='0': trying to write it without lowering AND(EN1,EN2) will not generate any SPI error but command will be simply ignored for the specific bit.

Once written, CMD2 B12 changes the status of the output GCR_INT_I (refer to *Section 3.5.1*).

b) SDI bit B9: BstDisEN

This bit is accessible for writing only if AND(EN1,EN2)='0': trying to write it without lowering AND(EN1,EN2) will not generate any SPI error but command will be simply ignored for the specific bit.

Once written, CMD2 B9 determines how to behave in case of activation of BST_DIS pin. In case this bit is set and activating BST_DIS pin brings the device to switch-off BST_CLK till BST_DIS pin becomes low (refer to *Section 3.4.1*).

c) SDI bit B8: SHT_PH

This bit is accessible for writing only if AND(EN1,EN2)='0': trying to write it without lowering AND(EN1,EN2) will not generate any SPI error but command will be simply ignored for the specific bit.

Once written, CMD2 B8 determines how to behave in case of shoot-through detected. In case this bit is not set (default) a shoot-through in any phase will prevent the actuation of all commands, only the involved phase is inhibited otherwise (refer to *Section 3.5.2*).

d) VSC_{TST} (B7) = '1' activates Test Function for short circuit level ('0' is the default value).

e) VOV_{TST} (B6) = '1' activates Test Function for VCC over-voltage level ('0' is the default value).

f) SDI bit B5: Short_PH

This bit is accessible for writing only if AND(EN1,EN2)='0': trying to write it without lowering AND(EN1,EN2) will not generate any SPI error but command will be simply ignored for the specific bit.

Once written, CMD2 B5 determines how to behave in case of external FET (both HS and LS) short detected. In case this bit is not set (default) a short in any phase will prevent the actuation of all commands, only the involved phase is inhibited otherwise (refer to *Section 3.5.3*).

4. CMD3 register - Current Sense amplifier offset calibration: B(15:13) = 011

a) SDI bit DIS_BST$_{ov}$ (B12)

This bit is accessible for writing only if AND(EN1,EN2) = '0': trying to write it without lowering AND(EN1,EN2) will not generate any SPI error but command will be simply ignored for the specific bit. Once set to '1', CMD3 B12 disables the over voltage protection on the boost regulator BST_C pin. This bit defaults to '0'.

b) SDI bits TRIM24 to TRIM10 (B9 to B0)

The input offset of both current sense amplifiers can be calibrated separately by properly setting the bits of the CMD3 SPI Register. Such a register can be accessed through SDI bits B(9:0). Bits B(9:5) are dedicated to offset calibration of Current Sense amplifier 2, while bits B(4:0) are dedicated to current sense amplifier 1. The encoded value is a signed representation, and the values "10000" and "00000", both correspond to 0 mV calibration.

Table 31. Current sense amplifier input offset calibration

Current sense amplifier 2(1) calibration input offset	B9(B4)= Trim24 (Trim14)	B8(B3)= Trim23 (Trim13)	B7(B2)= Trim22 (Trim12)	B6(B1)= Trim21 (Trim11)	B5(B0)= Trim20 (Trim10)
-15 mV	0	1111			
-14 mV	0	1110			
-13 mV	0	1101			
...	0	...			
-3 mV	0	0011			
-2 mV	0	0010			
-1 mV	0	0001			
0 mV	0	0000			
0 mV	1	0000 (0000 = Default)			
+1 mV	1	0001			
+2 mV	1	0010			
+2 mV	1	0011			
...	1	...			
+13 mV	1	1101			
+14 mV	1	1110			
+15 mV	1	1111			

5. CMD4 register - Fault effect enabling B(15:13)=100

In order to avoid unsafe change of fault management settings, as for the CMD1 register, it is not possible to write CMD4 register during normal Output Gate Drive operation. For this reason at least one Enable signal EN1 or EN2 must be deasserted in order to update the register.

Since the Enable signals EN1 and EN2 also affect the output gate drives, a deglitch filter is implemented on both of them. This filter is active on the falling edges of EN1 or EN2 signal.

If EN1 and EN2 are both asserted while a SPI cycle CMD4 or CMD1 with WE=1 is ongoing, then a SPI communication error is generated and the corresponding SPI command is ignored.

The effect of any fault (except Shoot Through) can be selectively masked from Micro Controller setting at '0' proper register. FS_FLAG status and SDO report are not affected since fault detection always acts in the same way. Default values for these bits is '1' (fault effect enabled). Once the fault effect is re-enabled with SPI communication the IC reacts to fault as described in the specific paragraph if the fault is still present.

Table 32. CMD4 SDI SPI bits vs. enabled fault

CMD4 SDI SPI BIT	Name	Description (Default value='1')
B9	EN_Vcc_{OV}	It enables VCC_{OV} fault effect in case of VCC_{OV} fault detection
B8	EN_Vcc_{UV}	It enables VCC_{UV} fault effect in case of VCC_{UV} fault detection
B7	EN_UV_HS	It enables UV_HS fault effect in case of UV_HS fault detection
B6	EN_UV_LS	It enables UV_LS fault effect in case of UV_LS fault detection
B5	EN_V_{SCHS1}	It enables V_{SCHS1} fault effect in case of V_{SCHS1} fault detection
B4	EN_V_{SCHS2}	It enables V_{SCHS2} fault effect in case of V_{SCHS2} fault detection
B3	EN_V_{SCHS3}	It enables V_{SCHS3} fault effect in case of V_{SCHS3} fault detection
B2	EN_V_{SCLS1}	It enables V_{SCLS1} fault effect in case of V_{SCLS1} fault detection
B1	EN_V_{SCLS2}	It enables V_{SCLS2} fault effect in case of V_{SCLS2} fault detection
B0	EN_V_{SCLS3}	It enables V_{SCLS3} fault effect in case of V_{SCLS3} fault detection

6. CMD4 SPI command register

SDI bit B12: REGOFF_EN

This bit is accessible for writing only if AND(EN1,EN2)='0': trying to write it without lowering AND(EN1,EN2) will generate SPI error.

Once written, CMD4 B12 determines if the REG_OFF procedure is active or not (default: not active).

REG_OFF procedure (active only if CMD4 B12 is set; refer also to *Section 3.3*)

Lowering EN1 external pin triggers the procedure to switch off regulators that supply the HS and LS FET drivers: filter time, active only on the falling edge of the EN1 signal, is implemented: 8*tosc ≤ TFILT ≤ 16*tosc.

Once the procedure has been triggered, device behaves as follows:

REG_OFF = '1', EN_PWM = "000", FS_FLAG = '0', DIAG2 bit B6 set

In order to re-engage, the correct procedure is to toggle AND(EN1,EN2) then read DIAG2 SPI register (to verify that bit B6 is set).

Toggling of AND(EN1,EN2) will re-engage the output commands (EN_PWM = "111") while subsequent reading of DIAG2 register will re-engage HS/LS drivers supply (REG_OFF = '0') and release FS_FLAG.

In order to avoid activating output commands while regulators that supply the HS and LS FET drivers are in power-up phase (this could generate current shape distortion)

microprocessor must guarantee a dis-overlap between reading of DIAG2 register and PWM commands toggling.

5.1.1 SDO

Table 33. SDO bit map definition

Item	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
CMD0	0	0	0	0	-	-	DT1	DT0	IG_1	IG_0	G21	G20	Off2	G11	G10	Off1
CMD1	0	0	1	EN_THSD	-	-	EN_VBOV	EN_VBUV	SC_LS1	SC_LS0	SC_HS1	SC_HS0	VBOV2	VBOV1	VccOV2	VccOV1
CMD2	0	1	0	GCR_INT_I	-	-	BST_DIS_EN	SHT_PH	VSCTST	VOVTST	ShortPH	-	Undefined	Undefined	Undefined	Undefined
CMD3	0	1	1	DIS_BSTov	-	-	TRIM24	TRIM23	TRIM22	TRIM21	TRIM20	TRIM14	TRIM13	TRIM12	TRIM11	TRIM10
CMD4	1	0	0	REGOFF_EN	-	-	EN_VccOV	EN_VccUV	EN_UV_HS	EN_UV_LS	EN_VSCHS1	EN_VSCHS2	EN_VSCHS3	EN_VSCLS1	EN_VSCLS2	EN_VSCLS3
DIAG	1	1	0	THSD	VBOV	VBUV	VccOV	VccUV	UV_HS	UV_LS	VSCHS1	VSCHS2	VSCHS3	VSCLS1	VSCLS2	VSCLS3
DIAG2	1	1	1	-	-	-	BSTDIS_RB(1)	EN1_RB	AND(EN1_EN2)_RB	REGOFF_RB	BST_C_OV	GCR_OL	GCR_STG	SHT3	SHT2	SHT1

1. Not cleared after read.

1. SDO CMD1 to CMD4 registers - Response to SDI commands: B(15:13)=000 till 100

SDO responds in the current SPI cycle with the content of the command register CMDn (n=1 to 4) that is being addressed in the previous SPI cycle. In such a way the controller may verify the command data being stored in the proper register (WE=1 in the previous SPI cycle), or simply verify the correct IC data retention of initially programmed commands (WE=0).

2. SDO DIAG register - Diagnostic read cycle: B(15:13) = 110

During its operation the IC detects diagnostic data that is made available at SDO SPI output pin. Such diagnostic data is mainly related to output gate drivers, in order to check for example under voltage condition on high-side or low-side (UV_HS and UV_LS) together with over current information due to a short circuit fault on each external high and low-side FET (VSCHS1-2-3 and VSCLS1-2-3). Additionally the device diagnostic allows also to check Thermal Shutdown Fault (THSD), under and over voltage condition on VB line (VBUV and VBOV) and VCC line (VccOV, VccUV).

Effects described in the following sections take into account that the corresponding Fault Enable bit is set to '1'.

a) TH_SD (B12). Thermal shutdown.

Once Thermal shutdown threshold temperature is reached, all the FET drivers are disabled and a cumulative fault information is available at FS_FLAG pin and through SPI reading cycle, together with FET status (enable/disable). After cooling down the FET drivers are automatically re-enabled once the temperature becomes lower than (T_{ot} -T_{hys}: see *Table 8*) and the information about FET status (enable/disable) is available at SDO pin through an SPI reading cycle. After cooling down the SPI diagnostic bit remains set, and the pin FS_FLAG remains asserted low. A SPI diagnostic read cycle clears the THSD bit and deactivates high the FS_FLAG pin.

The filter time applied to this fault works on both edges of the input signal.

b) VB_OV (B11) and VB_UV (B10). VB over-voltage and under-voltage

When the device is active and an under or over-voltage condition on VB line is present for a time longer than Td_VB, the fault is detected and internally latched. Upon detection of under or over-voltage of VB, the FET drivers and the BOOST regulator are disabled, the proper SPI bit is set and the FS_FLAG is asserted low.

After removal of the fault condition (VB returns inside its normal range), the BOOST is automatically re-enabled, the FET drivers instead are restarted by cycling EN signal (internal AND of EN1 and EN2 pins) from high to low to high. A SPI diagnostic read cycle clears the SPI diagnostic flag releases the FS_FLAG pin to high.

The filter time applied to this fault works on both edges of the input signal.

c) Vcc_OV (B9) and Vcc_UV (B8). VCC over-voltage and under-voltage

When an over-voltage condition appears on the VCC line for a time longer than Td_Vcc, the fault is detected and internally latched, the device is then disabled.

In case of detected under or over-voltage of VCC, the FET drivers and the BOOST regulator are disabled, the proper SPI bit is set and the FS_FLAG is asserted low.

After removal of the fault condition (Vcc returns inside its normal range), the BOOST is automatically re-enabled, the FET drivers are restarted by cycling EN signal (internal AND of EN1 and EN2 pins) from high to low to high. A SPI diagnostic read cycle clears the SPI diagnostic flag and releases the FS_FLAG pin to high.

The filter time applied to this fault works on both edges of the input signal.

d) UV_HS (B7). High-side FET drivers supply under-voltage

The voltage difference between boost output pin and high-side Drain connection is monitored and, if it falls down below VG_UV_HS threshold for a time longer than tUV_UG, a high-side under-voltage fault is detected and internally latched. All the FET drivers are disabled and fault information is available at FS_FLAG pin and at SDO pin through an SPI reading cycle.

The fault flag for the high-side FET drivers supply under-voltage is related to a BOOST regulator under - voltage.

In case of detected fault, the FET drivers are disabled, the proper SPI bit is set and the FS_FLAG is asserted low. After removal of the fault condition, the FET

drivers are restarted by cycling EN signal (internal AND of EN1 and EN2 pins) from high to low to high. A SPI diagnostic read cycle clears the SPI diagnostic flag and releases the FS_FLAG pin to high.

e) UV_LS (B6). Low-side FET drivers supply under-voltage

The voltage difference between the low-side gate driver supply pin VCAP and each of the low-side FET sources are monitored. In case VCAP is lower than VG_UV_LS threshold for a time longer than tUV_UG, then a low-side under-voltage fault is detected and internally latched. The low-side FET drivers supply under-voltage is active if the fault condition is present at least on one of the three channels.

In case of detected fault, the FET drivers are disabled, the proper SPI bit is set and the FS_FLAG is asserted low. After removal of the fault condition, the FET drivers are restarted by cycling EN signal (internal AND of EN1 and EN2 pins) from high to low to high. A SPI diagnostic read cycle clears the SPI diagnostic flag and releases the FS_FLAG pin to high.

f) VSC_HS1 to VSC_HS3 (B5 to B3). High-side PowerMOS over-current

The voltage difference between the high-side external power drain (VDH) and the source (SHS1-2-3) is monitored and, if it exceeds VSC_HS threshold for a time longer than TSCoff, then a high-side short circuit fault is detected and internally latched.

In case of detected fault, all FET drivers are disabled, the proper SPI bit is set and the FS_FLAG is asserted low. After removal of the fault condition, the FET drivers are restarted by cycling EN signal (internal AND of EN1 and EN2 pins) from high to low to high. A SPI diagnostic read cycle clears the SPI diagnostic flag and releases the FS_FLAG pin to high.

g) VSC_LS1 to VSC_LS3 (B2 to B0). Low-side PowerMOS over-current

The voltage difference between low-side external power drain (SHS1-2-3) and source (SLS1-2-3) is monitored and, if it exceeds the VSC_LS threshold for a time longer than TSCoff, then a low-side short circuit fault is detected and internally latched.

In case of detected fault, all FET drivers are disabled, the proper SPI bit is set and the FS_FLAG is asserted low. After removal of the fault condition, the FET drivers are restarted by cycling the EN signal (internal AND of EN1 and EN2 pins) from high to low to high. A SPI diagnostic read cycle clears the SPI diagnostic flag and releases the FS_FLAG pin to high.

3. SDO DIAG2 register - Diagnostic read cycle: B(15:13) = 111

Below, it is described the meaning of each diagnostic bit in case of DIAG2 active.

a) SDO bit B9: BST_DIS_RB

BST_DIS_RB informs about the status of that a BST_DIS pin (not cleared after read).

b) SDO bit B8: EN1_RB

EN1_RB informs about the status of EN1 filtered input (not cleared after read).

c) SDO bit B7: AND(EN1,EN2)_RB

AND(EN1,EN2)_RB informs about the status of AND(EN1,EN2) signal (not cleared after read).

d) SDO bit B6: REGOFF_RB

e) REGOFF_RB informs that a REG_OFF procedure has been triggered by EN1 lowering. Reading back this bit will re-engage FS_FLAG and cause REG_OFF='0'.

f) SDO bit B5: BST_C_OV

BST_C_OV informs about the status of boost over voltage level.

Filter time duration: 16*tosc ≤ TFILT ≤ 20*tosc (active on both directions)

effect when validated: BST_CLK = 0, BST_EN = 1,
BST_HYST = 1, FS_FLAG = 0; EN_PWM[3:1] no change

re-engagement: BST_CLK self re-engagement when fault disappears
FS_FLAG re-engaged after DIAG2 reading and fault cleared

g) SDO bit B4: GCR_OL

GCR_OL informs about the status of the GCR pin open load condition (i.e. too high resistive value).

Filter time duration: 16*tosc ≤ TFILT ≤ 20*tosc (active on both directions)

effect when validated: GCR_INT_I = 1

re-engagement: GCR_INT_I = 0 self re-engagement when fault disappears
FS_FLAG re-engaged after DIAG2 reading and fault cleared

h) SDO bit B3: GCR_STG

GCR_STG informs about the status of the GCR pin short to ground condition (i.e. too low resistive value).

Filter time duration: 16*tosc ≤ TFILT ≤ 20*tosc (active on both directions)

effect when validated: GCR_INT_I = 1

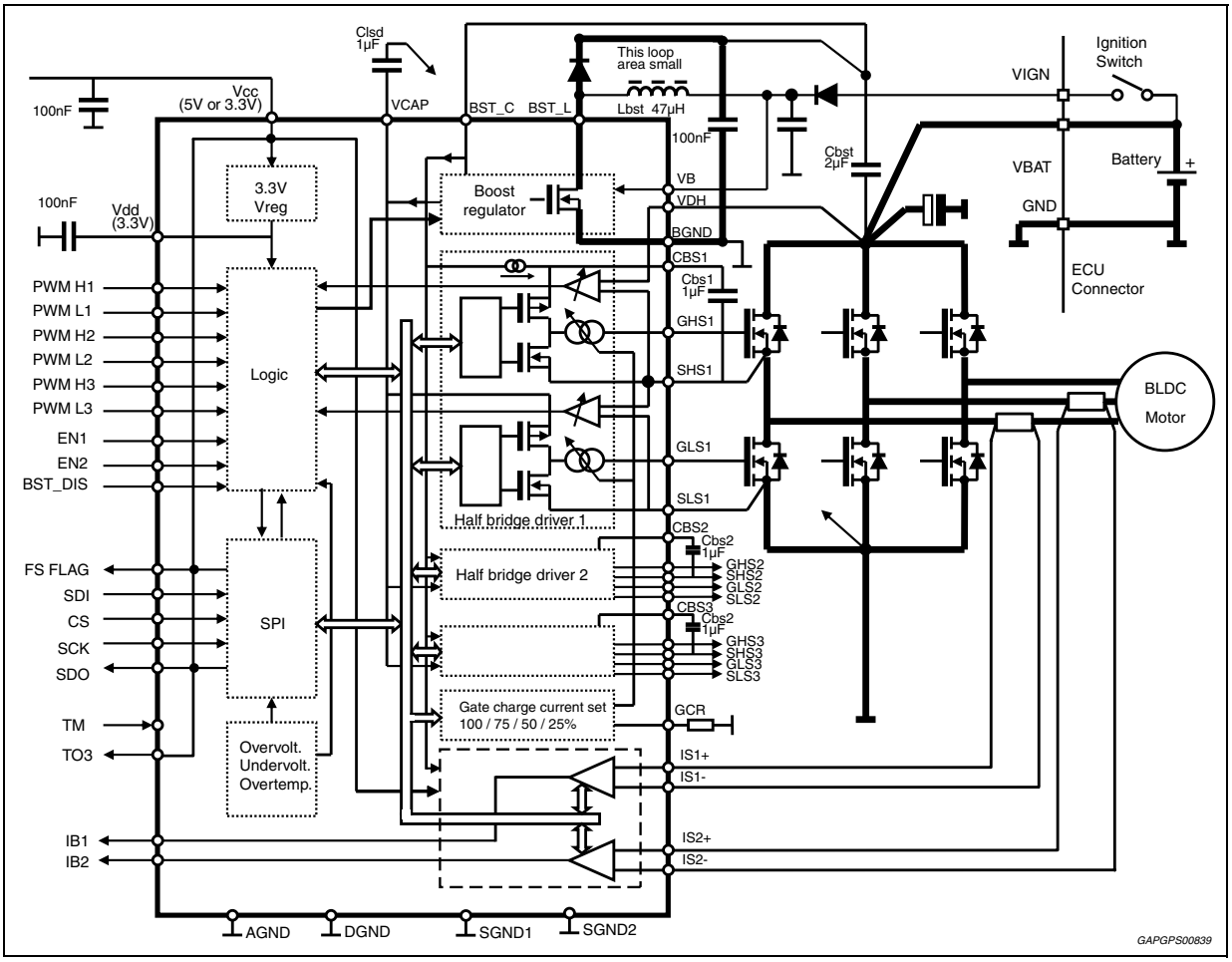
re-engagement: GCR_INT_I = 0 self re-engagement when fault disappears
FS_FLAG re-engaged after DIAG2 reading and fault cleared

i) SDO bit B<2:0>: SHT<X>

Shoot Through on specific phase has occurred: FS_FLAG remains low till the fault is cleared by a read back of DIAG2 frame.

6 Application circuit

Figure 7. Three-phase motor control



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of *ECOPACK* packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

7.1 TQFP64 (10x10x1 mm exp. pad down) package mechanical data

Figure 8. TQFP64 (10x10x1 mm exp. pad down) package mechanical drawing

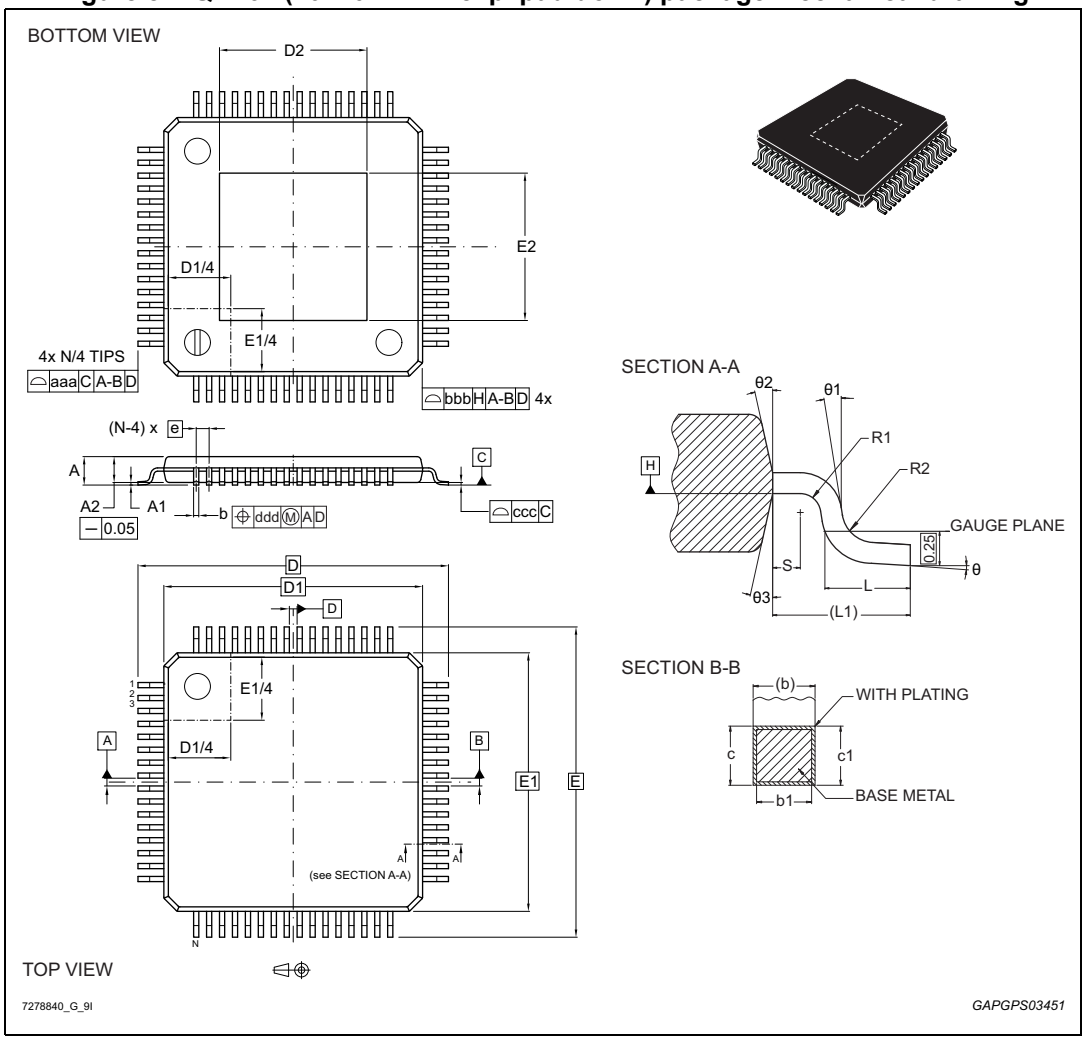


Table 34. TQFP64 (10x10x1 mm exp. pad down) package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Θ	0°	3.5°	6°	0°	3.5°	6°
Θ1	0°	-	-	0°	-	-
Θ2	11°	12°	13°	11°	12°	13°
Θ3	11°	12°	13°	11°	12°	13°
A	-	-	1.20	-	-	0.0472
A1	0.05	-	0.15	0.002	-	0.0059
A2	0.95	1.0	1.05	0.0374	0.0394	0.0413
b	0.17	0.22	0.27	0.0067	0.0079	0.0091
b1	0.17	0.20	0.23	0.0067	0.0079	0.0091
c	0.9	-	0.20	0.0354	-	0.0079
c1	0.9	-	0.16	0.0354	-	0.0063
D	-	12.00 BSC	-	-	0.4724 BSC	-
D1[2]	-	10.00 BSC	-	-	0.3937 BSC	-
D2	VARIATION					
e	-	0.50 BSC	-	-	0.0197 BSC	-
E	-	12.00 BSC	-	-	0.4724 BSC	-
E1[2]	-	10.00 BSC	-	-	0.3937 BSC	-
E2	VARIATION					
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00 REF	-	-	0.0394 REF	-
N	-	64.00	-	-	2.5197	-
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
TOLERANCE OF FORM AND POSITION						
aaa	-	0.20	-	-	0.0079	-
bbb	-	0.20	-	-	0.0079	-
ccc	-	0.08	-	-	0.0031	-
ddd	-	0.07	-	-	0.0028	-
VARIATIONS						
Option A						
D2	-	4.50	-	-	0.1772	-

Table 34. TQFP64 (10x10x1 mm exp. pad down) package mechanical data (continued)

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
E2	-	4.50	-	-	0.1772	-
Option B						
D2	-	6.0	-	-	0.2362	-
E2	-	6.0	-	-	0.2362	-

1. Values in mm are converted into inches and rounded to 4 decimal digits.
2. Dimensions D1 and E1 do not include mold flash or protrusions.
Allowable mold flash or protrusion is “0.25 mm” per side.

7.1.1 TQFP64 exposed pad dimensions for L9907

Table 35. TQFP64 exposed pad dimensions for L9907

Ref	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
D2	5.85	6.0	6.15	0.2303	0.2362	0.2421
E2	5.85	6.0	6.15	0.2303	0.2362	0.2421

1. Values in mm are converted into inches and rounded to 4 decimal digits.

8 Revision history

Table 36. Document revision history

Date	Revision	Changes
30-Mar-2017	1	Initial release
29-Jun-2018	2	Corrected limits (LSL = 1 µs) for TSCoff digital filter time (short circuit shutdown delay) in *Table 15 on page 23*. Updated: – Operating VB range, extension to 4.2 V; – ISxx range: VDH+4 V in *Table 5 on page 17* – Inserted note (2) for differential driver stage in *Table 6: Absolute maximum ratings*; – Corrected in *Table 13 on page 21*, V_{CAP} range, with LSL limit to 7.5 V; – Corrected B8 description in *Table 29 on page 32*; – Added note in *Table 28* reference regarding power supply configuration for 48 V boardnet.
07-Aug-2019	3	Updated: – High level digital input LSL from 2 V to 1.9 V in *Table 11*; – LSL of overdrive for V_{BST}, V_{CAP} and V_{CBS} set to 8.5 V in *Table 13*.
20-Jul-2020	4	Typing error.