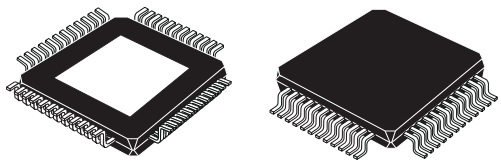
L99ASC03G

Brushless / sensorless 3-phase motor pre-driver for automotive applications

Datasheet - production data



TQFP48-EP

Features

- AEC-Q100 qualified
- 5 V low-drop voltage regulator (200 mA continuous mode)
- Very low current consumption in standby mode (typ. 15 µA)
- ST SPI interface for control and diagnostics
- Window watchdog and fail-safe functionality
- Two separate power supply pins
- Three half-bridge drivers to control external MOSFETs (configurable by SPI)
- Full drive of external MOSFETs down to 6 V input voltage
- Input pin for each gate driver (with cross-current protection)
- Two-stage charge pump supporting 100% duty cycle
- PWM operation up to 80 kHz (not restricted)
- Current-sense amplifier (configurable by SPI)
- Disable input to turn off gate driver outputs
- Analog multiplexer output to monitor external power supply voltages and internal junction temperature
- Advanced BEMF detection IP
- Overcurrent protection (programmable)
- Drain-source monitoring and open-load detection
- TQFP48 7 x 7 x 1 mm with Exposed Pad (4.5 x 4.5 mm) package

Applications

Mechatronic three-phase motor application such as engine cooling fans, fuel pumps, water pumps, oil pumps

Description

The L99ASC03G is a multifunctional system IC designed for three-phase motor control applications.

The device features a voltage regulator to supply an external microcontroller and an operation amplifier for motor current sensing. It is designed to control six external N-channel MOSFETs in bridge configuration to drive three-phase motors in automotive applications. All gate driver outputs are controlled by separate inputs.

The integrated Serial Peripheral Interface (SPI) makes it possible to adjust device parameters, control all operating modes and read out diagnostic information.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and real
TQFP48-EP	L99ASC03G	L99ASC03GTR

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1 Block diagram and pin descriptions

Figure 1. Block diagram

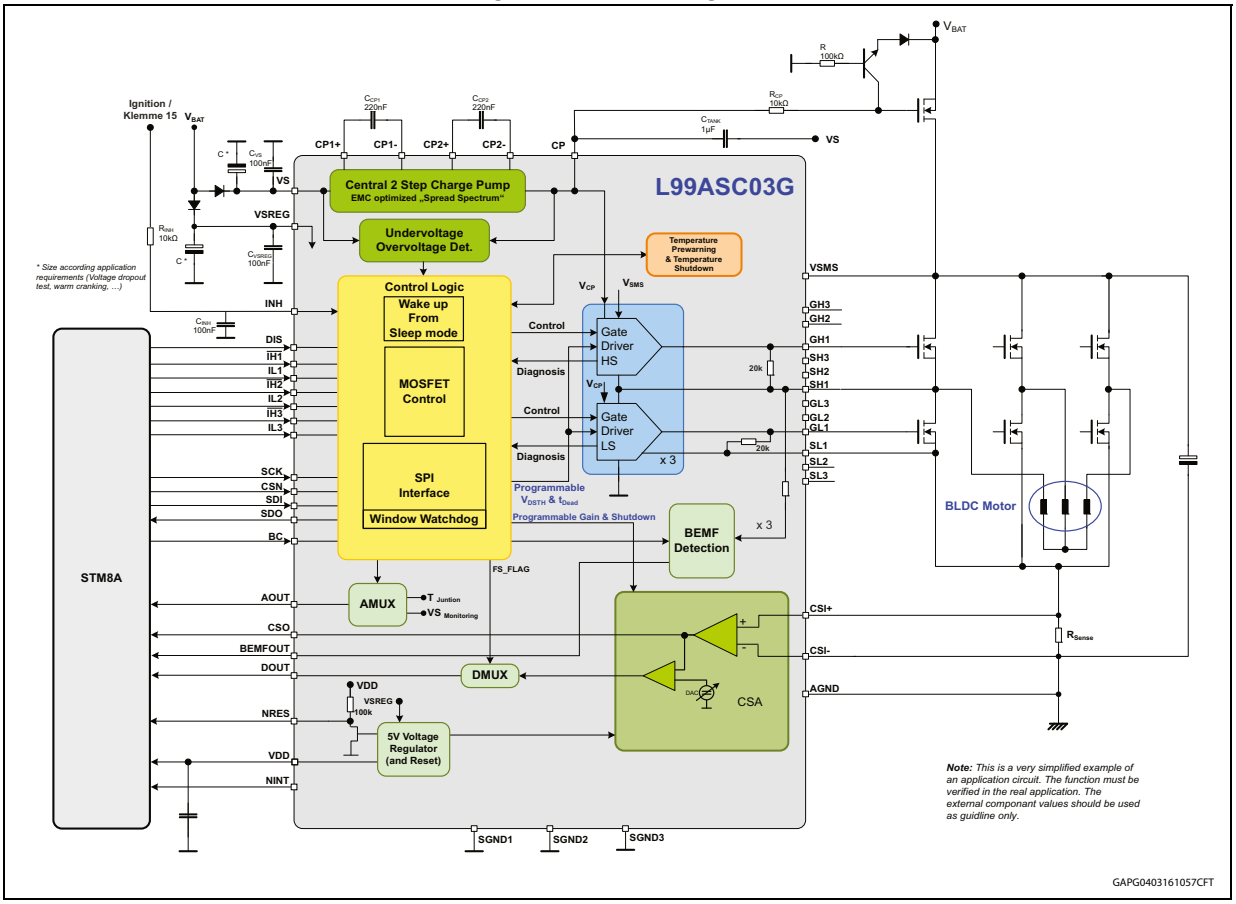


Table 2. Pin definition and function

Pin number	Symbol	Function	I/O type
1	SL3	Source of external low-side MOSFET 3	I/O
2	CSI+	Current-sense amplifier positive input	I
3	CSI-	Current-sense amplifier negative input	I
4	SGND2	Signal Ground 2	GND
5	CSO	Current-sense amplifier output	O
6	IL3	Input of low-side switch 3	I
7	$\overline{IH3}$	Input of high-side switch 3	I
8	IL2	Input of low-side switch 2	I
9	$\overline{IH2}$	Input of high-side switch 2	I
10	IL1	Input of low-side switch 1	I
11	$\overline{IH1}$	Input of high-side switch 1	I

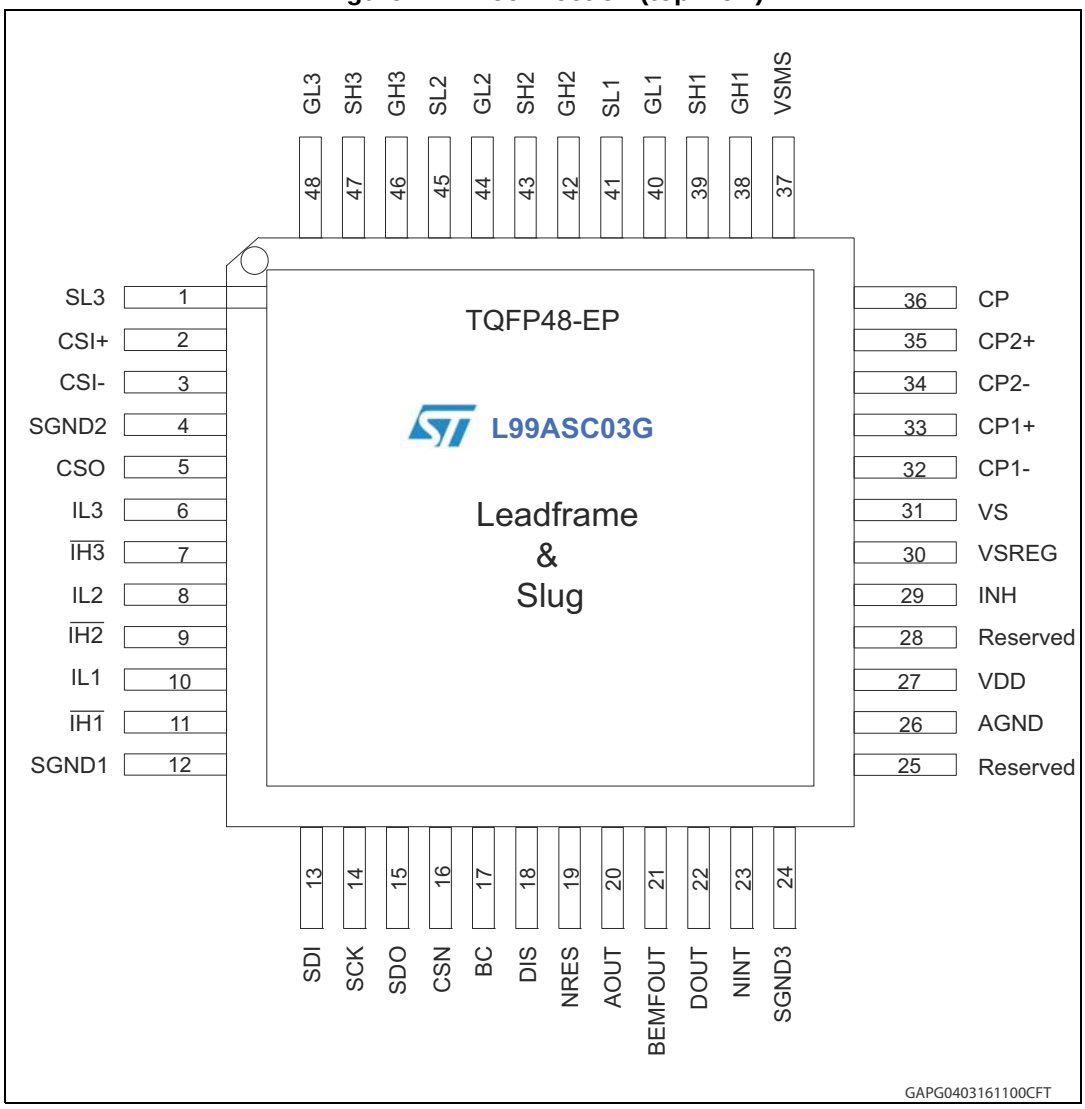
Table 2. Pin definition and function (continued)

Pin number	Symbol	Function	I/O type
12	SGND1	Signal ground 1	GND
13	SDI	SPI Serial data input	I
14	SCK	SPI clock input	I
15	SDO	SPI Serial data output	O
16	CSN	SPI Chip Select Not input	I
17	BC	Block Commutation Sync Pin	I
18	DIS	Disable input	I
19	NRES	NReset output	O
20	AOUT	Analog multiplexer output	O
21	BEMFOUT	Back EMF output	O
22	DOUT	Digital multiplexer output	O
23	NINT	Interrupt output	O
24	SGND3	Signal ground 3	GND
25	Reserved	Pin must be kept not connected	Not to be connected
26	AGND	Analog ground	GND
27	VDD	Voltage regulator output	O
28	Reserved	Pin must be kept not connected	Not to be connected
29	INH	Inhibit input (wake-up)	I
30	VSREG	Voltage regulator power supply	I
31	VS	Charge pump power supply	I
32	CP1-	Charge pump pin for capacitor 1, negative side	O
33	CP1+	Charge pump pin for capacitor 1, positive side	O
34	CP2-	Charge pump pin for capacitor 2, negative side	O
35	CP2+	Charge pump pin for capacitor 2, positive side	O
36	CP	Charge pump output	O
37	VSMS	Motor supply sense pin	I
38	GH1	Gate of external high-side MOSFET 1	O
39	SH1	Source of external high-side MOSFET 1	I/O
40	GL1	Gate of external low-side MOSFET 1	O
41	SL1	Source of external low-side MOSFET 1	I/O
42	GH2	Gate of external high-side MOSFET 2	O
43	SH2	Source of external high-side MOSFET 2	I/O
44	GL2	Gate of external low-side MOSFET 2	O

Table 2. Pin definition and function (continued)

Pin number	Symbol	Function	I/O type
45	SL2	Source of external low-side MOSFET 2	I/O
46	GH3	Gate of external high-side MOSFET 3	O
47	SH3	Source of external high-side MOSFET 3	I/O
48	GL3	Gate of external low-side MOSFET 3	O

Figure 2. Pin connection (top view)



2 Device description

2.1 Supply pins (V_S, V_{SREG}, V_{SMS})

The device has three different supply input pins. V_S and V_{SREG} have to be protected against negative voltages, while V_{SMS} is robust against negative voltages.

The two-stage charge pump is supplied from V_S. External capacitors are used to achieve high current capability of the charge pump. The gate drivers (for both high-side and low-side MOSFETs) are supplied from the charge pump to ensure full drive of the external MOSFETs.

The internal power-on reset (POR) circuitry and the V_{DD} voltage regulator are supplied from the V_{SREG} pin. Some external protection has to be provided in the application for V_S and V_{SREG} to prevent the capacitor connected to these pins from being discharged by negative transients or low input voltage.

V_{SMS} is used to monitor the power supply of the external MOSFETs and as a reference for the BEMF detection.

2.1.1 V_S, V_{SREG} and V_{SMS} overvoltage warning

In case any of the supply inputs reach the overvoltage warning threshold, the corresponding overvoltage warning flag is set. This flag can be cleared by an SPI “Read & Clear” command provided that the cause of the warning is no longer present.

2.1.2 V_S, V_{SREG} and V_{SMS} overvoltage

In case any of the supply inputs reach the overvoltage threshold, the corresponding overvoltage flag is set. This flag can be cleared by an SPI “Read & Clear” command provided that the cause of the overvoltage is no longer present.

In case of V_S and V_{SMS} overvoltage, the gate drivers are disabled, along with other functions (for further details see *Table 5*). V_{SREG} overvoltage is used only for information.

2.1.3 V_S, V_{SREG} and V_{SMS} undervoltage

In case any of the supply inputs reach the undervoltage threshold, the corresponding undervoltage flag is set. This flag can be cleared by an SPI “Read & Clear” command provided that the cause of the undervoltage is no longer present.

The V_s, V_{SMS} and V_{SREG} undervoltage flags are used only for information.

2.2 V_{DD} (5V) voltage regulator

The device integrates a fully protected low-drop voltage regulator, which is designed for very fast transient response.

The voltage regulator provides a 5 V output and a continuous load current up to 200 mA to supply external devices (e.g.an external microcontroller). In addition, this regulator powers the internal 5 V loads such as the I/O pins and the current-sense amplifier (CSA). The voltage regulator is protected against overload and overtemperature. The output voltage is

stable for output capacitor greater than/equal to 660 nF (ESR < 50 mΩ) close to the device. An additional external capacitor up to 47 µF is permitted.

In case of a short circuit to GND on V_{DD} when V_{DD} is turned on (V_{DD} < V_{DDFAIL} for at least 4 ms), the device automatically enters the V_{BAT} Standby Mode and the V_{DDFAIL} flag is set. Reactivation of the device is possible through a wake-up event. The V_{DDFAIL} flag can be cleared by an SPI “Read & Clear” command, once the short circuit is removed and the device leaves the V_{BAT} Standby Mode.

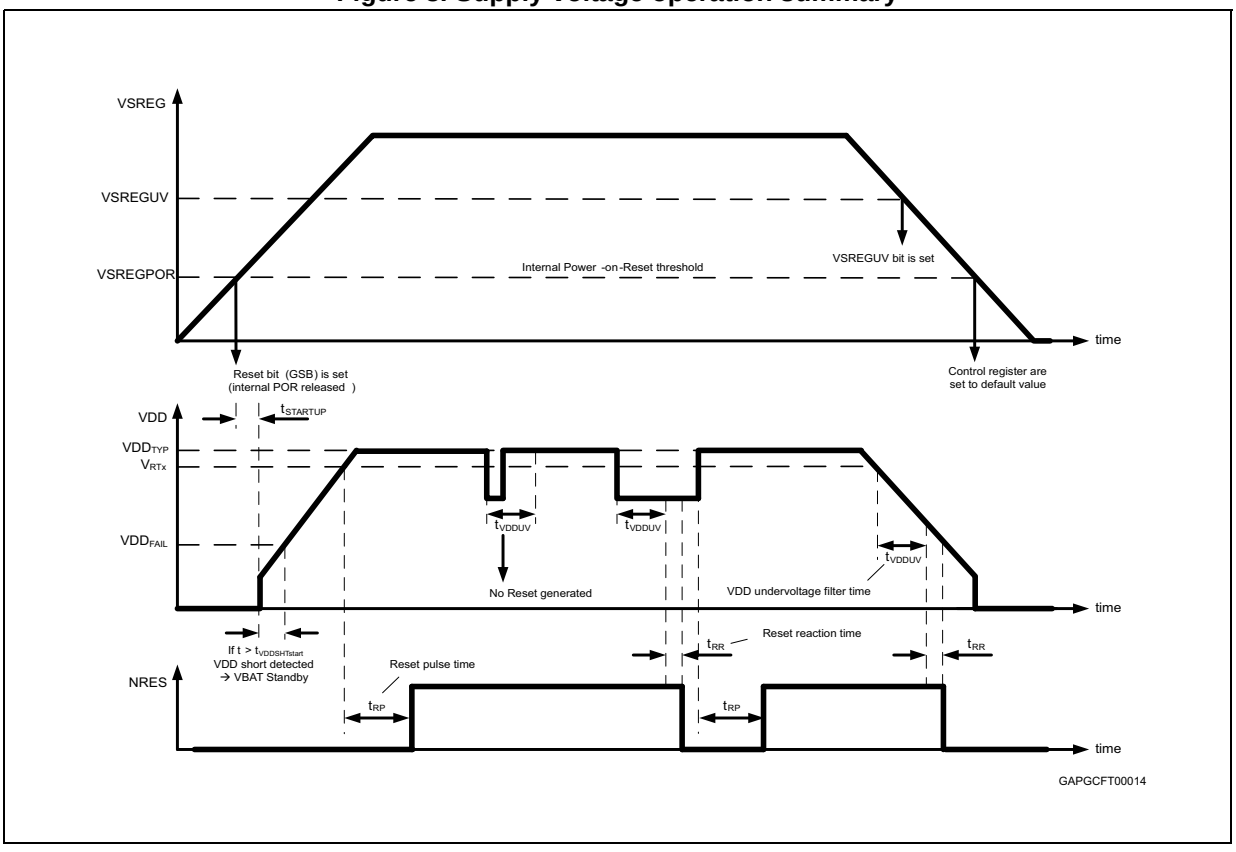
2.3 NRES reset output

In case the V_{DD} regulator is turned on and its output voltage rises above the V_{DD} reset threshold, the reset pin NRES is pulled up to V_{DD} by an internal pull-up resistor after a delay equal to t_{RP} (typ. 2 ms).

A reset pulse is generated if:

- V_{DD} drops below the V_{DD} reset threshold (VRT1 or VRT2, configurable by SPI through the VDD_VTH bit). In this case, the V_{DDUV} flag is also set and can be cleared by an SPI "Read & Clear" command, once the V_{DD} rises back above the programmed VDD_UV threshold.
- a watchdog failure occurs.

Figure 3. Supply voltage operation summary



2.4 Watchdog

A window watchdog is integrated in the device. The watchdog supervises the operation of the external microcontroller in Active Mode and, if the ICMP bit is set to '0' and $I_{VDD} > I_{CMP}$, also in V_{DD} Standby Mode.

When the device powers up and the NRES pin is released, the watchdog is started with a long open window (typ. 65 ms). The microcontroller has to write the WDTRIG bit to '1' within this time in order to terminate the long open window and start the window watchdog. After that, the watchdog has to be serviced properly by alternating the logic value written to the WDTRIG bit within the watchdog open window. A correct watchdog trigger immediately starts the next cycle.

After eight consecutive watchdog failures, the V_{DD} regulator is turned off for a time equal to t_{VDDoff} (typ. 200 ms). In case seven additional and consecutive watchdog failures occur, the V_{DD} regulator is completely turned off and the device enters V_{BAT} Standby Mode.

A watchdog failure causes a reset pulse at the NRES pin and the deactivation of the gate drivers (fail-safe condition, for further details see *Table 5*).

When the device is in Flash Mode, the watchdog is disabled. Besides even in V_{DD} Standby Mode with I_{CMP} = 1 the WDG is always disabled. If the WDDIS bit is set to '1' in Flash Mode and then a transition to Active Mode occurs, the watchdog remains disabled in Active Mode until the next POR.

After a WDG failure event, after a VDD_UV event or after a wake event from V_{BAT} Standby Mode the watchdog starts again in LOW mode. Once properly toggled the WDGTRIG bit, writing the same WDGTRIG bit value anywhere within the WDG window does not generate any WDG failure event.

Figure 4. Watchdog in normal operation mode (part 1)

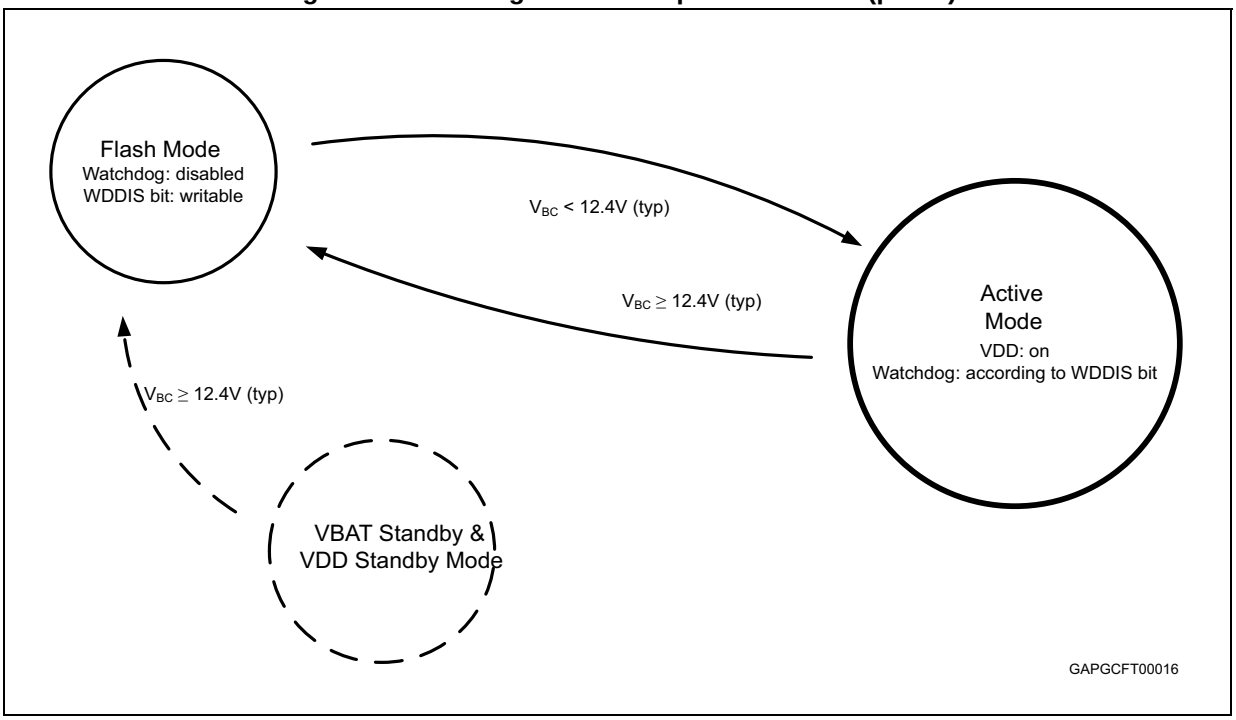


Figure 5. Watchdog in normal operation mode (part 2)

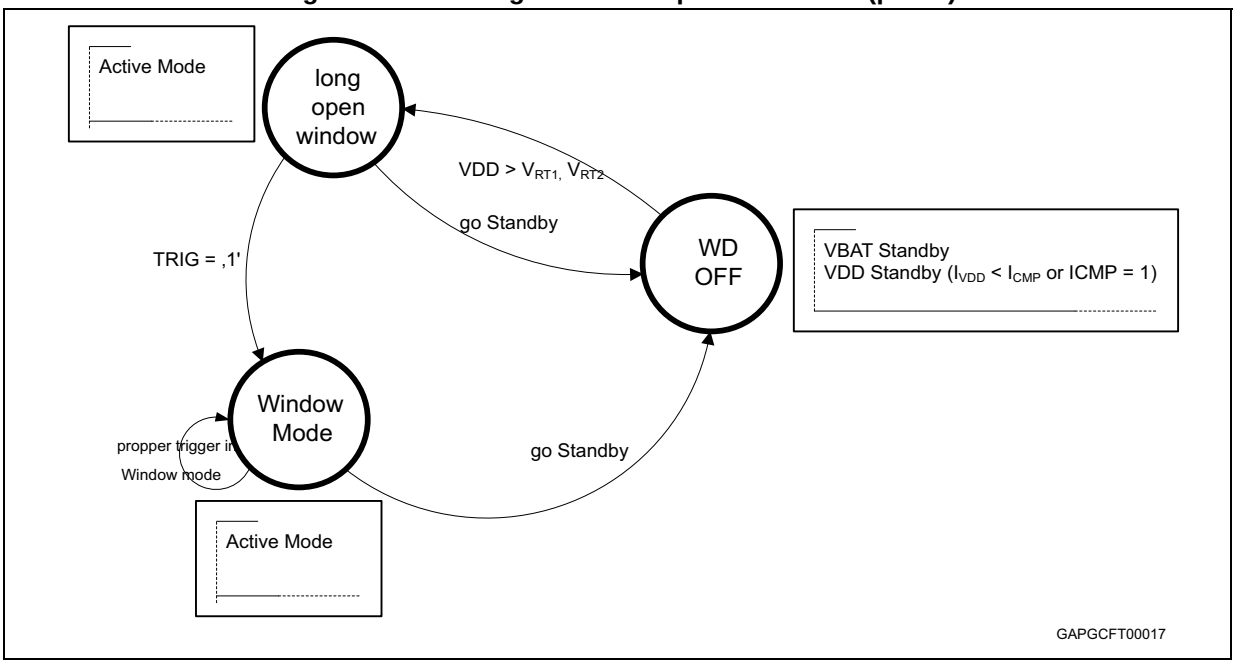


Figure 6. Watchdog in Flash Mode

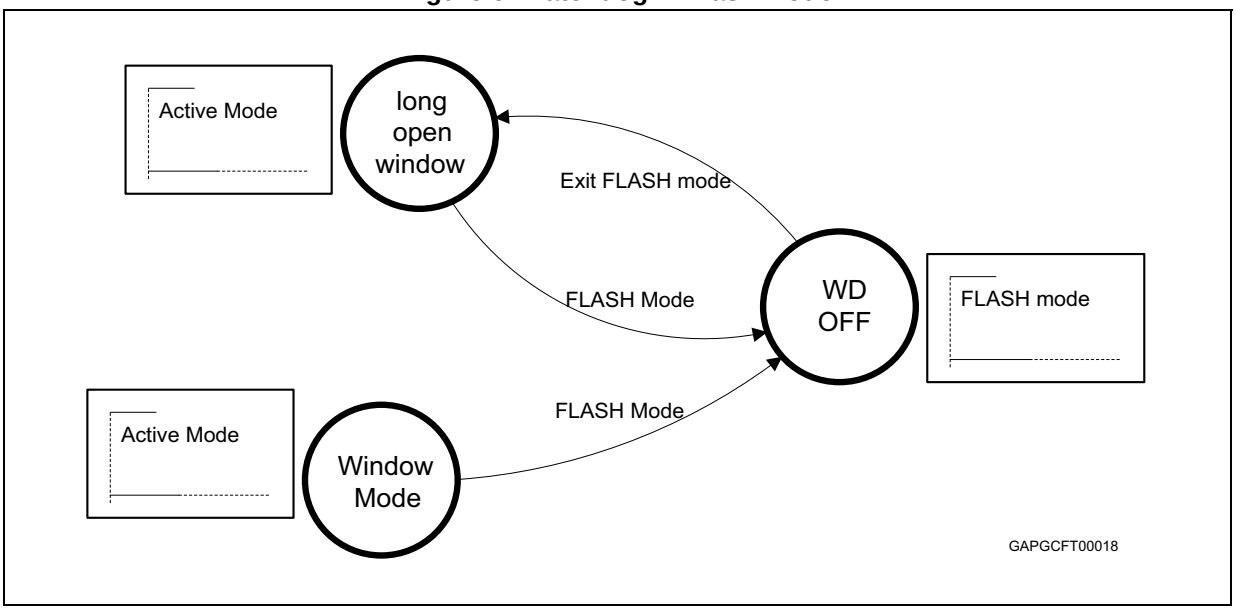
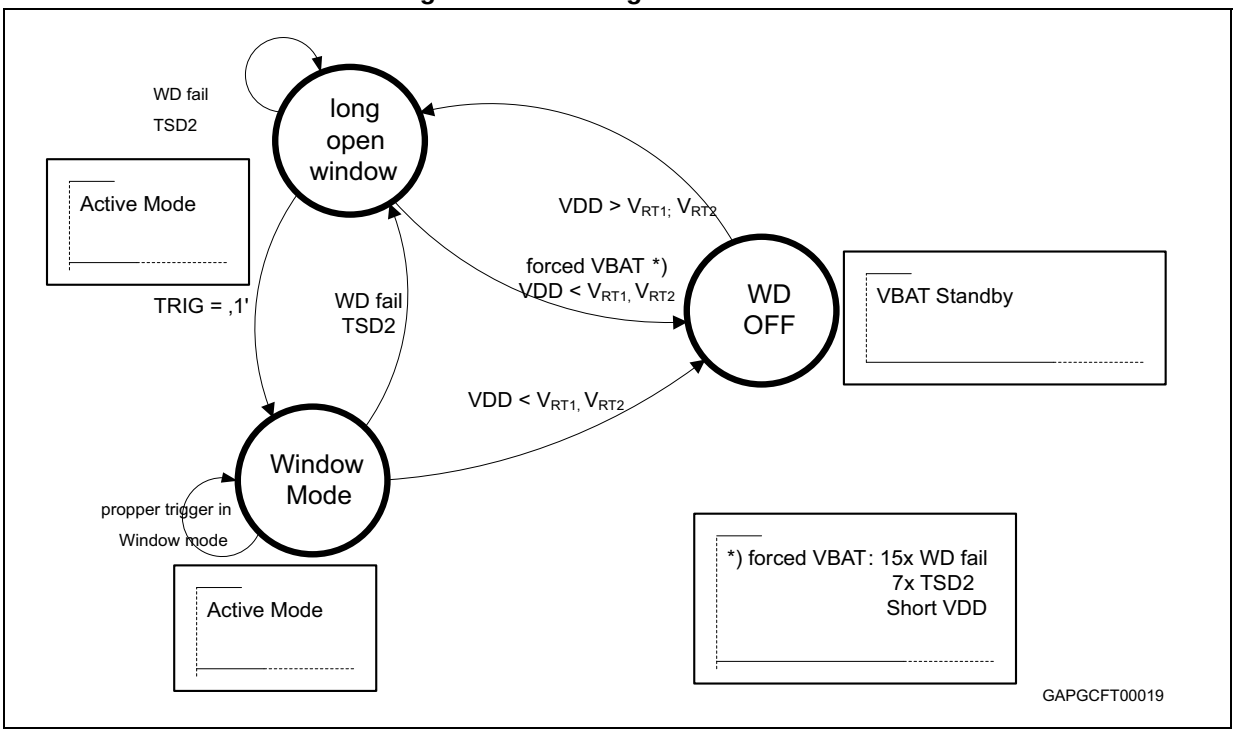


Figure 7. Watchdog in failure mode



2.5 Device operating modes

The device can be operated in four different modes:

- **Active Mode**
- **Flash Mode**
- **VDD Standby Mode**
- **VBAT Standby Mode**

2.5.1 Active Mode

The device operates with all its functions being available (VDD regulator, watchdog, gate drivers, etc).

2.5.2 Flash Mode

To program the system microcontroller, the L99ASC03G can be operated in Flash Mode where the internal watchdog is disabled and the other functions (see *Table 3*) remain available. Flash mode is entered by applying on the BC pin a voltage higher than $V_{BC,rising}$; to guarantee the proper behavior of the device, the rising V_{BC} slope must not exceed 10 V/µs.

In case $V_{BC} = V_{BC,rising}$ during device power-up (V_{SREG} connecting to VBAT), it has to be assured that the SDI pin is at GND level (V_{SDI} < 1.3 V, no external pull-up).

2.5.3 VDD Standby Mode

When the device is in VDD Standby Mode, the gate drivers, the charge pump and the CSA are disabled (SPI activation or INH pin will act as a wake-up). To supply the microcontroller in a low-power mode, the VDD voltage regulator remains active. After any wake-up event, the device switches to Active Mode and a negative pulse (typ. 56 µs) is generated on NINT pin.

The transition from Active Mode to VDD Standby Mode is selected through the STBYSEL and the GOSTBY bits.

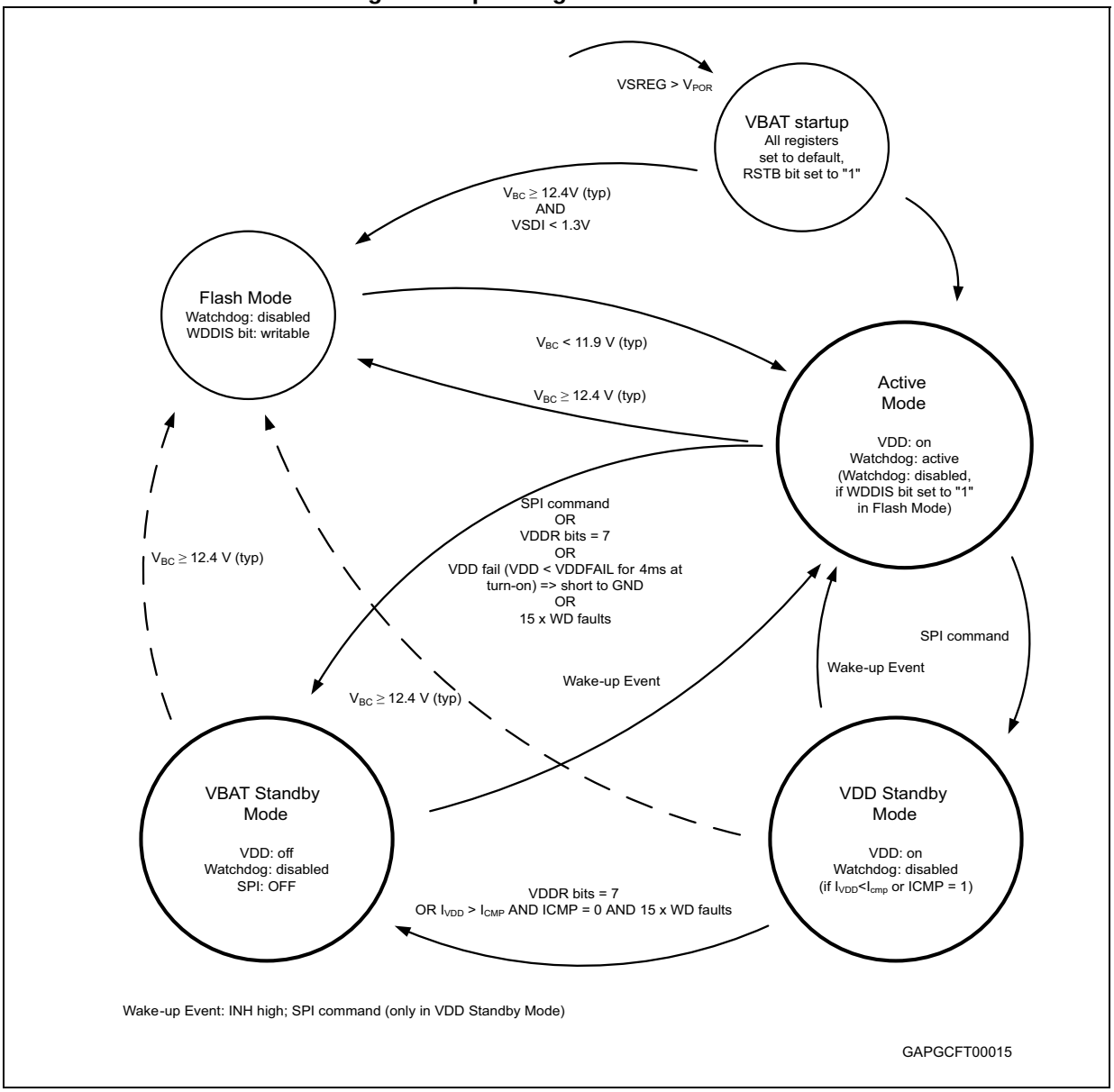
2.5.4 VBAT Standby Mode

When in VBAT Standby Mode, the VDD voltage regulator is turned off to achieve the lowest current consumption and the device monitors the occurrence of a wake-up event. After any wake-up event, the device transitions to Active Mode. The internal SPI register content is preserved.

The transition from Active Mode to VBAT Standby Mode is selected through the STBYSEL and the GOSTBY bits. This transition can also occur in case of persistent fault conditions.

2.5.5 Device mode state diagram

Figure 8. Operating mode transitions



2.5.6 Functional overview

Table 3. Functional overview

Function	Operating mode				
	Active mode		FLASH mode	VDD standby	VBAT standby
	Normal	Fail-safe			
VDD voltage regulator	ON(1)		ON	ON	OFF
Reset generator	ON		ON	ON	OFF
Interrupt generator	OFF		OFF	ON	ON
Window watchdog	ON		OFF	OFF(2)	OFF
Gate driver	ON	OFF	ON	OFF	OFF
Charge pump	ON	OFF	ON	OFF	OFF
CSA	ON	OFF	ON	OFF	OFF
BEMF module	ON	OFF	ON	OFF	OFF
Oscillator	ON		ON	OFF(3)	OFF(3)
Diagnostics	ON		ON	OFF(4)	OFF

1. OFF in case T_j > TSD2
2. ON when I_{VDD} > I_{CMP} and SPI bit I_{CMP} = 0
3. ON during wake-up event, temperature and I_{CMP} filtering
4. Temperature, I_{CMP} monitoring and V_{DD} undervoltage detection are active

2.6 DIS pin

The DIS pin allows turning off the gate drivers when applying an external signal to it. A logic low signal enables the gate drivers, whereas a logic high signal disables the gate drivers. The state of the DIS pin is reported in the DISABLE flag. To activate the gate drivers, the DIS pin has to be pulled low and the DISABLE flag has to be cleared by an SPI "Read & Clear" command. An internal pull-up resistor is integrated for this pin.

2.7 INH pin

The INH pin can be used as a wake-up source connected to ignition through an external resistor. An internal comparator detects a high level and generates a wake-up event. The INHST bit reflects the current logic state of this pin.

2.8 Thermal warning and thermal shutdown

To allow for different application requirements, two temperature modes with their respective diagnostics can be selected via SPI.

2.8.1 Normal mode: TEMPM = ‘0’ (TW1, TSD1, TSD2)

If the junction temperature reaches the TW1 threshold, the TW1 flag is set and latched as a thermal warning for the external microcontroller. In case the junction temperature increases and reaches the TSD1 threshold, the gate drivers and the charge pump are disabled and the TSD1/TW2 flag is set and latched. If the junction temperature rises further and reaches the TSD2 threshold, the VDD regulator is also turned off to reduce power dissipation and the TSD2 flag is set and latched. A counter (VDDR bits) is increased upon the VDD turn-off. After a time equal to t_{TSD}, the VDD regulator is turned on again. If the VDDR bits reach the '111' state, the device is forced into VBAT Standby Mode. This mode is left upon any wake-up event.

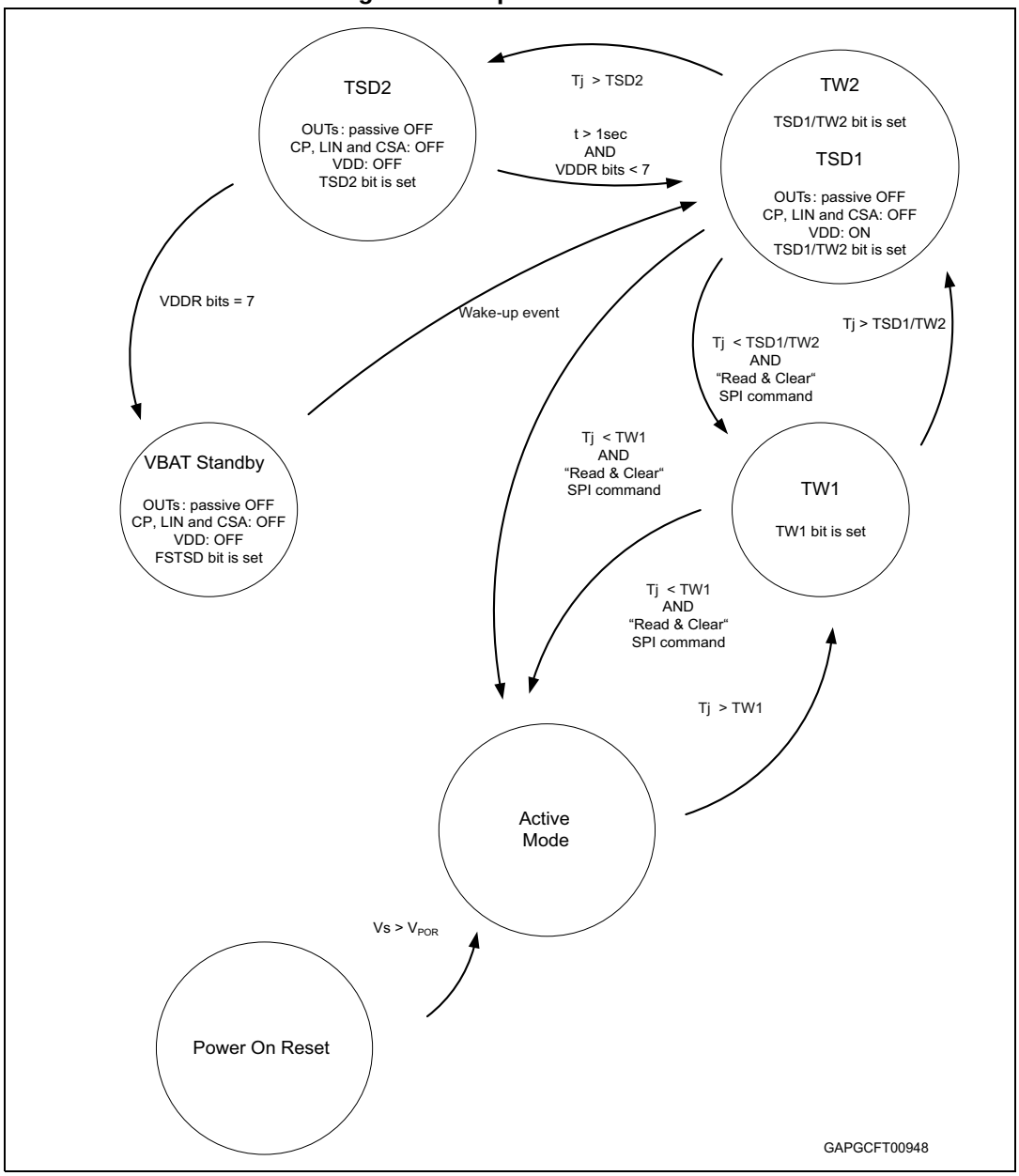
The TW1, TSD1/TW2 and TSD2 flags can all be cleared by an SPI Read & Clear command, provided that the junction temperature is below the respective temperature threshold.

2.8.2 Warning mode: TEMP = ‘1’ (TW1, TW2, TSD2)

If the junction temperature reaches the TW1 threshold, the TW1 flag is set and latched as a first thermal warning for the external microcontroller. In case the junction temperature increases and reaches the TW2 threshold, the TSD1/TW2 flag is set and latched as a second thermal warning. If the junction temperature rises further and reaches the TSD2 threshold, the gate drivers and the charge pump are disabled, the VDD regulator is turned off to reduce power dissipation and the TSD2 flag is set and latched. A counter (VDDR bits) is increased upon the VDD turn-off. After a time equal to t_{TSD}, the VDD regulator is turned on again. If the VDDR bits reach the '111' state, the device is forced into VBAT Standby Mode. This mode is left upon any wake-up event.

The TW1, TSD1/TW2 and TSD2 flags can all be cleared by an SPI Read & Clear command, provided that the junction temperature is below the respective temperature threshold.

Figure 9. Temperature modes



2.9 Wake-up events

A wake-up event in standby mode generates a transition to Active Mode. Three possible wake-up sources are defined, as illustrated in *Table 4*.

Table 4. Wake-up events

Wake-up source	Description
SPI Access	CSN pin low and first rising edge on SCK pin, active only in VDD Standby Mode
INH	High level on the INH pin, active in both standby modes

All wake-up events from VDD Standby Mode generate a low-pulse on NINT pin for 56 µs (typical).

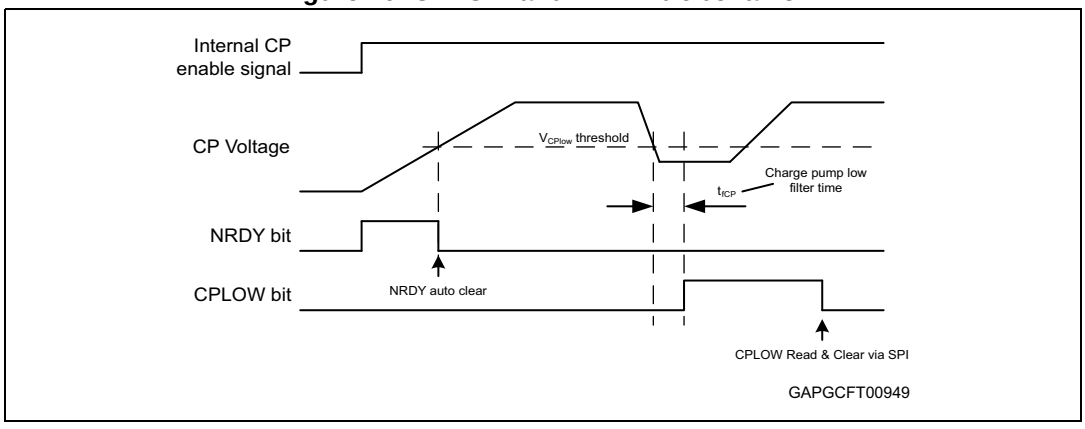
2.10 Charge pump

The two-stage charge pump is supplied from the V_S pin. External charging capacitors are used to achieve a high current capability of the charge pump. In VBAT Standby Mode, VDD Standby Mode or after thermal shutdown the charge pump is disabled. It is also possible to disable the charge pump by setting the CPDIS bit to "1".

In case the charge pump output voltage remains below the V_{CPLOW} threshold for longer than t_{fCP}, all gate drivers are switched off (resistive path to source) and the CPLOW flag is set and latched. The NRDY flag shows that the charge pump is not ready after a startup condition.

In order to minimize electromagnetic emissions, the charge pump frequency can be modulated in a programmable range through the WOBM and WOBF bits.

Figure 10. CPLOW and NRDY bit behavior



2.11 Gate drivers

Each of the three half-bridge drivers is controlled independently by dedicated inputs for the high-side driver (IHx, active low, with internal pull-up resistor) and for the low-side driver (ILx, active high, with internal pull-down resistor). All the gate drivers feature a minimum cross-current protection time (dead-time) t_{CCP} (programmable through the CCT bits) and

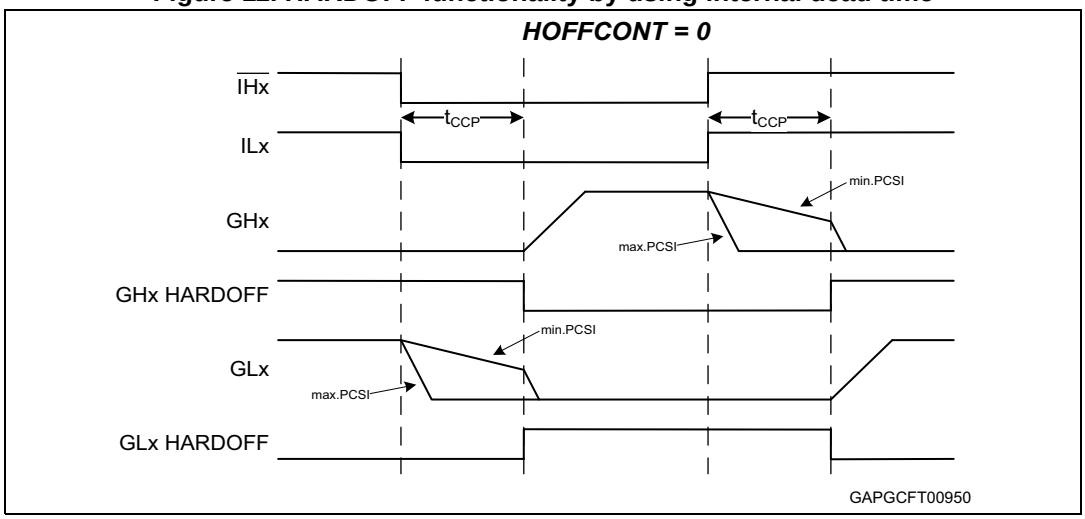
shoot-through protection. The minimum t_{CCP} is applied between outputs GHx and GLx only if a lower (or null) dead-time is present between inputs ILx and $\overline{IHx}$ (see *Figure 18*). In case the $\overline{IHx}$ and the ILx input of a half bridge are active at the same time, both gate driver outputs (high side and low side) are turned off. In addition, if $\overline{IHx}$ and ILx are both driven active for longer than t_{CCP}, the affected half bridge is disabled and the ST(x) error flag is set. To re-enable the half bridge, this fault condition has to be removed and the corresponding ST(x) flag has to be reset through an SPI "Read & Clear" command.

The gate driver circuit limits the gate-source voltage of the external MOSFETs. All gate driver circuits are independent of each other and use their source connection to the external MOSFET as a reference.

In order to drive different MOSFETs and adjust the gate currents according to external conditions (e.g. temperature), the source and sink current (i.e. the charging and discharging current) of the gate driver can be programmed via SPI.

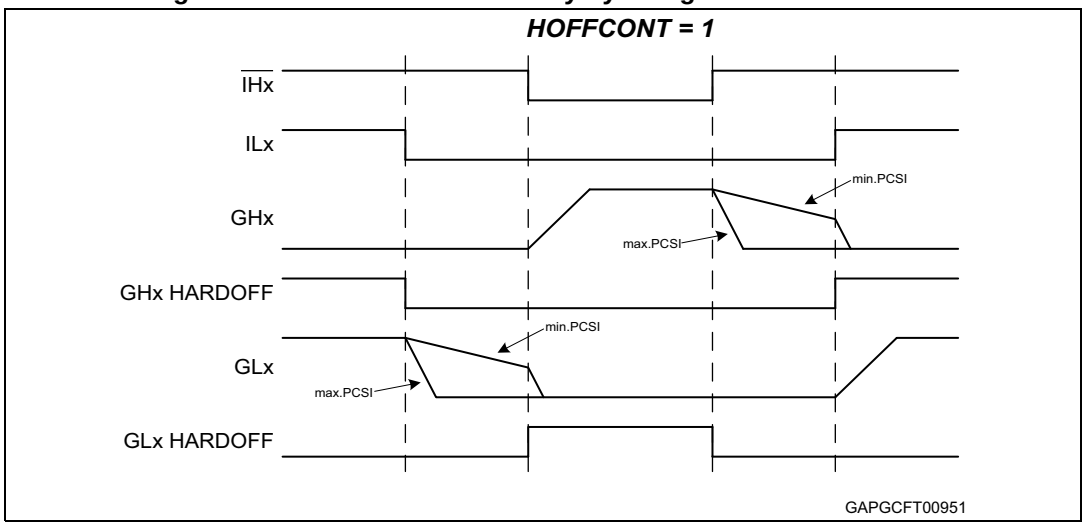
The HARDOFF feature is an additional measure against cross-current conduction in a half bridge. When the HOFFCONT bit is set to 0, any of the outputs GHx and GLx is switched off using maximum sink current (max PCSI) after a t_{CCP} from related turn-off command. When the HOFFCONT bit is set to 1, any of the outputs GHx and GLx is switched off using maximum sink current (max PCSI) as soon as the complementary output signal (respectively GLx or GHLx) goes to high.

Figure 11. HARDOFF functionality by using internal dead time



1. Propagation delay is omitted for convenience.

Figure 12. HARDOFF functionality by using external dead time



1. Propagation delay is omitted for convenience.

2.12 Drain-source monitoring

2.12.1 Drain-source monitoring in ON state (short-circuit detection)

The drain-source voltage of each activated external MOSFET is monitored by internal comparators to detect short circuits to ground or battery. In case the voltage drop over the external MOSFET exceeds the threshold voltage VSCd, the corresponding DSHS(x) or DSLS(x) flag is set. In addition, if the DSFT_DIS bit is set to "0", the affected MOSFET is turned off and the related gate driver is disabled.

The drain-source monitoring has a filter time and is only active when the corresponding gate driver is in source condition.

The threshold voltage VSCd can be programmed in four steps between 0.5 V and 2 V via SPI.

2.12.2 Drain-source monitoring in OFF state (open-load / short-circuit detection)

In Active Mode, each gate driver sources a current of typ. 500 µA at the SHx pins in OFF condition. By programming the ISTEST(x) bits to "1", a sink current of typ. 800 µA is applied to the corresponding pin.

By using these internal test currents, an open load, a leakage to GND or to battery can be detected on each motor phase in OFF state, i.e. without turning on the external MOSFETs.

If the ISTEST_EN bit is set to "1", the drain-source voltage monitoring is enabled also in OFF condition and the Status Register 7 reflects the result of the voltage comparison (i.e. drain-source voltage below or above the programmed threshold) in real time (i.e. the status bits are not latched) and without setting the FE bit in the Global Status Byte. See *Section 2.18: Diagnostics* for more details about diagnostics.

In order to allow the SHx pins to go below GND, the current sink has a diode in series and the sink current will disappear below 0.8V. Therefore, when using the test currents, the drain-source voltage threshold should be programmed to a value greater than 0.8V.

2.13 Current-sense amplifier

The current-sense amplifier (CSA) is designed for low-side current measurement in automotive motor control applications. The CSA differential input stage measures the voltage generated by the motor current over an external shunt resistor. The input common-mode range allows the CSA input pins to go below GND, as typically required in PWM motor control applications due to switching transients. The CSA gain can be programmed over a wide range by setting the GCSA bits.

In case of zero differential input voltage, the output voltage is at half scale:

VCSO = 0.5 * VDD

2.14 Overcurrent detection

To protect the application from overcurrent, an overcurrent threshold can be programmed via SPI by setting the OCTH bits. The CSA output is compared to the programmed threshold. In case of overcurrent, the CSAOC flag is set and, depending on the DMUX bit, the DOUT output goes high. In addition, if the OCSHUTD bit is set, the gate drivers are disabled.

The overcurrent detection feature can be used to estimate the rotor position of the motor at standstill without any rotation by applying voltage to the motor windings and detecting overcurrent with respect to an appropriate threshold.

2.15 BEMF module

The programmable BEMF (back electromotive force) module integrated in the device provides a flexible means to support those applications where the BLDC motor is driven in sensorless mode and that are based on BEMF detection.

2.15.1 BEMF comparator

Depending on the PWM driving method used in the application, three different comparators can be selected through the BEMFMOD bits to detect the BEMF zero-crossing point. BEMF detection can be done during the PWM ON state or the PWM OFF state. In the former case, the $V_{SMS}/2$ comparator (i.e. internally referenced to half of the V_{SMS} supply) can be used. In the latter case, the GND comparator (i.e. internally referenced to GND) or the V_{SMS} comparator (i.e. internally referenced to the V_{SMS} supply) can be used, depending on whether the PWM signal is applied to the external high-side or low-side MOSFET (this reflects the setting of the BEMFSW bit).

As some applications may require advancing the timing of a phase commutation (“pre-commutation”), it is possible to add an offset to the internal reference voltage of the $V_{SMS}/2$ comparator. The absolute offset value can be programmed through the BEMFOS bits. To achieve pre-commutation, the offset sign (i.e. positive or negative) has to vary, depending on whether the BEMF is rising or falling. The offset sign can be selected via SPI by programming the BEMFSIGN bit.

2.15.2 BEMF comparator sampling

In order to avoid unwanted commutations of the BEMF comparator due to PWM switching and spurious noise on the motor phases, an intelligent sampling mechanism is implemented to detect the BEMF zero-crossing point. Depending on the BEMFSW bit (PWM switching mode), BEMFMOD bit (comparator selection) and BEMFPOL bit, it is possible to select the triggering instant used to sample and latch the output of the selected BEMF comparator, which is in turn made available at the BEMFOUT pin. The following cases are possible:

- PWM on high-side MOSFET
  - BEMF detection in PWM ON state, BEMF sampling on PWM switch turn-off
  - BEMF detection in PWM OFF state, BEMF sampling on PWM switch turn-on or complementary PWM switch turn-off
- PWM on low-side MOSFET
  - BEMF detection in PWM ON state, BEMF sampling on PWM switch turn-off
  - BEMF detection in PWM OFF state, BEMF sampling on PWM switch turn-on or complementary PWM switch turn-off

It is worth noting that this method allows having a stabilized BEMF signal at the motor phase before the phase voltage can change, thanks to the turn-on and turn-off delay associated to the gate driver and the external MOSFET.

If no PWM is applied to the motor (100% duty cycle), the output of the BEMF comparator can be sampled by using an internal clock edge. In this case, the BEMFBY bit has to be set.

2.15.3 BEMF commutation driving mode

The BEMFCNT bits are used to set the motor phase to be monitored by the BEMF comparator. According to BEMFCM bit value, BEMFCNT bits can be either programmed through SPI by the system microcontroller or automatically updated by L99ASC03G.

In particular:

- If BEMFCM = '0', the external microcontroller is intended to update BEMFCNT bits through SPI command every time the BEMF comparator has to monitor another motor phase.
- If BEMFCM = '1', the BMFCNT bits are automatically increased (if BEMFDIR = '0') or decreased (if BEMFDIR = '1') whenever the L99ASC03G receives a triggering pulse on BC pin. In order to properly operates, triggering pulse amplitude on BC pin must be coherent with $V_{in\,H}$ (see *Table 24*) electrical parameter.

2.16 Digital multiplexer (DOUT)

An integrated digital multiplexer provides a digital signal on the DOUT pin. Depending on the setting of the DMUX bit and of the OCFT_DIS bit, it is possible to select between a fail-safe flag signal, a CSA overcurrent flag signal or the overcurrent comparator output.

2.17 Analog multiplexer (AOUT)

By setting the AMUX bits via SPI, an integrated analog multiplexer provides an output voltage proportional to the input supply voltages (V_S, V_{SREG} or V_{SMS}), to the internal chip temperature T_j or to the CSA reference voltage.

2.18 Diagnostics

All diagnostic functions are internally filtered and each fault/warning condition has to be valid for a defined time before the corresponding status bit is set in the status register. The filters are used to improve the noise immunity of the device. Several error types and warnings can be distinguished. All errors and warnings are reported in the corresponding status bits and are mirrored in the associated bits of the Global Status Byte (GSB).

- The device reacts to several error types by changing its state. The different error types can be grouped as follows:
- fail-safe errors (mirrored in the FS bit of the GSB)
- device errors (mirrored in the DE bit of the GSB)
- functional errors (mirrored in the FE bit of the GSB)
- physical-layer errors (mirrored in the PLE bit of the GSB)
- SPI errors (mirrored in the SPIE bit of the GSB)

In order for the device to recover from an error condition, the error itself must be removed and the associated status bit in the device has to be cleared via SPI by a “Read & Clear” command.

Warning functions are intended only for information and will not change the state of the device. Warnings are mirrored in the GW bit of the GSB. To clear a warning, the source of the warning must be removed and the associated flag has to be cleared via SPI by a “Read & Clear” command.

Table 5. Diagnostics overview

Source	Cause	Event type	Diagnosis	Device action	Clear error / warning flag
MCU	Watchdog not triggered or triggered out of the open window	FS (FS = 1 in the GSB)	FSWD = 1; Watchdog fail counter WDF>0	– NRES asserted low – Gate drivers actively discharged; charge pump, CSA and BEMF module OFF – Control registers (except Control Register 1 and DSFT_DIS) reset to default value	– After NRES is released, write WDTRIG = 1 during watchdog long open window to reset WDF counter bits – Read & Clear FSWD

Table 5. Diagnostics overview (continued)

Source	Cause	Event type	Diagnosis	Device action	Clear error / warning flag
VDD	Short circuit at VDD turn-on	FS (FS = 1 in the GSB)	VDDFAIL = 1	– Gate drivers actively discharged; charge pump, CSA and BEMF module OFF – Control registers (except Control Register 1 and DSFT_DIS) reset to default value	Read & Clear VDDFAIL
	Undervoltage (V_{DD} < reset threshold)	FS (FS = 1 in the GSB)	VDDUV = 1	– NRES asserted low – Gate drivers actively discharged; charge pump, CSA and BEMF module OFF – Control registers (except Control Register 1 and DSFT_DIS) reset to default value	Read & Clear VDDUV
	Undervoltage warning (V_{DD_VTH} = 0 and V_{DD} < V_{RT2})	GW (GW = 1 in the GSB)	VRT2LOW = 1	– None	Read & Clear VRT2LOW
SPI	SDI short circuit to GND or VDD	FS and SPIE (FS = 1 and SPIE = 1 in the GSB)	SPI_DI = 1 and SPIE = 1 in the GSB	– Gate drivers actively discharged; charge pump, CSA and BEMF module OFF – Control registers (except Control Register 1 and DSFT_DIS bits) reset to default value – SPI frame ignored	Read & Clear SPI_DI
	CSN timeout or SCK clock count other than 0 or 16	GW and SPIE (GW = 1 and SPIE = 1 in the GSB)	SPI_FL = 1 and SPIE = 1 in the GSB	SPI frame ignored	Read & Clear SPI_FL

Table 5. Diagnostics overview (continued)

Source	Cause	Event type	Diagnosis	Device action	Clear error / warning flag
Input supply	V_S undervoltage ($V_S < V_{SUV}$)	DE (DE = 1 in the GSB)	V_{SUV} = 1	None	Read & Clear V_{SUV}
	V_S overvoltage ($V_S > V_{SOV}$)	DE (DE = 1 in the GSB)	V_{SOV} = 1	Gate drivers actively discharged; charge pump disabled	Read & Clear V_{SOV}
	V_{SMS} overvoltage ($V_{SMS} > V_{SMSOV}$)	DE (DE = 1 in the GSB)	V_{SMSOV} = 1	Gate drivers actively discharged; charge pump disabled	Read & Clear V_{SMSOV}
	V_{SREG} or V_{SMS} undervoltage ($V_{SREG} < V_{SREGUV}$ or $V_{SMS} < V_{SMSUV}$)	GW (GW = 1 in the GSB)	V_{SREGUV} = 1 or V_{SMSUV} = 1	None	Read & Clear V_{SREGUV} or V_{SMSUV}
	V_{SREG} overvoltage ($V_{SREG} > V_{SREGOV}$)	GW (GW = 1 in the GSB)	V_{SREGOV} = 1	None	Read & Clear V_{SREGOV}
	V_S, V_{SREG} or V_{SMS} overvoltage warning	GW (GW = 1 in the GSB)	V_{SOVW} = 1 or $V_{SREGOVW}$ = 1 or V_{SMSOVW} = 1	None	Read & Clear V_{SOVW}, $V_{SREGOVW}$ or V_{SMSOVW}
DIS pin	DIS pin at logic high	FE (FE = 1 in the GSB)	DISABLE = 1	Gate drivers actively discharged	Read & Clear DISABLE
CSA	Overcurrent	– GW (GW = 1 in the GSB) if OCSHUTD = 0 – FE (FE = 1 in the GSB) if OCSHUTD = 1	CSAOC = 1	Gate drivers actively discharged if OCSHUTD = 1	Read & Clear CSAOC
Gate drivers	Drain-source monitor threshold	– GW (GW=1 in the GSB) if DSFT_DIS=1 – FE (FE=1 in the GSB) if DSFT_DIS=0	DSLS(x) = 1 or DSHS(x) = 1	Affected gate driver actively discharged if DSFT_DIS = 0	Read & Clear DSLS(x) or DSHS(x)
	Shoot-through protection activated	FE (FE = 1 in the GSB)	ST(x) = 1	Affected half-bridge actively discharged	Read & Clear ST(x)

Table 5. Diagnostics overview (continued)

Source	Cause	Event type	Diagnosis	Device action	Clear error / warning flag
Temperature	T_j > TW1	GW (GW = 1 in the GSB)	TW1 = 1	None	Read & Clear TW1
	T_j > TW2	GW (GW = 1 in the GSB)	TW1 = 1 TSD1/TW2 = 1	None	Read & Clear TSD1/TW2 (and TW1)
	T_j > TSD1	DE (DE = 1 in the GSB)	TW1 = 1 TSD1/TW2 = 1	Gate drivers actively discharged; charge pump, CSA and BEMF module OFF	Read & Clear TSD1/TW2 (and TW1)
	T_j > TSD2	FS (FS = 1 in the GSB)	TW1 = 1 TW2/TSD1 = 1 TSD2 = 1	– Gate drivers actively discharged; charge pump, CSA and BEMF module OFF – Control registers (except control register 1 and DSFT_DIS bit) reset to default value – VDD turned off	Read & Clear TSD2
Charge pump	Charge pump undervoltage (VCP<VCPLOW) when charge pump running	- GW (GW = 1 in the GSB) if CPLOWM = 0 - FE (FE = 1 in the GSB) if CPLOWM = 1	CPLOW = 1	Gate drivers disabled if CPLOWM = 1	Read & Clear CPLOW
	Charge pump undervoltage (VCP<VCPLOW) after charge pump is enabled	- GW (GW = 1 in the GSB) if CPLOWM = 0 - FE (FE = 1 in the GSB) if CPLOWM = 1	NRDY = 1	Gate drivers disabled regardless of CPLOWM control bit value	Self cleared

Some specific fail-safe errors will force the device to transition to VBAT Standby Mode in order to avoid potential damage to the system. *Table 6* provides an overview of these cases. The device leaves the VBAT Standby Mode upon any wake-up event.

Table 6. Forced V_{BAT} standby mode

Source	Cause	Diagnosis	Clear error flag
MCU	Watchdog not triggered or triggered out of the open window for 15 consecutive times (WDF = 1111)	FSWD = 1	Read & Clear FSWD

Table 6. Forced V_{BAT} standby mode (continued)

Source	Cause	Diagnosis	Clear error flag
VDD	Short circuit at VDD turn-on	VDDFAIL = 1	Read & Clear VDDFAIL
Temperature	Tj>TSD2 for 7 times (VDDR = 111)	TSD2 = 1	Read & Clear TSD2

Figure 13. Persistent watchdog failure (V_{BAT} Standby Mode entered after 15 watchdog faults)

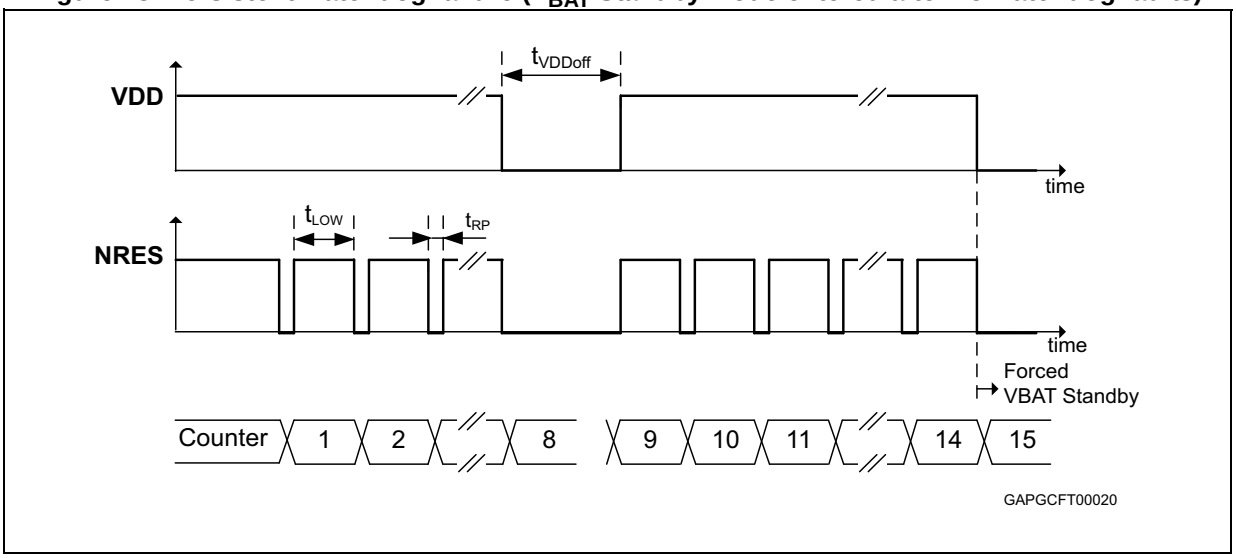
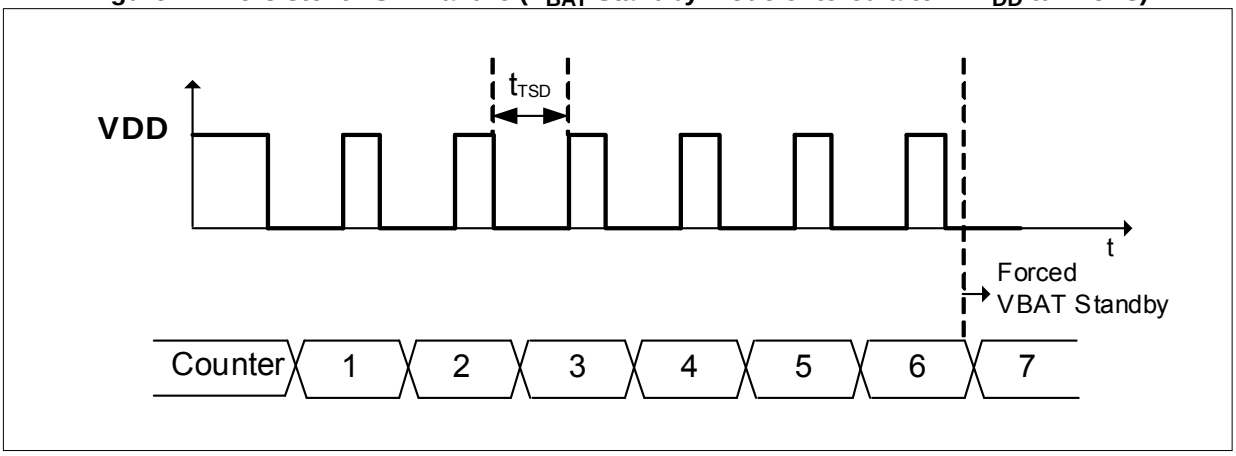


Figure 14. Persistent TSD2 failure (V_{BAT} Standby Mode entered after 7 V_{DD} turn-offs)



2.19 Serial peripheral interface (ST SPI standard)

A 16-bit ST SPI is used for bi-directional communication with an external microcontroller.

Through SPI it is possible to trigger the watchdog, control the operating modes, adjust some device parameters and read out diagnostic information of several device modules.

During standby modes, the SPI is generally deactivated.

The SPI has to be driven in the following mode:

CPOL = 0 and CPHA = 0.

For this mode, input data are sampled on the low-to-high transition of the clock SCK and output data are changed on the high-to-low transition of SCK.

This device is not limited to microcontroller with a built-in SPI. Only three CMOS-compatible output pins and one input pin will be needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the SDO pin will reflect the global error flag (fault condition) of the device.

- Chip Select Not (CSN)

  The input pin is used to select the serial interface of this device. When CSN is high, the output pin (SDO) will be in high-impedance state. In case CSN is stuck at GND, a timeout is implemented which sets the SDO back to high-impedance to release the SPI network. A low signal activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame.

- Serial Data In (SDI)

  The input pin is used to transfer data serially into the device. The data applied to the SDI will be sampled on the rising edge of the SCK signal and shifted into an internal 16-bit shift register. On the rising edge of the CSN signal, the contents of the shift register will be transferred to Data Input Register. The writing to the selected Data Input Register is only enabled if exactly 16 bits are transmitted within one communication frame (CSN low). Only frames with 0 or 16 clock pulses are accepted. All others will be ignored and a communication error will be reported with the next SPI command. This safety function is implemented to avoid activating of the output stages in case of a wrong communication frame.

Note: Due to this safety functionality, SPI daisy chaining is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.

- Serial Data Out (SDO)

  The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level, depending on the global error flag (fault condition). The first rising edge of the SCK input after a high-to-low transition of the CSN pin will transfer the content of the selected status register into the data out shift register. Each subsequent falling edge of the SCK will shift the next bit out.

- Serial Clock (SCK)

  The SCK input is used to synchronize the input and output serial bit streams. The data input (SDI) is sampled on the rising edge of the SCK and the data output (SDO) will change with the falling edge of the SCK signal. The SPI can be driven with a SCK frequency up to 4.5 MHz.

3 Electrical specifications

3.1 Absolute maximum ratings

Table 7. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{SREG}	Voltage regulator power supply voltage	-0.3 to 40	V
V_S	Charge pump power supply voltage	-0.3 to 40	V
V_{SMS}	Sensed motor supply voltage	-5 to 40(1)	V
V_{DD}	Stabilized supply voltage	-0.3 to 6	V
V_{IHX}, V_{ILX}	Gate driver control voltage range	-0.3 to V_{DD}	V
V_{SLX}, V_{SHX}	Source signal voltage range	-5 to 40(1)	V
V_{GLX}	Gate signal voltage range	-5 to V_{SLX} + 15(1)	V
V_{GHX}		-5 to V_{SHX} + 15(1)	V
V_{CSIP}, V_{CSIN}	Current sense amplifier input voltage range	-5 to V_{DD}(1)	V
V_{CSO}, V_{AOUT}	Current sense amplifier output voltage range; analog output MUX	-0.3 to V_{DD}	V
V_{CP1-}, V_{CP2-}	HV signal range	-0.3 to V_S	V
V_{CP1+}, V_{CP2+}, V_{CP}	HV signal range	V_S - 0.3 to V_S + 17	V
V_{SDI}, V_{SCK}, V_{SDO}	SPI logic I/O voltage range	-0.3 to V_{DD}	V
V_{TXD}, $V_{RXD/NINT}$, V_{DIS}, V_{NRESET}, V_{DOUT}, V_{BEMF}, V_{CSN}	Logic I/O voltage range	-0.3 to V_{DD}	V
V_{INH}	High Voltage Logic I/O voltage range	-0.3 to 40	V
V_{BC}	High Voltage Logic I/O voltage range	-0.3 to 20	V

1. -7 V for < 1.5 µs transients

Note: All maximum ratings are absolute ratings. Exceeding any of these values may cause an irreversible damage of the integrated circuit!

3.2 Operating range

Table 8. Operating range

Symbol	Parameter	Value	Unit
V_{SREG}	Voltage regulator power supply voltage	6 to 28	V
V_S	Charge pump power supply voltage	6 to 28	V

Table 8. Operating range (continued)

Symbol	Parameter	Value	Unit
V_{SMS}	Sensed motor supply voltage	6 to 28	V
V_{CSIP}, V_{CSIN}	Current sense amplifier input voltage range	-1 to 1	V
V_{SDI}, V_{SCK}, V_{CSN}	SPI logic input voltage range	0 to V_{DD}	V
V_{TXD}, V_{DIS}, V_{INH}	Logic input voltage range	0 to V_{DD}	V

3.3 ESD protection

Table 9. ESD protection

Parameter	Value	Unit
HBM all pins	±2	kV
CDM all pins	±500	V
CDM corner pins	±750	V

Note: HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114-D
HBM with all unzapped pins grounded

3.4 Thermal data

Table 10. Operation junction temperature

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{stg}	Storage temperature		-55		150	°C
T_j	Operating junction temperature		-40		150	°C
T_{J_Peak}	Dynamic junction temperature 100hrs over lifetime(1)			160		°C
$R_{th\ j\text{-}amb}$	Thermal resistance to ambient(2)			33		°C/W
$R_{th\ j\text{-}case}$	Thermal resistance to case			12		°C/W

1. According to the mission profile.
2. IC soldered on 2s2p PCB thermally enhanced.

Table 11. Temperature warning and thermal shutdown

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
TW1	Temp. warning threshold 1	TEMPM = X	120	135	150	°C
TW2	Temp. warning threshold 2	TEMPM = 1	140	155	170	°C
TSD1	Thermal shutdown threshold 1	TEMPM = 0				°C
TSD2	Thermal shutdown threshold 2	TEMPM = X	160	175	190	°C

Table 11. Temperature warning and thermal shutdown (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{SDH}	Thermal shutdown hysteresis			5		°C
$t_{TW/TSD}$	Thermal filter time			16		µs

3.5 Electrical characteristics

Voltages are referred to ground and currents are assumed positive, when the current flows into the pin. The device is operated in the specified operating range, unless otherwise specified.

Table 12. Supply and supply monitoring

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SOVW}, $V_{SREGOVW}$, V_{SMSOVW}	Overvoltage warning threshold		18	20	22	V
V_{SOV}, V_{SREGOV}, V_{SMSOV}	Overvoltage threshold		28.1	30	32	V
V_{SOVH}, $V_{SREGOVH}$, V_{SMSOVH}	Overvoltage hysteresis			2		V
V_{SUV}, V_{SREGUV}, V_{SMSUV}	Under-voltage threshold	V_S, V_{SREG}, V_{SMS} decreasing	5.2	5.5	5.7	V
V_{SUVH}, $V_{SREGUVH}$, V_{SMSUVH}	Undervoltage hysteresis			0.4		V
t_{fVS}, t_{fVREG}, t_{fVSMS}	Overvoltage and undervoltage filter time		30		80	µs
I_S	Current consumption	V_S = V_{SREG} = V_{SMS} = 12 V; active mode; open outputs		5	10	mA
I_{SREG}	Current consumption	V_S = V_{SREG} = V_{SMS} = 12 V; active mode; open outputs		15	25	mA
I_{SREGQ} + I_{SMQ} +I_{SQ}	Quiescent current in V_{BAT} stand-by	V_S = V_{SREG} = V_{SMS} = 12 V; V_{BAT} standby (no wakeup); T_{Test} = -40°C to 25°C; open outputs		24	38.5	µA
	Quiescent current in V_{DD} stand-by	V_S = V_{SREG} = V_{SMS} = 12 V; V_{DD} standby; SCK = INH = $\overline{SDI}$ = ILx = 0; CSN = DIS = $\overline{IHx}$ = 1; T_{Test} = -40°C to 25°C; open outputs		40	57	µA
I_{SMS}	V_{SMS} DC input current	V_S = V_{SREG} = V_{SMS} = 12 V; active mode; SLx vs. GND			2	mA

Table 13. Power-on RESET (V_{SREG})

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{PORSREG,rising}$	Threshold (V_{SREG} increasing)	All outputs open			4.5	V
$V_{PORSREG,falling}$	Threshold (V_{SREG} decreasing)	All outputs open	3		4	V
$V_{PORSREG,hyst}$	Hysteresis	All outputs open		0.3		V

Table 14. Voltage regulator V_{DD}

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DD}	Output voltage	I_{load} = 0 mA to 200 mA 6 V <Vs < 18 V -40°C < Tj < 150°C	4.865	5.0	5.1	V
t_{SST}(1)	Startup settling time from V_{DD} standby to Active mode (no NRES)	20 µA to 50 mA; V_{DD} ± 2%; C_{EXT} = 47 µF; dI/dt = 50 mA/µs			250	µs
		20 µA to 100 mA; V_{DD} ± 2.5%; C_{EXT} = 47 µF; dI/dt = 100 mA/µs			130	µs
V_{DP}	Drop-out Voltage	I_{LOAD} = 50 mA; V_{SREG} = 4.5 V		0.2	0.4	V
		I_{LOAD} = 100 mA; V_{SREG} = 4.5 V		0.3	0.5	V
I_{DD}	Output current in active mode	Max. continuous load current			200	mA
$I_{DDinrush}$(1)	Inrush current capability	V_{SREG} > 6 V; V_{DD} > V_{RT2}; $C_{EXT} \geq$ 4.7 µF			200	mA
I_{DDpeak}	Peak output current	V_{SREG} > 6 V; V_{DD} > V_{RT2}			300	mA
$I_{DDshort}$	Short circuit output current	Current limitation	300	600	950	mA
t_{TSD}	V_{DD} deactivation time after thermal shutdown		0.8	1.0	1.5	s
$ICMP_{RISE}$	Current comparator rising threshold	Rising current		3.6	4.6	mA
$ICMP_{FALL}$	Current comparator falling threshold	Falling current	2.0	3.4		mA
$ICMP_{H}$	Current comparator hysteresis			0.2		mA
V_{DDFAIL}	V_{DD} fail threshold	V_{DD} short to ground during startup	1.8	2	2.2	V
$t_{VDDFAIL}$	V_{DD} short to ground detection time	V_{DD} short to ground during startup	3.4	4.0	7.0	ms
dV_{DD}/dt	dV_{DD}/dt at regulator turn-on	C_{CER} = 680 nF; C_{ELE} = 47 µF; $I(V_{DD})$ = 10 mA. Slope from 0.5 V to 1 V and slope from 1 V to 0.9 * V_{DD}. If current limitation is reached, the slope is controlled by the current limitation and output capacitor.	3		30	V/ms

Table 14. Voltage regulator V_{DD} (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{DDso,max}$	Maximum V_{DD} output voltage at regulator turn-on	C_{CER} = 680 nF; C_{ELE} = 47 µF; $I(V_{DD})$ = 10 mA. Internal soft-start function			5.3	V
PSRR(1)	Power supply rejection ratio (specified by design)	V_r = 0.5 Vpp; fr = 100 Hz; C_{CER} = 680 nF		60		dB

1. Guaranteed by design.

Table 15. NRES reset output (V_{DD} supervision), NINT

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{RT1}	V_{DD} reset threshold 1	V_{DD} increasing; V_{DD_VTH} = 0	3.55	3.7	3.85	V
		V_{DD} decreasing; V_{DD_VTH} = 0	3.15	3.3	3.45	V
V_{RT1H}	V_{DD} reset threshold 1 hysteresis			0.4		V
V_{RT2}	V_{DD} reset threshold 2	V_{DD} increasing; V_{DD_VTH} = 1	4.45	4.65	4.8	V
		V_{VDD} decreasing; V_{DD_VTH} = 1	4.4	4.6	4.75	V
V_{RT2H}	V_{DD} reset threshold 2 hysteresis			0.06		V
V_{RESETL}	NRES pin low output voltage	V_{DD} > 1 V; I_{RESET} = 1 mA		0.2	0.4	V
R_{RESET}	NRES pull up internal resistor		60	110	204	kΩ
t_{RR}	NRES reaction time	At I_{LOAD} = 1 mA		20		µs
t_{RP}	NRES pulse time		1.7	2	3.5	ms
t_{VDDoff}	V_{DD} turn-off time			200		ms
t_{VDDUV}	V_{DD} undervoltage filter time		13		28	µs
t_{NINT}	NINT pulse time			56		µs

Table 16. Watchdog

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{LOW}	Long open window		48	65	70	ms
t_{CW}	Closed window		2.6		4.7	ms
t_{WDP}	Watchdog period		16		23	ms

Figure 15. Watchdog timing (Long, Early, Late and Safe Window)

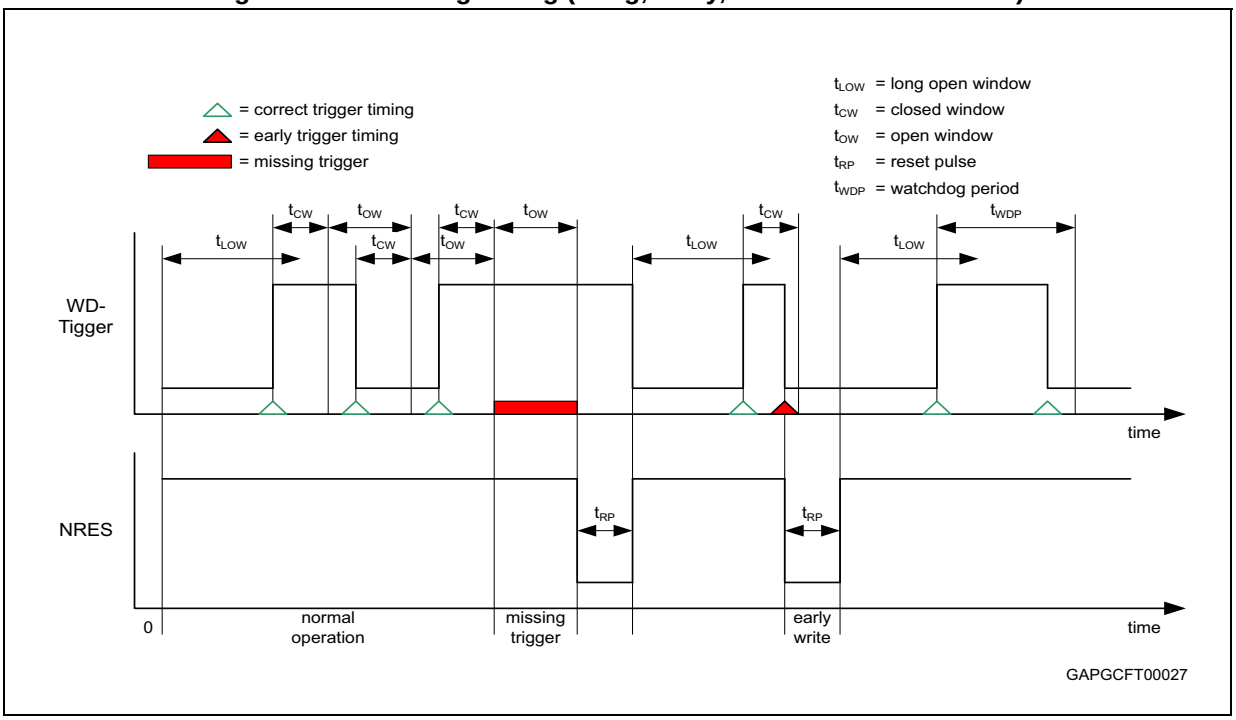


Figure 16. Watchdog missing

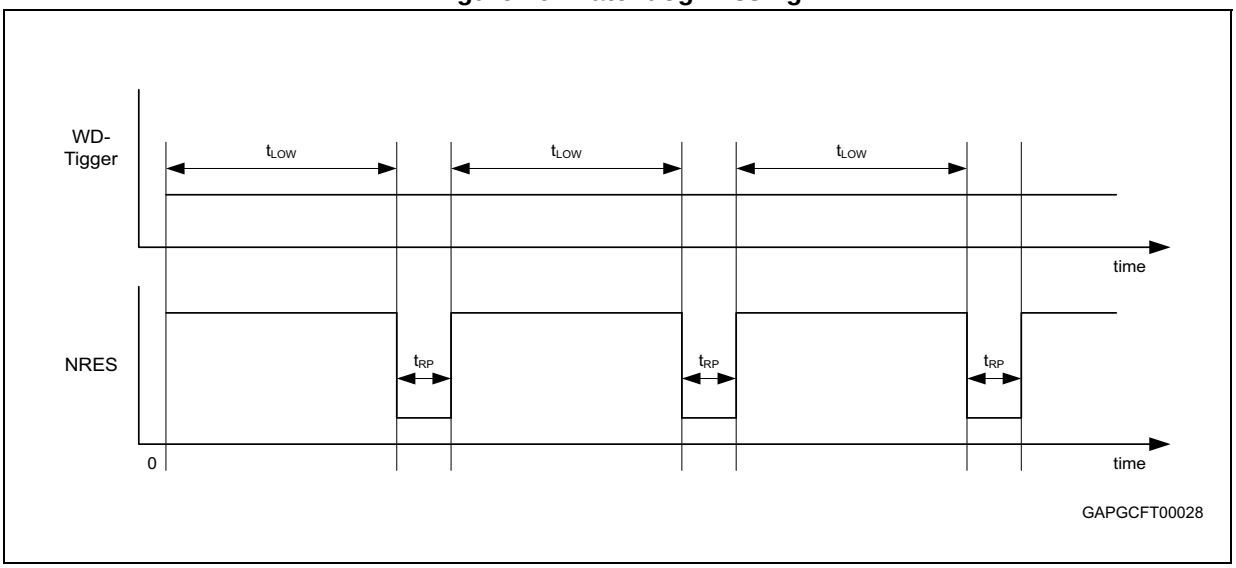


Figure 17. Watchdog early, late and safe window

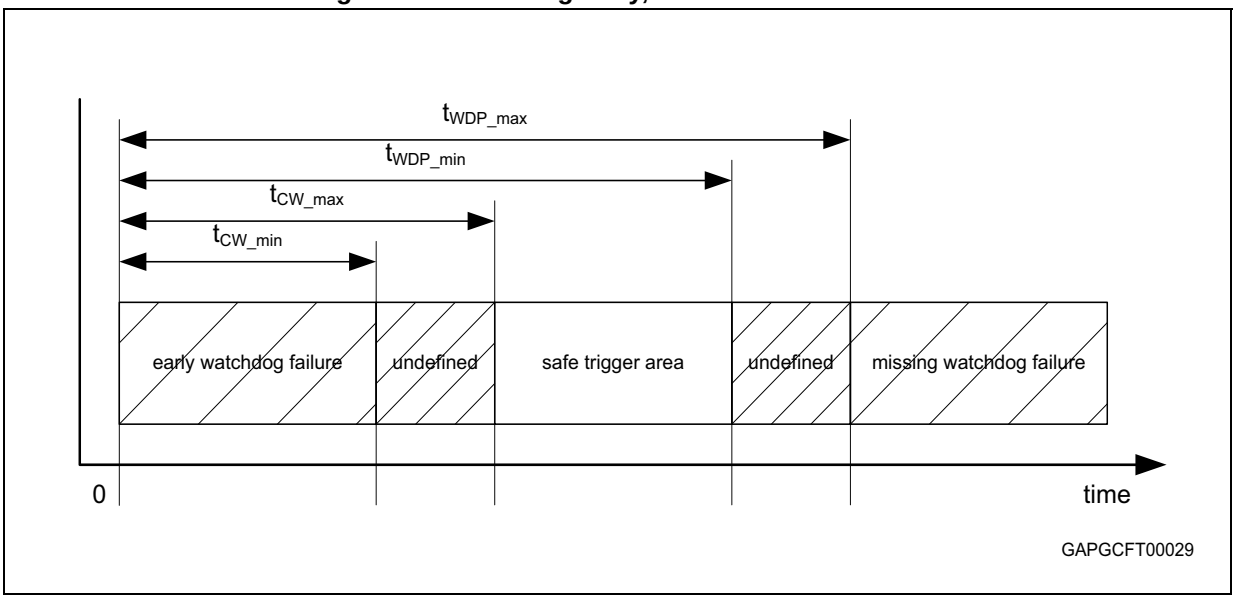


Table 17. Charge pump output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CP}	Charge pump output voltage	V_S = 6 V; I_{CP} = -20 mA; C_{CPx} = 220 nF; C_{CP} = 1 µF	V_S + 7.7			V
		V_S = 6 V; I_{CP} = 20 mA; C_{CPx} = 220 nF; C_{CP} = 1 µF; -40 °C < T_j < 25 °C	V_S + 8.3			V
		V_S = 12 V; I_{CP} = 0 mA; C_{CPx} = 220 nF; C_{CP} = 1 µF	V_S + 11	V_S + 13	V_S + 16.5	V
I_{CP}	Charge pump output current	V_S = 12 V; V_{CP} = V_S + 10 V; C_{CPx} = 220 nF; C_{CP} = 1 µF	20			mA
V_{CPLOW}	Charge pump low voltage threshold		V_S + 5.6	V_S + 6.0	V_S + 6.75	V
f_{CP}	Clock frequency (internal oscillator)		140	200	260	kHz
t_{fCP}	Charge pump low filter time		6		14	µs

Table 18. Gate driver for external MOSFET

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
High-side gate drivers DC parameter						
$I_{GHx(on)}$	Turn-on maximum peak current (SOURCE stage)	T_j = 25°C; PCSO = 1111		-250		mA
	Turn-on minimum peak current (SOURCE stage)	T_j = 25°C; PCSO = 0001		-20		mA

Table 18. Gate driver for external MOSFET (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{GHx(off)}$	Turn-off maximum peak current (SINK stage)	V_{SHx} = 0 V; PCSI = 1111; T_j = 25°C		500		mA
	Turn-off minimum peak current (SINK stage)	V_{SHx} = 0 V; PCSI = 0001; T_j = 25°C		40		mA
V_{GHxH}	High-level voltage	V_S = 6 V; I_{CP} = 20 mA	V_{SHx} + 7			V
		V_S = 12 V; I_{CP} = 20 mA	V_{SHx} + 9	V_{SHx} + 11	V_{SHx} + 13	V
R_{GSHx}	Gate-source passive discharge resistance		16	20	24	kΩ
Low-side driver DC parameter						
$I_{GLx(on)}$	Turn-on maximun peak current (SOURCE stage)	T_j = 25°C; PCSO = 1111		-185		mA
	Turn-on minimum peak current (SOURCE stage)	T_j = 25°C; PCSO = 0001		-12		mA
$I_{GLx(off)}$	Turn-off maximun peak current (SINK stage)	V_{SLx} = 0 V; PCSI = 1111; T_j = 25°C		700		mA
	Turn-off minimum peak current (SINK stage)	V_{SLx} = 0 V; PCSI = 0001; T_j = 25°C		40		mA
V_{GLxH}	High-level voltage	V_S = 6 V; I_{CP} = 20 mA	V_{SLx} + 7			V
		V_S = 12 V; I_{CP} = 20 mA	V_{SLx} + 9	V_{SLx} + 11	V_{SLx} + 13	V
R_{GSLx}	Gate-source passive discharge resistance		16	20	24	kΩ
Gate drivers dynamic parameters						
t_{PGXxLH}	Propagation delay time, low to high	V_S = 12 V; C_G = 10 nF	300		700	ns
	Propagation delay time, high to low	V_S = 12 V; C_G = 10 nF	100		170	ns
t_{PGXx}	Propagation delay time, channel difference	V_S = 12 V; C_G = 10 nF			115	ns
t_{GXxR}	Rise time (20% to 80%)	V_S = 12 V; C_G = 10 nF		250		ns
t_{GXxF}	Fall time (80% to 20%)	V_S = 12 V; C_G = 10 nF		150		ns
t_{CCP}	Programmable cross-current protection time	CCT = 000	100		200	ns
		CCT = 001	300		400	ns
		CCT = 010	500		600	ns
		CCT = 011	700		800	ns
		CCT = 100	900		1000	ns
		CCT = 101	1200		1300	ns
		CCT = 110	1600		1700	ns
		CCT = 111	2000		2100	ns

Timings are measured at 20% and 80% for falling and rising transitions.

Figure 18. Cross-current protection time generation when $\overline{IHx}$ and ILx are tied together

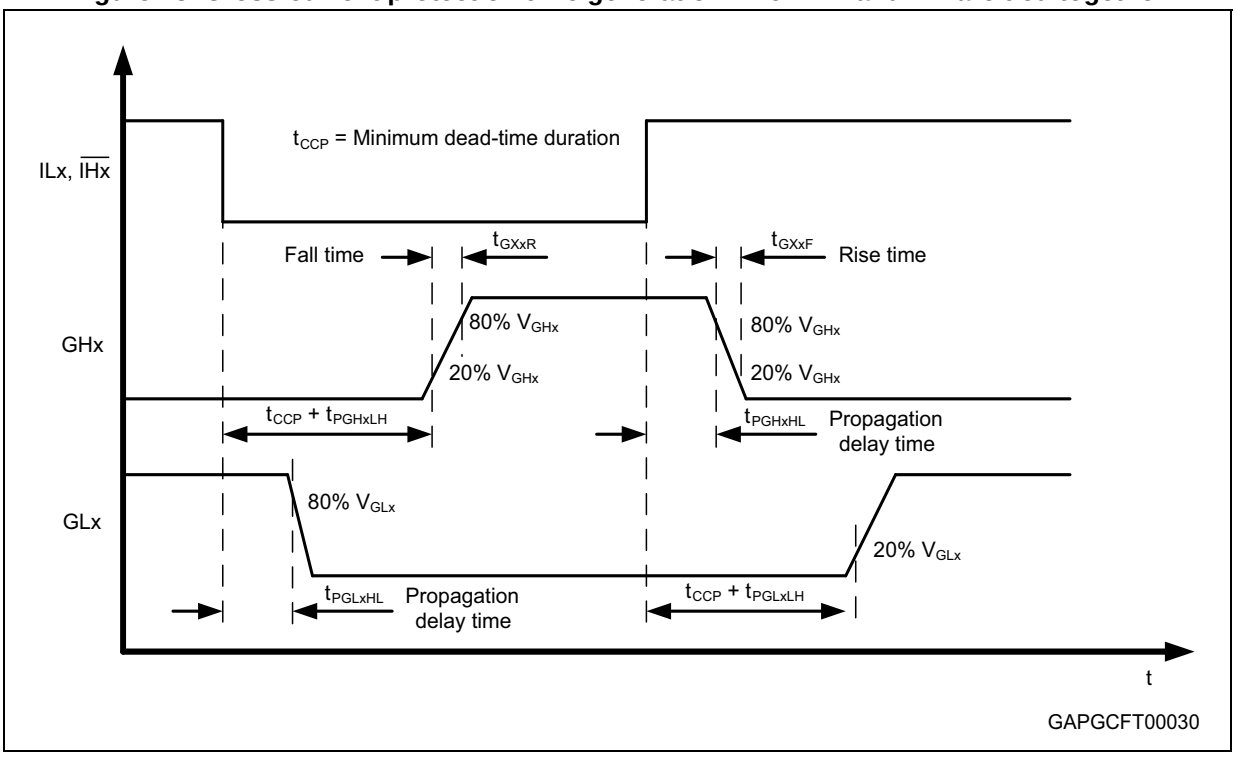


Figure 19. Cross-current protection time generation when at $t_{DT} > t_{CCP}$ is provided an input

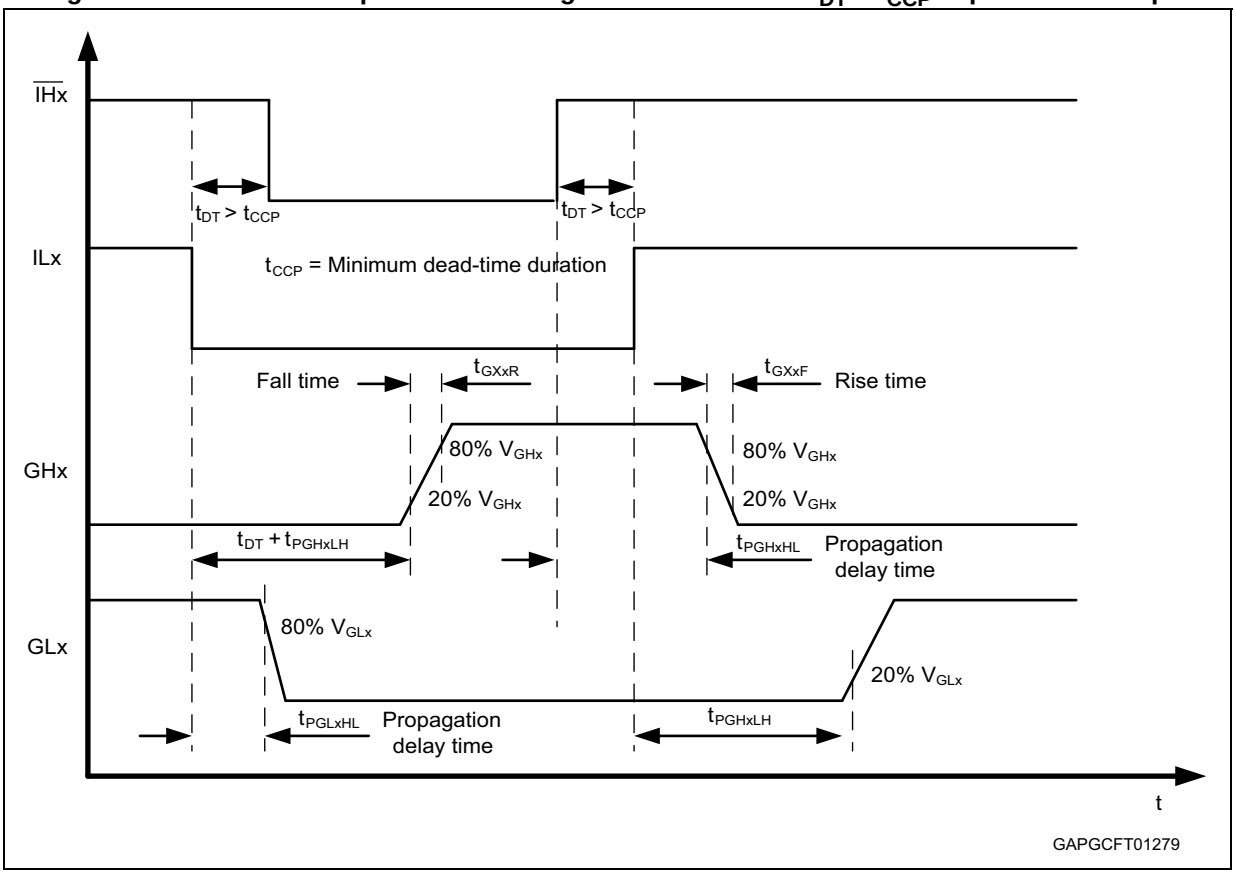


Table 19. Drain source monitoring

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SCd1}	Drain-source voltage threshold 1	DSMTH = 00	0.4	0.5	0.6	V
V_{SCd2}	Drain-source voltage threshold 2	DSMTH = 01	0.9	1.0	1.1	V
V_{SCd3}	Drain-source voltage threshold 3	DSMTH = 10	1.35	1.5	1.65	V
V_{SCd4}	Drain-source voltage threshold 4	DSMTH = 11	1.85	2.0	2.15	V
t_{b1}	Blanking time DS Monitor	DSMFT = 0	1.0	1.2	1.5	µs
t_{b2}	Blanking time DS Monitor	DSMFT = 1	2.0	2.4	3.0	µs
t_{f1}	Filter time DS Monitor	DSMFT = 0	1.0	1.2	1.5	µs
t_{f2}	Filter time DS Monitor	DSMFT = 1	2.0	2.4	3.0	µs
I_{SHx}	Diagnostic source current	All gate drivers off; ISTEST(x) = 0		-500		µA
	Diagnostic sink current	All gate drivers off; ISTEST(x) = 1		1		mA

Table 20. V_S, V_{SREG}, V_{SMS} and T_j monitoring (AOUT)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SxOUT}	V_{SxOUT} voltage ratio	A_{OUT} sinking/ sourcing 2 mA	0.106	0.125	0.144	
V_{TROOM}	T_{SENSE} output voltage (5 * VBE)	V_S = 12 V, T_j = 25°C	—	3.7	—	V
$\Delta V/\Delta T_j$	Temperature coefficient	T_j = -40°C to 130°C	—	-7.85	—	mV/°C

Table 21. Current-sense amplifier

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
CSA DC parameters						
A_{20}	DC gain	GCSA = 00	18.4	19.6	20.4	
A_{30}	DC gain	GCSA = 01	29.4	30	30.6	
A_{70}(1)	DC gain	GCSA = 10	67.9	70	72.1	
A_{100}(1)	DC gain	GCSA = 11	97.5	100	102.5	
$\Delta A_X/\Delta T_j$	Gain temperature drift				100	ppm/°C
V_{IO}	Input offset voltage	-200 mV < CSI- < 1 V	-3.5		3	mV
V_{ICM}	Common-mode input voltage range		-1		1	V
V_{CSOH}	Output high level	I_L = -1 mA	V_{DD} - 0.2			V
V_{CSOL}	Output low level	I_L = 1 mA			0.2	V
$V_{CS-IL=0}$	Output level at I_{LOAD} = 0	CSI+ = CSI-; I_{CSO} = 0		V_{DD} / 2		
I_{CSO}	Current output capability			2		mA
CSA dynamic parameters						
SR	Slew rate V_{CSO} 10% to 90%	R_L = 10 kΩ; C_L = 100 pF		2		V/µs
t_{set}	Recovery time V_{CSO} = 95%	R_L = 10 kΩ; C_L = 100 pF; Vdiff: 1 V step to 100 mV; Gain = 20			3	µs
CMRR(1)	Input common mode rejection ratio 20 * log ((V_{ICM} / ΔV_{CSO}) * A_X)	V_{ICM} = 0.7 * sin (2*π*0.1 MHz)	60			dB

1. Guaranteed by design.

Table 22. Overcurrent detection

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{oOCMIN}	Minimum output overcurrent threshold voltage(1)	OCTH = 00001		140		mV
V_{oOCMAX}	Maximum output overcurrent threshold voltage(1)	OCTH = 11111		2.35		V
t_{fOC}	Overcurrent filter time		4		6	µs

1. Positive threshold referred to V_{DD}/2.

Table 23. BEMF detection

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{BEMFx}	Comparator threshold of V_{SMS} / 2 comparator	V_{SMS} = 12 V; BEMFMOD = 1	V_{SMS} / 2 - 0.13	V_{SMS} / 2	V_{SMS} / 2 + 0.13	V
ΔV_{BEMFx}	Minimum comparator offset of V_{SMS} / 2 comparator	V_{SMS} = 12 V; BEMFMOD = 1; BEMFOS = 001		0.0025 * V_{SMS}		mV
ΔV_{BEMFx}	Maximum comparator offset of V_{SMS} / 2 comparator	V_{SMS} = 12 V; BEMFMOD = 1; BEMFOS = 111	0.16 * V_{SMS} - 0.13	0.16 * V_{SMS}	0.16 * V_{SMS} + 0.13	V
V_{BEMFx}	Comparator threshold of GND comparator	V_{SMS} = 12 V; BEMFMOD = 0; BEMFSW = 0	-0.1	0	0.1	V
V_{BEMFx}	Comparator threshold of V_{SMS} comparator	V_{SMS} = 12V; BEMFMOD = 0; BEMFSW = 1	V_{SMS} - 0.1	V_{SMS}	V_{SMS} + 0.1	V
t_{COMP}	Comparator delay time	(V_{SMS} ± 200 mV) / 2		2		µs

Table 24. I/Os; $\overline{IHx}$, ILx, DIS, BC, BEMF, DOUT

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{in\ L}$	Input low level				1.6	V
$V_{in\ H}$	Input high level		1.8		5.5	V
$V_{in\ Hyst}$	Input hysteresis			0.4		V
$V_{BC,rising}$	Threshold for entering Flash Mode, rising voltage		11.4	12.4	13.5	V
$V_{BC,falling}$	Threshold for entering Flash Mode, falling voltage		10.9	11.9	13.0	V
R_{DIS} / R_{IHx}	Pull up resistor at input DIS, $\overline{IHx}$		50	100	200	kΩ
R_{BC} / R_{ILx}	Pull down resistor at input BC, ILx		50	100	200	kΩ
t_{dDIS}(1)	Activation delay time				4.5	µs
V_{BEMFL} / V_{DOUTL}	Output low level	I_{LOAD} = 1 mA		0.2	0.4	V
V_{BEMFH} / V_{DOUTH}	Output high level	I_{LOAD} = -1 mA	V_{DD} - 0.4 V			V
I_{BEMF} / I_{DOUT}	Current output capability			2		mA
C_I(1)	Input capacitance			10		pF
C_O(1)	Output capacitance			30		pF

1. Not tested guaranteed by design.

Table 25. INH input

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{TH}	Current threshold			80	120	µA
I_{PD}	Pull-down current	V_{IN} = 12 V	30	70		µA
I_H	Current hysteresis		5	10	20	µA
t_{AMIN}	Minimum activation time		55		110	µs

3.6 SPI electrical characteristics

Table 26. CSN input

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{in,L}$	Input voltage low level				1.3	V
$V_{in,H}$	Input voltage high level		2.0		V_{DD}	V
$V_{in,Hyst}$	Input hysteresis			0.4		V
R_{CSN}	CSN pull-up resistor		50	100	200	kΩ

Table 27. SCK, SDI input

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{set}	Delay time from standby to active mode	Switching from standby to active mode. Time until output drivers are enabled after CSN going to high.		160	300	µs
$V_{in,L}$	Input voltage low level				1.3	V
$V_{in,H}$	Input voltage high level		2.0		V_{DD}	V
$V_{in,Hyst}$	Input hysteresis			0.4		V
R_{SCK}, R_{SDI}	Pull-down resistor at SCK and SCI		50	100	200	kΩ

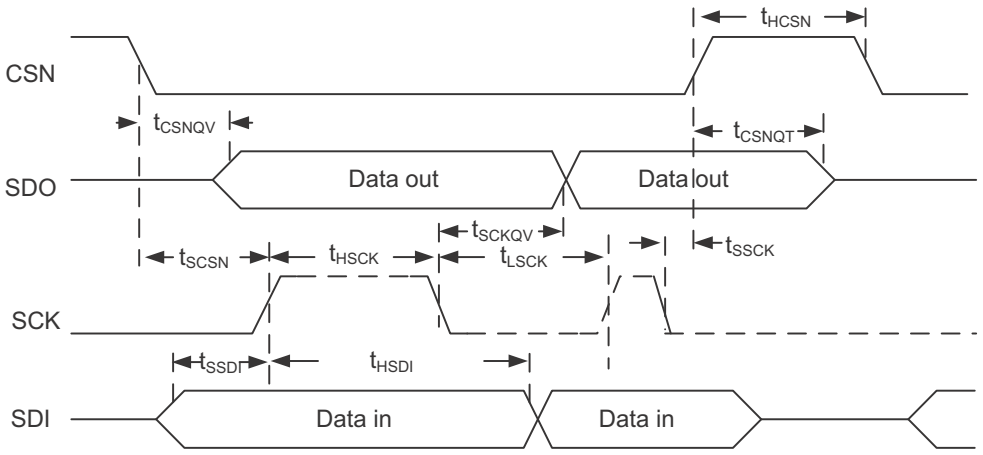
Table 28. SDO output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SDOL}	Output low level	I_{SDO} = 1 mA		0.2	0.4	V
V_{SDOH}	Output high level	I_{SDO} = -1 mA	V_{DD} - 0.4			V
I_{SDOLK}	Output leakage current	V_{SDO} = V_{DD}	-1		1	µA

Table 29. SPI timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{SCK}	Serial clock frequency				4.5	MHz
t_{CSNQV}	CSN falling until SDO valid	C_{out} = 50 pF			100	ns
t_{CSNQT}	CSN rising until SDO tristate	C_{out} = 50 pF			150	ns
t_{SCKQV}	SCK falling until SDO valid	C_{out} = 50 pF			90	ns
t_{SCSN}	CSN setup time before SCK rising		100			ns
t_{SSDI}	SDI setup time before SCK rising		40			ns
t_{HSDI}	SDI hold time after SCK rising		40			ns
t_{HSCK}	Minimum SCK high time		105			ns
t_{LSCK}	Minimum SCK low time		105			ns
t_{HCSN}	Minimum CSN high time		4			µs
t_{SSCK}	SCK setup time before CSN rising		100			ns
$t_{r\ SDO}$	SDO rise time (20 % / 80 %)	C_{OUT} = 50 pF; I_{LOAD} = -1 mA		50	100	ns
$t_{f\ SDO}$	SDO fall time (20 % / 80 %)	C_{OUT} = 50 pF; I_{LOAD} = 1 mA		50	100	ns
$t_{CSNTimeout}$	CSN low timeout			65		ms

Figure 20. SPI – timing



t_{CSNQV} : CSN falling until SDO valid
t_{CSNQT} : CSN rising until SDO tristate
t_{SCKQV} : SCK falling until SDO valid
t_{SCSN} : CSN setup time before SCK rising
t_{SSDI} : SDI setup time before SCK rising
t_{HSDI} : SDI hold time after SCK rising
t_{HSCK} : minimum SCK high time
t_{LSCK} : minimum SCK low time
t_{HCSN} : minimum CSN high time
t_{SSCK} : SCK setup time before CSN rising

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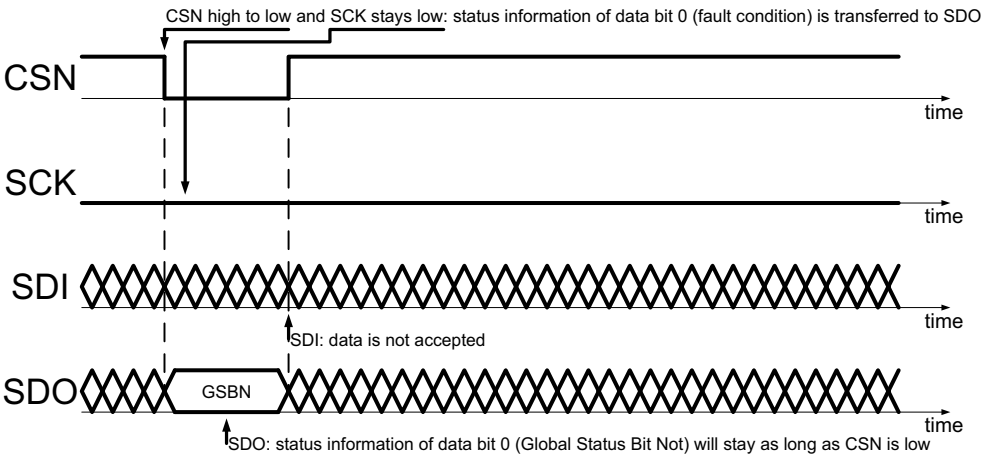
Figure 21. SPI global status register access



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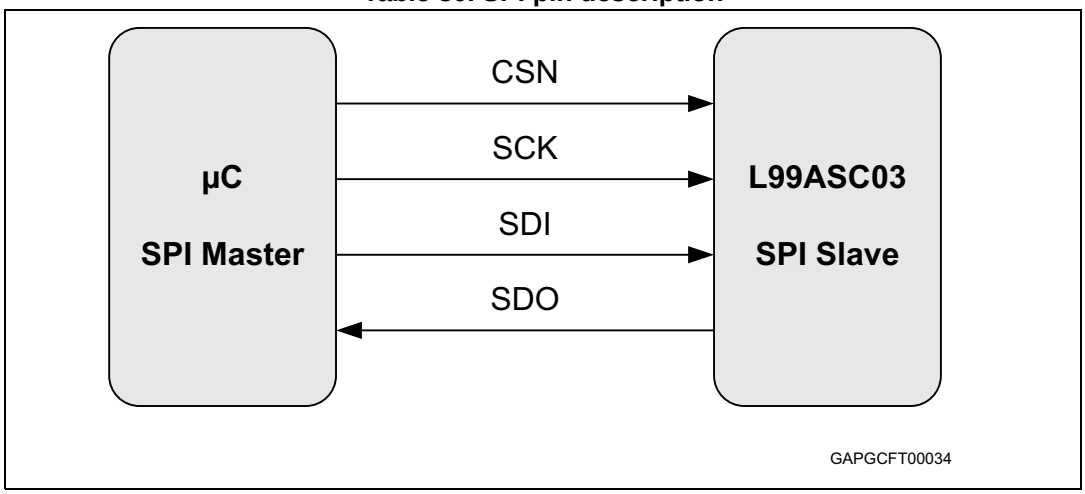
4 ST-SPI Protocol

4.1 Physical layer

Table 30. SPI pin description



4.1.1 Signal description

Chip Select Not (CSN)

The communication interface is deselected, when this input signal is logically high. A falling edge on CSN enables and starts the communication while a rising edge finishes the communication and the sent command is executed when a valid frame was sent. During communication start and stop the Serial Clock (SCK) has to be logically low. The Serial Data Out (SDO) is in high impedance when CSN is high or a communication timeout was detected.

Serial Clock (SCK)

This SCK provides the clock of the SPI. Data present at Serial Data Input (SDI) is latched on the rising edge of Serial Clock (SCK) into the internal shift registers while on the falling edge data from the internal shift registers are shifted out to Serial Data Out (SDO).

Serial Data Input (SDI)

This input is used to transfer data serially into the device. Data is latched on the rising edge of Serial Clock (SCK).

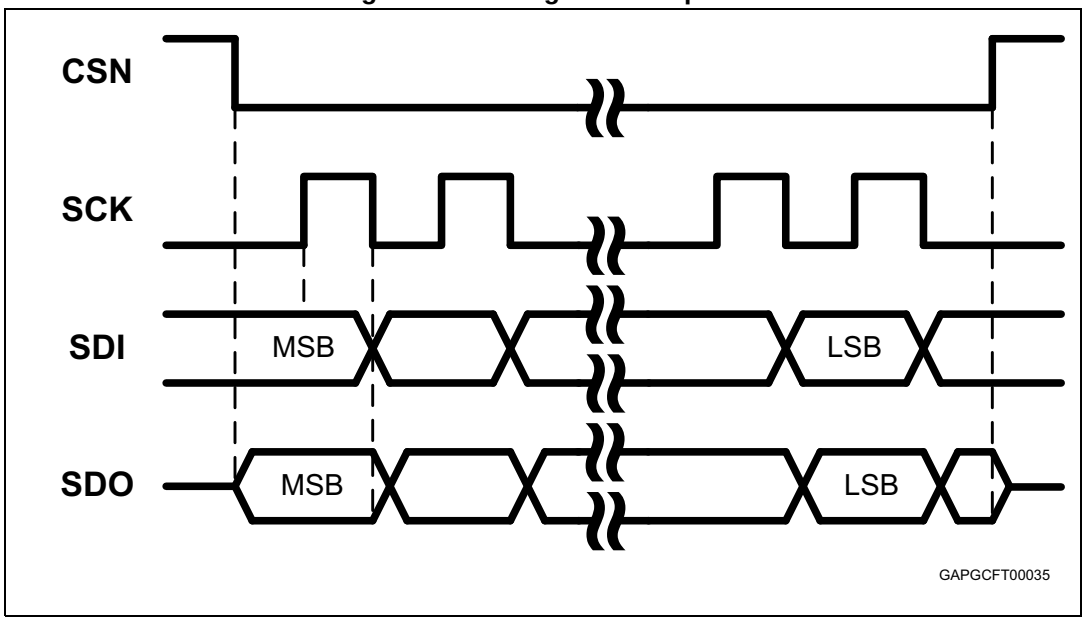
Serial Data Output (SDO)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCK).

4.1.2 Clock and data characteristics

A microcontroller with its SPI peripheral running in following mode can driven ST-SPI: CPOL = 0 and CPHA = 0.

Figure 22. SPI signal description



The communication frame starts with the falling edge of the CSN (Communication Start). SCK has to be low.

The SDI data is then latched at all following rising SCK edges into the internal shift registers.

After *Communication Start* the SDO will leave tristate mode and present the MSB of the data shifted out to SDO. At all following falling SCK edges data is shifted out through the internal shift registers to SDO.

The communication frame is finished with the rising edge of CSN. If a valid communication took place (e.g. correct number of SCK cycles), the requested operation by the OpCode will be performed (Write or Clear operation).

4.2 Protocol

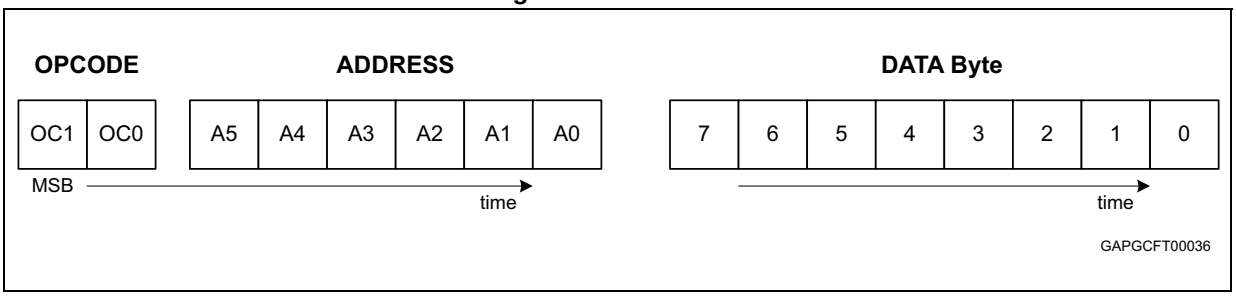
4.2.1 SDI frame

The Data-In Frame consist of 16 bits (OpCode+Address+Data).

The first two transmitted bits (MSB, MSB-1) contain the Operation Code, which represents the instruction which will be performed. The following 6 bits (MSB-2 to MSB-7) represent the address on which the operation will be performed.

The subsequent byte contains the payload data.

Figure 23. SDI frame



Operating codes

Table 31. Operation codes

OC1	OC0	Description
0	0	Write operation
0	1	Read operation
1	0	Read & Clear operation
1	1	Read Device information

The operating code is used to distinguish between different access modes to the registers of the slave device.

A Write Operation writes the payload data to the addressed register if a write access is allowed (e.g. Control Register, valid data). In addition, the content of the addressed register (the data present at Communication Start) is shifted out on the SDO pin.

A *Read Operation* shifts out the data present in the addressed register at *Communication Start*. The payload data is ignored and internal data are not modified. In addition a *Burst Read* can be performed.

A *Read & Clear Operation* will lead to a clear of addressed status bits. The bits to be cleared are defined first by address, second by payload bits set to ‘1’. In addition, the content of the addressed register (the data present at Communication Start) is shifted out on the SDO pin.

Status registers that change their status during a communication frame could be cleared by an ongoing Read & Clear Operation and would be reported neither in the ongoing communication frame nor in the next communication frame. To avoid missing information about any status change, it is recommended to clear the status bits that have been already reported in previous communication frames (Selective Bitwise Clear).

Address

Following the OpCode bits, the six Address bits are a fixed part of the communication frame. The six bits, in combination with the OpCode, allow access to a 2 x 64-wide address range.

Table 32. Device application access

Operating code	
OC1	**OC0**
0	0
0	1
1	0

Table 33. Device information read access

Operating code	
OC1	**OC0**
1	1

Table 34. Address range

Address	Data	Type	Address	Data	Type
3FH	Advanced operation code		3FH	Advanced operation code	
3EH		R/W or C	3EH	<GSB options>	R
				...	
			11H	<WD type>	R
			10H		R
			03H	<Device number 2>	R
			02H	<Device number 1>	R
			01H	<Device family>	R
00H		R/W or C	00H	<Company code>	R

The data contained in the *Device Information* address range is predefined by the ST-SPI Standard v4.0. The data is read only and represents device specific data like Device ID, SPI settings and Watchdog information. For details, please refer to *Section 4.3.1*

Advanced operation codes

Two Advanced Operation Codes can be used to set all control registers to the default value and to clear all status registers.

A 'set all control registers to default' command is performed when an OpCode '11' at address b'111111 is performed.

The Device Register 1 and DSFT_DIS bit are not cleared with this command and hold their content.

A 'clear all status registers' command is performed when an OpCode '10' at address b'111111 is performed.

Data-in payload

The Payload is the data transferred to the slave device with every SPI communication frame. The Payload always follows the OpCode and the Address bits.

For write accesses, the Payload represents the new data written to the addresses registers. For Read & Clear operations, the Payload indicates the clear of a Status Register in case of a '1' in the corresponding bit position.

For a Read Operation the Payload is not used. For functional safety reasons it is recommended to set unused Payload to '0'.

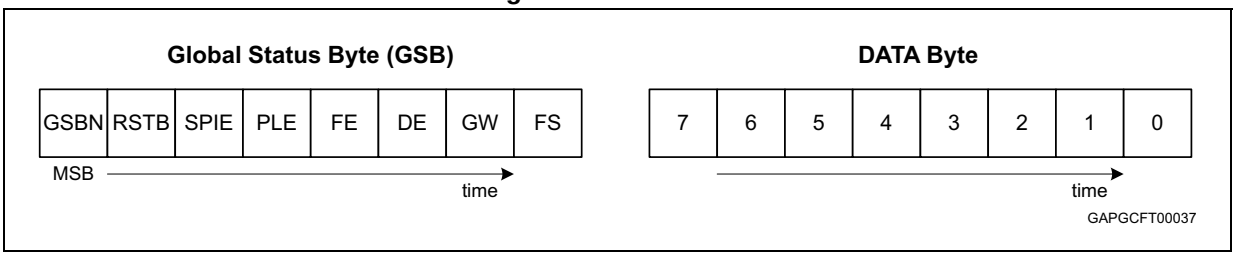
4.2.2 SDO frame

The Data-Out Frame consists of 16 bits (GSB+Data).

The first eight transmitted bits contain device status information and are latched into the shift register at the time of the *Communication Start*. These 8 bits are transmitted at every SPI transfer.

The subsequent byte contains the payload data and is latched into the shift register on the eighth positive SCK edge. This could lead to an inconsistency of data between the GSB and Payload due to different shift register load times. Anyhow, no unwanted Status Register clear should appear, as status information should just be cleared with a dedicated bit clear after read.

Figure 24. SDO frame



Data-out payload

The Payload is the data transferred from the slave device to the microcontroller with every SPI communication frame. The Payload always follows the OpCode and the Address bits of the frame that is currently being sent (In-Frame Response).

4.3 Addresses and data definition

4.3.1 Device information registers

The *Device Information Registers* can be read by using OpCode ‘11’. After shifting out the GSB, the 8-bit payload is transmitted.

Table 35. Device information read access operation code

Operating code	
OC1	**OC0**
1	1

Table 36. Device information registers

Address	Data	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FH	<Advanced option>									
3EH	<GSB options>	R	0	0	0	0H				
...	...		00H							
20H	<SPI CPHA test>	R	0	1	0	1	0	1	0	1
1FH	<WD bit pos. 14>$^{opt.}$	R	00H							
...	...	R	00H							
14H	<WD bit pos. 2>$^{opt.}$	R	C0H							
13H	<WD bit pos. 1>$^{opt.}$	R	41H							
12H	<WD type 2>	R	99H							
11H	<WD type 1>	R	49H							
10H	<SPI mode>	R	90H							
...	...	R	00H							
0AH	<Silicon version>	R	0H				0H			
09H	<Device number 8>	R	00H							
...	...	R	00H							
04H	<Device number 3>	R	10H							
03H	<Device number 2>	R	49H							
02H	<Device number 1>	R	55H							
01H	<Device family>	R	01H							
00H	<Company code>	R	00H							

4.4 SPI registers

Table 37. Complete device SPI register table

Address	Register name	Bit number								Mode
		15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	
	Global status byte	GSBN	RSTB	SPIE	PLE	FE	DE	GW	FS	R
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
0x01	Device Control Reg. 1	WDDIS	CPDIS	TEMPM	ICMP	VDD_VTH	STBYSEL	GOSTBY	WDTRIG	R/W
0x02	Device Control Reg. 2	BEMFCM	BEMFDIR	BEMFMOD	BEMFPOL	BEMFSW	DSMFBT	DSMTH(1)	DSMTH(0)	R/W
0x03	Device Control Reg. 3	BEMFSIGN	BEMFOS(2)	BEMFOS(1)	BEMFOS(0)	BEMFBY	BEMFCNT(2)	BEMFCNT(1)	BEMFCNT(0)	R/W
0x04	Device Control Reg. 4	PCSO(3)	PCSO(2)	PCSO(1)	PCSO(0)	PCSI(3)	PCSI(2)	PCSI(1)	PCSI(0)	R/W
0x05	Device Control Reg. 5	DMUX	AMUX(2)	AMUX(1)	AMUX(0)	WOBM	WOBF	Reserved	Reserved	R/W
0x06	Device Control Reg. 6	GCSA(1)	GCSA(0)	OCSHUTD	OCADC(4)	OCADC(3)	OCADC(2)	OCADC(1)	OCADC(0)	R/W
0x07	Device Control Reg. 7	HOFFCONT	CCT(2)	CCT(1)	CCT(0)	CPLOWM	ISTEST(3)	ISTEST(2)	ISTEST(1)	R/W
0x08	Device Control Reg. 8	—	—	—	—	—	DSFT_DIS	ISTEST_EN	OCFT_DIS	R/W
0x11	Device Status Reg. 1	CPLOW	NRDY	DISABLE	INHWAKE	SPIWAKE	Reserved	DEVST(1)	DEVST(0)	R/C
0x12	Device Status Reg. 2	SPI_DI	Reserved	Reserved	Reserved	INHST	VRT2LOW	VDDUV	VDDFAIL	R/C
0x13	Device Status Reg. 3	WDF(3)	WDF(2)	WDF(1)	WDF(0)	FSWD	WD75%	WD50%	WD25%	R/C
0x14	Device Status Register 4	—	VDDR(2)	VDDR(1)	VDDR(0)	—	TSD2	TSD1/TW2	TW1	R/C
0x15	Device Status Register 5	—	VSOV	VSOVW	VSUV	—	VSREGOV	VSREGOVW	VSREGUV	R/C
0x16	Device Status Register 6	ST(3)	ST(2)	ST(1)	CSAOC	SPI_FL	VSMSOV	VSMSOVW	VSMSUV	R/C
0x17	Device Status Register 7	—	—	DSLS(3)	DSHS(3)	DSLS(2)	DSHS(2)	DSLS(1)	DSHS(1)	R/C

4.4.1 SPI Control Registers

Global status byte

15	14	13	12	11	10	9	8
GSBN	RSTB	SPIE	Reserved	FE	DE	GW	FS

Type: R

Bit Bit description

[15] GSBN: GlobaleStatusByte Not

The GSBN bit is a logically NOR combination of Bit 8 to Bit 14. This bit can also be used as *Global Status Flag* without starting a complete communication frame, as it is present at SDO immediately after pulling CSN low.

[14] RSTB: Reset Bit

The RSTB bit indicates a device POR. In case this bit is set, all internal *Control Registers* are set to default and kept in that state until the bit is cleared. It is automatically cleared by any valid SPI communication.

[13] SPIE: SPI Error

The SPIE bit is a logical OR combination of errors related to a wrong SPI communication (wrong SCK count, CSN time-out and SDI stuck at errors). The SPIE is automatically cleared by a valid SPI communication.

[12] Reserved

[11] FE: Functional Error

The FE bit is a logical OR combination of errors caused by specific events. Functional errors turn into sink mode all or specific gate driver blocks.

[10] DE: Device Error

The DE bit is a logical OR combination of errors related to device specific blocks. Device Errors lead to the turn-off of specific functional blocks.

[9] GW: Global Warning

The GW bit is a logical OR combination of warning flags implemented in the device. Warning do not have any effects at all on the device.

[8] FS: Fail Safe

The FS bit is a logical OR combination of errors caused by specific events. Fail-safe Errors lead to the turn-off of specific functional blocks. All Device Control Registers are set to their default values, except Device Control Register 1 and DSFT_DIS bit.

4.4.2 Device Control Register 1

Device Control Register 1

	7	6	5	4	3	2	1	0
Bit name	WDDIS	CPDIS	TEMPM	ICMP	VDD_VTH	STBYSEL	GOSTBY	WDTRIG
Default values	0	0	0	0	1	0	0	0

Address: 0x1

Type: R/W

Description: In this register, device operating information is stored. This register is not set to default in case of fail-safe errors.

Bit Bit description

[7] WDDIS: WatchDog DISable (writable in FLASH mode only)
0: window watchdog enabled
1: window watchdog disabled

[6] CPDIS: Charge Pump DISable
0: charge pump enabled
1: charge pump disabled

[5] TEMPM: TEMPerature Mode selector
0: TW1 / TSD1 / TSD2 are active
1: TW1 / TW2 / TSD2 are active

[4] ICMP: VDD load current monitoring in VDD Standby Mode
0: monitoring enabled. The watchdog is disabled in VDD Standby Mode only if $I_{VDD} < I_{CMP}$
1: monitoring disabled. The watchdog is always disabled in VDD Standby mode

[3] VDD_VTH: VDD undervoltage monitoring reset threshold
0: low threshold selected
1: high threshold selected

[2] STBYSEL: STandBY SELect
0: VBAT Standby mode
1: VDD Standby mode

[1] GOSTBY: Go to Standby
0: no action
1: go-to-standby command (this bit is automatically cleared upon state transition).

[0] WDTRIG: WatchDog TRIGger Bit
Watchdog trigger bit (for a detailed description, please refer to *Section 2.4*).

4.4.3 Device Control Register 2

Device Control Register 2

	7	6	5	4	3	2	1	0
Bit name	BEMFCM	BEMFDIR	BEMFMOD	BEMFPOL	BEMFSW	DSMFBT	DSMTH(1)	DSMTH(0)
Default values	0	0	0	0	0	0	0	0

Address: 0x2

Type: R/W

Description: In this register static BEMF parameters and the drain-source monitoring parameters are set.

Bit Bit description

[7] BEMFCM: BEMFCNT updating source selection
0: The BEMFCNT can be updated only via SPI
1: The BEMFCNT can be updated only via positive pulses applied at the BC input pin

[6] BEMFDIR: BEMFCNT update direction (active only if BEMFCM = 1)
0: BEMFCNT increased at each positive pulse at the BC input pin
1: BEMFCNT decreased at each positive pulse at the BC input pin

[5] BEMFMOD: BEMF comparator selection
0: BEMF GND comparator (if BEMFSW = 0) used for BEMF detection
0: BEMF V_{SMS} comparator (if BEMFSW = 1) used for BEMF detection
1: BEMF $V_{SMS}/2$ comparator used for BEMF detection

[4] BEMFPOL: BEMF sampling point selection (active only if BEMFMOD=0)
0: BEMF detection upon turn-on of the PWM switch
1: BEMF detection upon turn-off of the complementary PWM switch

[3] BEMFSW: PWM switching method to drive the external MOSFET in a half bridge
0: PWM signal applied on HS
1: PWM signal applied on LS

[2] DSMFBT: drain-source monitoring filter and blanking time
0: 1.2 µs blanking and filter time selected
1: 2.4 µs blanking and filter time selected

[1:0] DSMTH: Drain Source Monitor threshold
00: 0.5 V
01: 1.0 V
10: 1.5 V
11: 2.0 V

4.4.4 Device Control Register 3

Device Control Register 3

	7	6	5	4	3	2	1	0
Bit name	BEMFSIGN	BEMFOS(2)	BEMFOS(1)	BEMFOS(0)	BEMFBY	BEMFCNT(2)	BEMFCNT(1)	BEMFCNT(0)
Default values	0	0	0	0	0	0	0	0

Address: 0x3

Type: R/W

Description: In this register, dynamic BEMF parameters are set.

Bit Bit description

[7] BEMFSIGN: offset sign for BEMF $V_{SMS}/2$ comparator
0: threshold of BEMF $V_{SMS}/2$ comparator increased by offset
1: threshold of BEMF $V_{SMS}/2$ comparator decreased by offset

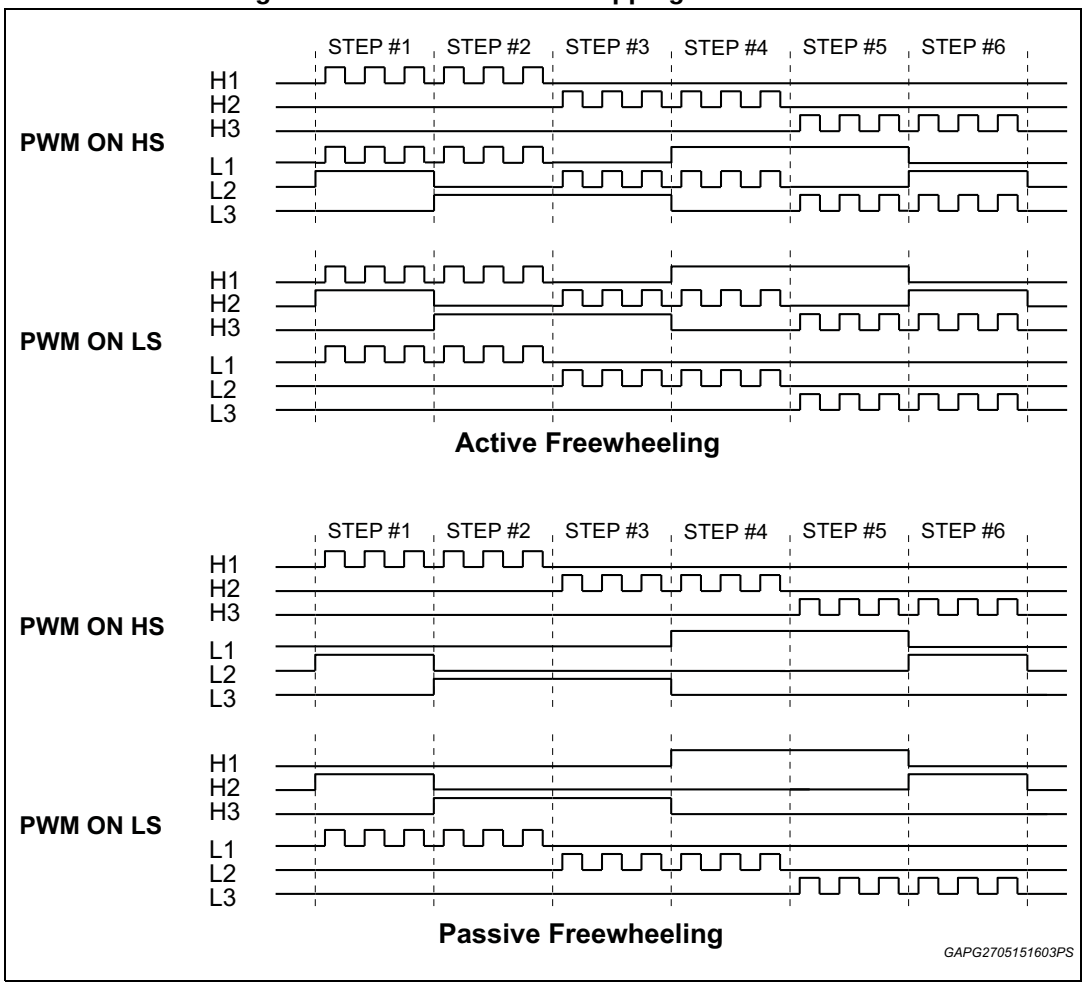
[6:4] BEMFOS: Offset Selection for BEMF $V_{SMS}/2$ comparator
000: BEMF offset = 0 V
001: BEMF offset = 0.0025 * V_{SMS}
010: BEMF offset = 0.005 * V_{SMS}
011: BEMF offset = 0.01 * V_{SMS}
100: BEMF offset = 0.02 * V_{SMS}
101: BEMF offset = 0.04 * V_{SMS}
110: BEMF offset = 0.08 * V_{SMS}
111: BEMF offset = 0.16 * V_{SMS}

[3] BEMFBY: BEMF comparator output sampling source selection
0: BEMF comparator output sampled on PWM edge, depending on BEMFMOD, BEMFPOL and BEMFSW
1: BEMF comparator output sampled by internal system clock

[2:0] BEMFCNT: BEMF motor-phase/step counter (see *Figure 25*)

	Step	Switch where PWM is applied	Switch always on	BEMF monitored at pin
000	Not used (phase multiplexer is OFF)			
001	1	GH1 or GL1	GL2 or GH2	SH3
010	2	GH1 or GL1	GL3 or GH3	SH2
011	3	GH2 or GL2	GL3 or GH3	SH1
100	4	GH2 or GL2	GL1 or GH1	SH3
101	5	GH3 or GL3	GL1 or GH1	SH2
110	6	GH3 or GL3	GL2 or GH2	SH1
111	Not used (phase multiplexer is OFF)			

Figure 25. BEMF detection stepping of BEMFCNT



4.4.5 Device Control Register 4

Device Control Register 4

	7	6	5	4	3	2	1	0
Bit name	PCSO(3)	PCSO(2)	PCSO(1)	PCSO(0)	PCSI(3)	PCSI(2)	PCSI(1)	PCSI(0)
Default values	0	0	0	0	0	0	0	0

Address: 0x4

Type: R/W

Description: In this register, the current for charging and discharging the gates of the external MOSFETs can be selected.

Bit Bit description

[7:4] PCSO: peak source current of gate drivers.
0000: PCSO = 0 mA
0001: PCSO = 15 mA
0010: PCSO = 25 mA
.....
1111: PCSO = 215 mA

[3:0] PCSI: Peak SInk Current of gate drivers.
0000: PCSI = 0 mA
0001: PCSI = 40 mA
0010: PCSI = 60 mA
.....
1111: PCSI = 600 mA

4.4.6 Device Control Register 5

Device Control Register 5

	7	6	5	4	3	2	1	0
Bit name	DMUX	AMUX(2)	AMUX(1)	AMUX(0)	WOBM	WOBF	Reserved	Reserved
Default values	0	0	0	0	0	0	0	1

Address: 0x5

Type: R/W

Bit Bit description

[7] DMUX: digital multiplexer output
0: FS flag selected
1: OC flag selected. In case the OCFT_DIS bit in Control Register 8 is "1", then the DOUT pin reflects directly the overcurrent comparator output and the CSAOC bit in Status Register 6 is not set if an overcurrent event occurs.

[6:4] AMUX: analog multiplexer output
000: OFF
001: 1/8 V_S
010: 1/8 V_{SREG}
011: 1/8 V_{SMS}
100: TJ
101: CSA reference voltage
110: CSA reference voltage is muxed to AOUT and CSO pins at the same time
111: not used

[3] WOBM: charge pump frequency modulation
0: frequency modulation enabled
1: frequency modulation disabled

[2] WOBF: charge pump modulation frequency
0: 16 kHz
1: 32 kHz

[1] Reserved, keep default value [0]

[0] Reserved

4.4.7 Device Control Register 6

Device Control Register 6

	7	6	5	4	3	2	1	0
Bit name	GCSA(1)	GCSA(0)	OCSHUTD	OCADC(4)	OCADC(3)	OCADC(2)	OCADC(1)	OCADC(0)
Default values	0	0	1	0	0	0	0	0

Address: 0x6

Type: R/W

Bit Bit description

[7:6] GCSA: CSA gain
00: 20
01: 30
10: 70
11: 100

[5] OCSHUTD: overcurrent shutdown
0: gate drivers are not deactivated in case of overcurrent (global warning reported)
1: gate drivers are deactivated in case of overcurrent (functional error reported)

[4:0] OCADC: overcurrent threshold
00000: OFF
00001: 150 mV
00010: 220mV
00011: 300mV
00100: 370 mV
00101: 440 mV
00110: 520 mV
00111: 590 mV
01000: 660 mV
01001: 740 mV
01010: 800 mV
01011: 880 mV
01100: 960 mV
01101: 1.03 V
01110: 1.1 V
01111: 1.18 V
10000: 1.25 V
10001: 1.32 V
10010: 1.39 V
10011: 1.47 V
10100: 1.54 V
10101: 1.61 V
10110: 1.68 V
10111: 1.76 V
11000: 1.84 V
11001: 1.9 V
11010: 1.98 V
11011: 2.05 V
11100: 2.13 V
11101: 2.2 V
11110: 2.28 V
11111: 2.35 V

4.4.8 Device Control Register 7

Device Control Register 7

	7	6	5	4	3	2	1	0
Bit name	HOFFCONT	CCT(2)	CCT(1)	CCT(0)	CPLOWM	ISTEST(3)	ISTEST(2)	ISTEST(1)
Default values	0	1	1	1	1	0	0	0

Address: 0x7

Type: R/W

Bit Bit description

[7] HOFFCONT: HARDOFF control
0: the full current discharge capability is activated when programmed cross-current time has elapsed
1: the full current discharge capability is activated upon the turn-on command of the complementary switch

[6:4] CTT: cross-current time.
See *Table 18: Gate driver for external MOSFET*

[3] CPLOWM: charge pump undervoltage monitoring
0: in case of charge pump undervoltage, only the CPLOW flag is set (global warning reported)
1: in case of charge pump undervoltage, the gate drivers are deactivated (functional error reported)

[2] ISTEST(3): sink current enable (used for open-load and short-circuit test)
0: disabled
1: sink current at SH3

[1] ISTEST(2): sink current enable (used for open-load and short-circuit test)
0: disabled
1: sink current at SH2

[0] ISTEST(1): sink current enable (used for open-load and short-circuit test)
0: disabled
1: sink current at SH1

4.4.9 Device Control Register 8

Device Control Register 8

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	—	DSFT_DIS	ISTEST_EN	OCFT_DIS
Default values	—	—	—	—	—	0	0	0

Address: 0x8

Type: R/W

Bit Bit description

[7:3] Reserved

[2] DSFT_DIS: drain-source fault disable.
This bit can be written only when the DISABLE bit (in status register 1) is "1", otherwise the write operation to this bit is ignored. Note: this bit is not set to default in case of fail-safe errors.
0: a drain-source monitoring error causes the turn-off of the affected driver (functional error reported)
1: a drain-source monitoring error does not cause the turn-off of the affected driver (global warning reported)

[1] ISTEST_EN: ISTEST enable
0: ISTEST disabled
1: ISTEST enabled

[0] OCFT_DIS: overcurrent filter time disable (for RPD)
0: overcurrent filter time enabled
1: overcurrent filter time disabled

4.4.10 Device Status Registers 1

Device Status Registers 1

	7	6	5	4	3	2	1	0
	CPLOW	NRDY	DISABLE	INHWAKE	SPIWAKE	Reserved	DEVST(1)	DEVST(0)
GSB reported	GW/FE(1)	GW/FE(1)	FE	Information	Information	—	Information	Information
Clear mode	Read & Clear	Auto cleared	Read & Clear	Read & Clear	Read & Clear	—	Read & Clear	

1. Depending on CPLOWM bit:
CPLOWM = 0, than GW
CPLOWM = 1, than FE

Address: 0x11

Type: R/C

Bit Bit description

[7] CPLOW: charge pump undervoltage detected

[6] NRDY: charge pump not ready (V_{CPLOW} threshold not reached after charge pump startup)

[5] DISABLE: DIS pin high detected

[4] WAKEINH: wake-up from INH detected

[3] WAKESPI: wake-up from SPI detected

[2] Reserved

[1:0] DEVST: device status
00: Active mode
01: V_{DD} standby mode
10: V_{BAT} standby mode/ POR
11: Flash mode

After a device state transition to Active mode or Flash mode, the DEVST bits always report the previous device state. If an SPI "Read & Clear" command is performed on these bits, they will then report the current device state.

4.4.11 Device Status Registers 2

Device Status Registers 2

	7	6	5	4	3	2	1	0
	SPI_DI	Reserved	Reserved	Reserved	INHST	VRT2LOW	VDDUV	VDDFAIL
GSB reported	FS	—	—	—	Information	GW	FS	FS
Clear mode	Read & Clear	—	—	—	Information	Read & Clear	Read & Clear	Read & Clear

Address: 0x12

Type: R/C

Bit Bit description

[7] SPI_DI: short circuit on SDI pin detected (all 0's or all 1's detected on SDI pin)

[6] Reserved

[5] Reserved

[4] Reserved

[3] INHST: INH pin status (0: logic LOW; 1: logic HIGH)

[2] VRT2LOW: VDD detected to be below the VRT2 threshold, in case the VRT1 reset threshold is selected (VDD_VTH = 0).

[1] VDDUV: VDD undervoltage detected

[0] VDDFAIL: VDD FAIL detected

4.4.12 Device Status Registers 3

Device Status Registers 3

	7	6	5	4	3	2	1	0
	WDF(3)	WDF(2)	WDF(1)	WDF(0)	FSWD	WD75%	WD50%	WD25%
GSB reported	Information				FS	Information	Information	Information
Clear mode	Auto cleared with valid WDTRIG toggle				Read & Clear	—	—	—

Address: 0x13

Type: R/C

Bit Bit description

[7:4] WDF: watchdog fault counter

[3] FSWD: watchdog fault occurred

[2:0] WD: counter monitor (these bits represent the percentage of the time elapsed between the POR or the last watchdog trigger and the end of the watchdog period)

4.4.13 Device Status Registers 4

Device Status Registers 4

	7	6	5	4	3	2	1	0
	—	VDDR(2)	VDDR(1)	VDDR(0)	—	TSD2	TSD1/TW2	TW1
GSB reported	Information				—	FS	DE/GW(1)	GW
Clear mode	Read & Clear on any of the VDD_R(x) bits				—	Read & Clear	Read & Clear	Read & Clear

1. Depending on TEMPM bit
   If TEMPM = 0, then DE
   If TEMPM = 1, then GW

Address: 0x14

Type: R/C

Bit Bit description

[7] Reserved

[6:4] VDDR: thermal shutdown event counter

[3] Reserved

[2] TSD2 detected

[1] TSD1/TW2 detected

[0] TW1 detected

4.4.14 Device Status Registers 5

Device Status Registers 5

	7	6	5	4	3	2	1	0
	—	VSOV	VSOVW	VSUV	—	VSREGOV	VSREGOVW	VSREGUV
GSB reported	—	DE	GW	DE	—	GW	GW	GW
Clear mode	—	Read & Clear	Read & Clear	Read & Clear	—	Read & Clear	Read & Clear	Read & Clear

Address: 0x15

Type: R/C

Bit Bit description

[7] Reserved

[6] VSOV: V_S overvoltage detected

[5] VSOVW: V_S overvoltage warning detected

[4] VSUV: V_S undervoltage detected

[3] Reserved

[2] VSREGOV: V_{SREG} overvoltage detected

[1] VSREGOVW: V_{SREG} overvoltage warning detected

[0] VSREGUV: V_{SREG} undervoltage detected

4.4.15 Device Status Registers 6

Device Status Registers 6

	7	6	5	4	3	2	1	0
	ST(3)	ST(2)	ST(1)	CSAOC	SPI_FL	VSMSOV	VSMSOVW	VSMSUV
GSB reported	FE	FE	FE	GW/FE(1)	GW	DE	GW	GW
Clear mode	Read & Clear	Read & Clear	Read & Clear	Read & Clear	Read & Clear	Read & Clear	Read & Clear	Read & Clear

1. Depending on OCSHUTD bit
   If OCSHUTD = 0, then GW
   If OCSHUTD = 1, then FE

Address: 0x16

Type: R/C

Bit Bit description

[7] ST(3): HS3 and LS3 driven active at the same time (forbidden state / shoot-through detection)

[6] ST(2): HS2 and LS2 driven active at the same time (forbidden state / shoot-through detection)

[5] ST(1): HS1 and LS1 driven active at the same time (forbidden state / shoot-through detection)

[4] CSAOC: CSA overcurrent event detected

[3] SPI_FL: CS timeout or wrong number of SCLK cycles (other than 0 or 16) detected

[2] VSMSOV: V_{SMS} overvoltage detected

[1] VSMSOVW: V_{SMS} overvoltage warning detected

[0] VSMSUV: V_{SMS} undervoltage detected

4.4.16 Device Status Registers 7

Device Status Registers 7

	7	6	5	4	3	2	1	0
	—	—	DSLS(3)	DSHS(3)	DSLS(2)	DSHS(2)	DSLS(1)	DSHS(1)
GSB reported	—	—	FE/GW(1)	FE/GW(1)	FE/GW(1)	FE/GW(1)	FE/GW(1)	FE/GW(1)
Clear mode	—	—	Read & Clear	Read & Clear	Read & Clear	Read & Clear	Read & Clear	Read & Clear

1. Depending on DSFT_DIS bit
If DSFT_DIS = 0, then FE
If DSFT_DIS = 1, then GW

Address: 0x17

Type: R/C

Bit Bit description

[7] Reserved

[6] Reserved

[5] DSLS3: drain-source overvoltage detected on LS3

[4] DSHS3: drain-source overvoltage detected on HS3

[3] DSLS2: drain-source overvoltage detected on LS2

[2] DSHS2: drain-source overvoltage detected on HS2

[1] DSLS1: drain-source overvoltage detected on LS1

[0] DSHS1: drain-source overvoltage detected on HS1

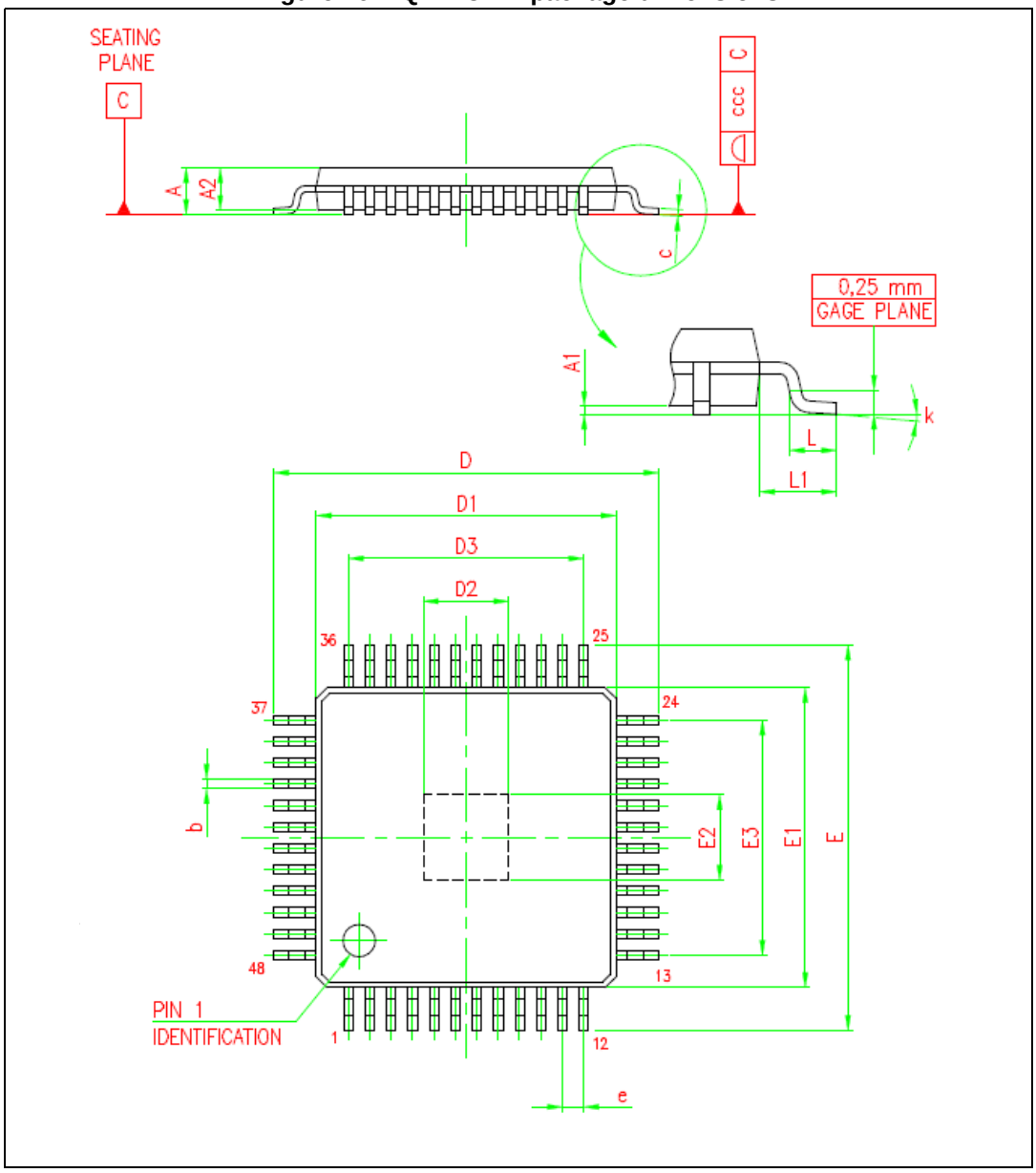
5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.1 TQFP48-EP mechanical data

Figure 26. TQFP48-EP package dimensions



Note: D2 and E2 not in scale in the drawing.

Table 38. TQFP48-EP mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.20
A1	0.05		0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09		0.20
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
D2		4.50	
D3		5.50	
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
E2		4.50	
E3		5.50	
e		0.50	
L	0.45	0.60	0.75
L1		1.00	
k	0°	3.5°	7°
ccc			0.08

6 Revision history

Table 39. Document revision history

Date	Revision	Changes
04-Mar-2016	1	Initial release
12-Jul-2016	2	Updated *Table 9: ESD protection*; *Table 12: Supply and supply monitoring*; *Table 14: Voltage regulator VDD*.