L99PM60J

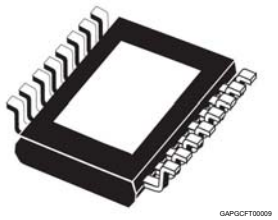
Power management IC with LIN transceiver

Features

- One 5 V low-drop voltage regulators (100 mA, continuous mode)
- No electrolytic capacitor required on regulator output (only 220 nF ceramic typ.)
- Ultra-low quiescent current in $V_{BAT\text{-}standby}$ (7 µA) and $V_{1\text{-}standby}$ (45 µA)
- Window watchdog and advanced fail-safe functionality
- Configurable fail-safe output
- Programmable reset threshold (4.6 V; 3.5 V)
- V_S monitoring / temperature measurement
- LIN 2.1 compliant (SAE J2602 compatible) transceiver
- High-speed LIN Flash mode up to 100 Kbit/s
- ST SPI interface for mode control and diagnostics
- 2 high-side drivers, e.g. LED or HALL ($R_{DSon,typ}$ = 7 Ω)
- 2 low-side drivers ($R_{DSon,typ}$ = 2 Ω)
- Outputs are short-circuit protected
- Direct drive feature for high sides
- Temperature warning and thermal shutdown

Applications

- Automotive ECUs requiring LIN and power management features such as door zone, and body control modules



PowerSSO-16

Description

The L99PM60J is a power management system IC that features one low-drop regulator, a direct drive for high-side drivers, and a LIN 2.1 compliant SAE J2602 transceiver.

The integrated standard serial peripheral interface (SPI) controls all L99PM60J operation modes and provides driver diagnostic functions.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-16	L99PM60J	L99PM60JTR

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1 Block diagram and pin descriptions

Figure 1. block diagram

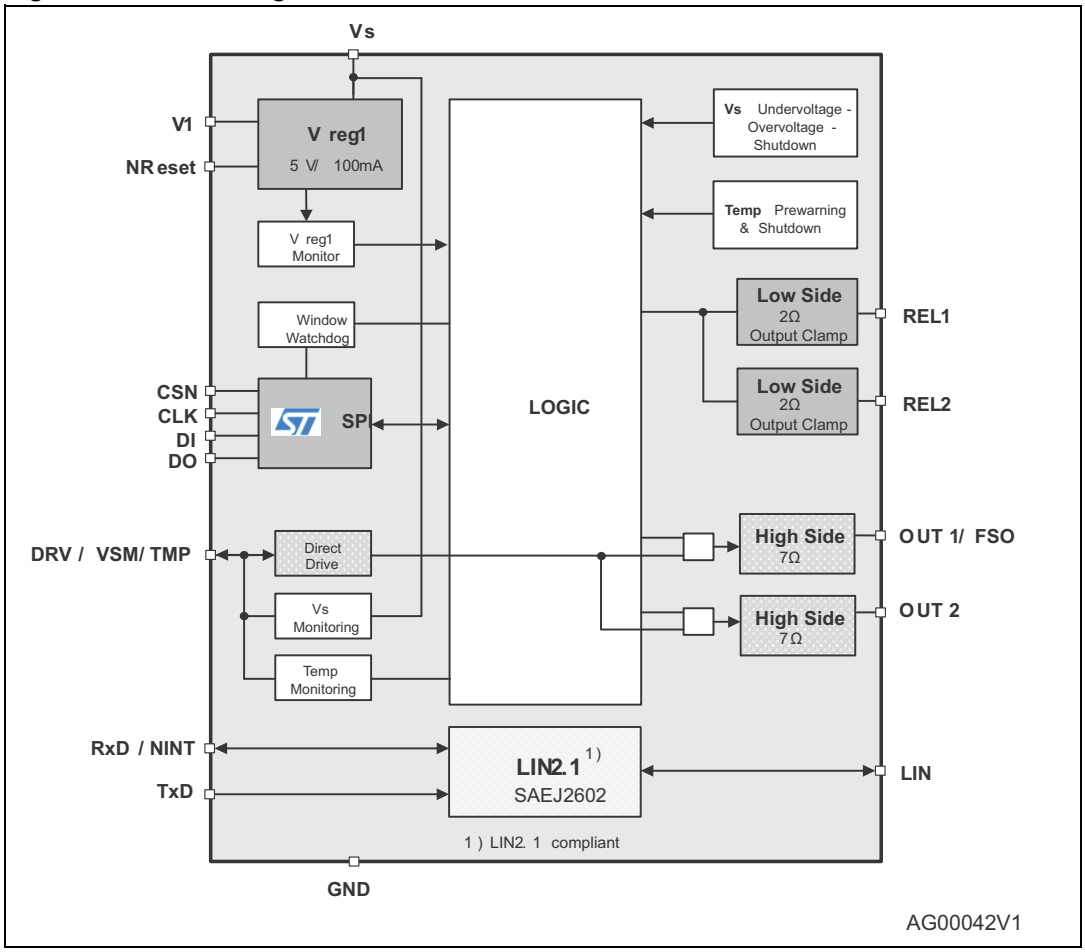


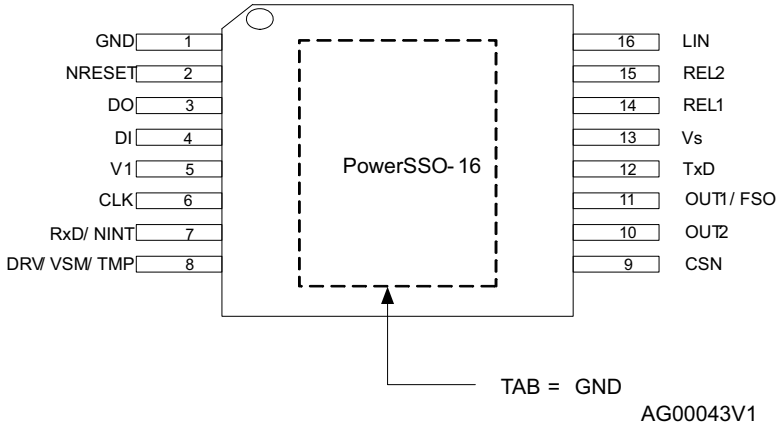
Table 2. Pin descriptions and functions

Pin	Symbol	Function
1	GND	Ground
2	NRESET	NReset output to micro controller; Internal pull-up of typ. 100 KΩ (reset state = LOW)
3	DO	SPI: serial data output
4	DI	SPI: serial data input
5	V1	Voltage regulator 1 output: 5 V supply e.g. micro controller
6	CLK	SPI: serial clock input
7	RxD/NINT	Receiver output of the LIN 2.1 transceiver or interrupt:
8	DRV/VSM/TMP	Direct drive for high-side drivers OUT1/2; V_S and temperature monitoring
9	CSN	SPI: chip select not input

Table 2. Pin descriptions and functions (continued)

Pin	Symbol	Function
10	OUT2	High side drivers (7 Ω, typ.): to supply e.g. LED's, HALL sensors, external contacts
11	OUT1/FSO	High side driver (7 Ω, typ.): to supply e.g. LED's, HALL sensors, external contacts
12	TxD	Transmitter input of the LIN 2.1 transceiver
13	V_S	Power supply voltage
14	REL1	Low side driver (2 Ω typ.): e.g. relay
15	REL2	Low side driver (2 Ω typ.): e.g. relay
16	LIN	LIN bus line

Figure 2. Pin connection PowerSSO-16 (top view)



Note: It is recommended to connect pin GND directly to the Heat Slug.

2 Detailed description

2.1 Voltage regulator

The L99PM60J contains a fully protected low drop voltage regulator, which is designed for very fast transient response. The output voltage is stable with loads capacitors ≥ 220 nF

The V_1 voltage regulator provides 5 V supply voltage and up to 100 mA continuous load current and is mainly intended for supply of the system microcontroller. The V_1 regulator is embedded in the power management and failsafe functionality of the device and operates according to the selected operating mode.

In addition the regulator V_1 drives the L99PM60J internal 5 V loads. The voltage regulator is protected against overload and overtemperature. An external reverse current protection has to be provided by the application circuitry to prevent the input capacitor from being discharged by negative transients or low input voltage. Current limitation of the regulator ensures fast charge of external bypass capacitors. The output voltage is stable for ceramic load capacitors ≥ 220 nF.

If device temperature exceeds TSD1 threshold, all outputs (OUTx, RELx, LIN) are deactivated except V_1. Hence the micro controller has the possibility for interaction or error logging. In case of exceeding TSD2 threshold (TSD2 > TSD1), also V_1 is deactivated (see state chart *Figure 11*). A timer is started and the voltage regulator is deactivated for t_{TSD}. During this time, all other walk-up sources (LIN) are disabled. After 1 sec., the voltage regulator tries to restart automatically. If the restart fails 7 times without clearing and thermal shutdown condition still exists, the L99PM60J enters the $V_{BAT\text{-}standby}$ mode.

In case of short to GND at "V_1" after initial turn on ($V_1 < V_{1fail}$ for t > tv1short) the L99PM60J enters the $V_{BAT\text{-}standby}$ mode. Reactivation (wake-up) of the device can be achieved with signals from LIN.

2.1.1 Voltage regulator failure

The $V_{1,}$ regulator output voltage is monitored.

In case of a drop below the V_1 – fail thresholds ($V_1 < V_{1fail}$ for $t > t_{V1fail}$), the V_1 -fail bit is latched. The fail bits can be cleared by a dedicated SPI command.

Short to ground detection

At power-on, in case of short detection on V_1, the regulator output switches off after $t_{V1short}$ and the L99PM60J turns to forced $V_{BAT\text{-}standby}$ mode. The forced V_{BAT} TSD2/SHTV1 and V_{1fail} lists are set.

During Normal mode, once the regulator exceeded the V_{1fail} threshold, in case of short detection on V_1, the device turns to force $V_{BAT\text{-}standby}$ mode only after thermal shutdown TSD2 detection. In this case the forced V_{BAT} TSD2/SHTV1 bit is set.

V_1 undervoltage warning

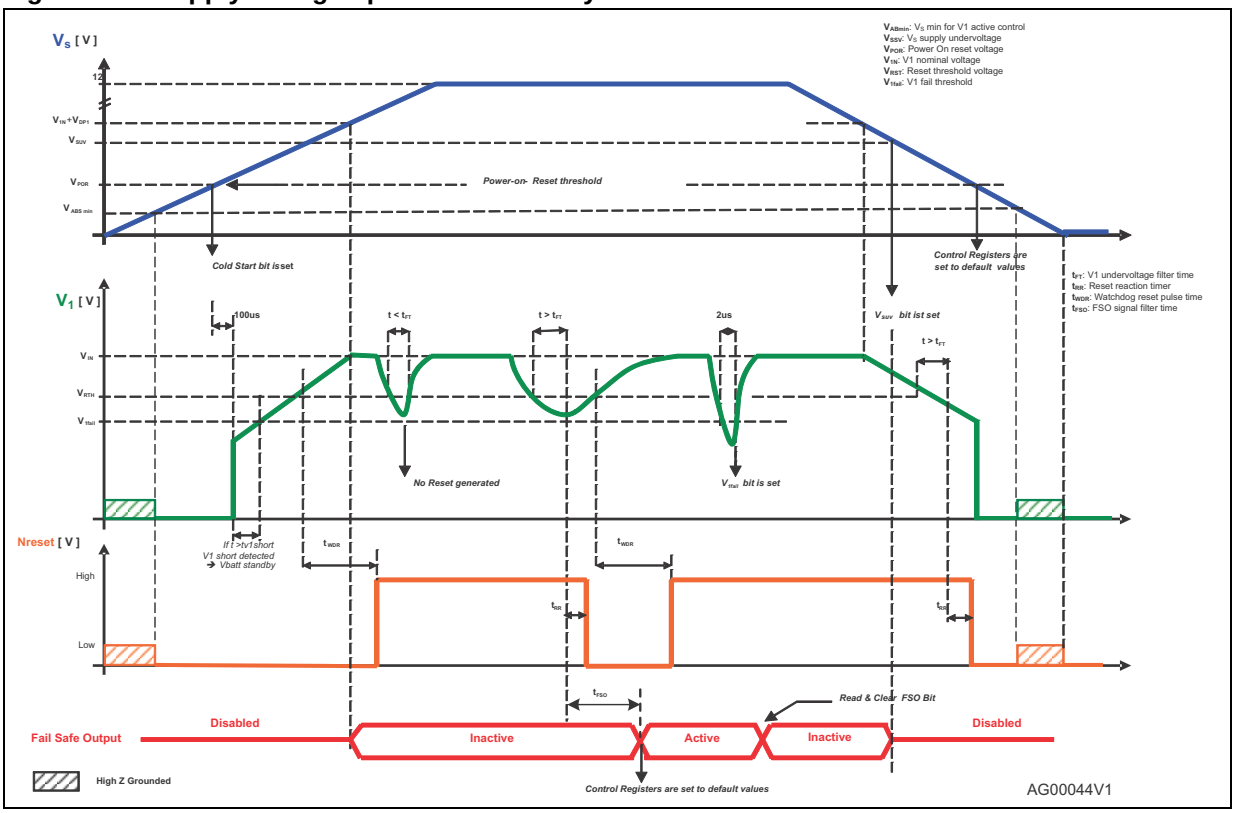
For the L99PM60J 2 different V_1 reset thresholds can be selected. The higher threshold V_{RT2} is set by default. If the lower threshold is selected the V_1 undervoltage warning flag is set, if the voltage on V_1 output drops below the higher threshold. This Bit is latched and can be read and optionally cleared.

V_1 failure failsafe activation

If the voltage on V_1 output drops below the selected V_1 reset threshold the RESET output is pulled to ground. If the V_1 output voltage remains below the V_1 reset threshold for longer than t_{FSO}, fail safe mode is activated additionally. For more details about failsafe please refer to chapter Fail safe mode

2.1.2 Voltage regulator behaviour

Figure 3. Supply voltage operation summary



2.2 Power control in operating modes

The L99PM60J can be operated in 4 different operating modes:

- Active
- Flash
- $V_{1\text{-standby}}$
- $V_{BAT\text{-standby}}$

2.2.1 Active mode

All functions are available and the device is controlled by the ST SPI Interface.

2.2.2 Flash mode

To program the system microcontroller, the L99PM60J can be operated in Flash Mode where the internal watchdog is disabled. In addition the SPI-Interface and low power modes are not available in Flash Mode.

The mode can be entered if the following condition is applied

$V_{CSN} \geq V_{Flash}$

At exit from Flash Mode ($V_{CSN} < V_{flash}$) no NReset pulse is generated and the watchdog starts with a Long Open Window.

Note: "High" level for flash mode selection is $V_{CSN} \geq V_{flash}$. For all other operation modes, standard 5V logic signals are required.

2.2.3 $V_{1\text{-standby}}$ mode

The transition from Active Mode to $V_{1\text{-standby}}$ mode is controlled by SPI.

To supply the micro controller in a low power mode, the voltage regulator 1 (V_1) remains active. In order to reduce the current consumption, the regulator goes in low current mode as soon as the supply current of the microcontroller goes below the I_{CMP} current threshold. At this transition, the L99PM60J also deactivates the internal watchdog.

Relay outputs and LIN Transmitter are switched off in $V_{1\text{-standby}}$ Mode. High side Outputs remain in the configuration programmed prior to the standby command.

A cyclic contact supply (for cyclic monitoring of external contacts) can be activated by SPI and using the Direct Drive Input (DRV).

Each wake up event sets the device into the active mode and forces the RxD/NINT pin to the low level.

Note: Input TxD must be at recessive (high) level and CSN must be at high level in order to achieve minimum standby current in $V_{1\text{-standby}}$ Mode.

Interrupt

The interrupt signal (linked to RxDL/NINT internally) indicates a wake-up event from $V_{1\text{-standby}}$ mode. In case of activity on LIN or SPI access the NINT pin is pulled low for $t_{Interupt}$

In case of $V_{1\text{-standby}}$ mode and ($I_{V1} > I_{CMP}$), the device remains in standby mode, the V_1 regulator switches to high current mode and the watchdog starts. No Interrupt signal is generated.

2.2.4 $V_{BAT\text{-standby}}$ mode

The transition from Active Mode to $V_{BAT\text{-standby}}$ mode is initiated by an SPI command.

In $V_{BAT\text{-standby}}$ Mode, the voltage regulator, relay outputs and LIN transmitter are switched off. High side outputs remain in the configuration programmed prior to the standby command.

In $V_{BAT\text{-standby}}$ mode the current consumption of the L99PM60J is reduced to a minimum level.

Note: Inputs TXDL and CSN must be terminated to GND in $V_{BAT\text{-}standby}$ to achieve minimum standby current.

This can be achieved with the internal ESD protection diodes of the microcontroller (microcontroller is not supplied in this mode; V_1 is pulled to GND).

2.3 Wake up from standby modes

A wake-up from standby mode switches the device to active mode. This can be initiated by one or more of the following sources:

Table 3. Wake up sources

Wake up source	Description
LIN bus activity	Always active
$I_{V1} > I_{CMP}$	Device remains in $V_{1\text{-}standby}$ mode with watchdog enabled (If I_{CMP} = 0) and V_1 goes into High Current Mode (Increased Current Consumption). No interrupt is generated.
SPI Access	Always active (except in $V_{BAT\text{-}standby}$ mode) Wake up event: CSN is low and first rising edge on CLK

All wake-up events from $V_{1\text{-}standby}$ mode (except $I_{V1} > I_{CMP}$) are indicated to the microcontroller by a low-pulse at RxDL/NINT (duration: $t_{Interupt}$)

Wake-up from $V_{1\text{-}standby}$ by SPI Access might be used to check the interrupt service handler.

2.4 Cyclic contact supply

In $V_{1\text{-}standby}$ mode, any high side driver output (OUT1..2) can be used to supply external contacts. Direct drive feature for high side drivers must be enabled by SPI to control the high side driver outputs by DRV/VSM/TMP pin.

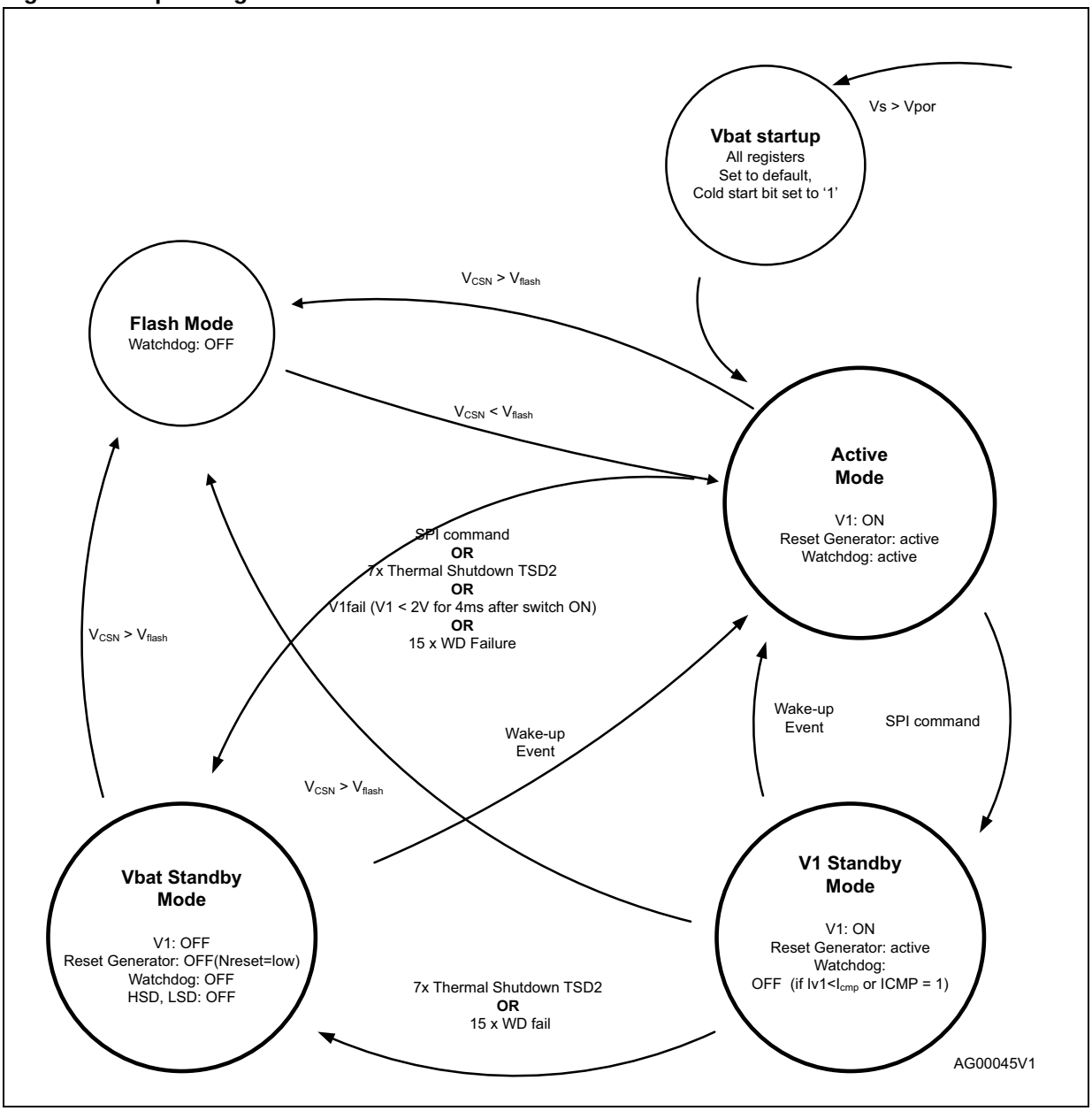
2.5 Functional overview (truth table)

Table 4. Functional overview (truth table)

Function	Comments	Operating Modes		
		Active mode	$V_{1\text{-standby}}$ static mode (cyclic sense)	$V_{BAT\text{-standby}}$ static mode (cyclic sense)
Voltage-regulator, V_1	V_{OUT} = 5 V	On	On(1)	Off
Reset-generator		On	On	Off
Window watchdog	V_1 monitor	On	Off (on: I_V1 > $I_{CMP\text{-threshold}}$ and I_{CMP} = 0)	Off
Direct drive		On / Off(2)	On / Off(2)	Off
Relay driver		On	Off	Off
LIN	LIN 2.1	On	Off(3)	Off(3)
FSO (if configured by SPI), active by default	Fail safe output	OUT1/FSO OFF(4)	OUT1/FSO OFF(4)	OUT1/FSO OFF(4)
Oscillator		On	(5)	Off
V_S-monitor		On	(6)	Off

1. Supply the processor in low current mode.
2. Selectable from SPI
3. The bus state is internally stored when going to standby mode. A change of bus state leads to a wake-up after exceeding of internal filter time
4. ON in Failsafe Condition: If Standby mode is entered with active Fail Safe mode, the output remains ON in Standby mode.
5. Activated when direct drive feature is enabled from SPI and DRV/VSM/TMP pin is high.
6. ON when OUT1/2 are activated during direct drive

Figure 4. Operating modes – main states



2.6 Window – watchdog

During normal operation, the watchdog monitors the micro controller within a t_{SW} trigger cycle

In $V_{BAT\text{-}standby}$ and Flash program modes, the watchdog circuit is automatically disabled. After wake-up, the watchdog starts with a long open window. After serving the watchdog, the microcontroller may send the device back to $V_{1\text{-}standby}$ mode

After power-on or standby mode, the watchdog is started with a long open window t_{LW}. The long open window allows the micro controller to run its own setup and then to trigger the

watchdog via the SPI. The trigger is finally accepted when the CSN input becomes HIGH after the transmission of the SPI word.

Writing '1' to the watchdog trigger bit terminates the long open window and start the window watchdog Subsequently, the micro controller has to serve the watchdog by alternating the watchdog trigger bit within the safe trigger area (refer to watchdog chapter). A correct watchdog trigger signal immediately starts the next cycle.

After 8 watchdog failures in sequence, the V_1 regulator is switched off for t_{V1Off} If subsequently, 7 additional watchdog failures occur, the V_1 regulator is completely turned off and the device goes into $V_{BAT\text{-}standby}$ mode until a walk-up occurs.

In case of a Watchdog failure, the outputs (RELx, OUTx) are switched off and the device enters fail safe mode (i. e. all control registers are set to default values, except OUT1 when not used as FSO.)

The following diagrams illustrate the Watchdog behavior of the L99PM60J. The diagrams are split into 3 parts. First diagram shows the functional behavior of the watchdog without any error. The second diagram covers the behavior covering all the error conditions, which can affect the watchdog behavior. Third diagram shows the transition in and out of FLASH mode. All three diagrams can be overlapped to get all the possible state transitions under all circumstances. For a better readability, those transitions have been split in normal operating, operating with errors and flash mode.

Figure 5. Watchdog in normal operating mode (no errors)

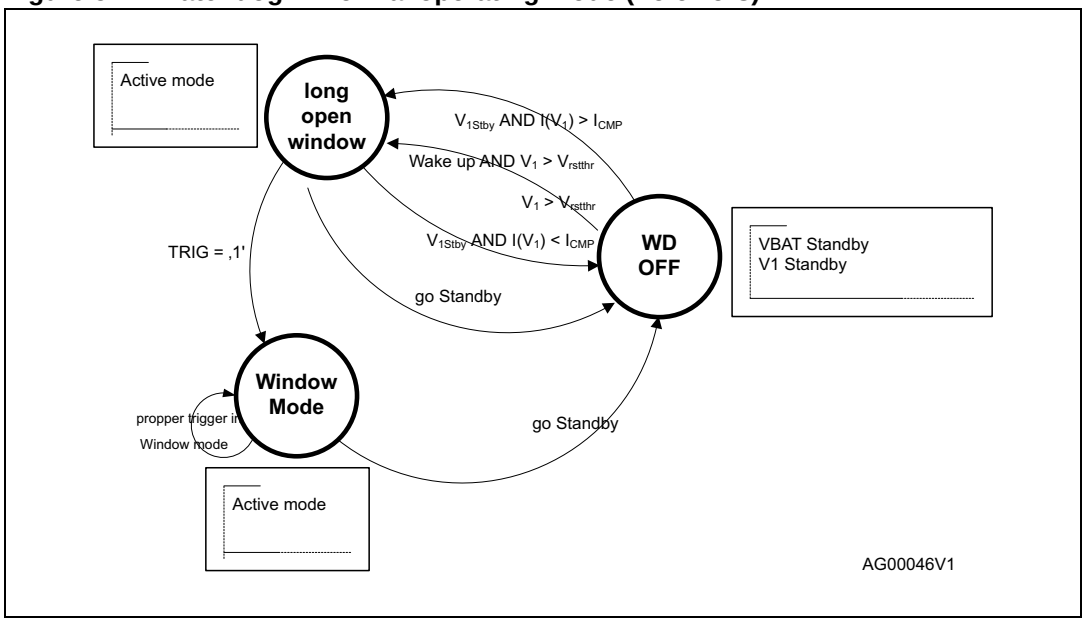


Figure 6. Watchdog with error conditions

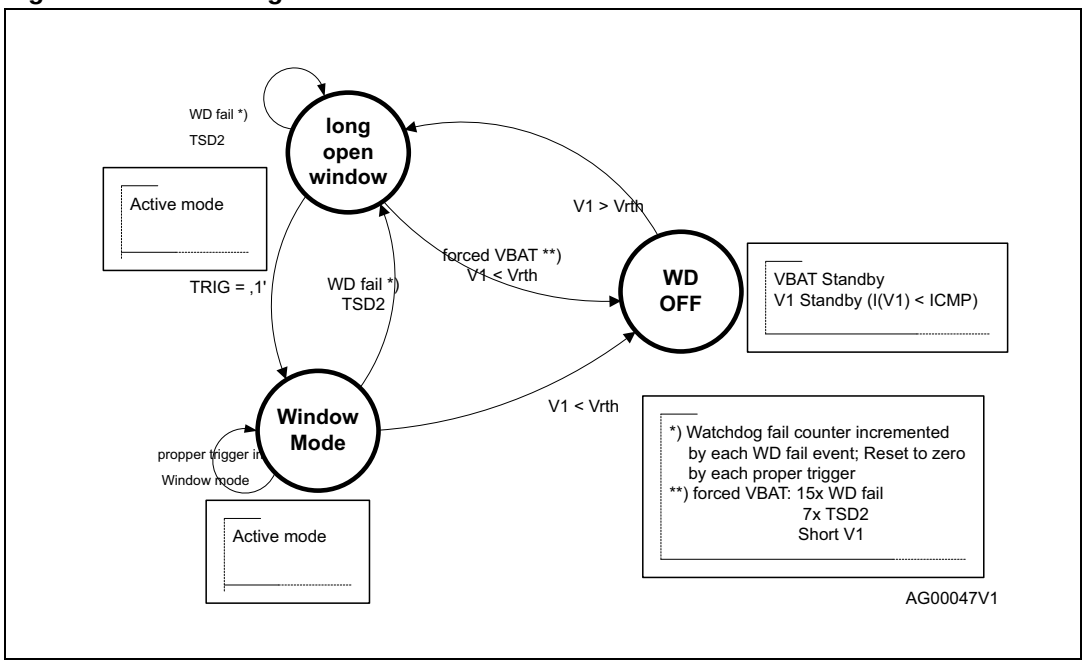
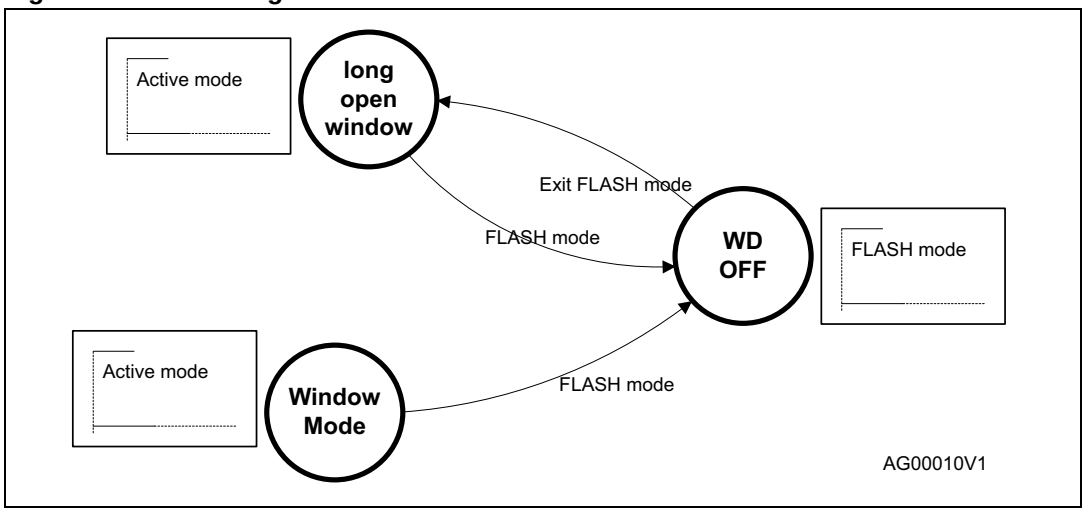


Figure 7. Watchdog in FLASH Mode



2.7 Fail Safe mode

2.7.1 Temporary failures

L99PM60J enters Fail Safe mode in case of:

- Watchdog failure
- V_1 turn on failure
  - V_1 short ($V_1 < V_{1fail}$ for $t > t_{v1short}$)
- V_1 undervoltage ($V_1 < V_{rth}$ for $t > t_{UV1}$)
  - Fail Safe Mode only entered if $V_S > V_{SUV}$
- Thermal Shutdown TSD2
- SPI failure
  - DI stuck to GND or V_{CC} (SPI frame = ’00 00’ or ‘FF FF’)

The Fail Safe functionality is also available in $V_{1\text{-standby}}$ Mode. During $V_{1\text{-standby}}$ Mode the Fails Safe Mode is entered in the following cases:

- V_1 undervoltage ($V_1 < V_{RTH}$ for $t > t_{V1FS}$)
  - Fail Safe Mode only entered if $V_S > V_{SUV}$
- Watchdog failure (if watchdog still running due to $I_{V1} > I_{CMP}$)
- Thermal Shutdown TSD2

In Fail Safe Mode the L99PM60J returns to a default state with all outputs turned off. The Fail Safe condition is indicated to the remaining system. The conditions during Fails Safe Mode are:

- All outputs are turned off
- All Control Registers are set to default values (except OUT1/FSO configuration). Write operations to Control Registers are blocked until the Fail Safe condition is cleared
- LIN Transmitter and SPI remains on
- Corresponding Failure Bits in Status Registers are set.
- FSO Bit (Bit 0 Global Status Register) is set
- OUT1/FSO is activated if configured as Fail Safe Output

OUT1 is configured as Fail Safe Output unless it is disabled by SPI.

If the Fail Safe Mode was entered it keeps active until the Fail safe condition is removed and the Fail Safe was read by SPI. Depending on the root cause of the Fail Safe, the actions to quit Fail safe Mode can be different.

Table 5. Fail safe conditions and exit modes

Failure source	Failure condition	Diagnosis	Exit from Fail Safe Mode
µC (oscillator)	Watchdog, early write failure or expired window	Failsafe = 1; WDfail = n + 1	Propper trigger in Window mode and read fail safe bit
V_1	Short at turn-on	Failsafe = 1; forced sleep TSD2/SHTV1 = 1	Read&Clear SR3 after wake
	$V_1 < V_{rth}$ for $t > t_{FSO}$ (Failsafe mode only entered when $V_S > V_{SUV}$)	Failsafe = 1; $V_{1fail} = 1$(1)	$V_1 > V_{rth}$ Read Failsafe bit
Temperature	T_j > TSD2	Failsafe = 1; TW = 1; TSD1 = 1; TSD2 = 1	T_j < TSD2 Read&Clear SR4
SPI	DI short to GND or V_{CC}	Failsafe = 1	Valid SPI command

1. if $V_1 < V_{1fail}$ (for $t > t_{v1fail}$)
The failsafe bit is located in the Global Status Register (Bit 0)

2.7.2 Nonrecoverable failures – entering forced $V_{BAT\text{-}standby}$ mode

If the failsafe condition persists and all attempts to return to normal system operation fail, the L99PM60J enters the *Forced Vbatstby Mode* in order to prevent damage to the system. The *Forced Vbatstby* Mode can be terminated by any regular wake-up event. The root cause of the *Forced Vbatstby* is indicated in the SPI Status Registers

The *Forced Vbatstby Mode* is entered in case of:

- Multiple Watchdog Failures: Forced Sleep WD = 1 (15x watchdog failure)
- Multiple Thermal Shutdown 2: Forced Sleep TSD2/SHTV1 = 1 (7x TSD2)
- V_1 short at turn-on: Forced Sleep TSD2/SHTV1 = 1 ($V_1 < V_{1fail}$ for $t > t_{v1short}$)

Table 6. Failures management

Failure Source	Failure Condition	Diagnosis	Exit from Failsafe Mode
µC (Oscillator)	15 consecutive Watchdog Failures	Failsafe=1 ForcedSleepWD =1	Wake-up TRIG=1 during LOWi Read & Clear SR3
V_1	short at turn-on	Failsafe=1 ForcedSleepTSD2/SHTV1=1	Read&Clear SR3 after wake-up
Temperature	7 times TSD2	Failsafe=1 TW=1 TSD1=1 TSD2=1 ForcedSleepTSD2/SHTV1=1	Read&Clear SR4 after wake-up Read&Clear SR3 after wake-up

Figure 8. Recovery after forced VBAT due to multiple watchdog failure

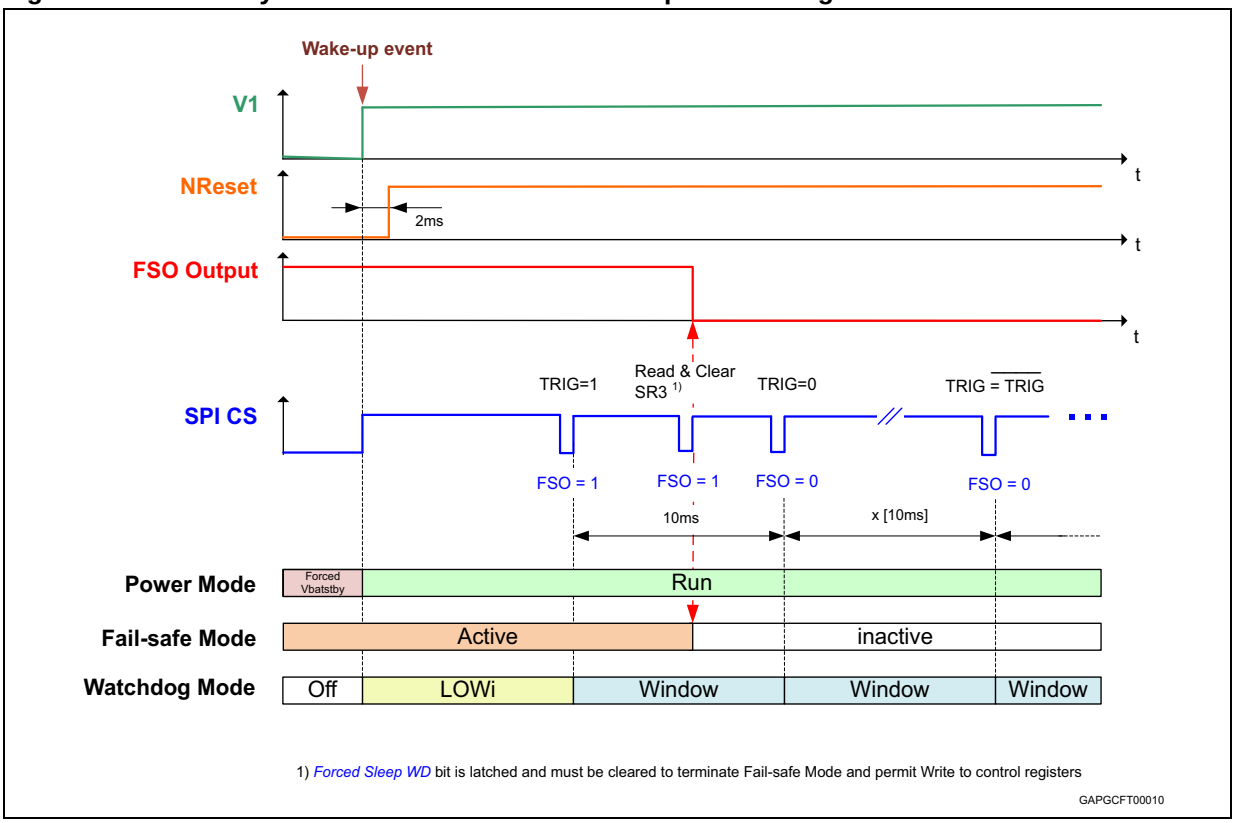


Figure 9. Recovery after forced VBAT due to multiple TSD2 failure

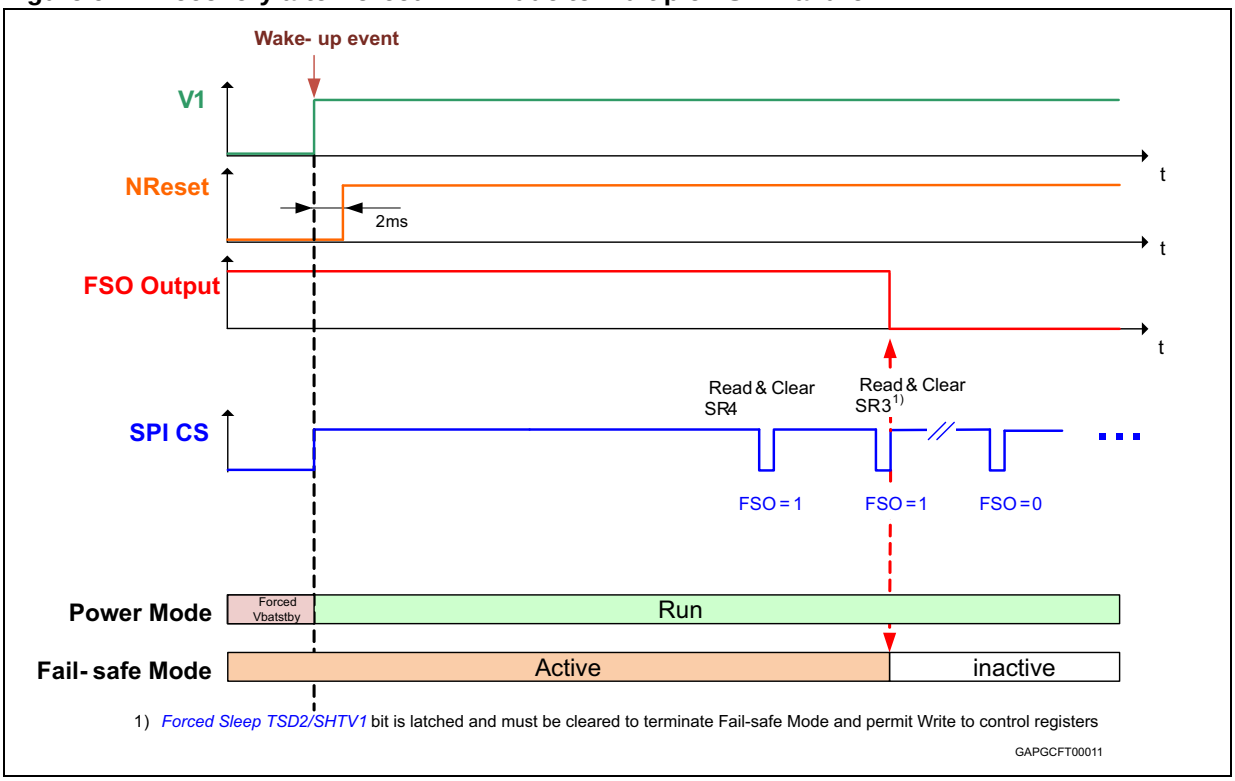
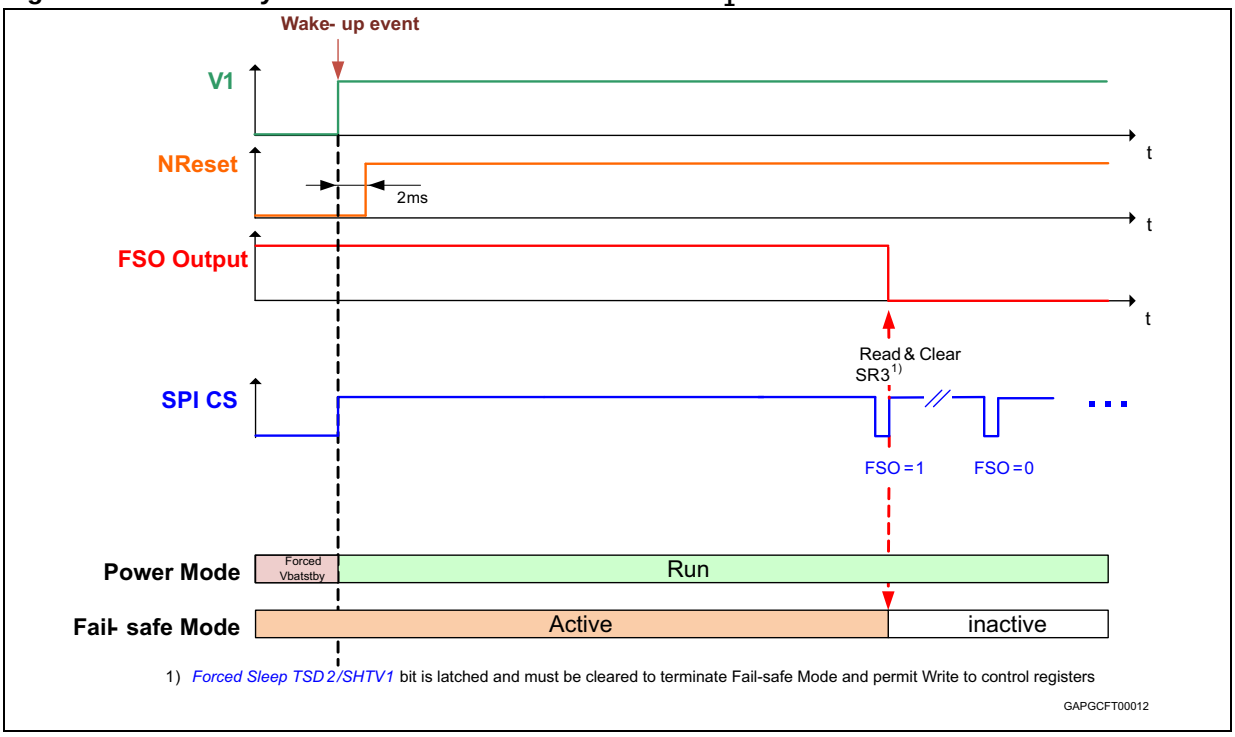


Figure 10. Recovery after forced VBAT due to short at V_1 failure



2.7.3 Fail Safe Output (OUT1)

The device provides a high side output (OUT1) which can be used as Failsafe output. The default configuration after power on for OUT1 is Failsafe output.

The Failsafe output is protected against

- Overvoltage and undervoltage (undervoltage can be masked by SPI for OUT1). See *Control Register 2*.
- Overcurrent

In case of overcurrent condition, FSO switches off. The according status bit is latched and can be read and optionally cleared by SPI. The drivers remain off until the status is cleared.

In case overvoltage or undervoltage condition, FSO is switched off. The according status bit is latched and can be read and optionally cleared by SPI. The drivers remain off until the status is cleared.

With the OUT UV shutdown enable bit (Control Register 2) the FSO can be excluded from a switch off in case of Vs Undervoltage. If the bit is set to '1' the driver switches off, otherwise the drivers remain on.

In case of open-load condition, the according status register is latched. The status can be read and optionally cleared by SPI. The FSO is not switch off.

Note: The maximum voltage and current applied to the High Side Outputs is specified in chapter 4 'Absolute Maximum Ratings'. Appropriate external protection may be required in order to respect these limits under application conditions.

2.8 Reset output (NRESET)

If V_1 is turned on and the voltage exceeds the V_1 reset threshold, the reset output "NRESET" is pulled up by internal pull up resistor to V_1 voltage after a reset delay time t_{Reset}. This is necessary for a defined start of the micro controller when the application is switched on. Since the NRESET output is realized as an open drain output it is also possible to connect an external NRESET open drain NRESET source to the output. It must be considered that as soon the NRESET is released from the L99PM60J the watchdog timing starts.

A reset pulse t_{Reset} is generated in case of:

- V_1 drops below V_{rth} (configurable by SPI) for more than V_{1UFT}
- Watchdog failure

2.9 LIN bus interface

General features:

- Speed communication up to 20kbit/s.
- LIN 2.1 compliant (SAE J2602 compatible) transceiver.
- Function range from +40V to -18V DC at LIN Pin.
- GND disconnection fail safe at module level.
- Off mode: does not disturb network.
- GND shift operation at system level.
- Micro controller Interface with CMOS compatible I/O pins.
- ESD and transient immunity according to ISO7637 and EN / IEC61000-4-2
- Matched output slopes and propagation delay

In order to further reduce the current consumption in standby mode, the integrated LIN bus interface offers an ultra low current consumption.

2.9.1 Error handling

The L99PM60J provides the following 3 error handling features which are not described in the LIN Spec. Revision 2.1, but are realized in different stand alone LIN transceivers / micro controllers to switch the application back to normal operation mode.

At Vs > Vpor (i.e. Vs power-on reset threshold), the LIN transceiver is enabled.

The LIN transmitter is disabled in case of the following errors:

- Dominant TxDL time out
- LIN permanent recessive
- Thermal shutdown 1
- V_S overvoltage / V_S undervoltage

The LIN receiver is not disabled in case of any failure condition.

Dominant TxD time out

If TXD is in dominant state (low) for more than $t_{dom(TXDL)}$(typ) the transmitter is disabled. The status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared. This feature can be disabled via SPI.

Permanent recessive

If TXD changes to dominant (low) state but RXD signal does not follow within t_{LIN}, the transmitter is disabled. The Status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

Permanent dominant

If the bus state is dominant (low) for more than $t_{dom(TXDL)}$ (typ.) a permanent dominant status is detected. The Status bit is latched and can be read and optionally cleared by SPI. The transmitter is not switched off

2.9.2 Wake up (from LIN)

In standby mode the L99PM60J can receive a wake up from LIN bus. For the wake up feature the L99PM60J logic differentiates two different conditions.

Normal wake up

Normal wake up can occur when the LIN transceiver was set in standby mode while LIN was in recessive (high) state. A dominant level at LIN for $t > t_{linbus}$, switches the L99PM60J to active mode. A interrupt is generated at the RXD/NINT pin.

Wake up from short to GND condition

If the LIN transceiver was set in standby mode while LIN was in dominant (low) state, recessive level at LIN for t_{linbus}, switches the L99PM60J to active mode. An interrupt is generated at the RXD/NINT pin.

Note: A wake up caused by a message on the bus starts the voltage regulator and the microcontroller to switch the application back to normal operation mode.

2.10 Serial Peripheral Interface (ST SPI Standard)

A 16 bit SPI is used for bi-directional communication with the micro controller.

During active mode, the SPI

- triggers the watchdog
- controls the modes and status of all L99PM60J modules (incl. input and output drivers)
- provides driver output diagnostic
- provide L99PM60J diagnostic (incl. overtemperature warning, L99PM60J operation status)

The SPI can be driven by a micro controller with its SPI peripheral running in following mode:

CPOL = 0 and CPHA = 0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to micro controller with a built-in SPI. Only three CMOS-compatible output pins and one input pin are needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-pin reflects the global error flag (fault condition) of the device.

Chip Select Not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) is in high impedance state. A low signal activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame.

Serial Data In (DI)

The input pin is used to transfer data serial into the device. The data applied to the DI is sampled at the rising edge of the CLK signal and shifted into an internal 16 bit shift register. At the rising edge of the CSN signal the contents of the shift register is transferred to Data Input Register. The writing to the selected Data Input Register is only enabled if exactly 16 bits are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame is ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.

Serial Data Out (DO)

The data output driver is activated by a logical low level at the CSN input and goes from high impedance to a low or high level depending on the global error flag (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin transfers the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK shifts the next bit out.

Serial Clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) changes with the falling edge of the CLK signal. The SPI can be driven with a CLK Frequency up to f_{CLK}.

3 Protection and diagnosis

3.1 High side driver outputs

The device provides a total of 2 high side outputs Out1,2, (7 Ω typ. at @ 25C) to drive e.g. LED's or hall sensors

The high side outputs are protected against

- Overvoltage and undervoltage (undervoltage can be masked by SPI for OUT1). See *Section : Control Register 2*
- Overcurrent
- Overtemperature[a]

In case of overcurrent or overtemperature (TSD1) condition, the drivers switches off. The according status bit is latched and can be read and optionally cleared by SPI. The drivers remain off until the status is cleared.

In case overvoltage/undervoltage condition, the drivers is switched off. The according status bit is latched and can be read and optionally cleared by SPI. The drivers remain off until the status is cleared. The driver can be excluded from undervoltage shutdown.

With the OUT UV shutdown enable bit (Control Register 2) the drivers can be excluded from a switch off in case of Vs undervoltage. If the bit is set to '1' the driver switches off, otherwise the drivers remain on.

In case of open-load condition, the according status register is latched. The status can be read and optionally cleared by SPI. The High sides is not switch off.

In case of a fail safe condition, the high side drivers are switched off. The control bits are set to default values. (Except OUT1/FSO if it is used as a High-side Output)

Note: The maximum voltage and current applied to the High Side Outputs is specified in chapter 4 'Absolute Maximum Ratings'. Appropriate external protection may be required in order to respect these limits under application conditions.

3.1.1 OUT1 reprogramming

To change the setting for OUT1 from FSO (default) to normal output configuration (ON/OFF or Direct Drive) a SPI safety sequence is required. First write command with a specific pattern to CONF Register needs to be provided in order to enable the write access for configuration bits of OUT1. With an SPI write command to Control Register 1 the bits for OUT1 can be modified.

The write command to Control Register 1 must follow the write command to the CONF Register (no other SPI command in between these 2 commands)

Safety Sequence:

1. Write to Conf Register (0x0011 1111; 1010 101x)
   x: don't care for unlocking sequence but according to description of watchdog timing
2. Write to Ctrl Register 1 (0x0000 0001; xxxx xxxx)
   x: values according to description of Ctrl Reg1

a. Except OUT1 when configured as FSO

3.2 Low side driver outputs REL1, REL2

The outputs REL1, REL2 (R_{DSon} = 2 Ω typ. at 25 °C) are specially designed to drive relay loads.

Typical relays used have the following characteristics:

Relay type 1: ON-state: R = 160 Ω typical ±10%, L = 300 mH: Off-state: 240 mH
Relay type 2: ON-state: R = 220 Ω typical ±10 %, L = 420 mH: Off-state: 330 mH

The outputs provide an active output Zener clamping (44 V typ) feature for the demagnetisation of the relay coil, even though a load dump condition exists.

The low side drivers switch off in case of:

- V_S overvoltage and undervoltage (can be masked by SPI) Control Register 2, Bit0
- Overcurrent
- Overtemperature

In case of overload or overtemperature (TSD1) condition, the drivers switches off. The according status bit is latched and can be read and optionally cleared by SPI. The drivers remain off until the status is cleared.

In case V_S overvoltage and undervoltage condition, the drivers is switched off. The according status bit is latched and can be read and optionally cleared by SPI. The drivers remain off until the status is cleared.

With the LS OVUV shutdown enable bit (Control Register 2) the drivers can be excluded from a switch off in case of overvoltage and undervoltage. If the bit is set to ‘1’ the driver switches off, otherwise the drivers remain on.

3.3 SPI diagnosis

Digital diagnosis features are provided by SPI (for details please refer to *Section 7.2: SPI registers*)

- V_1 reset threshold programmable
- Overtemperature including pre warning
- Open-load separately for each OUT1,2
- Overload status separately for each output stage
- $V_{S\text{-}supply}$ overvoltage/undervoltage
- $V_{1\text{-}fail}$ bit
- V_1 undervoltage
- Chip Reset bit (start from power-on reset)
- Number of unsuccessful V_1 restarts after thermal shutdown
- Number of sequential watchdog failures
- LIN diagnosis (permanent recessive/dominant, dominant TxD)
- Device state (wake-up from V1stby or Vbatstby)
- Forced Vbatstby after WD-fail, forced Vbatstby after overtemperature
- Watchdog timer state (diagnosis of watchdog)
- Failsafe status
- SPI communication error

4 Power supply fail

Overvoltage and undervoltage detection on V_S

4.1 V_S overvoltage

If the supply voltage Vs reaches the overvoltage threshold (V_{SOV})

- The outputs OUT1,2, REL1,2 and LIN are switched to high impedance state (load protection).
- The overvoltage bit is set and can be cleared with a ‘Read and Clear’ command.
- Outputs REL1,2 can be excluded from a shutdown in case of overvoltage by SPI

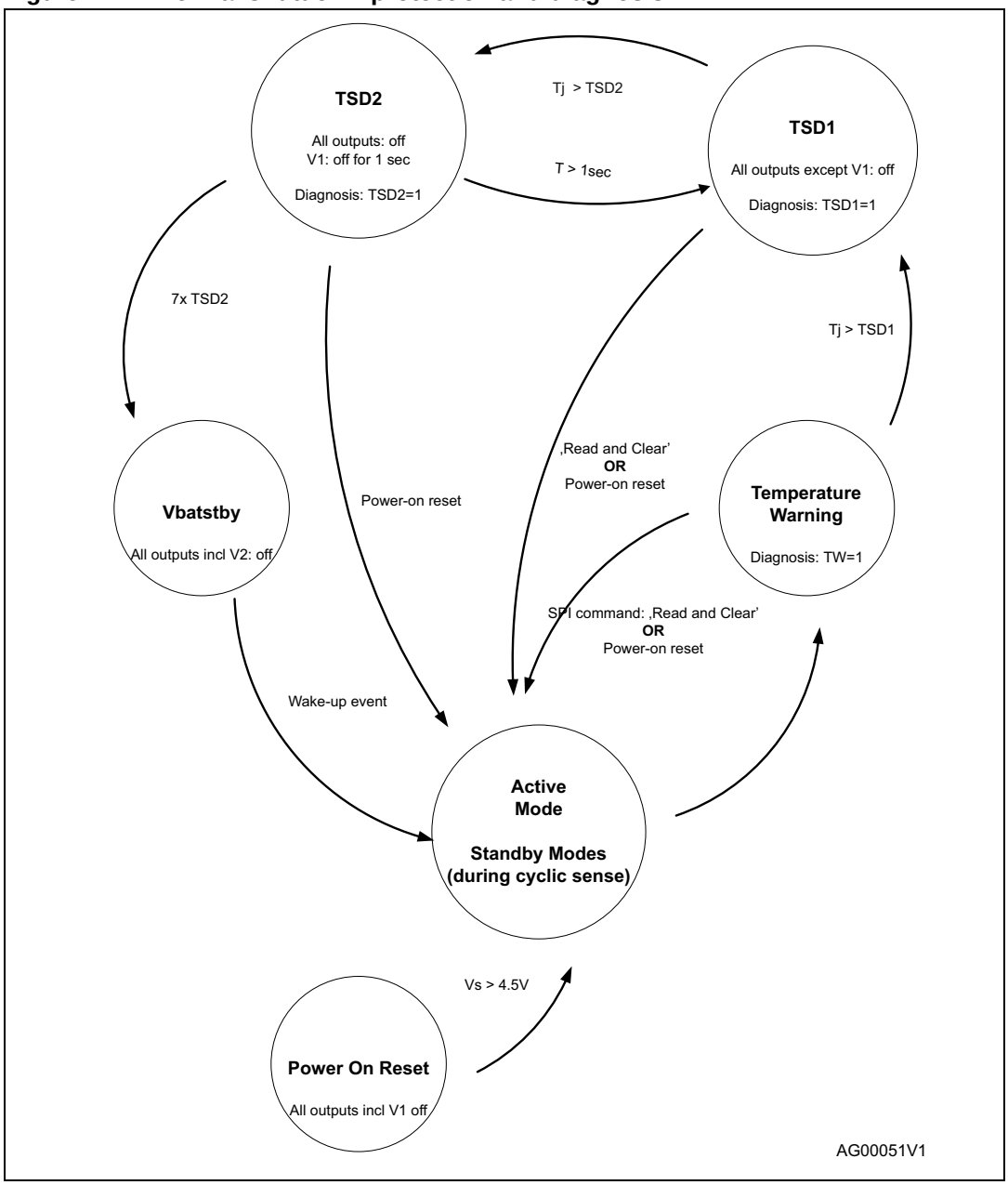
4.2 V_S undervoltage

If the supply voltage Vs drops below the undervoltage threshold voltage (V_{SUV})

- The outputs OUT1,2, REL1,2, LIN are switched to high impedance state.
- The undervoltage bit is set and can be cleared with the ‘Read and Clear’ command.
- Outputs REL1,2 can be excluded from a shutdown in case of undervoltage by SPI
- Output OUT1,2 can be excluded from a shutdown in case of undervoltage by SPI

4.3 Temperature warning and thermal shutdown

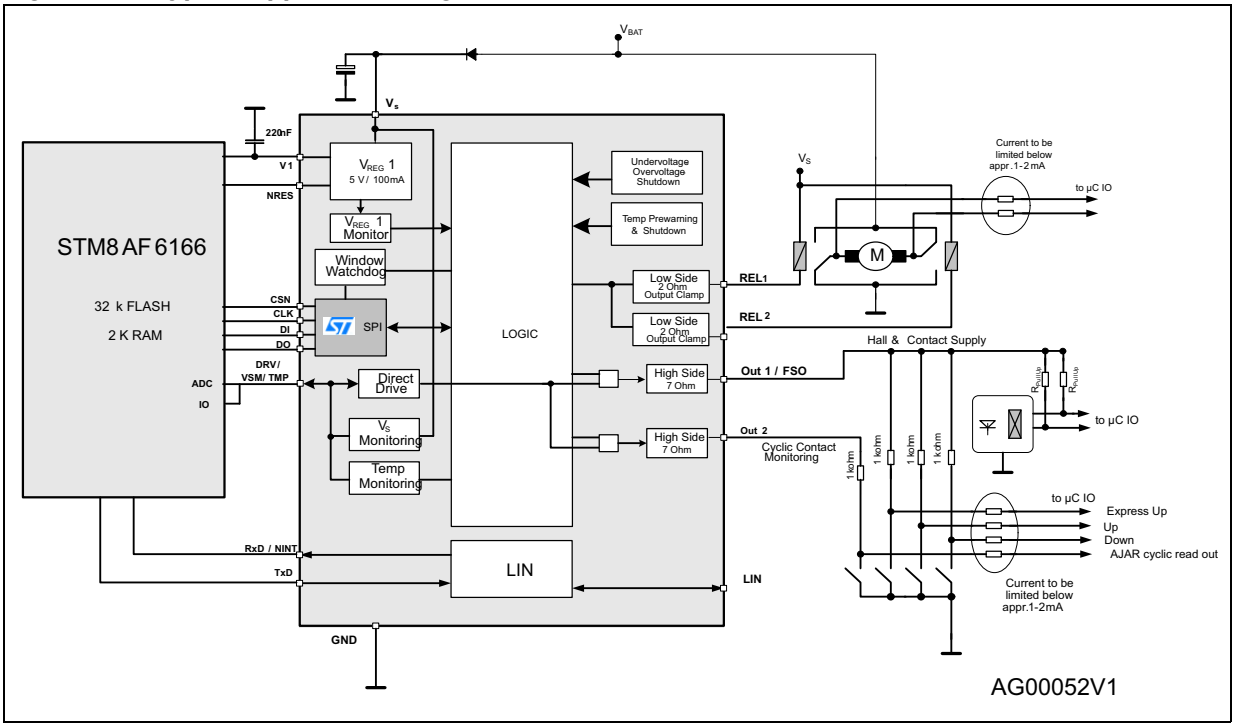
Figure 11. Thermal shutdown protection and diagnosis



Note: With the first transition into the TSD2 state failsafe mode is entered. The Thermal State machine recovers the same state were it was before entering Standby Mode. In case of a TSD2 it enters TSD1 state.

5 Typical application

Figure 12. Typical application diagram



6 Electrical specifications

6.1 Absolute maximum ratings

Table 7. Absolute maximum rating

Symbol	Parameter / test condition	Value [DC voltage]	Unit
V_S	DC supply voltage / "jump start"	-0.3 to +28	V
	Load dump	-0.3 to +40	V
V_1	Stabilized supply voltage, logic supply	-0.3 to +5.25	V
V_{DI} V_{CLK} V_{TXD} V_{DO} V_{RXD} V_{NRESET} V_{DRV}	Logic input / output voltage range	-0.3 to V_1 + 0.3	V
V_{CSN}	Multi Level Input	-0.3 to Vs + 0.3	V
V_{REL1} $V_{REL2,}$	Low-side output voltage range	-0.3 to +40	V
$V_{OUT1..2,}$	High-side output voltage range	-0.3 to V_S + 0.3	V
I_{In_put}	Current injection into V_S related input pins	10	mA
Iout_inj	Current injection into V_S related outputs	10	mA
V_{LIN}	LIN bus I/O voltage range	-20 to +40	V

Note: All maximum ratings are absolute ratings. Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit!

Loss of ground or ground shift with externally grounded loads: ESD structures are configured for nominal currents only. If external loads are connected to different grounds, the current load must be limited to this nominal current.

6.2 ESD protection

Table 8. ESD protection

Parameter	Value	Unit
All pins (1)	+/-2	kV
All output pins (2)	+/-4	kV
LIN	+/-8(2) +/-10(3) +/-7(4)	kV
All pins(5)	+/-500	V

Table 8. ESD protection (continued)

Parameter	Value	Unit
Corner pins(5)	+/-750	V
All pins(6)	+/-200	V

1. HBM (human body model, 100pF, 1.5 kΩ) according to MIL 883C, Method 3015.7 or EIA/JESD22A114-A
2. HBM with all none zapped pins grounded.
3. Indirect ESD Test according to IEC 61000-4-2 (150 pF, 330 Ω) and 'Hardware Requirements for LIN and Flexray Interfaces in Automotive Applications' (version 1.1, 2009-12-02)
4. Direct ESD Test according to IEC 61000-4-2 (150 pF, 330 Ω) and 'Hardware Requirements for LIN and Flexray Interfaces in Automotive Applications' (version 1.1, 2009-12-02); $C_{bus,LIN}$ = 220 pF
5. Charged device model
6. Machine model: C = 200 pF; R = 0 Ω

6.3 Thermal data

Table 9. Operating junction temperature

Symbol	Parameter	Value	Unit
T_j	Operating junction temperature	-40 to 150	°C
R_{thjA}	Thermal resistance junction / ambient	See *Figure 26*	°K/W

Table 10. Temperature warning and thermal shutdown

Symbol	Parameter		Min.	Typ.	Max.	Unit
$T_{W\ ON}$	Thermal overtemperature warning threshold	T_j(1)	120	130	140	°C
$T_{SD1\ OFF}$	Thermal shutdown junction temperature 1	T_j(1)	130	140	150	°C
T_{SD2OFF}	Thermal shutdown junction temperature 2	T_j(1)	150	160	170	°C
$T_{SD2\ ON}$		Hysteresis		5		°C
$T_{SD12hys}$						

1. Non-overlapping

6.4 Electrical characteristics

6.4.1 Supply and supply monitoring

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.

6 V ≤ V_S ≤ 18V; 4.8 V ≤ V_1 ≤ 5.2 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 11. Supply and supply monitoring

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{SAbsmin}$ (1)	V_S absolute minimum value for controlling V_1 and NReset outputs	V_S increasing / decreasing	—	2.5	—	V
V_S	Supply voltage range		6	13.5	18	V
V_{SUV}	VS UV-threshold voltage	V_S increasing / decreasing	5.11		5.81	V
V_{hyst_UV}	Undervoltage hysteresis		0.04	0.1	0.15	V
V_{SOV}	VS OV-threshold voltage	V_S increasing / decreasing	18		22	V
V_{hyst_OV}	Overvoltage hysteresis	Hysteresis	0.5	1	1.5	V
$I_{V(act)}$	Current consumption in active mode	V_S = 12 V; TxD LIN high; V_1 = 5 V; HS/LS drivers OFF; V_{LIN} > (V_S - 1.5 V)		6	12	mA
$I_{V(BAT)}$	Current consumption in $V_{BAT\text{-}standby}$ mode	V_S = 12 V; V_1 = OFF; V_{LIN} > (V_S - 1.5 V)	1	7	16	µA
$I_{V(V1)}$	Current consumption in $V_{1\text{-}standby}$ mode	V_S = 12 V; V_1 = 5 V; HS/LS drivers OFF; V_{LIN} > (V_S - 1.5 V); I_{v1} < I_{CMP_Fail}	10	48	70	µA
$I_{V(V1)CS}$	Current consumption in $V_{1\text{-}standby}$ during direct drive	V_S = 12 V; V_1 = 5 V; LS drivers OFF; V_{LIN} > (V_S - 1.5 V); I_{v1} < I_{CMP_Fail} $45\mu A + \frac{t_{on}}{t_{period}} \cdot 1750\mu A$ at t_{on} = 200 µs; t_{period} = 50 ms	50	55	60	µA

1. For V_S > $V_{Sabsmin}$ the V_1 and NRESET output are actively driven.
V_S < $V_{Sabsmin}$ the V_1 output is connected to ground by passive pull down resistor of 1MΩ.

6.4.2 Oscillator

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 4.5 V ≤ V_S ≤ 28 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 12. Oscillator

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
F_{CLK}	Oscillation frequency		0.808	1.0	1.35	MHz

6.4.3 Power-on reset (V_S)

All outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 13. Power-on reset (V_S)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{POR}	V_{POR} threshold	(V_S increasing)		3.45	4.5	V
V_{POR}	V_{POR} threshold	(V_S decreasing)(1)	2.2	2.6	3.5	V

1. This threshold is valid if Vs had already reached 7V previously

6.4.4 Voltage regulator V_1

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 28 V; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 14. Voltage regulator V_1

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_1	Output voltage			5.0		V
V_1	Output voltage tolerance Active mode	I_{LOAD} = 6 mA... 50 mA, V_S = 13.5 V			+/-2	%
Vhc1	Output voltage tolerance active mode, high current	I_{LOAD} = 50 mA... 100 mA, V_S = 13.5 V			+/-2.5	%
VSTB1	Output voltage tolerance $V_{1\text{-standby}}$ mode	I_{LOAD} = 0uA...5mA V_S = 13.5V	-2		+4.5	%
VDP1	Drop-out voltage	I_{LOAD} = 50 mA; V_S = 4.5 V		0.2	0.4	V
		I_{LOAD} = 100 mA; V = 4.5 V		0.3	0.5	V
ICC1	Output current in active mode	Max. continuous load current			100	mA
ICCmax1	Short circuit output current	Current limitation	400	600	950	mA
Cload1	Load capacitor1	Ceramic	0.22			µF
tTSD	V_1 deactivation time after thermal shutdown			1		s
I_{CMP_rise}	Current comp. rising threshold	Rising current	2.1	4.6	6.8	mA
I_{CMP_fail}	Current comp. falling threshold	Falling current	1.5	3.6	6.0	mA

Table 14. Voltage regulator V_1 (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{CMP_hys}	Current comp. hysteresis			0.5		mA
V_{1fail}	V_1 fail threshold	V_1 forced		2		V
t_{V1fail}	V_1 fail Filter time			2		us
$t_{V1short}$	V_1 short to ground detection filter time	V_1 short to ground		4		ms
t_{V1FS}	V_1 Fail safe filter time			2		ms

Note: Nominal capacitor value required for stability of the regulator. Tested with 220nF ceramic (+/- 20%). Capacitor must be located close to the regulator output pin.

6.4.5 Reset output (V_1 supervision)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. 4.0 V < V_S = 28 V; T_j = -40 to 130 °C, unless otherwise specified.

Table 15. Reset output (V_1 supervision)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{RT1}	Reset threshold voltage1	V_{V1} decreasing	3.35	3.5	3.65	V
V_{RT1}	Reset threshold voltage1	V_{V1} increasing	4.4	4.6	4.85	V
V_{RT2}	Reset threshold voltage2 (default)	V_{V1} increasing / decreasing	4.4	4.6	4.85	V
V_{RESET}	Reset pin low output voltage	V_1 > 1 V; I_{RESET} = 1 mA		0,2	0,4	V
R_{RESET}	Reset pull up int. resistor		60	110	204	kΩ
t_{RR}	Reset reaction time	@I_{LOAD} = 1 mA	6		40	µs
$V1_{UVFT}$	V_1 undervoltage filter time			16		µs
t_{Reset}	Reset delay time			2		ms

6.4.6 Watchdog

4.5 V < V_S < 28 V; 4.8 V < V_1 < 5.2 V; T_j = -40 to 130 °C, unless otherwise specified, see *Figure 13* and *Figure 14*)

Table 16. Watchdog

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{LW}	Long open window		48.75	65	81.25	ms
T_{EFW1}	Early failure window 1				4.5	ms
T_{LFW1}	Late failure window 1		20			ms
T_{SW}	Safe window 1		7.5	10	12	ms

Table 16. Watchdog (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{WDR}	Watchdog reset pulse time		1.5	2	2.5	ms
t_{V1Off}	V_1 deactivation duration after 8 consecutive WD failures		150	200	250	ms

Figure 13. Watchdog timing (missing watchdog trigger)

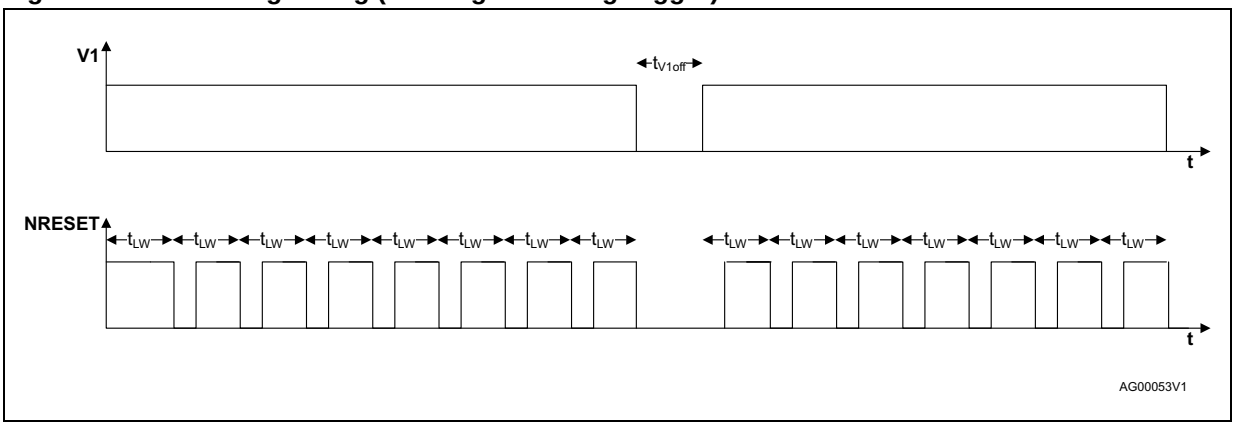
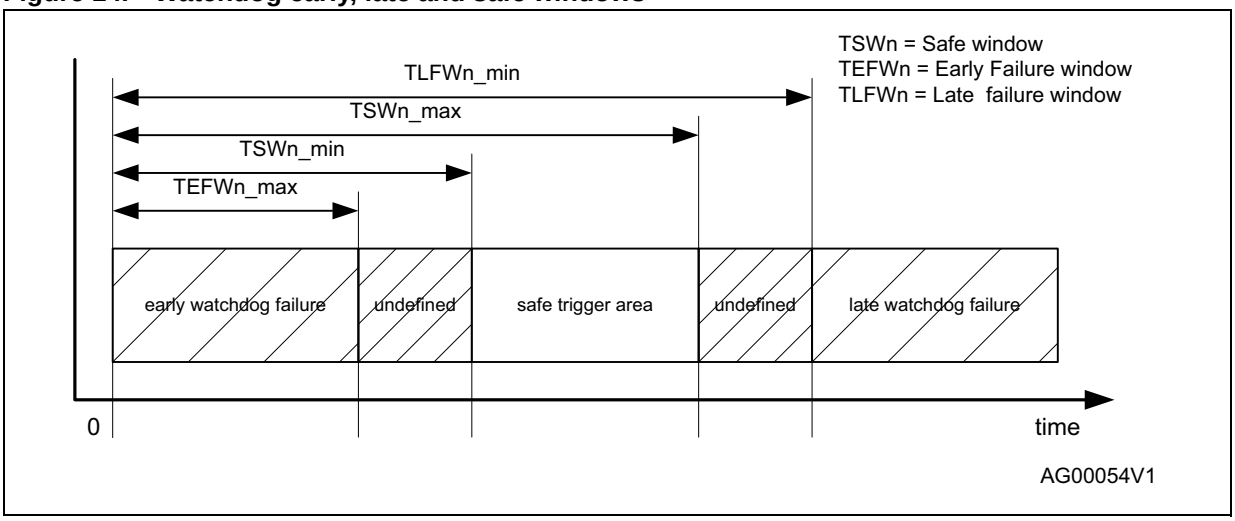


Figure 14. Watchdog early, late and safe windows



6.4.7 High-side outputs

Outputs (OUT1…2);

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

6 V $\leq V_S \leq$ 18 V; 4.8 V $\leq V_1 \leq$ 5.2 V; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 17. Output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
RDSON	DC output resistance	I_{LOAD} = 60 mA at T_j = 25 °C	0	7	12	Ω
IOUT	Short circuit shutdown current	8 V < V_S < 16 V	140	235	330	mA
t_{SCF}	Short circuit filter time	Tested by scan chain		64 * T_{OSC}		
IOLD	Open-load detection current 1		0.5	2	4.2	mA
t_{OLDT}	Open-load filter time	Tested by scan chain		64 * T_{OSC}		
SR	Slew rate		0.2	0.5	0.8	V/µs
t_{dONHS}	Switch ON delay time	0.2 V_S	5	35	60	µs
t_{dOFFHS}	Switch OFF delay time	0.8 V_S	20	95	150	µs
t_{SCF}	Short circuit filter time	Tested by scan chain		64 * T_{OSC}		
I_{FW}(1)	Loss of GND current (ESD structure)		100			mA

1. Parameter guaranteed by design

6.4.8 Low-side drivers

Outputs (REL1…2);

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

6 V ≤ V_S ≤ 18 V; 4.8 V ≤ V_1 ≤ 5.2 V; T_j = -40 to 130 °C, unless otherwise specified.

Table 18. Relay drivers

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{DSON}	DC output resistance	I_{LOAD} = 100 mA @ T_j = 25 °C	0	2	3	Ω
I_{OUT}	Short circuit shut down current	8 V < V_S < 16 V	250	375	500	mA
V_Z	Output clamp voltage(1)	I_{LOAD} = 100 mA	40	44	48	V
t_{ONHL}	Turn on delay time to 10% V_{OUT}		2.5	50	100	µs
t_{OFFLH}	Turn off delay time to 90% V_{OUT}		5	50	100	µs
t_{SCF}	Short circuit filter time	Tested by scan chain		64 * T_{OSC}		
SR	Slew rate		0.2	2	4	V/µs

1. The output is capable to switch off relay coils with the impedance of R_L = 160 Ω; L = 300 mH (R_L = 220 Ω; L = 420 mH); at V_S = 40 V (Load dump condition).

6.4.9 Direct drive / voltage supply monitoring

Input: DRV

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.

6 V ≤ V_S ≤ 18 V; 4.8 V ≤ V_1 ≤ 5.2 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 19. Input: DRV

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VDRVLOW	Input voltage low level	Normal mode, V_1 = 5 V	1.0	2.3	2.9	V
VDRVHIGH	Input voltage high level	Normal mode, V_1 = 5 V	1.5	2.8	3.8	V
VDRVHYS	VCSNHIGH – VCSNLOW	Normal mode, V_1 = 5 V	0.4	0.75	1.5	V
IDRVPD	Pull down current at input	Normal mode, V_{in} = 1.5 V	5	30	60	µA
C_{in}(1)	Input capacitance	0 V < V_1 < 5.2 V		25	35	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

Output: VSOUT

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.

6 V ≤ V_S ≤ 18 V; 4.8 V ≤ V_1 ≤ 5.2 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 20. Output: VSOUT

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VSOUT	Output voltage	V_S = 6 V; V_S = 10 V; V_S = 18 V	0.195 V_S	0.2 V_S	0.205 V_S	V
VSOUTUV	V_S output voltage in case of undervoltage	V_S = 4.5 V; VSM selected		0.0		V
VSOUTOV	V_S output voltage in case of overvoltage	V_S = 24 V; VSM selected		5.0		V
VTROOM	T_{SENSE} output voltage at 25 °C	V_S = 12 V; T = 25 °C		1.38		V
VTSENSE	T_{SENSE} output voltage	T = 25 °C; T= 130 °C; T = -40 °C		3.5		mV/K
I_{VSOUT}	Pull-up pull-down current ability			2		mA

6.4.10 LIN

LIN 2.1 compliant for Baud rates up to 20 kBit/s (SAE J2602 compatible) baud rate of the LIN bus can be upgraded up to 100 kBits by SPI bit configuration (LIN Flash bit 3 CR2).

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
6 V ≤ V_S ≤ 18 V; 4.8 V ≤ V_1 ≤ 5.2 V; $T_{junction}$ = -40 °C to 130 °C unless otherwise specified.

Table 21. LIN transmit data input: pin TXD

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{TXDOW}	Input voltage dominant level	Normal mode; V_1 = 5 V	0.8	1.9		V
$V_{TXDHIGH}$	Input voltage recessive level	Normal mode; V_1 = 5 V		2.9	3.5	V
V_{TXDHYS}	$V_{TXDHIGH} - V_{TXDOW}$	Normal mode; V_1 = 5 V	0.5	1.0	1.5	V
I_{TXDPU}	TXD pull up resistor	Normal mode; V_1 = 5 V		20		kΩ
I_{TXDPD}	TXD pull-down current	Test mode; V_{IN} = 10 V		480		µA

Table 22. LIN receive data output: pin RXD

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{RXDOW}	Output voltage dominant level	Normal mode; V_1 = 5 V; 2 mA		0.2	0.5	V
$V_{RXDHIGH}$	Output voltage recessive level	Normal mode; V_1 = 5 V; 2 mA	4.5			V

Table 23. LIN transmitter and receiver: pin LIN

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{Thdom}	Receiver threshold voltage recessive to dominant state		0.4 V_S	0.45 V_S	0.5 V_S	V
V_{Busdom}	Receiver dominant state				0.4 V_S	V
V_{Threc}	Receiver threshold voltage dominant to recessive state		0.5 V_S	0.55 V_S	0.6 V_S	V
V_{Busrec}	Receiver recessive state		0.6 V_S			V
V_{Thhys}	Receiver threshold hysteresis	$V_{Threc} - V_{Thdom}$	0.07 V_S	0.1 V_S	0.175 V_S	V
V_{THcnt}	Receiver tolerance center value	$(V_{Threc} + V_{Thdom}) / 2$	0.475 V_S	0.5 V_S	0.525 V_S	V
V_{Thwkup}	Receiver walk-up threshold voltage		1.0	1.5	2	V
$V_{THwkdwn}$	Receiver walk-up threshold voltage		V_S - 3.5	V_S - 2.5	V_S - 1.5	V
t_{linbus}	Dominant time for walk-up via bus	Sleep mode edge: recessive-dominant		64 * T_{OSC}		µs
$I_{LINDomSC}$	Transmitter input current limit in dominant state	$V_{TxD} = V_{TxDlow}$; $V_{LIN} = V_{batmax}$ = 18 V	40	100	180	mA
$I_{bus\_PAS\_dom}$	Input leakage current at the receiver incl. pull-up resistor	$V_{TxD} = V_{TxDhigh}$; V_{LIN} = 0 V; V_{BAT} = 12 V(1)	-1			mA
$I_{bus\_PAS\_rec}$	Transmitter input current in recessive state	$V_{TxD} = V_{TxDhigh}$; 8 V < V_{LIN} < 18 V; 8 V < V_{BAT} < 18 V; $V_{LIN} > V_{BAT}$			20	µA

Table 23. LIN transmitter and receiver: pin LIN (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{bus\_NO\_GND}$	Input current if loss of GND at device	GND = V_S; 0 V < V_{LIN} < 18 V; V_{BAT} = 12 V	-1		1	mA
I_{bus}	Input current if loss of V_{bat} at device	GND = V_S; 0 V < V_{LIN} < 18 V			100	µA
V_{LINdom}	LIN voltage level in dominant state	V_{TxD} = V_{TxDlow}; I_{LIN} = 40 mA			1.2	V
V_{LINrec}	LIN voltage level in recessive state	V_{TxD} = $V_{TxDhigh}$; I_{LIN} = 10 µA	0.8 Vs			V
R_{LINup}	LIN output pull up resistor	V_{LIN} = 0 V	20	40	60	kΩ

1. Slave Mode

Table 24. LIN transceiver timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{RXpd}	Receiver propagation delay time	t_{RXpd} = max(t_{RXpdr}, t_{RXpdf}); t_{RXpdf} = t(0.5 RXD) - t(0.45 V_{LIN}); t_{RXpdr} = t(0.5 RXD) - t(0.55 V_{LIN}); C_{RXD} = 20 pF; V_S = 12 V; R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 kΩ, C_{bus} = 6.8 nF; R_{bus} = 500 kΩ, C_{bus} = 10 nF			6	µs
t_{RXpd_sym}	Symmetry of receiver propagation delay time (rising vs. falling edge)	t_{RXpd_sym} = t_{RXpdr} – t_{RXpdf}	-2		2	µs
D1	Duty cycle 1	TH_{Rec}(max) = 0.744 * V_S; TH_{Dom}(max) = 0.581 * V_S; V_S = 7…18 V; t_{bit} = 50 µs; D1 = t_{bus_rec}(min)/(2 x t_{bit}) R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 kΩ, C_{bus} = 6.8 nF; R_{bus} = 500 kΩ, C_{bus} = 10 nF	0.396			
D2	Duty Cycle 2	TH_{Rec}(min) = 0.422 * V_S; TH_{Dom}(min) = 0.284 * V_S; V_S = 7.6 …18 V; t_{bit} = 50 µs; D1 = t_{bus_rec}(max)/(2 x t_{bit}) R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 kΩ, C_{bus} = 6.8 nF; R_{bus} = 500 kΩ, C_{bus} = 10 nF			0.581	
D3	Duty Cycle 3	TH_{Rec}(max) = 0.778 * V_S; TH_{Dom}(max) = 0.616 * V_S; V_S = 7…18 V; t_{bit} = 96 µs; D3 = t_{bus_rec}(min)/(2 x t_{bit}) R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 kΩ, C_{bus} = 6.8 nF; R_{bus} = 500 kΩ, C_{bus} = 10 nF	0.417			

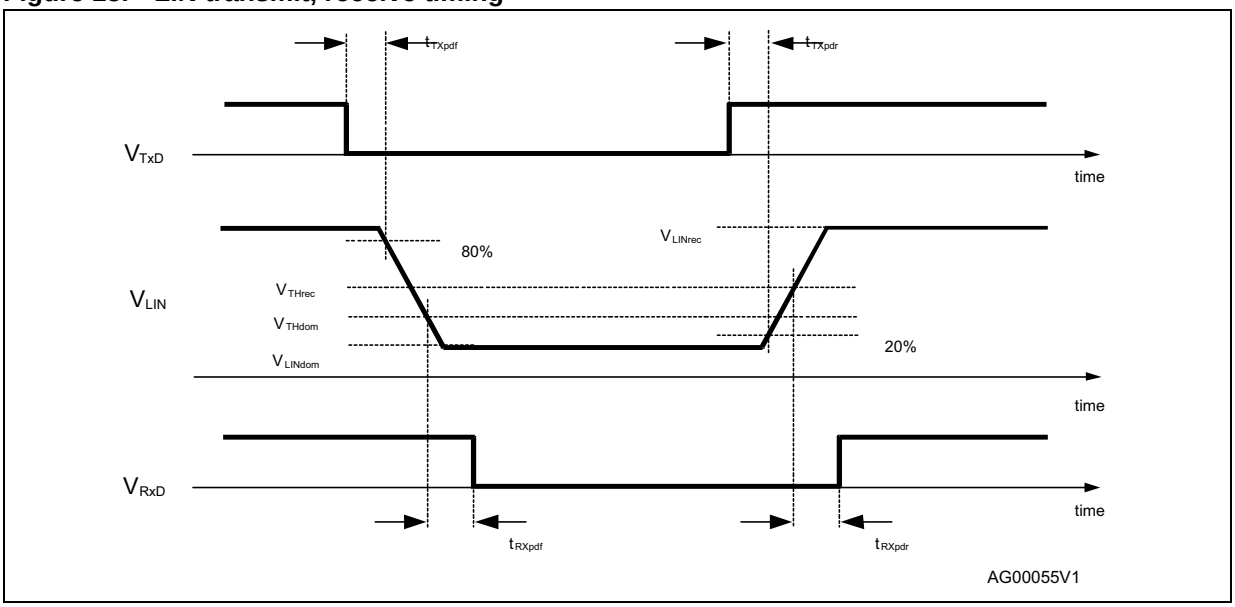
Table 24. LIN transceiver timing (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
D4	Duty Cycle 4	$TH_{Rec}(min) = 0.389 * V_S$; $TH_{Dom}(min) = 0.251 * V_S$; V_S = 7.6…18 V; t_{bit} = 96 µs; D1 = $t_{bus\_rec}(max)/(2 \times t_{bit})$ R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 kΩ, C_{bus} = 6.8 nF; R_{bus} = 500 kΩ, C_{bus} = 10 nF			0.590	
$t_{dom(TXDL)}$	TXDL dominant time-out			12		ms
t_{LIN}	LIN permanent recessive time-out			40		µs
RDSon	ON resistance			10.5	16	Ω

Table 25. LIN Flash mode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SRf	LIN slew rate falling edge	From 20% to 80% of V_{LIN}; V_S = 12 V; R_{bus} = 150 Ω; C_{bus} = 1 nF	—	13	—	V/µs

Figure 15. LIN transmit, receive timing



6.4.11 SPI

Input: CSN

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.

6 V ≤ V_S ≤ 18 V; 4.8 V ≤ V_1 ≤ 5.2 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 26. Input: CSN

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VCSNLOW	Input voltage low level	Normal mode; V_1 = 5 V	0.8	1.9	2.5	V
VCSNHIGH	Input voltage high level	Normal mode; V_1 = 5 V	1.5	2.9	3.5	V
VCSNHYS	VCSNHIGH – VCSNLOW	Normal mode; V_1 = 5 V	0.5	1.0	1.5	V
ICSNPU	CSN pull up resistor	Normal mode; V_1 = 5 V	10	20	35	kΩ
ICSNPD	CSN pull-down current	Test mode, V_{IN} = 10 V		480		µA

Input CSN for Flash mode

6 V ≤ V_S ≤ 18 V, 4.5 V ≤ V_1 ≤ 5.3 V; T_j = -40 °C to 130 °C; voltages are referred to GND, all outputs open

Table 27. Input CSN for Flash mode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{flashL}	Input level V_{CSN} exit Flash mode)	V_1 = 5 V	6.1	7.25	8.4	V
V_{flashH}	Input level V_{CSN} entering Flash mode	V_1 = 5 V	7.4	8.4	9.4	V
$V_{flashHYS}$	Input voltage hysteresis	V_1 = 5 V	0.6	0.8	1.0	V

Inputs: CLK, DI

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.

6 V ≤ V_S ≤ 18 V; 4.8 V ≤ V_1 ≤ 5.2 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 28. Inputs: CLK, DI

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{set}	Delay time from standby to active mode	Switching from standby to active mode. Time until output drivers are enabled after CSN going to high.		160	300	us
$V_{in\ L}$	Input low level	V_1 = 5 V	1.0	2.3	2.9	V
$V_{in\ H}$	Input high level	V_1 = 5 V	1.5	2.8	3.8	V
$V_{in\ Hyst}$	Input hysteresis	V_1 = 5 V	0.4	0.75	1.5	V
I_{in}	Pull down current at input	V_{IN} = 1.5 V	5	30	60	µA
C_{in} (1)	Input capacitance at input CSN, CLK, DI and $PWM_{1,2}$	0 V < V_1 < 5.2 V		10	15	pF
f_{CLK}	SPI input frequency at CLK				1	MHz

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

DI timing[(b)]

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.

6 V ≤ V_S ≤ 18 V; 4.8 V ≤ V_1 ≤ 5.2 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 29. DI timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{CLK}	Clock period	V_1 = 5 V	1000	—		ns
t_{CLKH}	Clock high time	V_1 = 5 V	400	—		ns
t_{CLKL}	Clock low time	V_1 = 5 V	400	—		ns
$t_{set\ CSN}$	CSN setup time, CSN low before rising edge of CLK	V_1 = 5 V	400	—		ns
$t_{set\ CLK}$	CLK setup time, CLK high before rising edge of CSN	V_1 = 5 V	400	—		ns
$t_{set\ DI}$	DI setup time	V_1 = 5 V	200	—		ns
$t_{hold\ DI}$	DI hold time	V_1 = 5 V	200	—		ns
$t_{r\ in}$	Rise time of input signal DI, CLK, CSN	V_1 = 5 V		—	100	ns
$t_{f\ in}$	Fall time of input signal DI, CLK, CSN	V_1 = 5 V		—	100	ns

Output DO

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.

6 V ≤ V_S ≤ 18 V; 4.8 V ≤ V_1 ≤ 5.2 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 30. Output DO

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DOL}	Output low level	V_1 = 5 V; I_D = -4 mA			0.5	V
V_{DOH}	Output high level	V = 5 V; I_D = 4 mA	4.5			V
I_{DOLK}	3-state leakage current	V_{CSN} = V_1; 0 V < V_{DO} < V_1	-10		10	µA
C_{DO}[(1)]	3-state input capacitance	V_{CSN} = V_1, 0 V < V_1 < 5.3 V		10	15	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

b. See *Figure 16: SPI – input timing*.

DO timing[c]

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.

6 V ≤ V_S ≤ 18 V; 4.8 V ≤ V_1 ≤ 5.2 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 31. DO timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{r\ DO}$	DO rise time	C_L = 100 pF; I_{LOAD} = -1 mA	—	50	100	ns
$t_{f\ DO}$	DO fall time	C_L = 100 pF; I_{LOAD} = 1 mA	—	50	100	ns
$t_{en\ DO\ tri\ L}$	DO enable time from 3-state to low level	C_L = 100 pF; I_{LOAD} = 1 mA; pull-up load to V_1	—	50	250	ns
$t_{dis\ DO\ L\ tri}$	DO disable time from low level to 3-state	C_L = 100 pF; I_{LOAD} = 4 mA; pull-up load to V_1	—	50	250	ns
$t_{en\ DO\ tri\ H}$	DO enable time from 3-state to high level	C_L = 100 pF; I_{LOAD} = -1 mA; pull-down load to GND	—	50	250	ns
$t_{dis\ DO\ H\ tri}$	DO disable time from high level to 3-state	C_L = 100 pF; I_{LOAD} = -4 mA; pull-down load to GND	—	50	250	ns
$t_{d\ DO}$	DO delay time	V_{DO} < 0.3 V_1; V_{DO} > 0.7 V_1; C_L = 100 pF	—	50	250	ns

CSN timing[d]

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.

6 V ≤ V_S ≤ 18 V; 4.8 V ≤ V_1 ≤ 5.2 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

Table 32. CSN timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{CSN\_HI(min)}$	Minimum CSN HI time, active mode	Transfer of SPI-command to Input register	6	—	—	µs

RXDL/NINT timing

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.

6 V ≤ V_S ≤ 18 V; 4.8 V ≤ V_1 ≤ 5.2 V; all outputs open; T_j = -40 °C to 130 °C, unless otherwise specified.

c. See *Figure 17: SPI – output timing*

d. See *Figure 18: SPI transition parameters*

Table 33. RXDL/NINT timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{Interupt}$	Interrupt pulse duration	Walk-up from V_{1stby} by LIN	—	56	—	µs

Figure 16. SPI – input timing

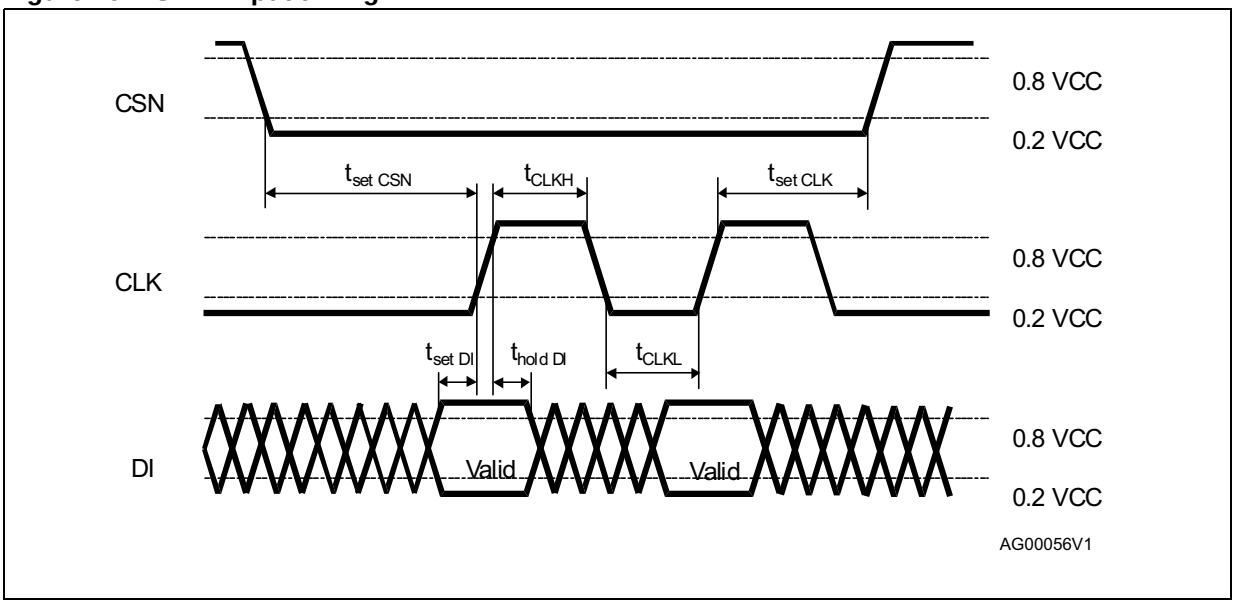


Figure 17. SPI – output timing

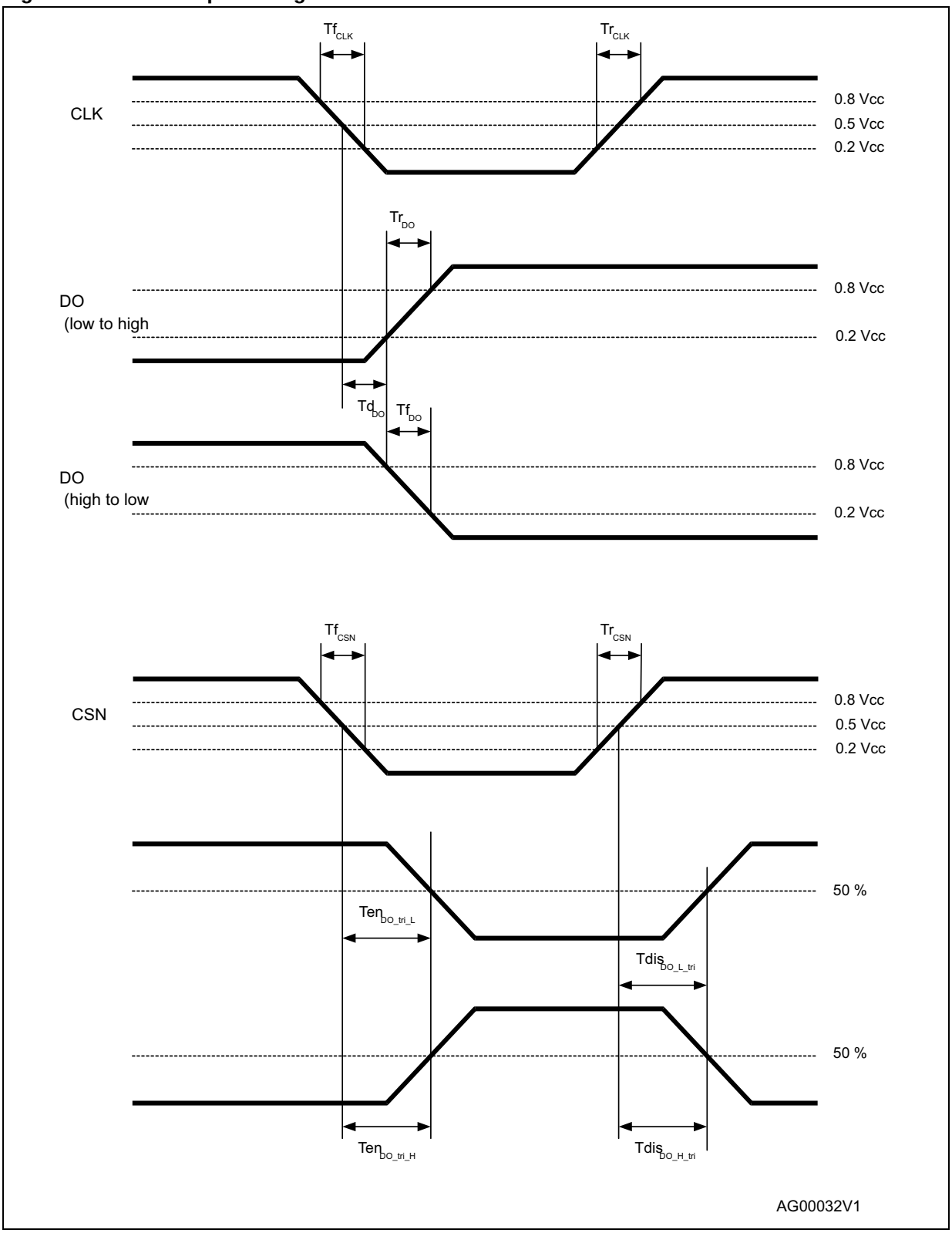


Figure 18. SPI transition parameters

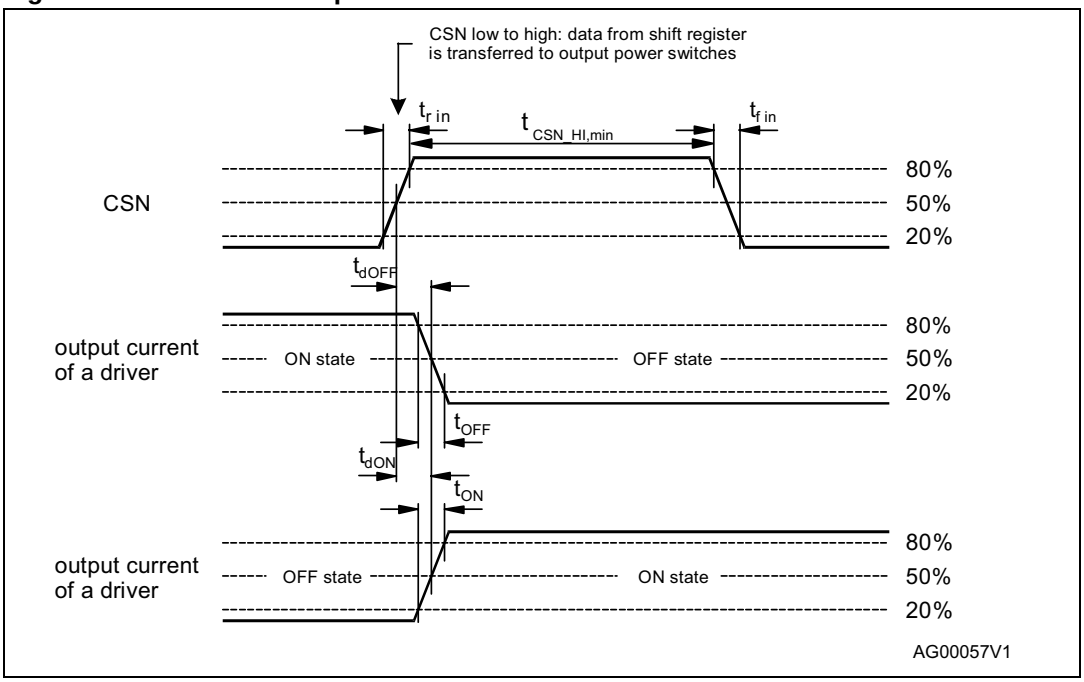
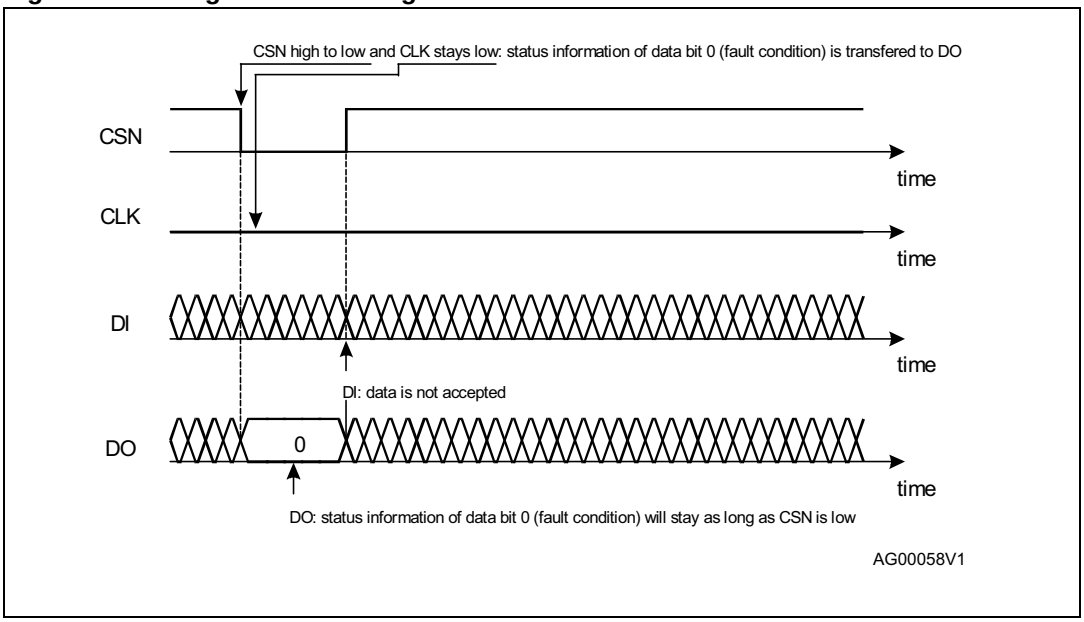


Figure 19. SPI global status register access



7 ST SPI

7.1 SPI communication flow

7.1.1 General description

The proposed SPI communication is based on a standard SPI interface structure using CSN (Chip Select Not), SDI (Serial Data In), SDO (Serial Data Out/Error) and SCK (Serial Clock) signal lines.

At device start-up the master reads the <*SPI-frame-ID*> register (ROM address 3EH) of the slave device. This 8-bit register indicates the SPI frame length (16bit) and the availability of additional features.

Each communication frame consists of an instruction byte which is followed by 1 data byte.

The data returned on SDO within the same frame always starts with the <Global Status> register. It provides general status information about the device. It is followed by 1 data byte (i.e. 'In-frame-response').

For write cycles the <*Global Status*> register is followed by the previous content of the addressed register.

For read cycles the <Global Status> register is followed by the content of the addressed register.

7.1.2 Command byte

Each communication frame starts with a command byte. It consists of an operating code which specifies the type of operation (<Write>, <Read>, <Read and Clear>, <Read Device Information>) and a 6 bit address. If less than 6 address bits are required, the remaining bits are unused but are reserved.

Table 34. Command byte

MSB							**LSB**
Op code		Address					
OC1	OC0	A5	A4	A3	A2	A1	A0

OCx: operating code

Ax: address

7.1.3 Operating code definition

Table 35. Operating code definition

OC1	**OC0**	**Meaning**
0	0	<Write mode>
0	1	<Read mode>

Table 35. Operating code definition (continued)

OC1	OC0	Meaning
1	0	<Read and clear status>
1	1	<Read device information>

The <Write Mode> <Read Mode> and <Read and Clear Status> operations allow access to the RAM of the device, i.e. to write to control registers or read status information.

A <Read and Clear Status> operation addressed to a device specific status register reads back and subsequently clear this status register.

A <Read and Clear Status> operation with address 3FH clears all status registers (including the Global Status Register). Configuration Register is read by this operation.

<Read Device Information> allows access to the ROM area which contains device related information such as the product family, product name, silicon version, register width and availability of a watchdog.

More detailed descriptions of the device information are available in ‘Read Device Information’.

7.1.4 Global status register[e]

Table 36. Global status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global error flag (GEF)	Communication error	Not (chip reset or comm error)	TSD2 or TSD1	TW	V_1 fail	V_S fail (OV/UV)	Fail safe

Table 37. Detailed global status register

Global error	Comm error	NOT(chip reset or comm error)	TSD1 or TSD2	TW	V_1 fail	V_S fail (OV / UV)	Fail safe		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex.**	**L99PM60J**
0	0	1	0	0	0	0	0	20	Default value in Normal mode - after correct WD trigger or after Read & Clear on Error Flags
1	0	0	0	0	0	0	0	80	Power ON - strong battery
1	0	0	0	0	0	1	0	82	Power ON - weak battery
1	1	0	0	0	0	0	0	C0	Communication error

e. See *Section 7.2: SPI registers* for details

Table 37. Detailed global status register (continued)

Global error	Comm error	NOT(chip reset or comm error)	TSD1 or TSD2	TW	V_1 fail	V_S fail (OV / UV)	Fail safe		
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex.**	**L99PM60J**
1	0	1	0	0	0	1	0	A2	V_S overvoltage or V_S undervoltage
1	0	1	0	0	0	0	1	A1	WD failure
1	0	1	0	0	0	0	1	A1	SPI error (DI stuck)
1	0	1	1	1	0	0	1	B9	TSD2
1	0	1	0	0	1	0	0	A4	V_1 fail
1	0	1	0	0	0	0	0	A0	Other device failure(1)

1. The Global Error Flag is raised due to a failure condition which is not reported in the Global Status Register. The Failure is reported in the Status Registers 1 – 4.

7.1.5 Configuration register

The <Configuration> register is accessible at RAM address 3FH.

The Configuration Register is implemented for compliance purpose to ST SPI Standard.

Table 38. Configuration register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	WD trigger

<*WD Trigger*>: this Bit is reserved to serve the watchdog.

Figure 20. Read configuration register

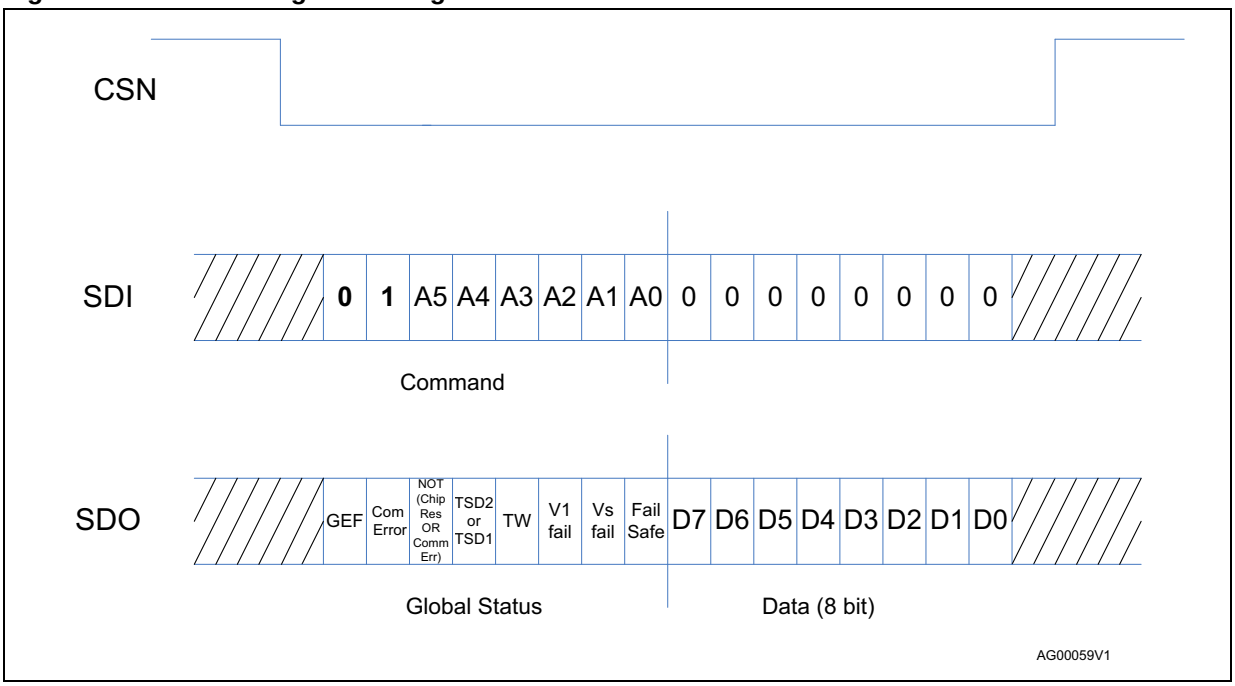
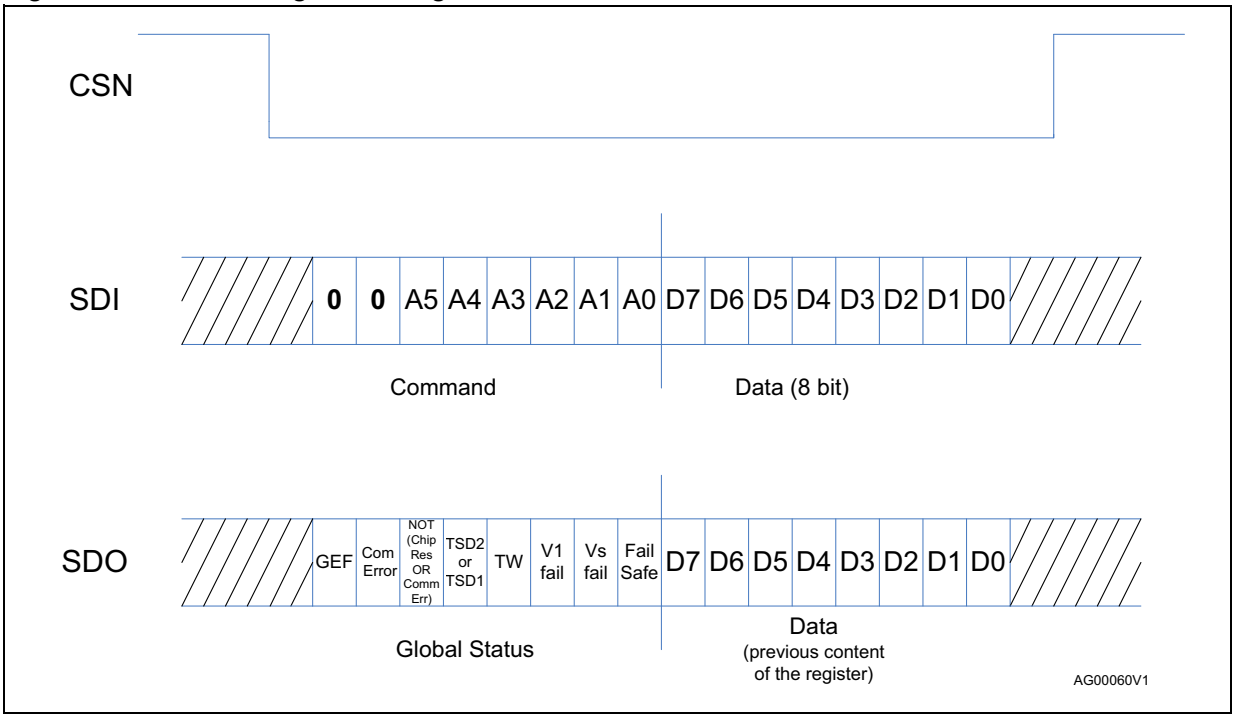


Figure 21. Write configuration register



7.1.6 Address mapping

Table 39. Addressing mapping

RAM Address	Description	Access
3FH	<Configuration>	R/W
14H	Status register 4	R
13H	Status register 3	R
12H	Status register 2	R
11H	Status register 1	R
02H	Control register 2	R/W
01H	Control register 1	R/W
00H	Reserved	R/W

ROM Address	Description	Access
3FH	Reserved	N/A
3EH	<SPI frame ID> Includes frame width and availability of watchdog	R
…	Unused	N/A
03H	<product code 2> Unique product identifier	N/A
02H	<product code 1> Unique product identifier	R
01H	<silicon version> Indicates Design Version	R
00H	<ID Header> Device family, max address of device information	R

The RAM memory area consists of 8 bit registers.

For the device information (ROM memory area) the eight bits of the memory cell are used.

All unused RAM and ROM addresses are read as ‘0’.

Note: 1 The register definition for RAM address 00H is unused. A register value of all 0 must cause the device to enter a failsafe state (interpreted as ‘SDI stuck to GND’ failure).

2 ROM address 3FH is unused. An attempt to access this address must be recognized as a communication error (‘SDI stuck to V_{CC}’ failure) and must cause the device to enter a failsafe state.

7.1.7 Write operation

The write operation starts with a Command Byte followed by 1 data byte.

Table 40. Write command format

MSB							LSB
Command byte							
Op Code		Address					
0	0	A5	A4	A3	A2	A1	A0
Data byte							
D7	D6	D5	D4	D3	D2	D1	D0

OC0, OC1: operating code (00 for ‘write’ mode)

A0 to A5: address bits

An attempt to write 00H at RAM address 00H is recognized as a failure (SDI stuck to GND). The device enters a failsafe state.

7.1.8 Format of data shifted out at SDO during write cycle

Table 41. Format of data shifted out at SDO during write cycle: global status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global error flag (GEF)	Comm error	Not (chip reset or comm error)	TSD2 or TSD1	TW	V_1 fail	V_S fail (OV/UV)	Fail safe

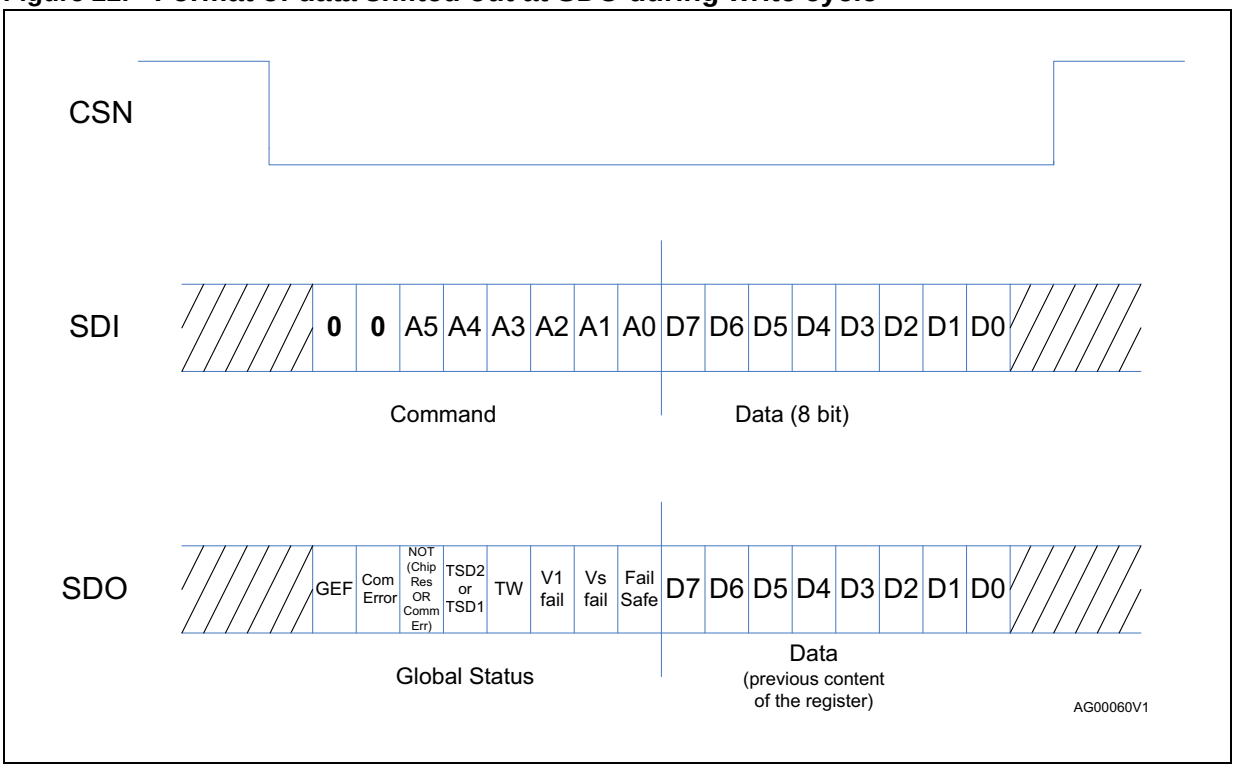
Table 42. Format of data shifted out at SDO during write cycle: data byte

MSB	Previous content of addressed register						LSB
D7	D6	D5	D4	D3	D2	D1	D0

Failures are indicated by activating the corresponding bit of the <Global Status> register.

The returned data byte represents the previous content of the accessed register.

Figure 22. Format of data shifted out at SDO during write cycle



7.1.9 Read operation

The Read operation starts with a Command Byte followed by 1 data byte.

The content of the data byte is ‘don’t care’. The content of the addressed register is shifted out at SDO within the same frame (‘in-frame response’).

Table 43. Read command format

MSB							LSB
Command byte							
Op code		Address					
0	1	A5	A4	A3	A2	A1	A0
Data byte							
0	0	0	0	0	0	0	0

OC0, OC1: operating code (01 for ‘read’ mode)

A0 to A5: address bits

7.1.10 Format of data shifted out at SDO during read cycle

Table 44. Format of data shifted out at SDO during read cycle: global status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global error flag (GEF)	Comm error	Not (chip reset or comm error)	TSD2 or TSD1	TW	V_1 fail	V_S fail (OV/UV)	Fail safe

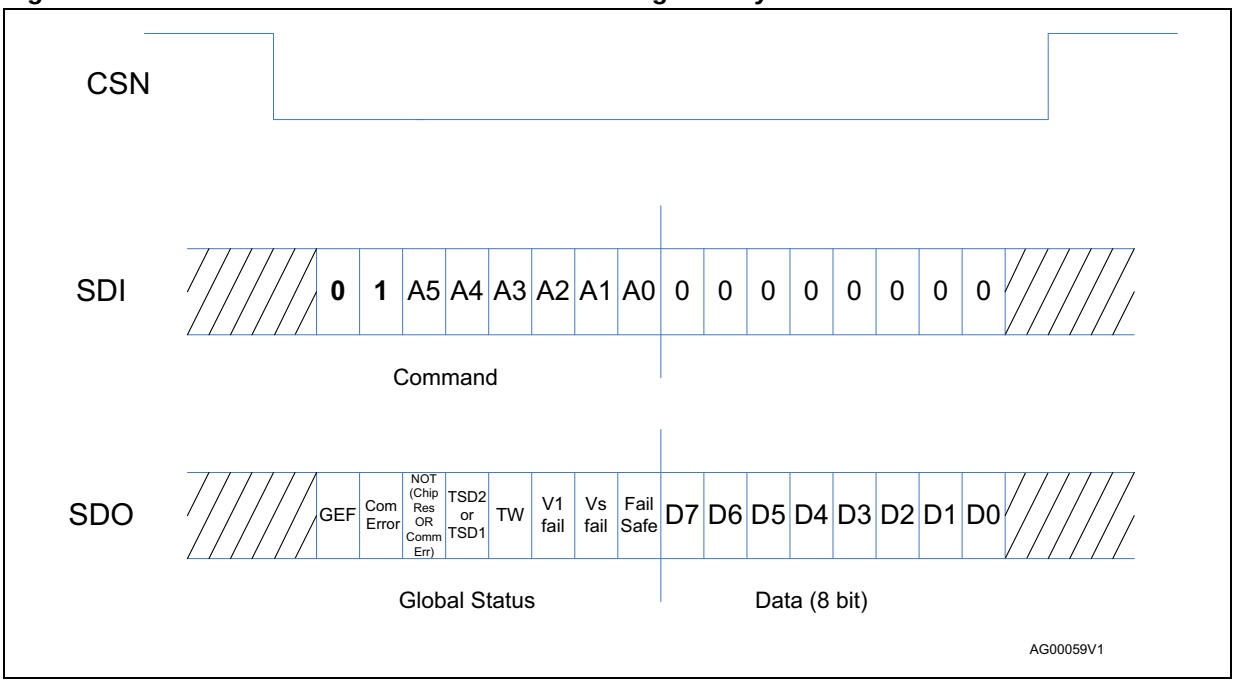
Table 45. Format of data shifted out at SDO during read cycle: data byte

MSB	Previous content of addressed register						LSB
D7	D6	D5	D4	D3	D2	D1	D0

Failures are indicated by activating the corresponding bit of the <Global Status> register.

The returned data byte represents the content of the register to be read.

Figure 23. Format of data shifted out at SDO during read cycle



7.1.11 Read and clear status operation

The ‘Read and Clear Status’ operation starts with a command byte followed by 1 data byte.

The content of the data byte is ‘don’t care’. The content of the addressed Status Register is transferred to SDO within the same frame (‘in-frame response’) and is subsequently cleared.

A ‘Read and Clear Status’ operation with address 3FH clears all Status registers (incl. the <*Global Status*> register). The Configuration Register is read by this operation.

Table 46. Read and clear status’ command format‘

MSB							**LSB**
Command byte							
Op code		Address					
1	0	A5	A4	A3	A2	A1	A0
Data byte							
0	0	0	0	0	0	0	0

OC0, OC1: operating code (10 for ‘read and clear status’ mode)

A0 to A5: address bits

7.1.12 Format of data shifted out at SDO during ‘Read and Clear Status’ operation

Table 47. Format of data shifted out at SDO during ‘Read and Clear Status’ operation: global status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global error flag (GEF)	Comm error	Not (chip reset or comm error)	TSD2 or TSD1	TW	V_1 fail	V_S fail (OV/UV)	Fail safe

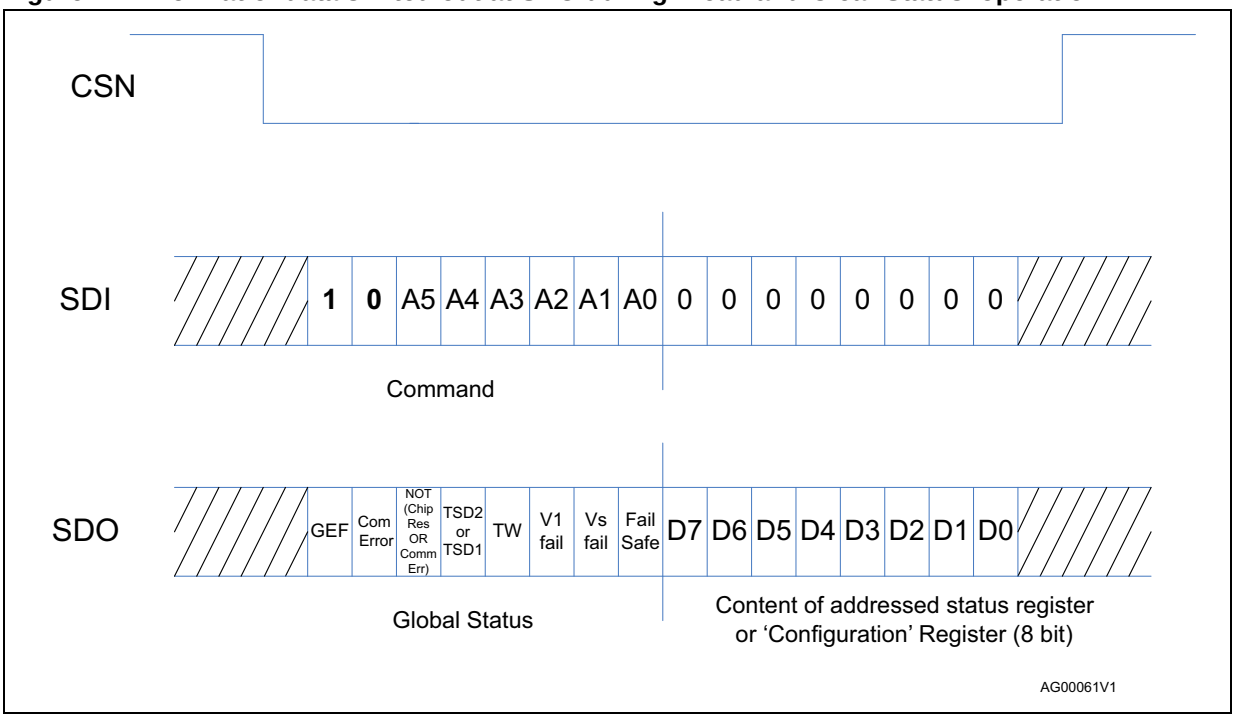
Table 48. Format of data shifted out at SDO during read cycle: data byte

MSB	Previous content of addressed register						LSB
D7	D6	D5	D4	D3	D2	D1	D0

Failures are indicated by activating the corresponding bit of the <Global Status> register.

The returned data byte represents the content of the register to be read.

Figure 24. Format of data shifted out at SDO during ‘Read and Clear Status’ operation



7.1.13 Read device information

The device information is stored at the ROM addresses defined below and is read using the respective operating code.

Table 49. Read device information

Op code		Address	Device information
OC1	OC0		
1	1	3FH	Reserved
1	1	3EH	<SPI frame ID> Includes frame width and availability of watchdog = 41H
1	1	04H to 3DH	Unused
1	1	03H	<product code 2> Unique product identifier; content = 4BH
1	1	02H	<product code 1> Unique product identifier; content = 0CH
1	1	01H	<silicon version> Indicates design version
1	1	00H	<ID Header> Device family, max address of device information. Content: 43H

The <*ID-Header*> (00H) indicates the product family and specifies the highest address which contains product information (the standard value, i.e. no additional product information registers are present, is 03H ➔ content of ID-Header is: XX00 0011)

Table 50. ID-Header

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Family identifier		Highest address containing device information					

Table 51. Family identifier

Bit 7	Bit 6	Meaning
0	0	VIPower
0	1	BCD
1	0	VIPower hybrid
1	1	Tbd

The <*Product Code 1*> *(*02H) and <*Product Code 2*> *(*03H) represents a unique code to identify the product name. The code is specified in the device datasheet.

The <*Silicon Version*> (01H) provides information about the silicon version according to the table below:

Table 52. Silicon version

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				Silicon version			

Definition of the silicon version code:

Table 53. Silicon version code

Bit3	Bit 2	Bit 1	Bit 0	Silicon version
0	0	0	0	First Silicon
0	0	0	1	V2
0	0	1	0	V3
0	0	1	1	V4
0	1	0	0	V5
0	1	0	1	V6
0	1	1	0	V7
0	1	1	1	V8
1	…	…	…	…

The <*SPI-frame-ID*> (ROM address 3EH) provides information about the register width (1, 2, 3 bytes) and the availability of ‘Burst Mode Read’ and watchdog.

Table 54. SPI-frame-ID

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BR	WD	X	X	X	32-bit	24-bit	16-bit

BR: Burst-Mode Read (1 = Burst-Mode Read is supported)

WD: Watchdog (1 = available, 0 = not available)

32-bit, 24-bit, 16-bit: width of SPI frame (see table below)

7.2 SPI registers

Overview command byte

Table 55. SPI register: command byte

Read/write		Address					
x	x	x	x	x	x	x	x

Table 56. SPI register: mode selection

Read/write		Mode selection
0	0	Write
0	1	Read
1	0	Read and clear
1	1	Read device info

Table 57. SPI register: CTRL register selection

CTRL register 1, 2						CTRL register selection
0	0	0	0	0	1	CTRL register1
0	0	0	0	1	0	CTRL register2

Table 58. SPI register: STAT register selection

STAT register. 1…4						STAT register selection
0	1	0	0	0	1	STAT register1
0	1	0	0	1	0	STAT register2
0	1	0	0	1	1	STAT register3
0	1	0	1	0	0	STAT register4

Overview of control register data bytes

Table 59. Overview of control register data byte

	1st data byte							
	Control register 1							
Defaults	1	1	1	1	0	0	0	0
Funct.	OUT2_2	OUT2_1	OUT1_2	OUT1_1	ICMP	Sandby select	Go standby	TRIG
Group	HS control				Mode control			
	Control register 2							
Defaults	0	0	0	1	0	1	1	1
Funct.	REL2	REL1	VSM EN	Reset level	LIN Flash	LIN TXD timeout enable	OUT UV shutdown enable	LS OVUV shutdown enable
Group	LS control		Other control					

Control Register 1

Table 60. Control register 1

Command byte								1st data byte
Read/ write		Address						
x	x	0	0	0	0	0	1	Data, 8bit

Table 61. Control register 1, 1st data byte

Group	HS control				Mode control			
Defaults	1	1	1	1	0	0	0	0
Funct.	OUT2_2	OUT2_1	OUT1_2	OUT1_1	ICMP	Standby select	Go standby	TRIG

Table 62. Control register 1, bits

Bit	Name	Comment
7	OUT2	Select mode of OUT2
6		See nested table below

OUT2_2	OUT2_1	Active mode	$V_{1\text{-standby}}$	$V_{BAT\text{-standby}}$
0	0	Off		
0	1	On		
1	0	VSM enable: 0 → Direct drive; 1 → Off	Direct drive	Off
1	1	VSM enable: 0 → Direct drive; 1 → Off	Direct drive	Off

Note: Note: In Direct Drive, Pin DRV/VSOUT, can be used as an input to directly switch on/off OUT2

Table 62. Control register 1, bits (continued)

<table>
<tr><th>Bit</th><th>Name</th><th>Comment</th></tr>
<tr><td>5</td><td rowspan="2">OUT1</td><td>Select mode of OUT1</td></tr>
<tr><td>4</td><td>
<table>
<tr><th>OUT2_2</th><th>OUT2_1</th><th>Active mode</th><th>$V_{1\text{-standby}}$</th><th>$V_{BAT\text{-standby}}$</th></tr>
<tr><td>0</td><td>0</td><td colspan="3">Off</td></tr>
<tr><td>0</td><td>1</td><td colspan="3">On</td></tr>
<tr><td>1</td><td>0</td><td>
<table>
<tr><td>VSM enable</td><td></td></tr>
<tr><td>0</td><td>Direct drive</td></tr>
<tr><td>1</td><td>Off</td></tr>
</table>
</td><td>Direct drive</td><td>Off</td></tr>
<tr><td>1</td><td>1</td><td>FSO</td><td>FSO</td><td>FSO</td></tr>
</table>
Note: In Direct Drive, Pin DRV/VSOUT, can be used as an input to directly switch on/off OUT1
To change the setting for OUT1 from FSO (default) to normal output configuration (ON/OFF or Direct Drive) a SPI safety sequence
Needs to be followed. First write command with a specific pattern to CONF Register needs to be provided in order to enable the write access
For configuration bits of OUT1. With an SPI write command to Control Register 1 the bits for OUT1 can be modified.
The Write command to Control Register 1 must follow the write command to the CONF Register (no other SPI command in between these 2 commands)
Safety Sequence:
– Write to Conf Register (0x0011 1111; 1010 101x)
x: don’t care for unlocking sequence but according to description of watchdog timing
– Write to Ctrl Register 1 (0x0000 0001; xxxx xxxx)
x: values according to description of Ctrl Reg1
</td></tr>
<tr><td>3</td><td>ICMP</td><td>V_1 load current supervision
– 0: enabled; watchdog is disabled in $V_{1\text{-standby}}$ when the $V_{1loadcurrent} < I_{CMPthreshold}$
– 1: disabled; Watchdog is automatically disabled when $V_{1\text{-standby}}$ is entered</td></tr>
<tr><td>2</td><td>Stby Select</td><td>Select standby mode
– 0: $V_{BAT\text{-standby}}$ mode
– 1: $V_{1\text{-standby}}$ mode</td></tr>
<tr><td>1</td><td>Go Stby</td><td>Execute standby mode
– 0: no action
– 1: execute standby mode</td></tr>
<tr><td>0</td><td>TRIG</td><td>Trigger bit for watchdog</td></tr>
</table>

Control Register 2

Table 63. Control register 2

Command byte								1st data byte
Read/ write		Address						
x	x	0	0	0	0	1	0	Data, 8bit

Table 64. Control register 2, 1st data byte

Group	LS control		Other control					
Defaults	0	0	0	1	0	1	1	1
Function	REL2	REL1	VSM enable	Reset level	LIN Flash	LIN TXD timeout enable	OUT UV shutdown enable	LS OVUV shutdown enable

Table 65. Control register 2, bits

Bit	Name	Comment
7	REL2	Select mode of REL2 REL2 = 0: Active mode: REL2 off; V_1 standby: REL2 off; V_{BAT} standby: REL2 off REL2 = 1: Active mode: REL2 on; V_1 standby: REL2 off; V_{BAT} standby: REL2 off
6	REL1	Select mode of REL1 REL2 = 0: Active mode: REL1 off; V_1 standby: REL1 off; V_{BAT} standby: REL1 off REL2 = 1: Active mode: REL1 on; V_1 standby: REL1 off; V_{BAT} standby: REL1 off
5	VSM enable	Select Pin DRV/VSOUT as input/output VSM enable = 0: Active mode: DRV/VSOUT pin used as input (direct drive)(1); V_1 standby / V_{BAT} standby: DRV/VSOUT pin used as input (direct drive)(1) VSM enable = 1: Active mode: OUT2_2 / OUT2_1 / DRV/VSOUT used as: 0 / 0 / Output (V_S/5 voltage); 0 / 1 / Output (V_S/5 voltage); 1 / 0 / Output (T_{SENSE} voltage); 1 / 1 / Output (V_S/5 voltage); V_1 standby / V_{BAT} standby: DRV/VSOUT pin used as input (direct drive)(1) 1. Usage of Direct Drive feature is not only related to the configuration of DRV/VSOUT as an input. Refer to truth table of OUT1/2 for the direct drive feature.

Table 65. Control register 2, bits

Bit	Name	Comment
4	Reset level	Select V_1 reset level – 0: 3.5 V – 1: 4.6 V
3	LIN Flash	Select maximum LIN communication speed – 0: 20 kbit/s – 1: 100 kbit/s
2	LIN TXD timeout enable	Enable / disable monitoring of TxD – 0: no TxD monitoring – 1: TxD monitoring; LIN transmitter is switched off if TXDL is dominant for t > 12 ms
1	OUT UV shutdown enable	Select undervoltage shutdown for HS driver – 0: no undervoltage shutdown – 1: undervoltage shutdown
0	LS OVUV shutdown enable	Shutdown of LS drivers in case of overvoltage / undervoltage 0: no shutdown of low sides in case of overvoltage / undervoltage 1: shutdown low sides in case of overvoltage / undervoltage

7.2.1 Status register

Table 66. Overview of status register data bytes

	1st data byte							
	Status register 1							
Funct.	OV	UV	OL OUT2	OL OUT1	OC OUT2	OC OUT1	OC REL2	OC REL1
Group	Diagnosis 1							
	Status register 2							
Funct.	Res	LIN perm dom	LIN TXD dom	LIN perm rec	Res	LIN Wake	Device State	Device State
Group	Diagnosis 2							
	Status register 3							
Funct.	WD Fail	WD Fail	WD Fail	WD Fail	Forced sleep WD	Forced sleep TSD/ShtV1	WD timer state1	WD timer state0
Group	Diagnosis 3							
	Status register 4							
Funct.	V_1 UV warn	V_1 restart	V_1 restart	V_1 restart	V_1 fail	TSD2	TSD1	TW
Group	Diagnosis 4							

Table 67. Global status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global error flag	Communication error(1)	NOT (chip reset or comm. error i.e. cold start(2)	TSD2 or TSD1(3)	TW	V_1 fail	Vs Fail (OV/UV)	Fail safe(4)

1. Invalid CLOCK COUNT
2. Cleared with CLR command on SR3
3. Cleared with “READ and CLEAR” on SR4
4. Cleared with a valid WD trigger (WD fail) or by clearing the corresponding status register related to failure

Status Register 1

Table 68. Status register 1, command and data byte

Command byte								1st data byte
Read/write		Address						
x	x	0	1	0	0	0	1	Data, 8bit

Table 69. Status register 1, data byte

	1st data byte							
Function	OV	UV	OL OUT2	OL OUT1	OC OUT2	OC OUT1	OC REL2	OC REL1
Group	Diagnosis 1							

Table 70. Status register 1, bits

Bit	Name	Comment
7	OV	Overvoltage event occurred since last read out Bit is latched until a “Read and clear” access
6	UV	Undervoltage event occurred since last read out Bit is latched until a “Read and clear” access
5	OL OUT2	Open-load event occurred since last read out Bit is latched until a “read and clear” access
4	OL OUT1	
3	OC OUT2	Overcurrent event occurred since last read out Bit is latched until a “read and clear” access
2	OC OUT1	
1	OC REL2	
0	OC REL1	

Status Register 2

Table 71. Status register 2, command and data byte

Command byte								1st data byte
Read/write		Address						
x	x	0	1	0	0	1	0	Data, 8bit

Table 72. Status register 2, data byte

	1st data byte							
Function	Res	LIN perm dom	LIN TXD dom	LIN perm rec	Res	LIN wake	Device state	Device state
Group	Diagnosis 2							

Table 73. Status register 2, bits

Bit	Name	Comment
7	Res	Reserved
6	LIN perm dom	LIN bus is dominant for t > 12 ms Bit is latched until a “Read and clear” access
5	LIN TXD dom	TxDL pin is dominant for t > 12 ms; Transmitter is disabled; Bit is latched until a “Read and clear” access

Table 73. Status register 2, bits (continued)

<table>
<tr><th>Bit</th><th>Name</th><th>Comment</th></tr>
<tr><td>4</td><td>LIN perm rec</td><td>LIN bus does not follow TxDL within 40 µs; Transmitter is disabled; Bit is latched until a “Read and clear” access</td></tr>
<tr><td>3</td><td>Res</td><td>Reserved</td></tr>
<tr><td>2</td><td>LIN wake</td><td>Wake up from LIN; Bit is latched until a “Read and clear” access</td></tr>
<tr><td>1</td><td>Device state</td><td rowspan="2">State from which the device woke up
<table><tr><th>Device state</th><th>Device state</th><th>State from which the device woke up</th></tr><tr><td>0</td><td>0</td><td>Active</td></tr><tr><td>0</td><td>1</td><td>$V_{1\text{-standby}}$</td></tr><tr><td>1</td><td>0</td><td>$V_{BAT\text{-standby}}$</td></tr></table>Bit is latched until a “read and clear access”.
After a “read and clear access”, the device state is updated.
After a wake up, device state is
– 01: $V_{1\text{-standby}}$
– 10: $V_{BAT\text{-standby}}$</td></tr>
<tr><td>0</td><td>Device State</td></tr>
</table>

Status Register 3

Table 74. Status register 3, command and data byte

<table>
<tr><th colspan="8">Command byte</th><th>1st data byte</th></tr>
<tr><td colspan="2">Read/write</td><td colspan="6">Address</td><td></td></tr>
<tr><td>x</td><td>x</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Data, 8bit</td></tr>
</table>

Table 75. Status register 3, data byte

	1st data byte							
Function	WD fail_3	WD fail_2	WD fail_1	WD fail_0	Forced sleep WD	Forced sleep TSD/ShtV1	WD timer State_1	WD timer State_0
Group	Diagnosis 3							

Table 76. Status register 3, bits

<table>
<tr><th>Bit</th><th>Name</th><th>Comment</th></tr>
<tr><td>7</td><td>WD fail_3</td><td rowspan="4">Number of missing watchdog triggers (15 missing Watchdog trigger forces the device into $V_{BAT\text{-standby}}$).
Bits are not clearable; are cleared with a proper Watchdog trigger</td></tr>
<tr><td>6</td><td>WD fail_2</td></tr>
<tr><td>5</td><td>WD fail_1</td></tr>
<tr><td>4</td><td>WD fail_0</td></tr>
</table>

Table 76. Status register 3, bits (continued)

<table>
<tr><th>Bit</th><th>Name</th><th>Comment</th></tr>
<tr><td>3</td><td>Forced sleep WD</td><td>Device was forced to VBAT mode because of multiple watchdog errors
Bits are latched until a read and clear access</td></tr>
<tr><td>2</td><td>Forced sleep TSD/ShtV1</td><td>Device was forced to VBAT or multiple thermal shutdown events or a short on V_1 during start-up.
Bits are latched until a read and clear access</td></tr>
<tr><td>1</td><td>WD timer state_1</td><td rowspan="2">Status of watchdog counter of selected watchdog timing
<table><tr><th>WD_timer_state_1</th><th>WD_timer_state_0</th><th>Counter</th></tr><tr><td>0</td><td>0</td><td>0% - 33%</td></tr><tr><td>0</td><td>1</td><td>33% - 66%</td></tr><tr><td>1</td><td>1</td><td>66% - 100%</td></tr></table>Bits are not clearable</td></tr>
<tr><td>0</td><td>WD timer state_0</td></tr>
</table>

Status Register 4

Table 77. Status register 4, command and data byte

<table>
<tr><th colspan="8">Command byte</th><th>1st data byte</th></tr>
<tr><td colspan="2">Read/write</td><td colspan="6">Address</td><td></td></tr>
<tr><td>x</td><td>x</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Data, 8bit</td></tr>
</table>

Table 78. Status register 4, data byte

<table>
<tr><th></th><th colspan="8">1st data byte</th></tr>
<tr><td>Function</td><td>V_1 UV warn</td><td>V_1 restart_2</td><td>V_1 restart_1</td><td>V_1 restart_0</td><td>V_1 fail</td><td>TSD2</td><td>TSD1</td><td>TW</td></tr>
<tr><td>Group</td><td colspan="8">Diagnosis 4</td></tr>
</table>

Table 79. Status register 4, bits

<table>
<tr><th>Bit</th><th>Name</th><th>Comment</th></tr>
<tr><td>7</td><td>V_1 UV warn</td><td>V_1 undervoltage pre-warning (V_1 < 4.5 V)
Bit is latched until a read and clear access</td></tr>
<tr><td>6</td><td>V_1 restart_2</td><td rowspan="3">Number of TSD2 events which caused a restart of V_1 regulator (7 TSD2 events forces the device into $V_{BAT\text{-}standby}$)
Bits are latched until a read and clear access</td></tr>
<tr><td>5</td><td>V_1 restart_1</td></tr>
<tr><td>4</td><td>V_1 restart_0</td></tr>
<tr><td>3</td><td>V_1 fail</td><td>V_1 fail (V_1 < 2 V for t > 2 µs) event occurred since last read out
Bit is latched until a “read and clear access”</td></tr>
</table>

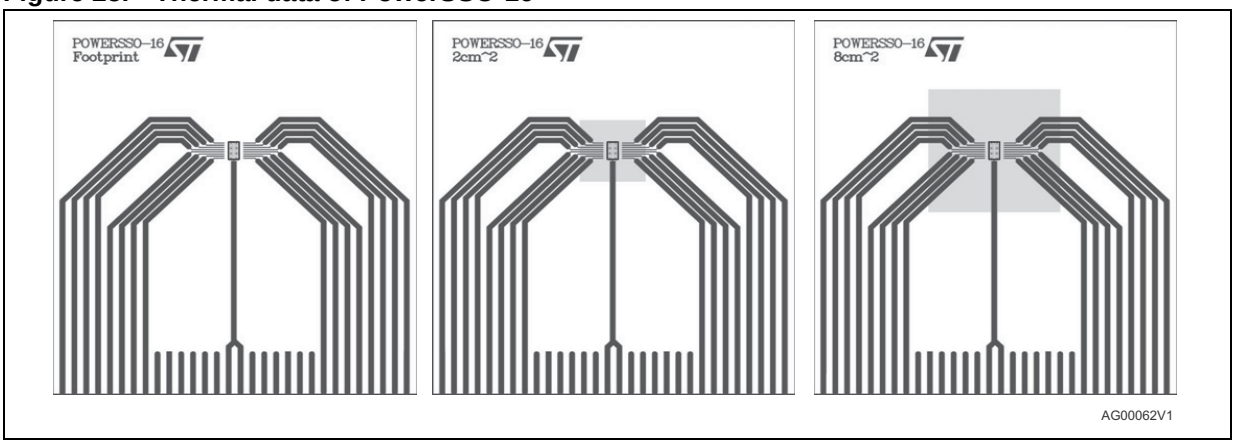
Table 79. Status register 4, bits (continued)

Bit	Name	Comment
2	TSD2	Thermal warning / shutdown1 / shutdown2 occurred since last readout Bits are latched until a “read and clear access”
1	TSD1	
0	TW	

8 Package and PCB thermal data

8.1 PowerSSO-16 thermal data

Figure 25. Thermal data of PowerSSO-16



Note: Board finish thickness 1.6 mm +/- 10%; Board double layer; Board dimension 77 x 86; Board Material FR4; Cu thickness 0.070 mm (front and back side); Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm; Footprint dimension 2.5 mm x 4.2 mm

Figure 26. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

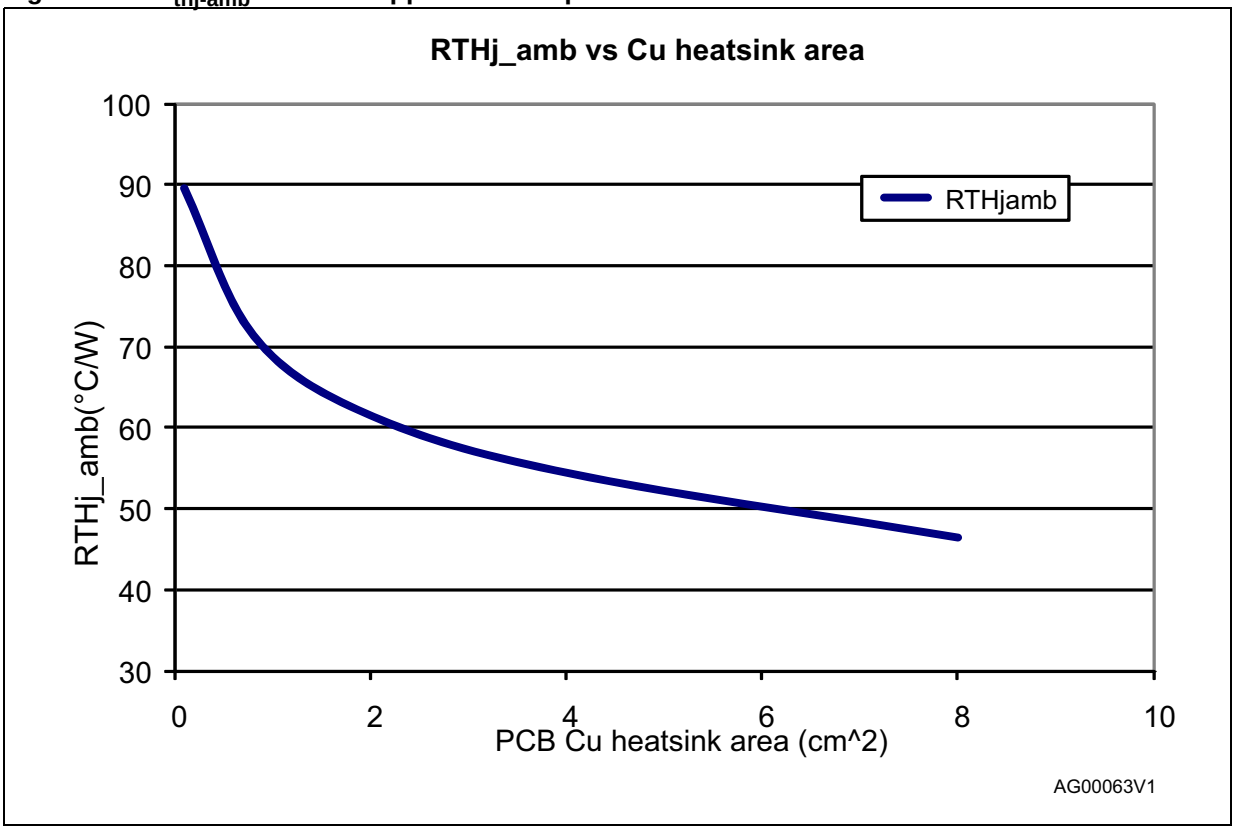


Figure 27. V_1 thermal impedance

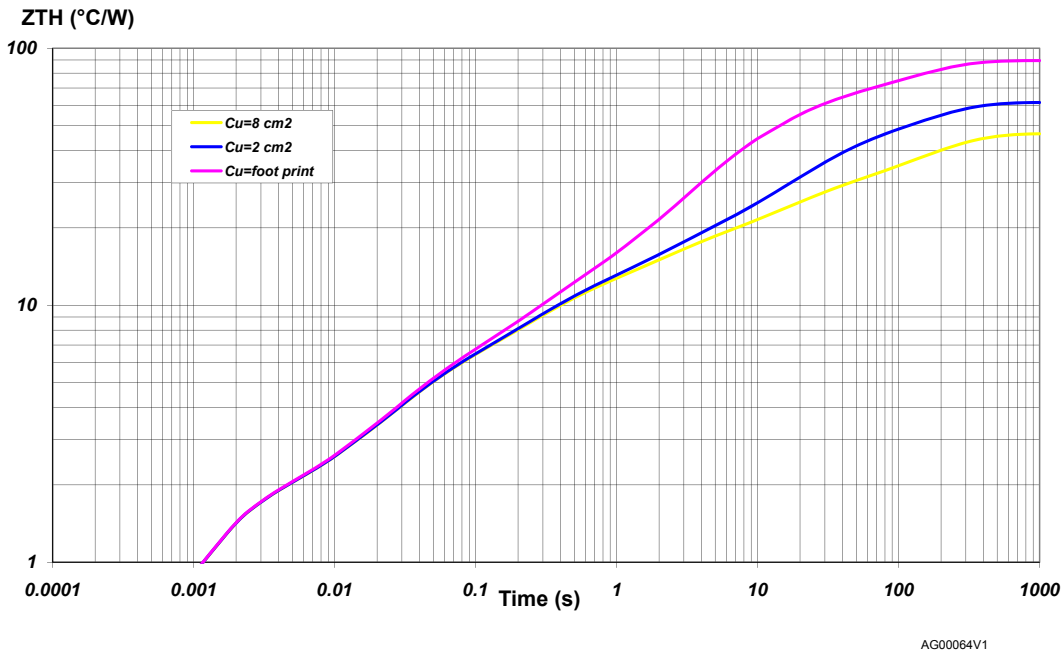
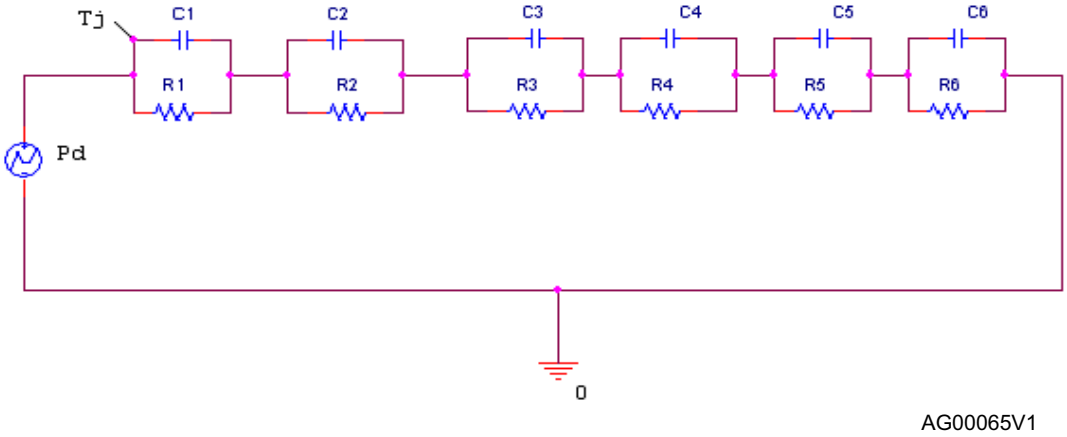


Figure 28. Thermal fitting model of V_1



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THp}(1-\delta)$$

where

$$\delta = t_p / T$$

Table 80. PowerSSO-16 thermal parameter

Area/island (cm^2)	FP	2	8
R1 (°C/W)	1.5		
R2 (°C/W)	3		
R3 (°C/W)	5		
R4 (°C/W)	20	6	6
R5 (°C/W)	28	21	10
R6 (°C/W)	32	25	21
C1 (W·s/°C)	0.0008		
C2 (W·s/°C)	0.01		
C3 (W·s/°C)	0.05		
C4 (W·s/°C)	0.2	0.3	0.3
C5 (W·s/°C)	0.5	1	1.5
C6 (W·s/°C)	4	6	8

9 Package and Packaging Information

9.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.ECOPACK® is an ST trademark.

9.2 PowerSSO-16 package information

Figure 29. PowerSSO-16 package dimensions

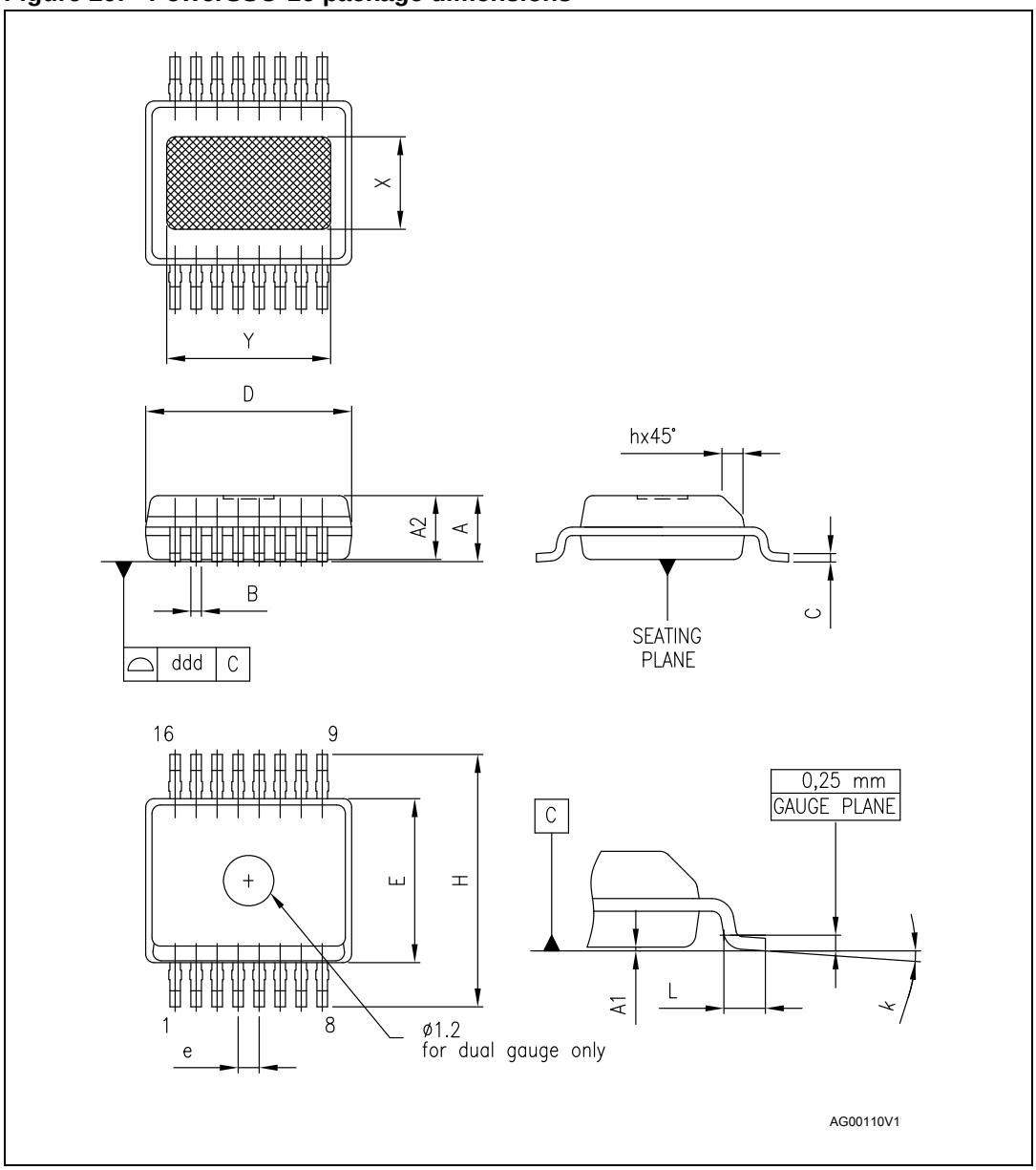
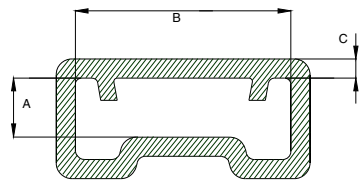


Table 81. PowerSSO-16 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.25		1.72
A1	0.00		0.10
A2	1.10		1.62
B	0.18		0.36
C	0.19		0.25
D	4.80		5.00
E	3.80		4.00
e		0.50	
H	5.80		6.20
h	0.25		0.50
L	0.40		1.27
k	0°		8°
X	1.90		2.50
Y	3.60		4.20
ddd			0.10

9.3 PowerSSO-16 packing information

Figure 30. PowerSSO-16 tube shipment (no suffix)

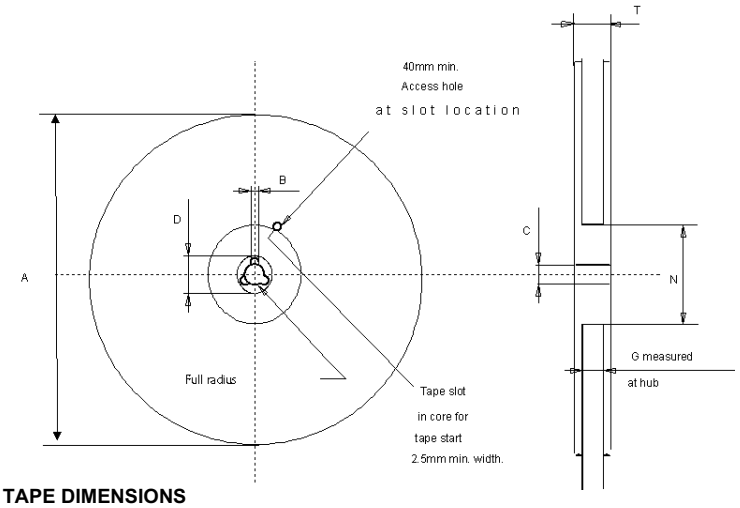


AG00111V1

Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	1.85
B	6.75
C (± 0.1)	0.6

All dimensions are in mm.

Figure 31. PowerSSO-16 tape and reel shipment (no suffix)



REEL DIMENSION

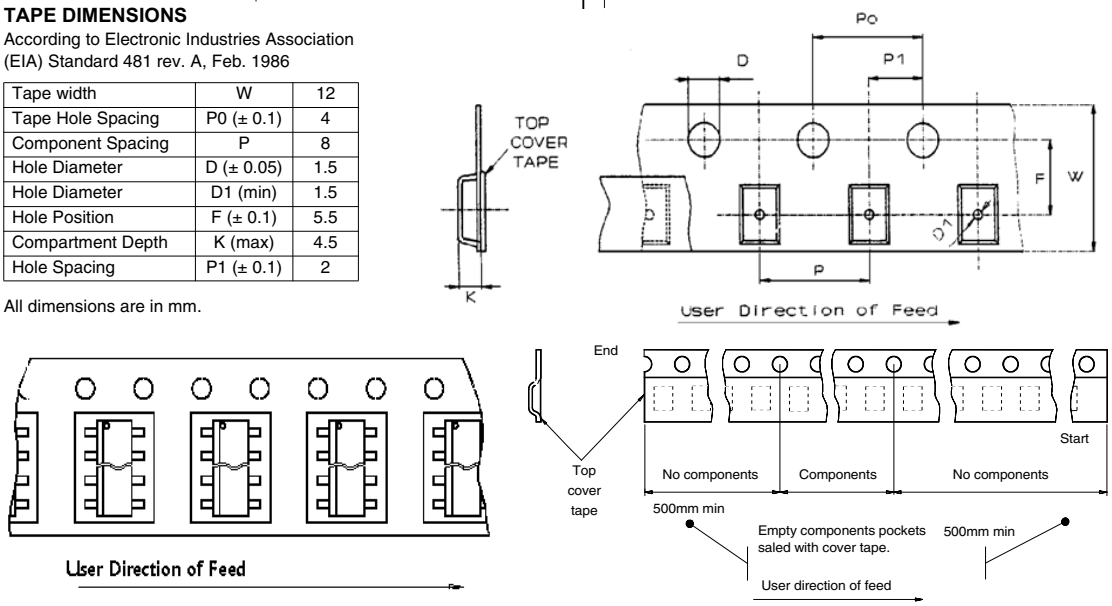
Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	12
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D (± 0.05)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.1)	5.5
Compartment Depth	K (max)	4.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.



AG00112V1

10 Revision history

Table 82. Document revision history

Date	Revision	Changes
26-Jan-2011	1	Initial release.
09-Mar-2011	2	Updated *Section 3.2: Low side driver outputs REL1, REL2* Updated *Figure 8: Recovery after forced VBAT due to multiple watchdog failure* *Table 11: Supply and supply monitoring*: – $I_{V(BAT)}$ ($V_{1\text{-standby}}$): updated test condition and minimum, typical and maximum values – $I_{V(V1)}$: updated typical value *Table 13: Power-on reset (V_S)* – V_{POR} (V_S decreasing): updated minimun and typical values *Table 14: Voltage regulator V_1* – VSTB1: updated minimum and maximum values – I_{CMP_rise}, I_{CMP_fail}: updated minimum, typical and maximum values *Table 15: Reset output (V_1 supervision)* – V_{RT2} (increasing/ decreasing): updated minimux, typical and maximum values *Table 17: Output* – IOLD: updated minimux, typical and maximum values *Table 18: Relay drivers* – V_Z: added typical value *Table 20: Output: VSOUT*: – VSOUT: added minimum and maximum values *Table 26: Input: CSN*: – ICSNPU: added minimum aln maximum values *Table 39: Addressing mapping* – Updated RAM address: inserted Control Register 1
25-Mar-2011	3	Updated following tables: – *Table 13: Power-on reset (V_S)*: V_{POR} decreasing: updated minimum value – *Table 14: Voltage regulator V_1*: I_{CMP_rise}: updated minimum value I_{CMP_fail}: updated minimum and maximum values – *Table 15: Reset output (V_1 supervision)*: V_{RT1}: added row V_{RT2}: updated test condition and maximum value
28-Apr-2011	4	Changed document state from preliminary data to final datasheet
03-Nov-2011	5	Updated *Figure 8: Recovery after forced VBAT due to multiple watchdog failure* *Table 11: Supply and supply monitoring*: – $I_{V(act)}$, $I_{V(BAT)}$, $I_{V(V1)}$: updated test conditions – $I_{V(V1)CS}$: added row
19-Sep-2013	6	Updated disclaimer.