

Automotive low dropout linear voltage regulator with configurable output voltage having 200 mA current capability




SO-8

PowerSSO-12

Features

Max. supply voltage (load dump)	V_S	40 V
Max. output voltage tolerance	ΔV_O	+/-2%
Output current	I_O	200 mA
Quiescent current	I_{qn}	$\leq 1 \mu A$ ⁽¹⁾

1. Maximum value with regulator disabled

- AEC-Q100 qualified 
- Operating DC power supply voltage range from 2.15 V to 28 V
- Battery and post regulation operating modes are allowed
- Low dropout voltage
- Low quiescent current consumption
- User-selectable output voltage (0.8 V; 1.2 V; 1.5 V; 1.8 V; 2.5 V; 2.8 V; 3.3 V or 5 V)
- Output voltage precision $\pm 2\%$
- Enable input for enabling/disabling the voltage regulator
- Output voltage monitoring with reset output
- Negligible ESR effect on output voltage stability for load capacitor
- Programmable autonomous watchdog through external capacitor (L99VR01J only)
- Undervoltage lockout UVLO
- Fast output discharge
- Thermal shutdown and short-circuit current limitation
- Advanced thermal warning and output overvoltage diagnostic (L99VR01J only)
- Programmable short-circuit output current (L99VR01J only)
- Wide operating temperature range ($T_J = -40^\circ C$ to $175^\circ C$ L99VR01J only)
- Documentation available for customers that need support when dealing with ASIL requirements as per ISO 26262

Product status link

[L99VR01](#)

Description

L99VR01 is a low dropout linear voltage regulator designed for automotive applications available in SO-8 and in PowerSSO-12 packages. The LDO delivers up to 200 mA of load current and consumes as low as 1 μ A of quiescent current when the regulator is disabled. The input is 40 V tolerant to withstand load dump, while the operating input voltage range is between 2.15 V and 28 V. The L99VR01 can be configured, through SELx pins, to generate a fixed selectable output voltage (0.8 V; 1.2 V; 1.5 V; 1.8 V; 2.5 V; 2.8 V; 3.3 V or 5 V). High output voltage accuracy ($\pm 2\%$) is kept over wide temperature range, line and load variation. The L99VR01 features enable, reset, autonomous watchdog, advanced thermal warning, fast output discharge and IShort control (IShort control, autonomous watchdog and advanced thermal warning are available only for the L99VR01J). The regulator output current is internally limited so that the device is protected against short-circuit and overload, besides it features over temperature protection; the short current value is configurable by an external resistance in the L99VR01J version. The L99VR01 can operate both in post regulation, attached to a pre-regulated voltage or directly connected to battery.

1 Block diagram and pins description

Figure 1. Functional block diagram of L99VR01S

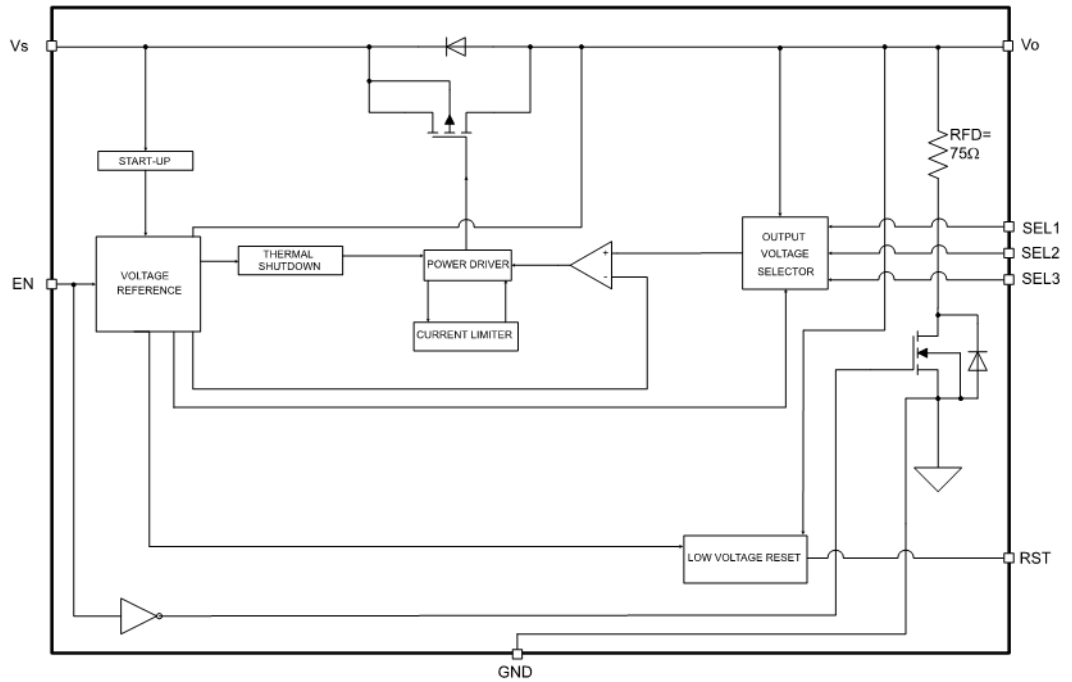
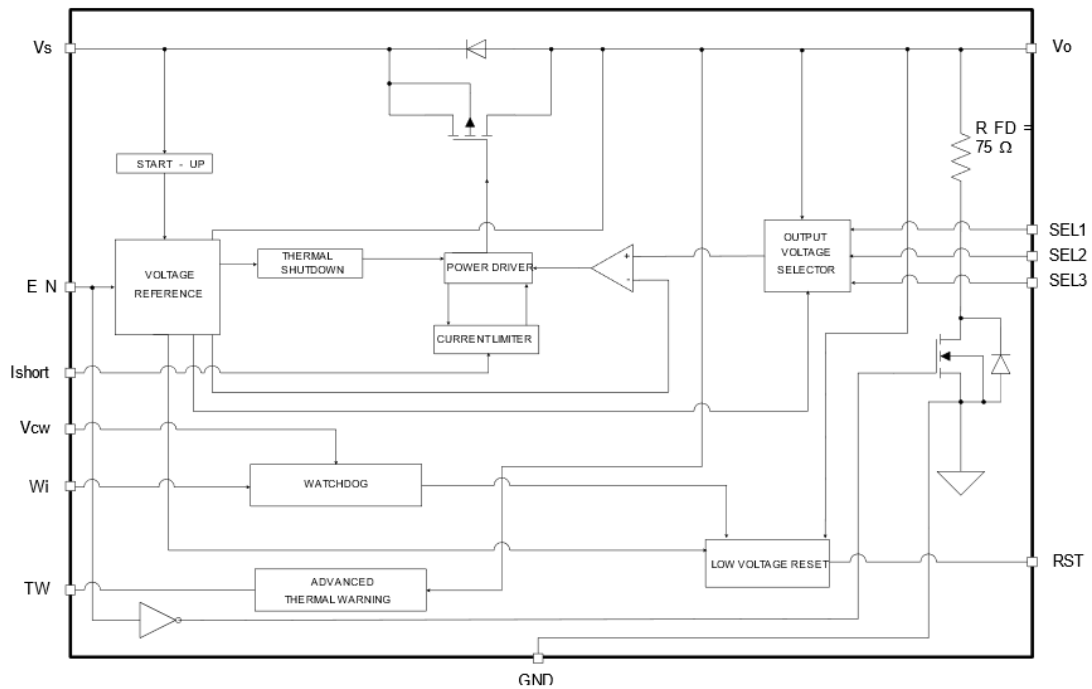
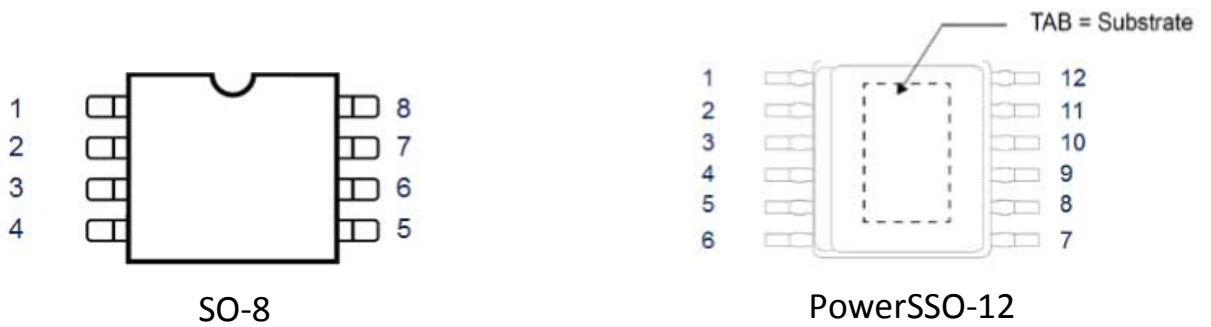


Figure 2. Functional block diagram of L99VR01J

Table 1. Pins description

Pin name	SO-8 pin	PowerSSO-12 pin	Function
V _S	1	1	Supply voltage. Block directly to ground with ceramic capacitor $\geq 4.7 \mu\text{F}$ and a 100 nF capacitor as close as possible to the pin
SEL1	2	2	Output voltage selectors.
SEL2	3	3	
SEL3	4	4	
TW		5	Advanced thermal warning output. If the device detects a junction temperature above the warning threshold, the pin is pulled low. If an overvoltage condition occurs, a square wave is provided through the TW output. Leave floating if not used.
I _{Short}		6	Programmable short circuit output current input pin. A resistor between Ishort pin and GND sets the short circuit output current value.
EN	5	7	Enable input. With the Enable high, regulator, watchdog and reset are operating. With the Enable low, regulator, watchdog and reset are shutdown, while the fast discharge circuit is turned on. Connect the Enable to V _S to keep the device always enabled
GND	6	8	Ground reference.
V _{CW}		9	Watchdog timer adjust. A capacitor between V _{CW} pin and GND sets the time response of the watchdog monitor (just for L99VR01J).

Pin name	SO-8 pin	PowerSSO-12 pin	Function
Wi		10	Watchdog refresh input. If the square wave frequency at this input pin is too low, a low pulse at RST pin is generated (just for L99VR01J).
RST	7	11	Reset output. It is pulled down when output voltage goes below V_{o_th} or frequency at Wi is too low (just for L99VR01J). Leave floating if not used.
V_O	8	12	Voltage regulator output. Block to ground with a capacitor $\geq 3.3 \mu\text{F}$ (needed for regulator stability).
TAB		TAB	Connected to ground

Figure 3. Pins configuration


2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the Table 2. Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0.3 to 28	V
V_S	Single pulse / $t_{max} < 400$ ms "transient load dump"	40	V
I_S	Input current	internally limited	
V_O	DC output voltage	-0.3 to 6.7	V
I_O	DC output current	internally limited	
V_{Wi}	Watchdog input voltage	-0.3 to $V_O + 0.3$	V
V_{CW}	Watchdog delay voltage	- 0.3 to $V_O + 0.3$	V
V_{rst}	Reset output voltage	-0.3 to $V_O + 0.3$	V
I_{rst}	Reset output current	Internally limited	
V_{tw}	Thermal warning output voltage	-0.3 to $V_O + 0.3$	V
I_{tw}	Thermal warning output current	Internally limited	
V_{sh_ctrl}	"Short current" control voltage	-0.3 to 3.6	V
V_{EN}	Enable input	-0.3 to $V_S + 0.3$	V
V_{SELx}	Selectors input voltage	-0.3 to $V_S + 0.3$	V
VESD HBM	ESD HBM voltage level (HBM-MIL STD 883C)	± 2	kV
VESD CDM	ESD CDM voltage level (CDM AEC-Q100-011)	± 500	V
	ESD CDM voltage level on corner pins (CDM AEC-Q100-011)	± 750	V

2.2 Thermal data

2.2.1 Thermal resistance

Table 3. Operation junction temperature

Item	Symbol	Parameter	Value		Unit
			PowerSSO-12	SO-8	
A.001	$R_{thj-case}$	Thermal resistance junction to case	8.5		°C/W
A.057	$R_{thj-lead}$	Thermal resistance junction to lead ⁽¹⁾		54.5	°C/W
A.002	$R_{thj-amb}$	Thermal resistance junction to ambient	27.4	71	°C/W

1. Measured on V_s

Note: the values quoted are for PCB 77 mm x 86 mm x 1.6 mm, FR4, four layers; Cu thickness 0.070 mm (outer layers) . Cu thickness 0.035 mm (inner layers), Thermal vias separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm.

2.2.2 Thermal protection

Table 4. Temperature threshold

Item	Symbol	Parameter		Test condition	Min.	Typ.	Max.	Unit
A.003	T_{prot_s} ⁽¹⁾	Thermal protection temperature		L99VR01S	150		180	°C
A.004	T_{prot_j} ⁽¹⁾	Thermal protection temperature		L99VR01J	175		200	°C
A.005	T_{prot_hyst}	Thermal protection hysteresis				11		°C
A.006	T_J	Operating junction temperature	SO-8	T_J	-40		150	°C
			Power-SSO-12		-40		175	
A.007	T_{stg}	Storage temperature		T_{stg}			150	°C

1. Thermal protection is guaranteed by design and characterization.

2.3 Electrical characteristics

Values specified in this section are for $V_S = 2.15 \text{ V to } 18 \text{ V}$, $T_J = -40 \text{ }^\circ\text{C to } +150 \text{ }^\circ\text{C}$, unless otherwise stated.

Table 5. Electrical characteristics

Item	Pin	Symbol	Parameter		Test condition	Min.	Typ.	Max.	Unit
A.008	V_O	V_O	Output voltage		$V_S = 2.15 \text{ to } 18 \text{ V}$ $I_O = 1 \text{ to } 200 \text{ mA}$ $\text{SEL_CONF}=[0;0;0]$	0.784	0.8	0.816	V
					$V_S = 2.15 \text{ to } 18 \text{ V}$ $I_O = 1 \text{ to } 200 \text{ mA}$ $\text{SEL_CONF}=[0;0;1]$	1.176	1.2	1.224	
					$V_S = 2.15 \text{ to } 18 \text{ V}$ $I_O = 1 \text{ to } 200 \text{ mA}$ $\text{SEL_CONF}=[0;1;0]$	1.470	1.5	1.530	
					$V_S = 2.45 \text{ to } 18 \text{ V}$ $I_O = 1 \text{ to } 200 \text{ mA}$ $\text{SEL_CONF}=[0;1;1]$	1.764	1.8	1.836	
					$V_S = 3.15 \text{ to } 18 \text{ V}$ $I_O = 1 \text{ to } 200 \text{ mA}$ $\text{SEL_CONF}=[1;0;0]$	2.450	2.5	2.550	
					$V_S = 3.45 \text{ to } 18 \text{ V}$ $I_O = 1 \text{ to } 200 \text{ mA}$ $\text{SEL_CONF}=[1;0;1]$	2.744	2.8	2.856	
					$V_S = 3.95 \text{ to } 18 \text{ V}$ $I_O = 1$ to 200 mA $\text{SEL_CONF}=[1;1;0]$	3.234	3.3	3.366	
					$V_S = 5.65 \text{ to } 18 \text{ V}$ $I_O = 1$ to 200 mA $\text{SEL_CONF}=[1;1;1]$	4.9	5	5.1	
A.009	V_O	I_O	DC output current		$V_O=0.8 \text{ V}; 1.2 \text{ V}; 1.5 \text{ V};$ $1.8 \text{ V}; 2.5 \text{ V}; 2.8 \text{ V}; 3.3 \text{ V};$ 5 V			200	mA
A.010	V_O	I_{short}	Short-circuit current lower value ⁽¹⁾	L99VR01J	$V_S = 4 \text{ V}$ for $V_O=3.3 \text{ V}$ $V_S = 5.8 \text{ V}$ for $V_O=5 \text{ V}$ with I_{short} pin connected to GND	30	65	100	mA
A.011	V_O	I_{short}	Short-circuit current upper value	L99VR01S	$V_S = 4 \text{ V}$ for $V_O=3.3 \text{ V}$ $V_S = 5.8 \text{ V}$ for $V_O=5 \text{ V}$ $I_{\text{short}} > I_O$	240	360	480	mA
				L99VR01J	$V_S = 4 \text{ V}$ for $V_O=3.3 \text{ V}$ $V_S = 5.8 \text{ V}$ for $V_O=5 \text{ V}$ with I_{short} pin floating; $I_{\text{short}} > I_O$				
A.012	V_S, V_O	$\Delta V_O / V_O$	Static line regulation		V_S is from V_{S_low} ⁽²⁾ to 18 V; $I_O = 1 \text{ mA}; 100 \text{ mA};$ 200 mA $V_O=3.3 \text{ V}; V_O=5 \text{ V}$			1	%
			Dynamic line regulation ⁽³⁾		V_S is from V_{S_low} ⁽²⁾ to 18 V; $T_r, f=1 \text{ ms}; I_O = 1 \text{ mA}; 50$ mA; 200 mA; $V_O= 3.3 \text{ V};$ $V_O=5 \text{ V}$			3	%

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.013	V _O	$\Delta V_O / V_O$	Static load regulation ⁽⁴⁾	I _O = 1 mA to 100 mA V _O = 3.3 V for V _S = 5 V; V _O = 5 V for V _S = 6 V			1	%
			Dynamic load regulation ^{(3) (4)}	I _O = 10 mA to 100 mA, Tr, f = 10 μs V _O = 3.3 V for V _S = 5 V; V _O = 5 V for V _S = 6 V			3	%
A.014	V _S , V _O	V _{dp}	Drop voltage ⁽⁵⁾	I _O = 150 mA V _O = 5 V			500	mV
				I _O = 150 mA V _O = 3.3 V				
				I _O = 150 mA V _O = 2.8 V				
				I _O = 150 mA V _O = 2.5 V				
				I _O = 150 mA V _O = 1.8 V			530	mV
				I _O = 200 mA V _O = 5 V				
				I _O = 200 mA V _O = 3.3 V				
				I _O = 200 mA V _O = 2.8 V				
				I _O = 200 mA V _O = 2.5 V				
				I _O = 200 mA V _O = 1.8 V				
A.015	V _S , V _O	PSRR	Power supply rejection ratio	V _S = 13.5 V; V _O = 5 V; I _O = 200 mA fr = 1 kHz		75 ⁽³⁾		dB
A.017	V _S , V _O	I _{qn}	Current consumption with regulator disabled I _{qn} = I _S – I _O	V _S = 3.5 V; 13.5 V, EN = low			1	μA
A.058	V _S , V _O	I _{qn_LL}	Current consumption with regulator enabled I _{qn_LL} = I _S – I _O	V _S = 3.5 V; 13.5 V, I _O = 0 μA; EN = high		75	100	μA
A.018	V _S , V _O	I _{qn_O}	Current consumption with regulator enabled I _{qn_O} = I _S – I _O	V _S = 3.5 V; 13.5 V, 0 < I _O ≤ 100 μA; EN = high		100	130	μA
A.019	V _S , V _O	I _{qn_50}	Current consumption with regulator enabled I _{qn_50} = I _S – I _O	V _S = 3.5 V; 13.5 V, I _O = 50 mA EN = high		1	1.3	mA
A.020	V _S , V _O	I _{qn_100}	Current consumption with regulator enabled I _{qn_100} = I _S – I _O	V _S = 3.5 V; 13.5 V, I _O = 100 mA EN = high		1.7	2.0	mA
A.021	V _S , V _O	I _{qn_200}	Current consumption with regulator enabled I _{qn_200} = I _S – I _O	V _S = 3.5 V; 13.5 V, I _O = 200 mA EN = high		3.1	3.5	mA

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.022	V _S	V _{UVLO_fall}	Undervoltage lockout, falling	V _O = 0.8 V; 1.2 V; 1.5 V; 1.8 V	1.5	1.6	1.7	V
				V _O = 2.5 V; 2.8 V; 3.3 V	2.3	2.4	2.55	
				V _O = 5 V	4.6	4.8	4.9	
A.023	V _S	V _{UVLO_rise}	Undervoltage lockout, rising	V _O = 0.8 V; 1.2 V; 1.5 V; 1.8 V	1.7	1.8	2.1	V
				V _O = 2.5 V; 2.8 V; 3.3 V	2.6	2.7	2.8	
				V _O = 5 V	4.9	5.1	5.3	

1. *Short typical value of 120 mA for t = 400 μs during the power on*
2. *V_{S_Low} = 3.5 V @ V_O = 0.8 V, 1.2 V, 1.5 V, 1.8 V & 2.5 V; V_{S_Low} = 5 V @ V_O = 2.8 V & 3.3 V, V_{S_Low} = 6 V @ V_O = 5 V*
3. *Parameters are guaranteed by design*
4. *Referred to Figure 30. Maximum load variation response*
5. *Considering that the minimum operating input voltage is 2.15 V, the dropout voltage (V_{dp}) is not defined for output voltages below 1.8 V.*

Table 6. Fast output discharge

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.024	V _O	R _{FD}	Fast discharge - pull down resistor	V _S = 3.95 V; 13.5 V; V _O = 3.3 V, V _O = 5 V EN = low	50	75	105	Ω

Table 7. Reset

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.025	RST	V _{rst_l}	Reset output low voltage	V _S = 5 V; 13.5 V R _{ext} ≥ 4.7 KΩ to V _O V _O = 3.3 V, V _O = 5 V			0.2 x V _O	V
A.026	RST	I _{rst_lkg}	Reset output high leakage current	V _{rst} = 0.8 V			1	μA
A.027	RST	V _{O_th}	V _O out of regulation – low threshold	V _S = 5 V; 13.5 V V _O decreasing V _O = 3.3 V, V _O = 5 V	13.5%	10%	6.5%	Below V _O
A.055	RST	V _{O_th_hyst}	V _O out of regulation – low threshold hysteresis	V _S = 5 V; 13.5 V; V _O increasing; V _O = 3.3 V; V _O = 5 V		2%		V _{O_th}
A.028	RST	T _{rr}	Reset reaction time	V _S = 5 V; 13.5 V; V _O = 3.3 V; V _O = 5 V	10	16	37	μs
A.029	RST	T _{rd}	Reset delay time	V _S = 5 V; 13.5 V; V _O = 3.3 V; V _O = 5 V	160	250	300	μs

Table 8. Watchdog (only for L99VR01J)

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.030	W _i	V _{ih}	Input high voltage ⁽¹⁾	V _S =5 V; 13.5 V V _O =3.3 V; V _O =5 V	0.7 x V _O			V
A.031	W _i	V _{il}	Input low voltage ⁽¹⁾	V _S = 5 V; 13.5 V V _O =3.3 V; V _O =5 V			0.25 x V _O	V
A.033	W _i	I _{wi}	Pull down current	V _{wi} = 3.3 V		6	10	μA
A.034	V _{CW}	V _{wlth}	Low threshold	V _S = 5V; 13.5 V V _O =3.3V; V _O =5V	10 %	13 %	16 %	V _O
A.035	V _{CW}	V _{wth}	High threshold	V _S = 5V; 13.5 V V _O =3.3V; V _O =5V	44 %	47 %	50 %	V _O
A.036	V _{CW}	I _{CWc}	Charge current	V _S = 5V; 13.5 V V _{CW} = 0.1V V _O =3.3V; V _O =5V	5	10	20	μA
A.037	V _{CW}	I _{CWd}	Discharge current	V _S = 5 V; 13.5 V V _{CW} = 2.5 V V _O =3.3 V; V _O =5 V	1.25	2.5	5	μA
A.040	V _{CW}	I _{w_off}	Watchdog deactivation current threshold	V _S = 5 V; 13.5 V V _O =3.3 V; V _O =5 V	0.6	1.05	1.5	mA
A.041	V _{CW}	I _{w_on}	Watchdog activation current threshold	V _S = 5 V; 13.5 V V _O =3.3 V; V _O =5 V	2.2	3.35	4.5	mA

1. Watchdog input requires a square wave signal (duty cycle of 50 %)

Table 9. Enable

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.042	EN	V _{En_low}	EN input low voltage				0.6	V
A.043	EN	V _{En_high}	EN input high voltage		1.5			V
A.045	EN	I _{En}	Pull down current	V _S = 13.5 V		4	12	μA

Table 10. Output voltages selectors

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.046	SELx	V _{SELx_low}	SELx input low voltage				0.3	V
A.047	SELx	V _{SELx_high}	SELx input high voltage		0.7			V
A.048	SELx	I _{SELx}	Pull down current	V _S = 3.5V; 13.5 V		0.1	0.4	μA

Table 11. Thermal warning and protection (only for L99VR01J)

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.049	TW	V _{Tw_low}	Thermal warning output low voltage	R _{ext} ≥ 4.7 kΩ to V _O V _O =3.3 V; V _O =5 V			0.2xV _O	V

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.050	TW	T_{warn}	Thermal warning temperature		140	150	160	°C
A.051	TW	$T_{\text{warn_hyst}}$	Thermal warning hysteresis		3	11	15	°C
A.052	V_O	OV	V_O overvoltage	$V_S = 5\text{ V}; 13.5\text{ V}; V_O$ increasing $V_O=3.3\text{ V}; V_O=5\text{ V}$	6.5%	10%	13.5%	Above V_O
A.056	V_O	O_{V_hyst}	V_O overvoltage hysteresis	$V_S = 5\text{ V}; 13.5\text{ V}; V_O$ decreasing $V_O=3.3\text{ V}; V_O=5\text{ V}$		2%		Below V_O
A.054	TW	T_{w_per}	Thermal warning square wave period	$V_S = 5\text{ V}; 13.5\text{ V}$ $V_O=3.3\text{ V}; V_O=5\text{ V}$	160	250	300	μs

Note: all parameters are guaranteed in the junction temperature range -40°C to 150°C (unless otherwise specified); L99VR01J device is still operative and functional at higher temperatures (up to 175°C). Parameters limit at higher junction temperature than 150°C may change respect to what is specified as per the standard temperature range. device functionality at high junction temperature is guaranteed by characterization. All parameters are guaranteed by design for V_O not reported in test condition.

Note: minimum input voltage values are achievable adopting an input ceramic capacitor: C5750X7R2A475M230KA – ceramic capacitor multistrate SMD, 4.7 μF, 100 V, ±20%, X7R, C series TDK.

2.4 Electrical characteristics curves

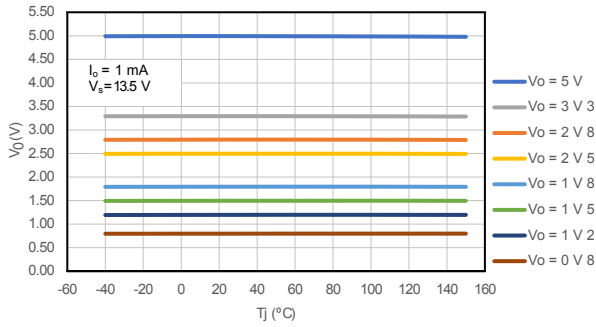
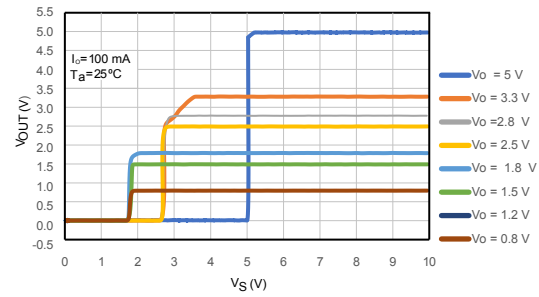
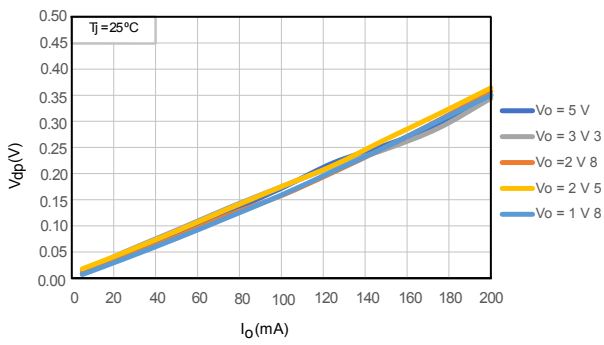
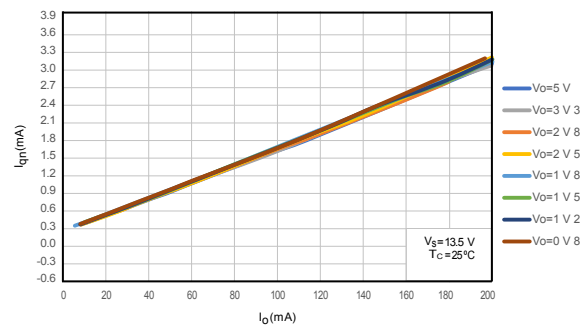
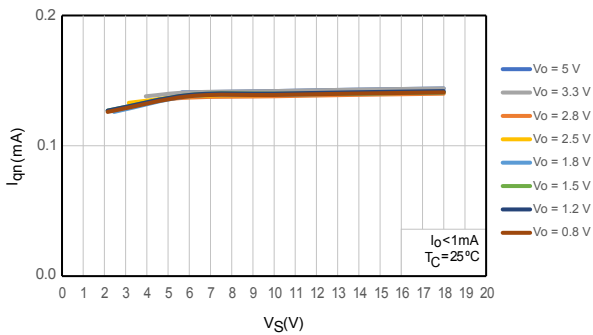
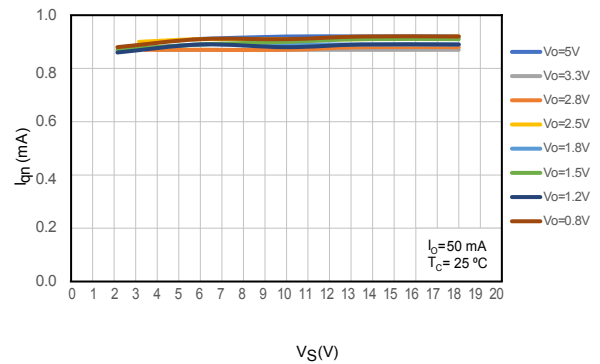
Figure 4. Output voltage vs Tj

Figure 5. Output voltage vs VS

Figure 6. Drop voltage vs output current

Figure 7. Current consumption vs output current

Figure 8. Current consumption vs input voltage ($I_o < 1 \text{ mA}$)

Figure 9. Current consumption vs input voltage ($I_o = 50 \text{ mA}$)


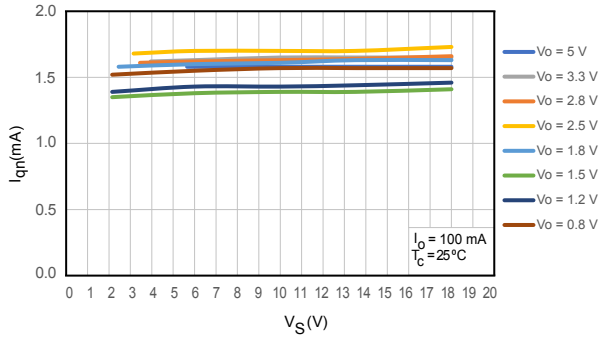
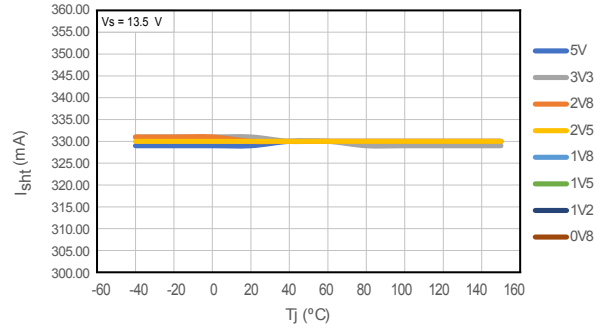
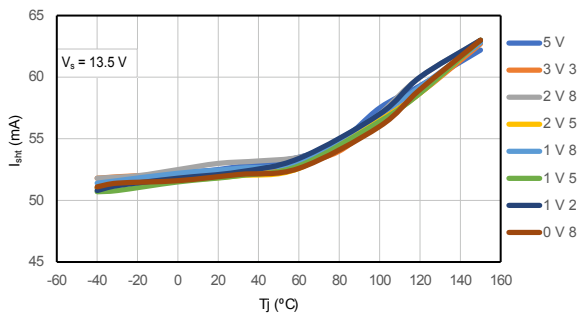
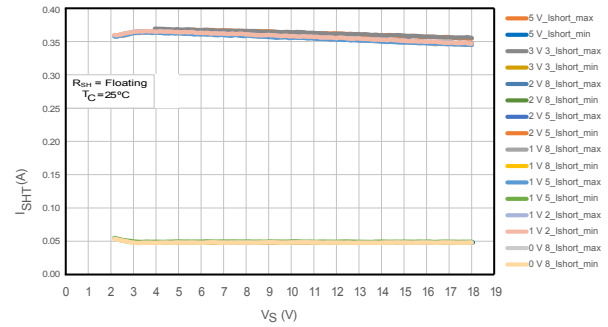
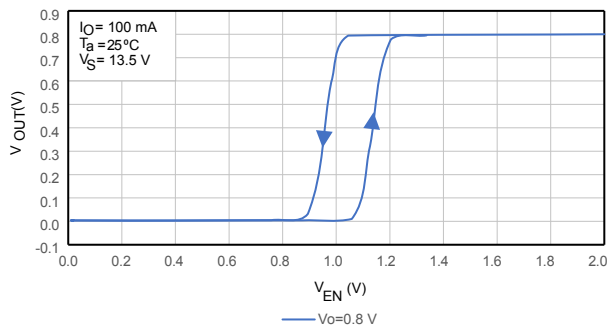
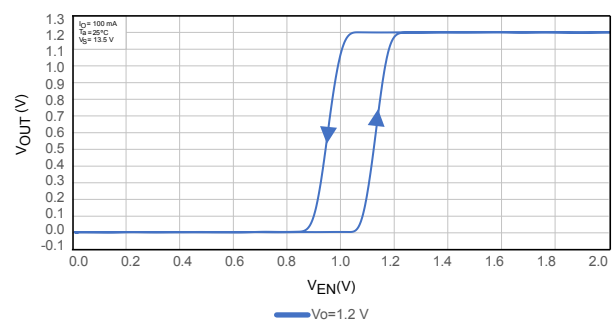
Figure 10. Current consumption vs input voltage ($I_O = 100 \text{ mA}$)

Figure 11. Short-circuit current vs T_j (I_{short} pin floating)

Figure 12. Short-circuit current vs T_j (I_{short} pin tied to GND)

Figure 13. Short-circuit current vs input voltage

Figure 14. Output voltage vs enable voltage ($V_O = 0.8 \text{ V}$)

Figure 15. Output voltage vs enable voltage ($V_O = 1.2 \text{ V}$)


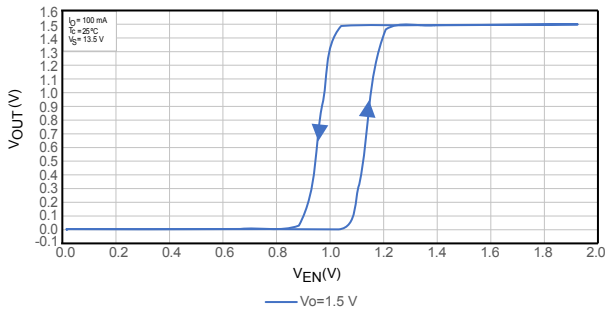
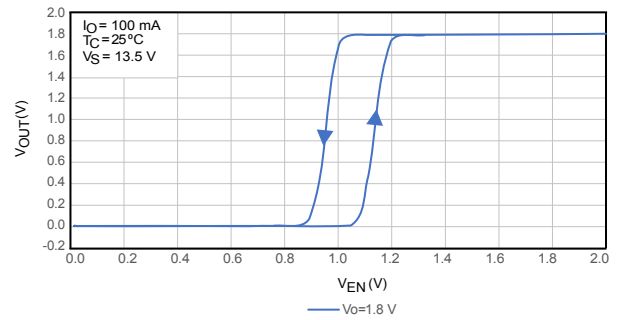
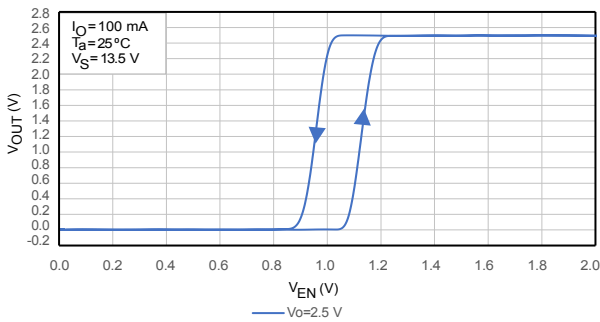
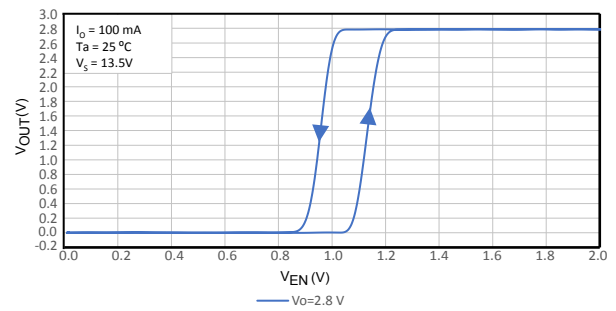
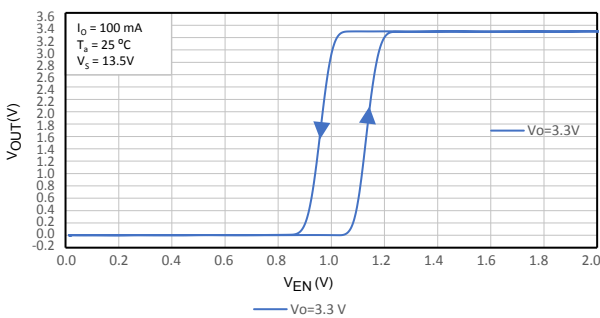
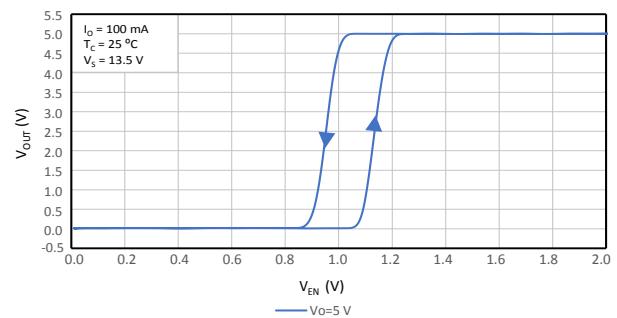
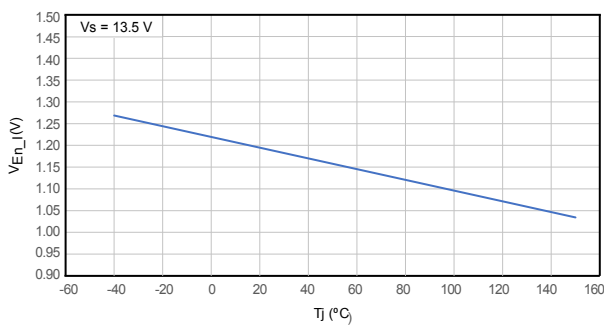
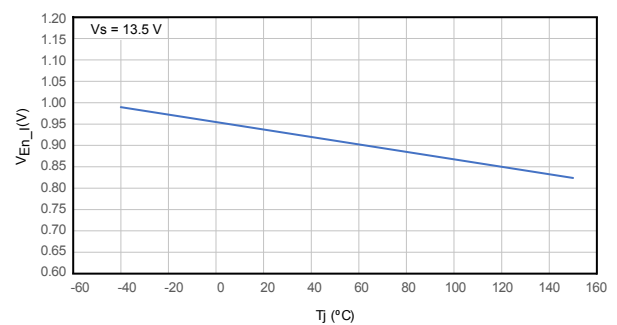
Figure 16. Output voltage vs enable voltage ($V_O = 1.5\text{ V}$)

Figure 17. Output voltage vs enable voltage ($V_O = 1.8\text{ V}$)

Figure 18. Output voltage vs enable voltage ($V_O = 2.5\text{ V}$)

Figure 19. Output voltage vs enable voltage ($V_O = 2.8\text{ V}$)

Figure 20. Output voltage vs enable voltage ($V_O = 3.3\text{ V}$)

Figure 21. Output voltage vs enable voltage ($V_O = 5\text{ V}$)

Figure 22. V_{EN_high} vs T_j

Figure 23. V_{EN_low} vs T_j


Figure 24. V_{whth} vs T_j

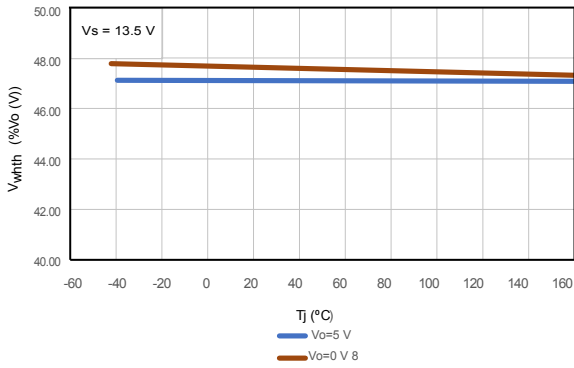


Figure 25. V_{wlth} vs T_j

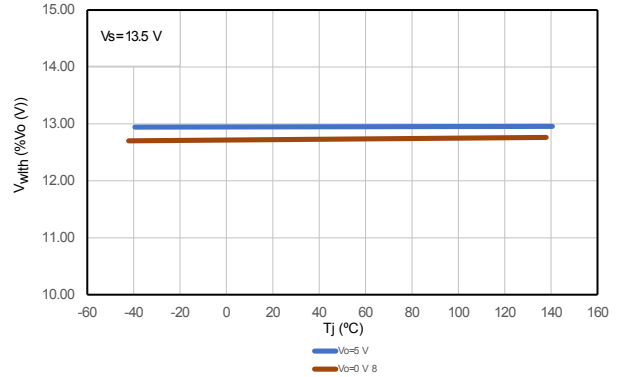


Figure 26. I_{cwc} vs T_j

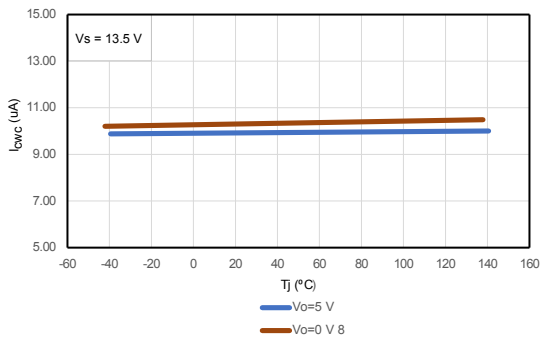


Figure 27. I_{cld} vs T_j

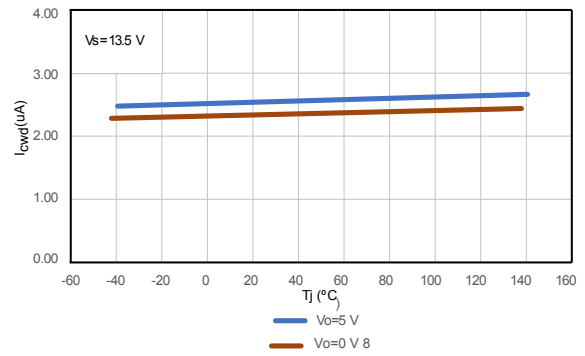
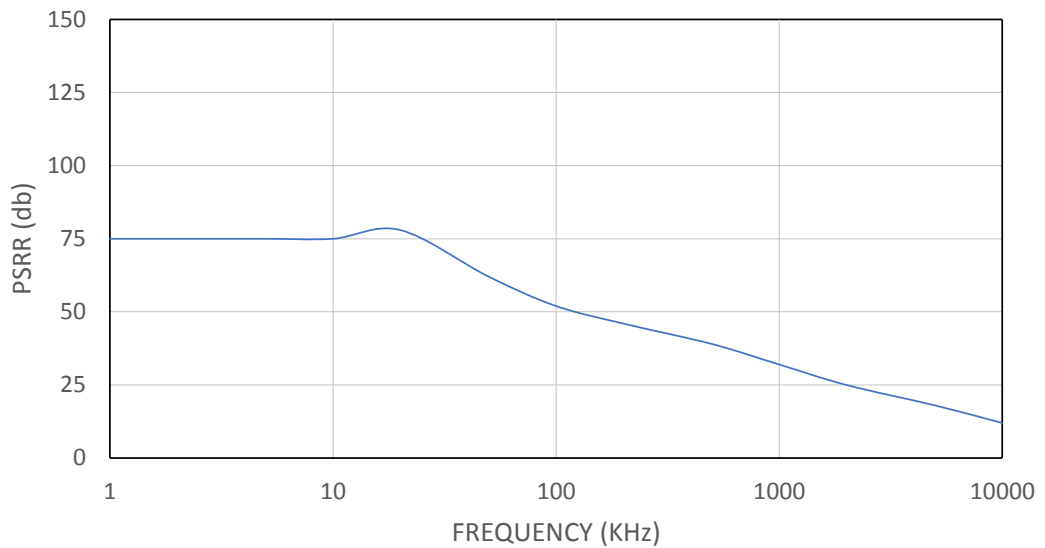
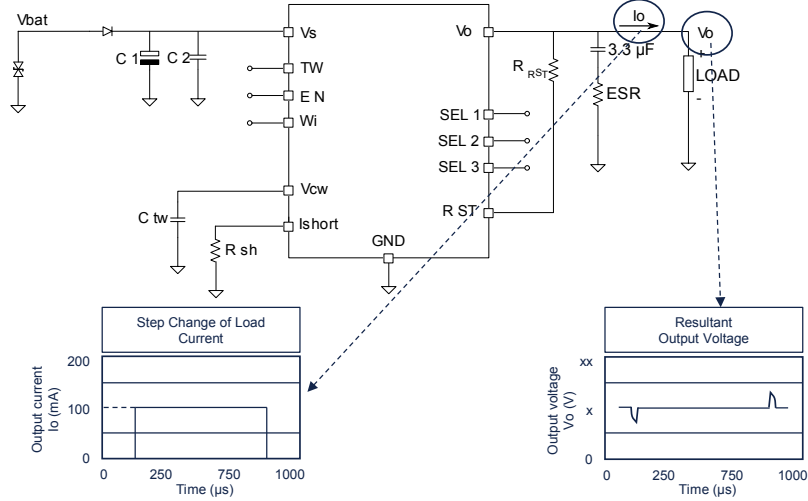
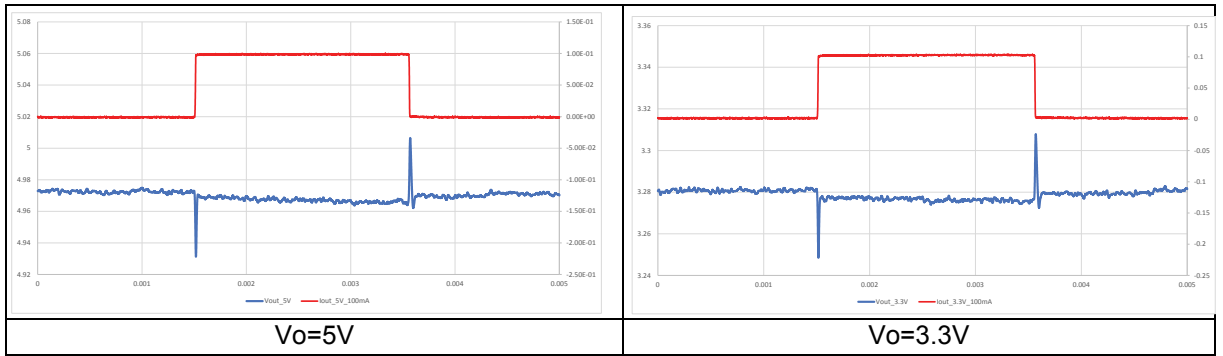


Figure 28. PSRR



3 Test circuit and waveforms plot

3.1 Load regulation

Figure 29. Load regulation test circuit

Figure 30. Maximum load variation response


4 Application information

Figure 31. Application schematic

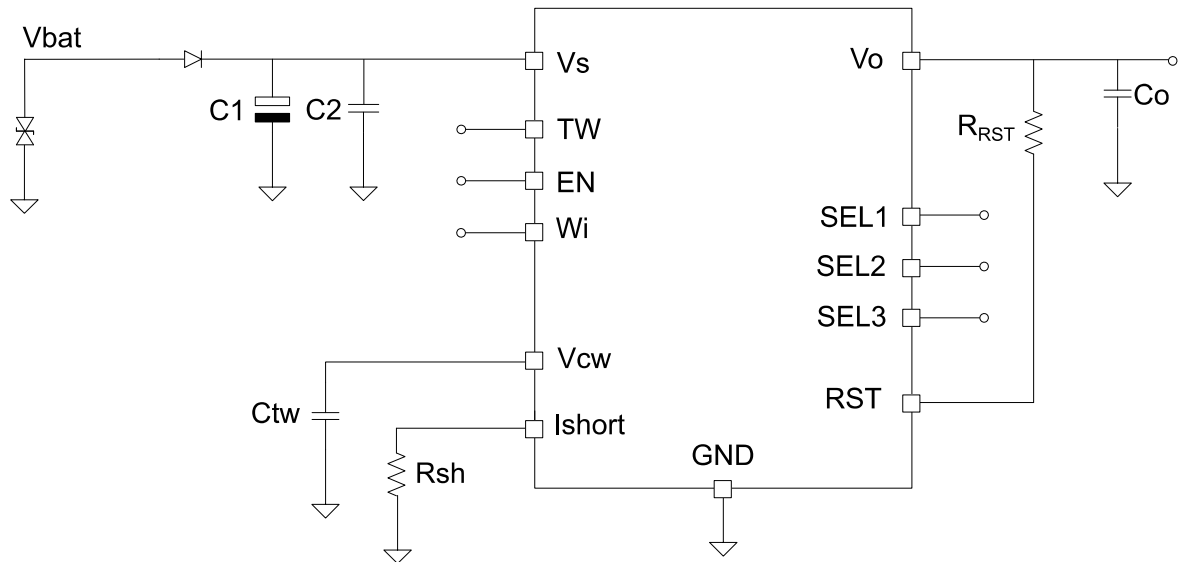
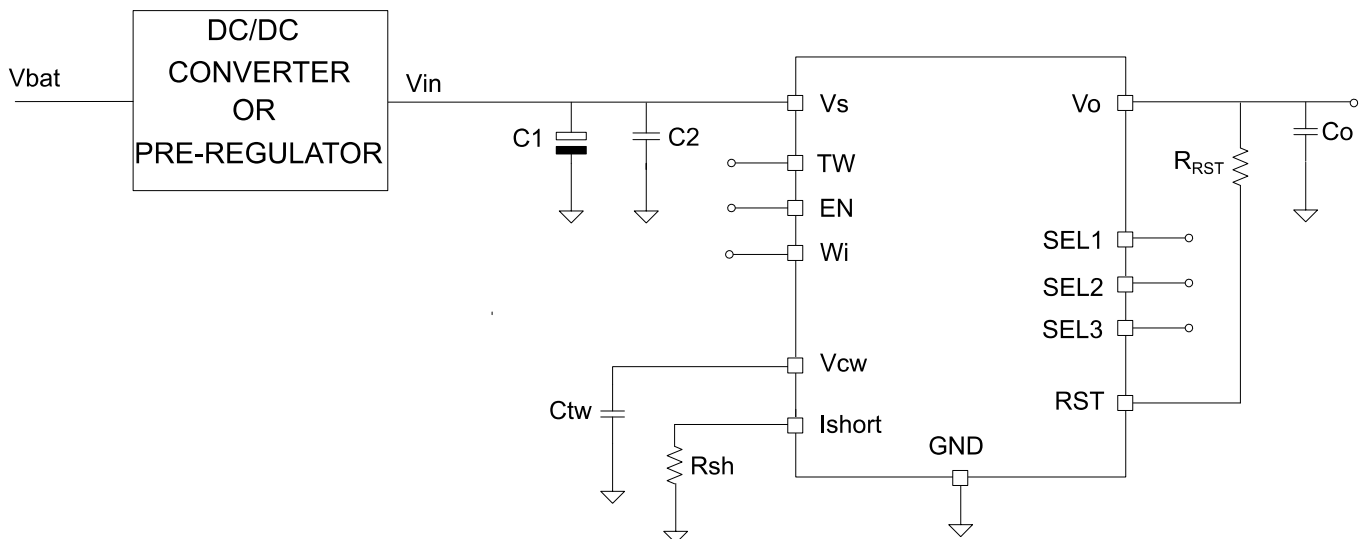


Figure 32. Application schematic – Post regulation



Input ceramic capacitor $C_2 \geq 4.7 \mu\text{F}$ is necessary for the regulator to operate properly. The other input capacitor C_1 can be used as backup supply for the application. The C_0 capacitor, connected to the output pin, is for bypassing to GND the high-frequency noise and it guarantees stability even during sudden line and load variations.

Suggested value is $C_0 = 3.3 \mu\text{F}$.

The ESR of the SMD output ceramic capacitor has a negligible effect on the stability of the L99VR01 family for capacitors with low ESR. A ceramic SMD capacitor is recommended on V_o pin.

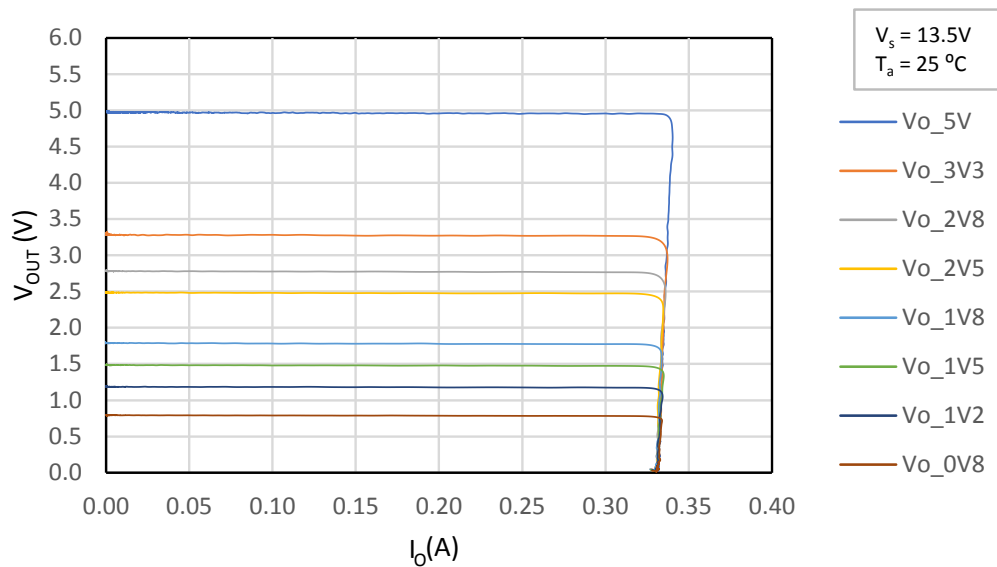
4.1 Voltage regulator

The voltage regulator uses a p-channel MOS transistor as a regulating element. With this structure, a very low dropout voltage at current up to $I_o = 200\text{ mA}$ is obtained. The high-precision of the output voltage ($\pm 2\%$) is obtained with a pre-trimmed reference voltage. The voltage regulator automatically adapts its own quiescent current to the output current level. In light load conditions the quiescent current goes down to $I_{qn_LL} = 75\ \mu\text{A}$ (low consumption mode). L99VR01 operates with reduced input voltage (post regulation) minimizing the internal power dissipation and maximizing the output current.

4.2 Output current limitation

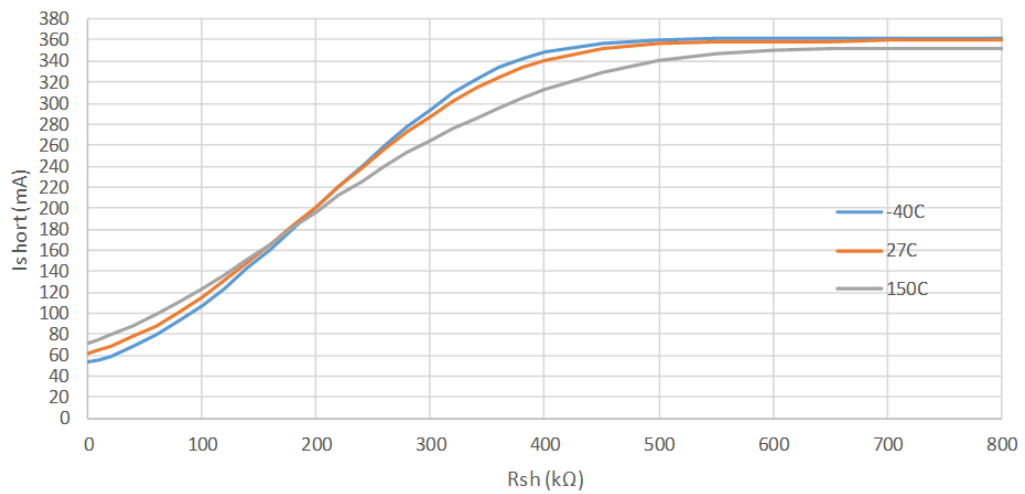
Output current limitation is present to protect the regulator and the application from overload condition, such as short to ground.

Figure 33. Behavior of output current versus regulated voltage V_o



The I_{short} current can be set in the range from 65 mA to 360 mA through an external resistor R_{sh} connected between I_{short} pin and ground (L99VR01J version only).

Figure 34. Ishort versus Rsh



Open pin (no resistance on the Ishort pin), is seen as a max resistance corresponding to the maximum Ishort current.

4.3 Output voltage selection

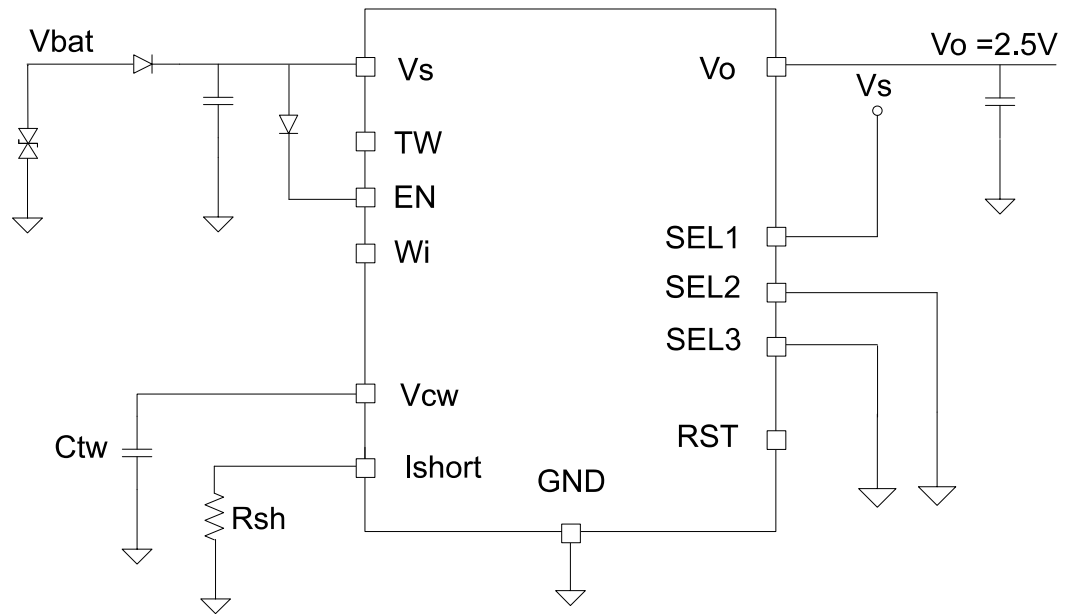
The L99VR01 can provide one out of 8 different output voltages. The combination of three digital input selectors (SELx) determines the output voltage according to the following truth table.

Table 12. Truth table

V _O	SEL1	SEL2	SEL3
5	1	1	1
3.3	1	1	0
2.8	1	0	1
2.5	1	0	0
1.8	0	1	1
1.5	0	1	0
1.2	0	0	1
0.8 (Default)	0	0	0

The SELx pins configuration is acquired at the device start-up (EN transition from low to high) and once configuration is acknowledged, it cannot be changed until next EN transition.

When all the pins are left not connected, the default configuration will be selected.

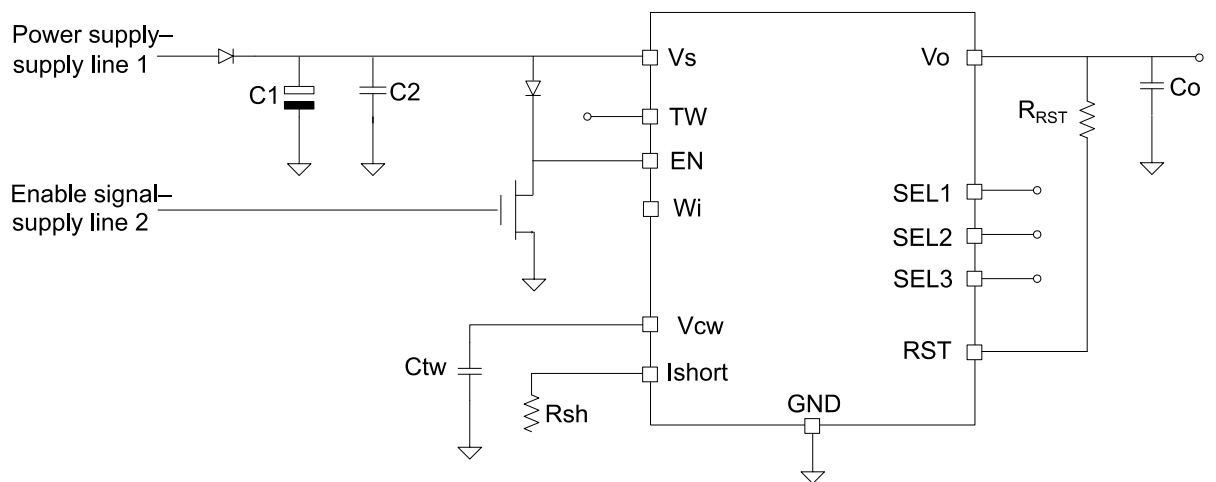
Figure 35. Example of output voltage selection


SELx pins are internally connected to GND via pull down current source.

4.4 Enable

The L99VR01 is enabled/disabled by the enable input; a high voltage signal switches the regulator ON. When the enable pin is set low, the output is switched-off, the current consumption of the device becomes as low as 1 μ A and the Fast Output Discharge circuit is activated.

It may happen that the enable pin must be driven by components supplied at a voltage different from the regulator supply voltage. In this case the EN input pin must be set high only once $V_S > 1.5$ V. A solution to drive the enable pin is depicted in the following figure.

Figure 36. Typical example of enable control


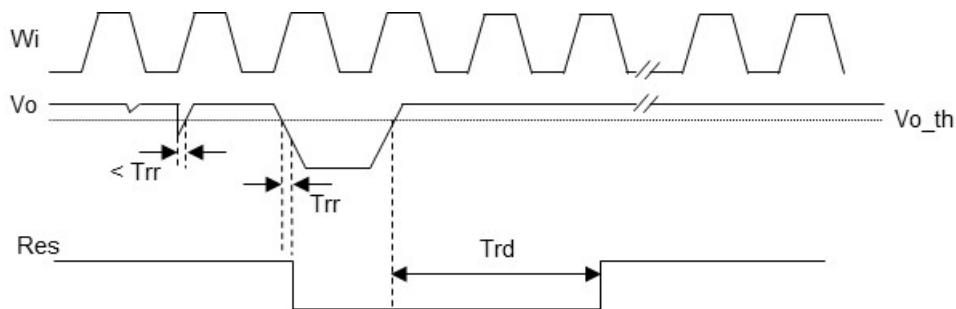
In any case, since the enable input voltage is linked to the maximum DC supply voltage (V_S) applied to the L99VR01 (-0.3 V to $V_S + 0.3$ V), special care must be adopted in driving EN pin to avoid exceeding absolute maximum rating.

Note: A diode ($0.25\text{ V} < V_F < 0.75\text{ V}$) connected in series with EN pin is requested only if the regulator is directly supplied by car battery.

4.5 Reset

The reset circuit supervises the output voltage V_O . If the output voltage falls below V_{O_th} then RST is pulled low with a reaction time T_{rr} . When the output voltage rises above $V_{O_th} + V_{O_th_hyst}$ then RST is pulled high with a delay time T_{rd} . The delay is generated by an internal circuit. The reset circuit is active when En is high. Being RST an open-drain output an external resistance (R_{rst}) is needed between the RST pin and the Vo pin. The external resistance value can be in a range between 4.7 K Ω and 20 K Ω . Leave the RST pin floating if not used. Be aware that the current flowing through the RST pin drawn from Vo when the RST pin is pulled low may affect the watchdog activation/deactivation based on the regulator output current consumption monitoring.

Figure 37. Reset timing diagram



4.6 Autonomous watchdog

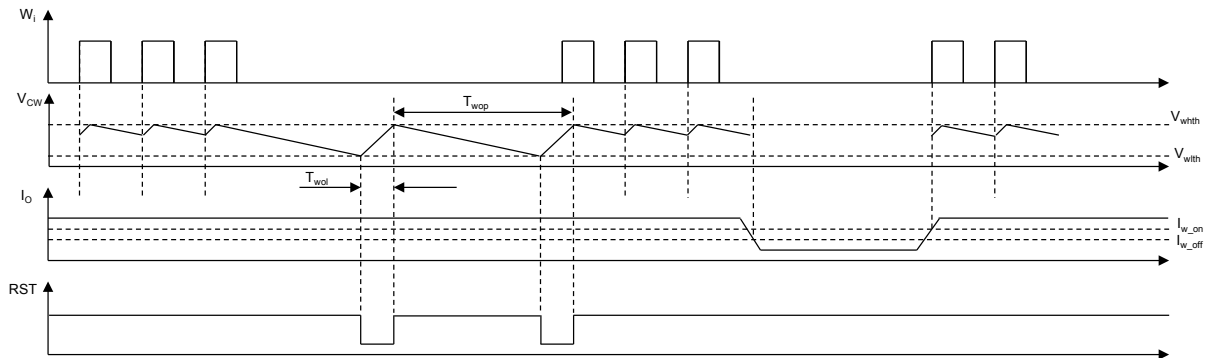
A supplied microcontroller is monitored by the watchdog input W_i (L99VR01J version only). If pulses are missing, the RST output pin is set low. The watchdog timeout can be set within a wide range with the external capacitor, C_{tw} . The watchdog circuit discharges the capacitor C_{tw} , with the constant current I_{CWd} . If the lower threshold V_{wlth} is reached, a watchdog reset is generated. To prevent this from happening the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage reaches the threshold V_{wlth} . To calculate the sawtooth period " T_{wop} ", taking care that the microcontroller triggers the positive edge during the discharge phase of C_{tw} (T_d), the following equations can be used:

$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{CWd} \times T_d$$

$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{CWc} \times T_{wol}$$

$$T_{wop} = T_d + T_{wol}$$

Every W_i positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold, V_{whth} , the current switches from charging to discharging. The result is a saw-tooth voltage at the watchdog timer capacitor C_{tw} . If a microcontroller operates in low power mode it will not be able to generate any pulse to refresh the voltage regulator watchdog, triggering so the microcontroller reset. In such a case, to avoid generating the microcontroller reset, the watchdog functionality will be automatically deactivated any time the microcontroller current consumption falls under the I_{w_off} threshold. On the other hand, when the current consumption rises above the I_{w_on} threshold the watchdog functionality will be once again activated. Once the regulator is enabled for the first time, if $I_o < I_{w_off}$ the watchdog will not be activated, while if $I_o > I_{w_off}$ the watchdog will be activated.

Figure 38. Watchdog timing diagram


Since the RST output pin is shared between the watchdog circuit and the output voltage monitoring circuit, for applications where the watchdog is not needed, to prevent the watchdog from generating RST pulses without anyhow losing the reset functionality of the Vo monitoring, the V_{cw} pin has to be connected to Vo. V_{cw} pin must be always tied to ground by an external capacitor (C_{tw}) when the watchdog is used.

Note: when the watchdog timer is used and the regulator recovers from a thermal shut-down event or recovers from an output under-voltage event (including the recovery from output under-voltage event at the regulator output turning on), the reset pin might be pulled back high with a delay longer than Trd , in the range between Trd and $Trd + Twol$ due to the watchdog that might affect the RST pin release. The watchdog will not affect the RST pin release in the case where recovering from a thermal shut-down event or recovering from an output under-voltage event (including the recovery from output under-voltage event at the regulator output turning on) the I_o drops below I_{w_off} before Trd . The output current I_o consists in the load current, the current drawn from the RST pin and the TW pin through the pull-down resistors connected to Vo when the RST and the TW pins are asserted low and the current needed to charge/discharge the output capacitor C_o .

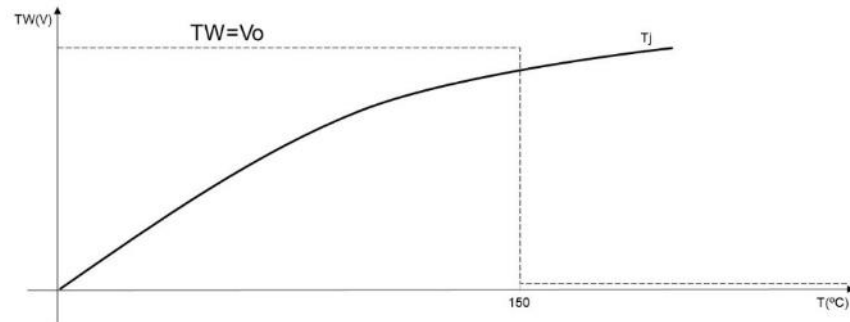
Note: when the watchdog timer is used, in case of an output under-voltage event not making Vo drop to zero volt, since the watchdog will still be running during the output under-voltage condition, the first watchdog timeout after the reset pin is released coming out of the output under-voltage event might occur before expected ($0 \leq \text{Timeout} \leq Twop - Twol$).

Table 13. Watchdog timer

Usage of watchdog timer	Connection of Vcw Pin
Watchdog timer is not used	Connect to the Vo pin
Watchdog timer is used	Connect to an external capacitor C_{tw}

4.7 Thermal warning and thermal shutdown

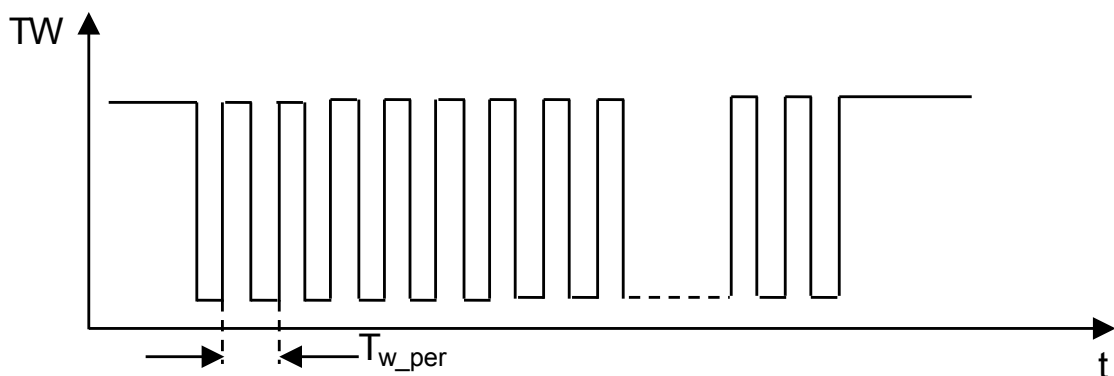
To warn the microcontroller about a severe temperature increase, a thermal warning output has been implemented (L99VR01J version only). If the device detects a junction temperature above T_{warn} , the advanced thermal warning (TW) output pin is pulled low while the voltage regulator and its features remain all active. The TW pin will return to its high logic level (equal to the Vo output value) once the temperature falls below the threshold $T_{warn} - T_{warn_hyst}$.

Figure 39. Thermal warning diagram


When junction temperature reaches the $T_{prot_j/s}$ thermal shutdown threshold the regulator output is quickly shut-off through the internal Fast Output Discharge circuit; to be reactivated, junction temperature has to decrease below $T_{prot_j/s} - T_{prot_hyst}$. Being TW an open-drain output an external resistance (R_{TW}) is needed between the TW pin and the Vo pin. The external resistance value can be in a range between 4.7 K Ω and 20 K Ω . Be aware that the current flowing through the TW pin drawn from Vo when the TW pin is pulled low may affect the watchdog activation/deactivation based on the regulator output current consumption monitoring. Leave floating if not used.

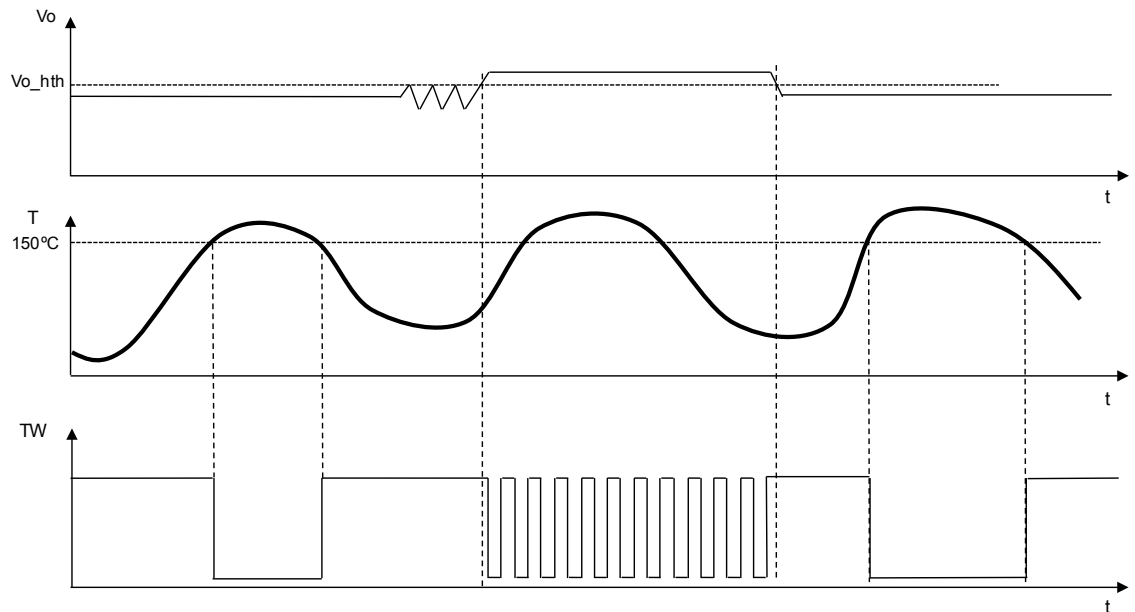
4.8 Overvoltage detection by advanced thermal warning read-out

The TW pin also provides diagnostics about output overvoltage (OV); to distinguish between a thermal warning event and an output overvoltage event, two different signals are generated at the same TW output pin. How reported in the previous paragraph a thermal warning event detection sets the TW pin LOW, instead an output overvoltage event generates a square wave at the TW pin (Figure 40. Square wave on TW pin generated during an overvoltage). Overvoltage detection has higher priority than thermal warning detection so that concurrence of thermal warning and over voltage events leads to a square wave like in the case of overvoltage detection (as shown in Figure 41. Warning signal caused by overvoltage and thermal warning on TW pin).

Figure 40. Square wave on TW pin generated during an overvoltage


A typical example of thermal warning and overvoltage failures management is depicted in Figure 41. Warning signal caused by overvoltage and thermal warning on TW pin.

Figure 41. Warning signal caused by overvoltage and thermal warning on TW pin

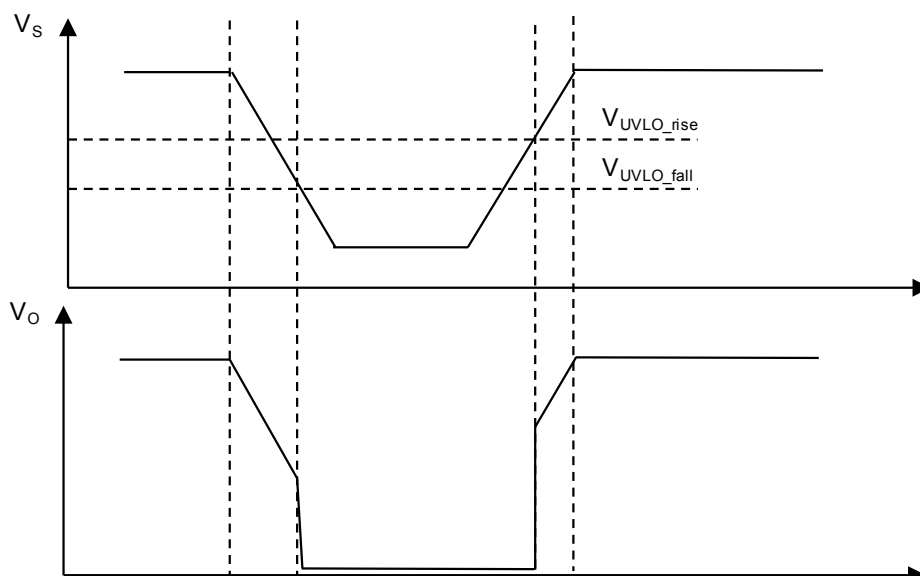


4.9 Fast output discharge

To assure a quick discharge of the external capacitor tied to the output pin down to around 1.3 V the L99VR01 uses an internal pulldown circuit. Activated each time the EN pin goes low, during thermal shut down and during undervoltage lockout, the output current will flow through the pulldown resistor of the fast output discharge circuit to ground. The fast output discharge feature is available for the output voltages $V_o = 2.5\text{ V}$ (SELx = [1;0;0]) $V_o = 2.8\text{ V}$ (SELx = [1;0;1]) $V_o = 3.3\text{ V}$ (SELx = [1;1;0]) and $V_o = 5\text{ V}$ (SELx = [1;1;1]).

4.10 Undervoltage lockout UVLO

The undervoltage lockout (UVLO) circuit allows a fast regulating element to turn off (activating the internal Fast Output Discharge circuit) if the input voltage drops below the threshold, V_{UVLO_fall} , avoiding undesired unknown output state during low input voltage. When the input voltage is above the V_{UVLO_rise} threshold, the regulating element is again turned on.

Figure 42. Undervoltage lockout on output voltage


4.11 Functional safety management

The device was designed to offer a set of features to support applications that need to fulfill functional safety requirements as defined by ASIL classification in ISO26262-2018. The IC was developed for different applications, hence can be considered a SEooC (Safety Element out of Context) as defined in the normative. Analysis of the IC's capability to reach the required safety level, should be made at system level under user responsibility.

The following device safety requirements have been considered for a typical application:

Table 14. Safety requirement

ID	Description
SR-001	Operation of the voltage regulator(s) is allowed till over temperature limit.
SR-002	Operation of voltage regulator(s) is enabled until programmed current limit is reached.
SR-003	Output voltage of regulator(s) shall remain within programmed range when RST pin is not asserted.
SR-004	Output voltage of regulator(s) shall remain within programmed range when square wave at TW pin is not generated.

Based on above requirements list the following safety mechanism has been implemented:

Table 15. Implemented safety mechanism

ID	Description	SR covered
SM1	Thermal sensor acting by TW pin	SR-004
SM2	Overtemperature protection	SR-001
SM3	Limitation on maximum output current	SR-002
SM4	Output voltage V_o monitoring for undervoltage detection	SR-002

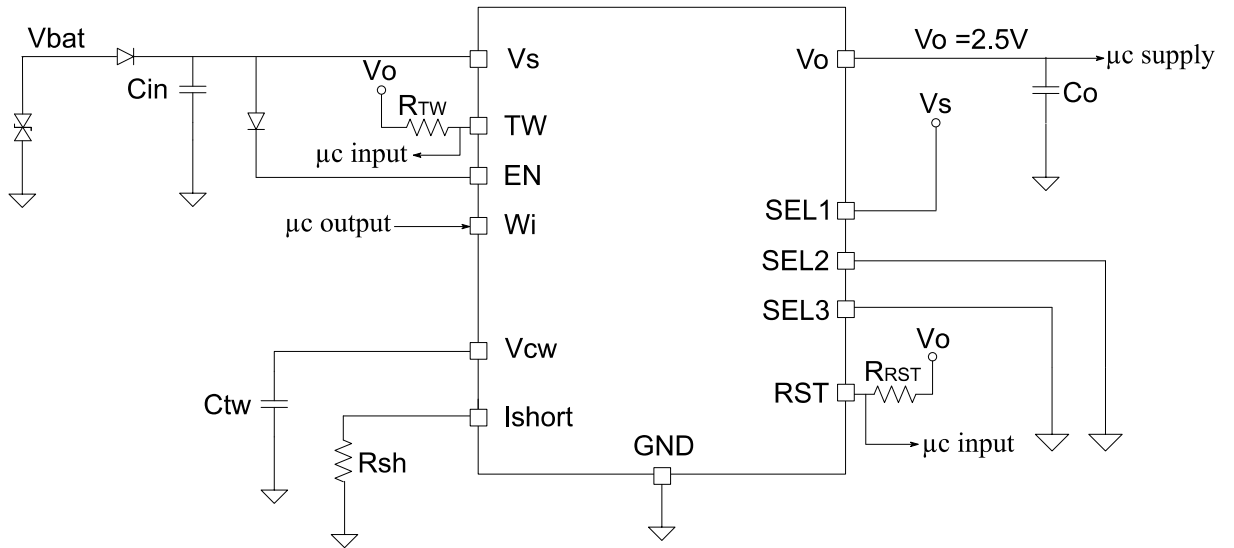
ID	Description	SR covered
SM5	Output voltage V_O monitoring for overvoltage detection	SR-002
SM6	RST reset assertion in case of V_O undervoltage detection	SR-003

In addition to the internal watchdog for checking the correct operation of the microcontroller, it can be considered a system-level safety mechanism.

More details about functional safety can be found in the device safety manual, provided on customer request.

5 Application

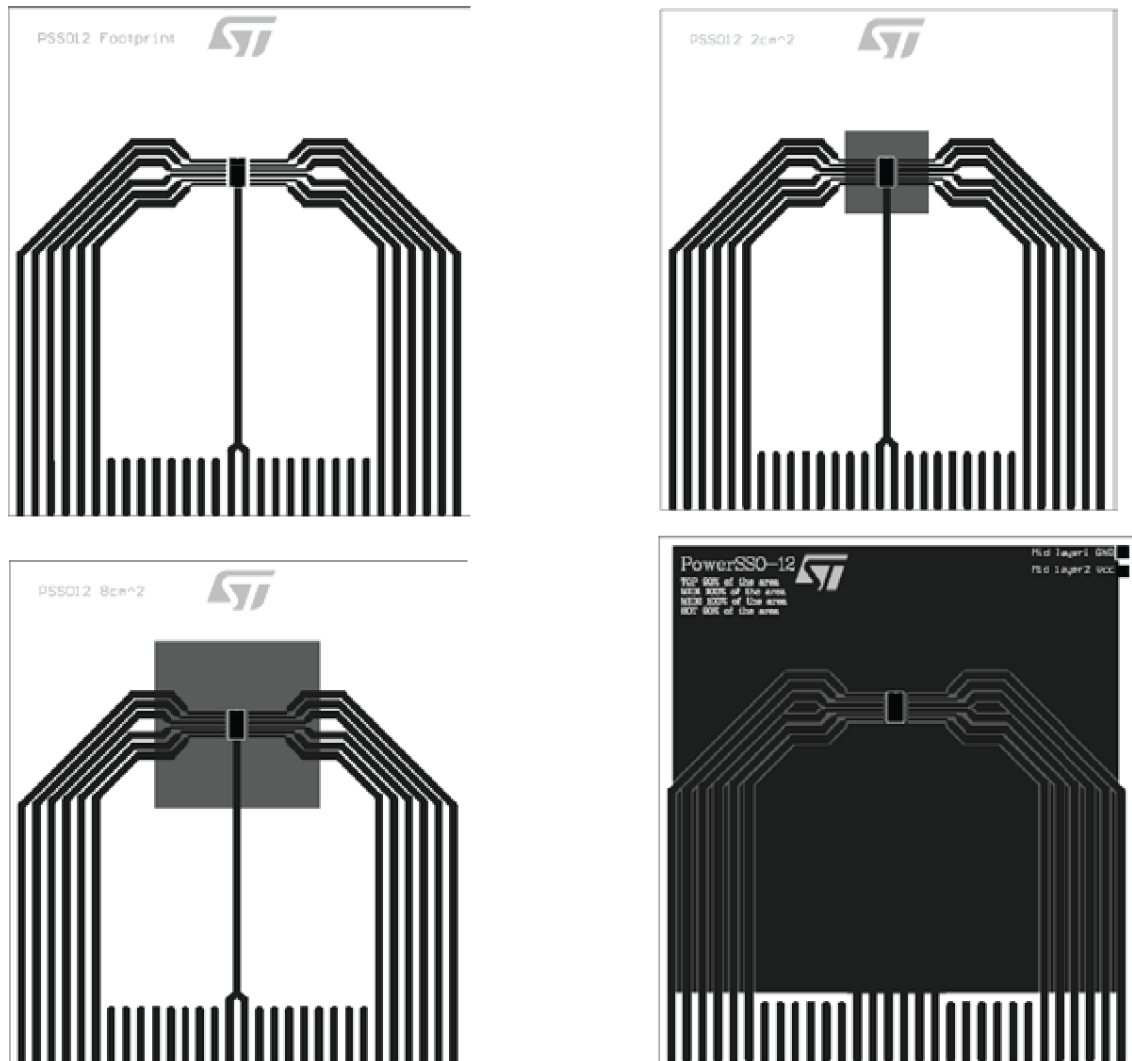
Figure 43. Typical application



6 Package and PCB thermal data

6.1 PowerSSO-12 Thermal data

Figure 44. PowerSSO-12 PC board



Note: layout condition of Rth and Zth measurements (PCB: Double layer and Four layers, Thermal Vias, FR4 area= 77 mm x 86 mm, PCB thickness=1.6 mm, Cu thickness=0.070 mm (front and back side), Cu thickness 0.035 mm (inner layers). Thermal vias separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm, Footprint dimension 2.2 mm x 2.9 mm.

Figure 45. Rthj-amb vs PCB copper area in open box free air condition (PowerSSO-12)

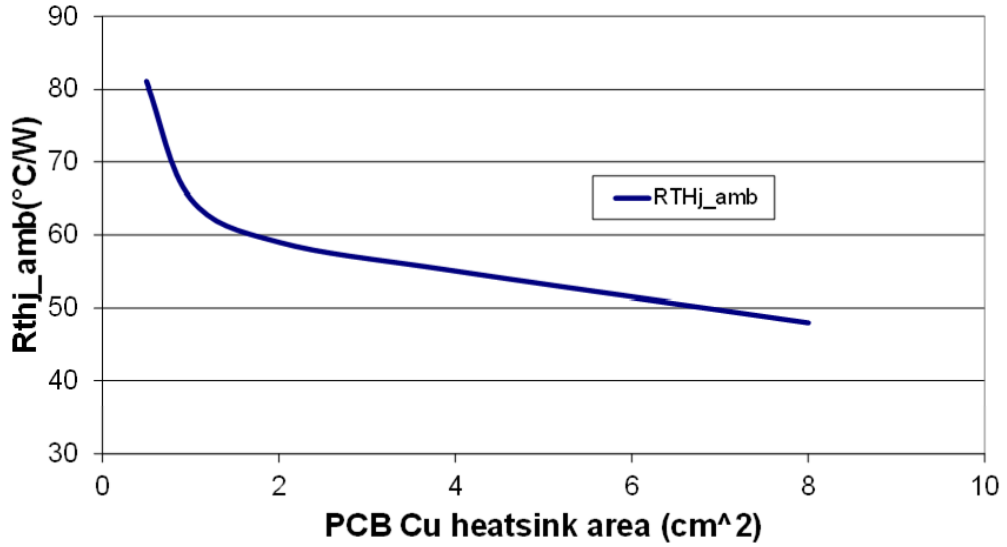
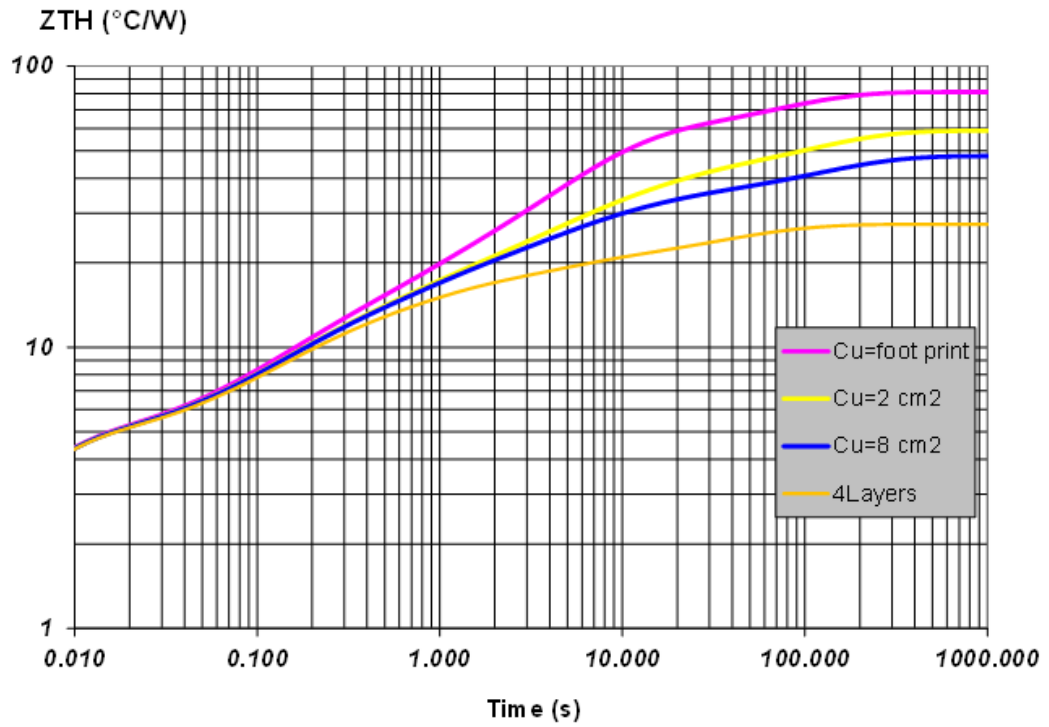


Figure 46. PowerSSO-12 thermal impedance junction ambient single pulse



Pulse calculation:

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$$

where $\delta = tp/T$

Figure 47. Thermal fitting model of a Vreg in PowerSSO-12

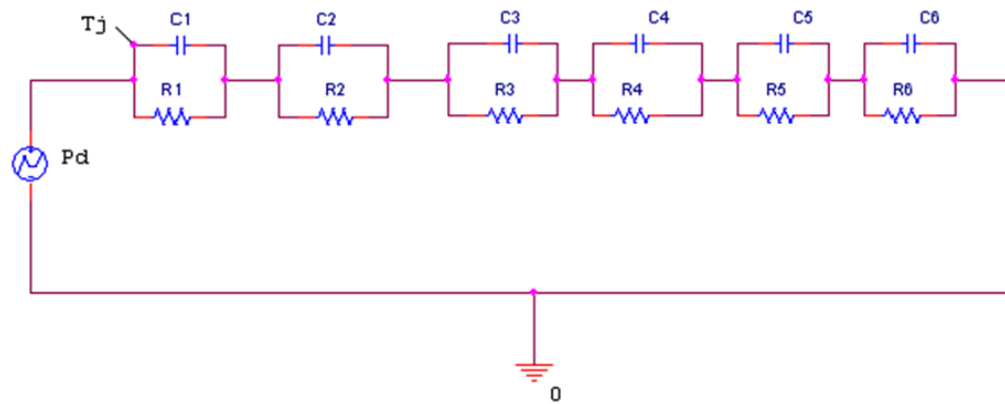
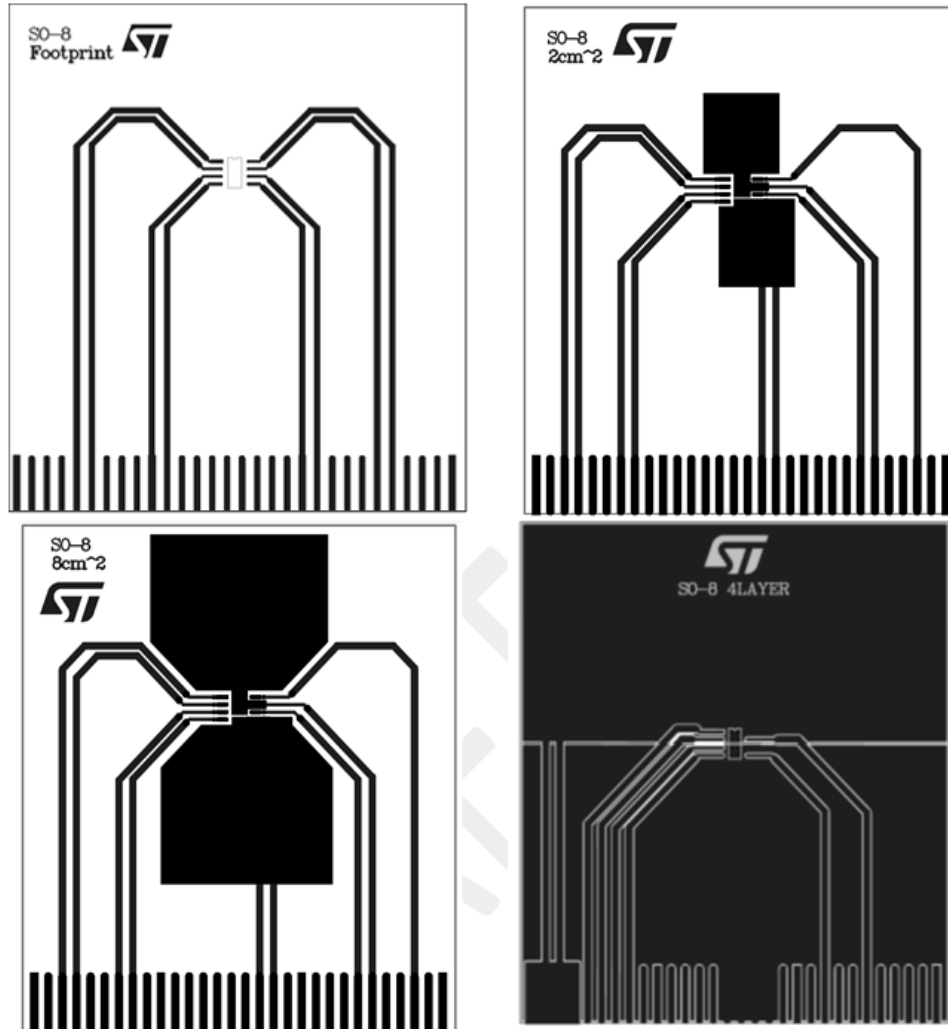


Table 16. PowerSSO-12 thermal parameter

Area/island (cm ²)	Footprint	2	8	4L
R1 (°C/W)	4.4			
R2 (°C/W)	4.5			
R3 (°C/W)	6			
R4 (°C/W)	18	9	8	4.5
R5 (°C/W)	22	15	10	4
R6 (°C/W)	26	20	15	4
C1 (W.s/°C)	0.001			
C2 (W.s/°C)	0.03			
C3 (W.s/°C)	0.1			
C4 (W.s/°C)	0.4	0.4	0.4	0.8
C5 (W.s/°C)	0.27	0.8	1	7
C6 (W.s/°C)	3	6	9	15

6.2 SO-8 thermal data

Figure 48. SO-8 PC board



Note: *Layout condition of Rth and Zth measurements (PCB: double layer and four layers; FR4 area = 77 mm x 86 mm; PCB thickness = 1.6 mm; Cu thickness = 0.070 mm (front and back side), Cu thickness 0.035mm (inner layers); Thermal via separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias of 0.025 mm, Footprint dimension 2.2 mm x 2.9 mm.*

Figure 49. Rthj-amb vs PCB copper area in open box free air condition

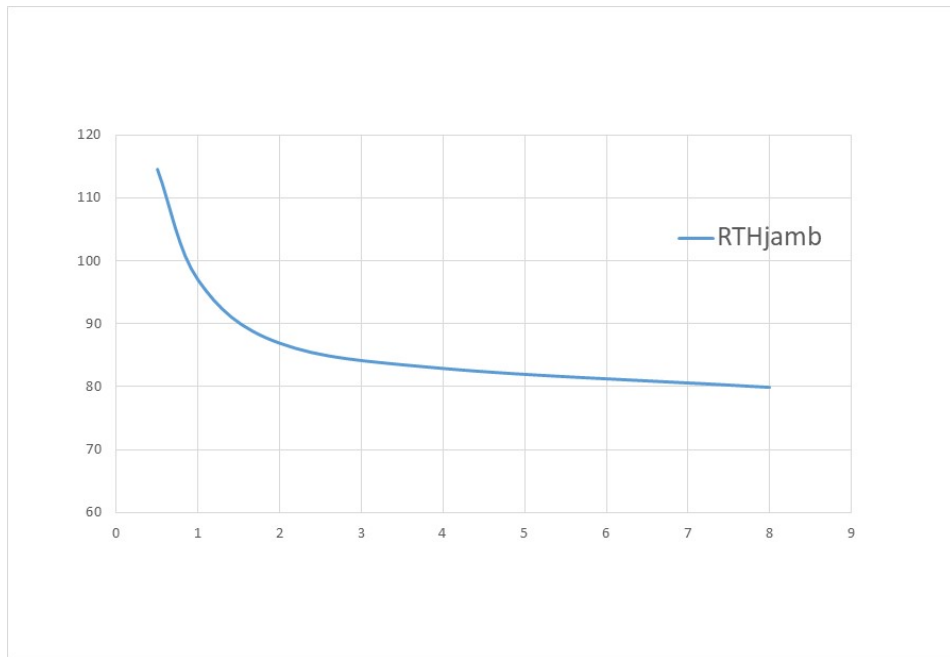
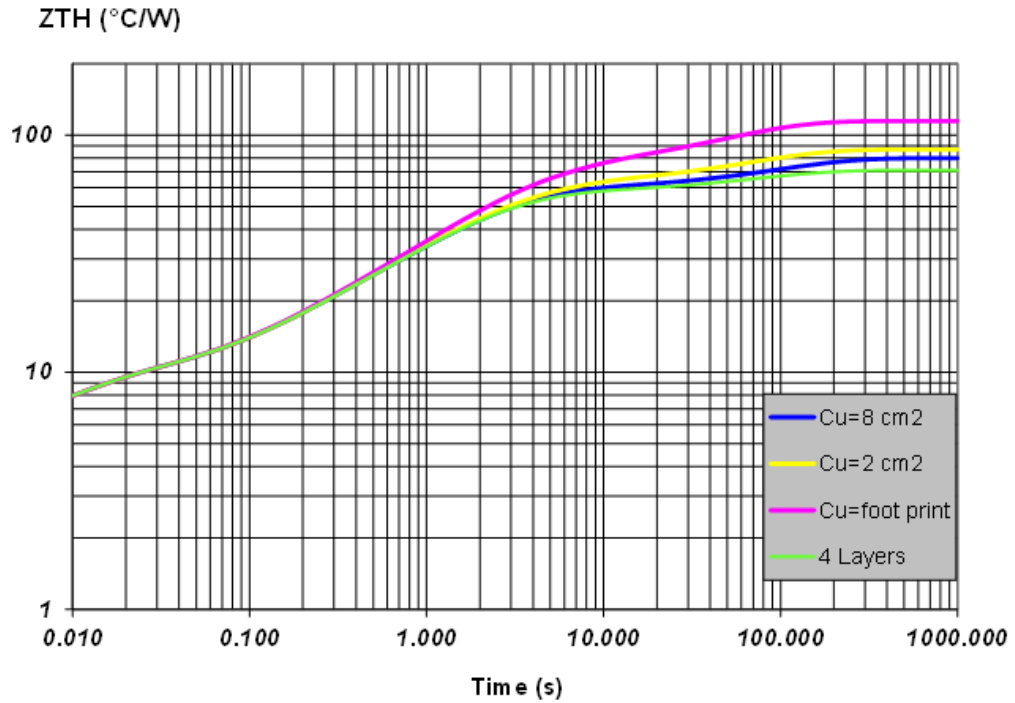


Figure 50. SO-8 thermal impedance junction ambient single pulse



Pulse calculation formula:

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$$

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$$

where $\delta = tp/T$

Figure 51. Thermal fitting model of a Vreg in SO-8

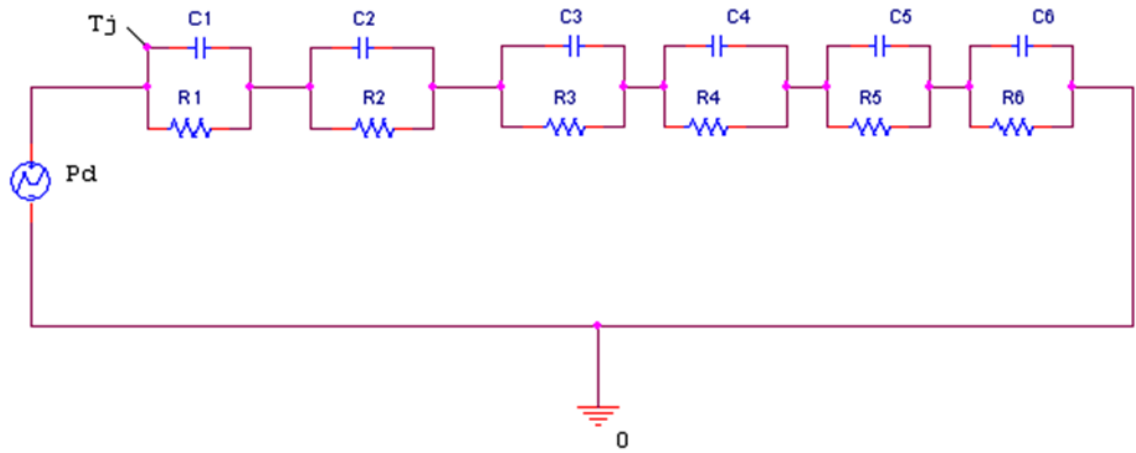


Table 17. SO-8 thermal parameter

Area/island (cm ²)	Footprint	2	8	4L
R1 (°C/W)	4.4			
R2 (°C/W)	4.5			
R3 (°C/W)	6			
R4 (°C/W)	28	23	23	23
R5 (°C/W)	30	24	21	19
R6 (°C/W)	41.6	25	21	14
C1 (W.s/°C)	0.0001			
C2 (W.s/°C)	0.002			
C3 (W.s/°C)	0.03			
C4 (W.s/°C)	0.05			
C5 (W.s/°C)	0.15			
C6 (W.s/°C)	1.4	3	5	5.5

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 PowerSSO-12 package information

Figure 52. PowerSSO-12 package dimensions

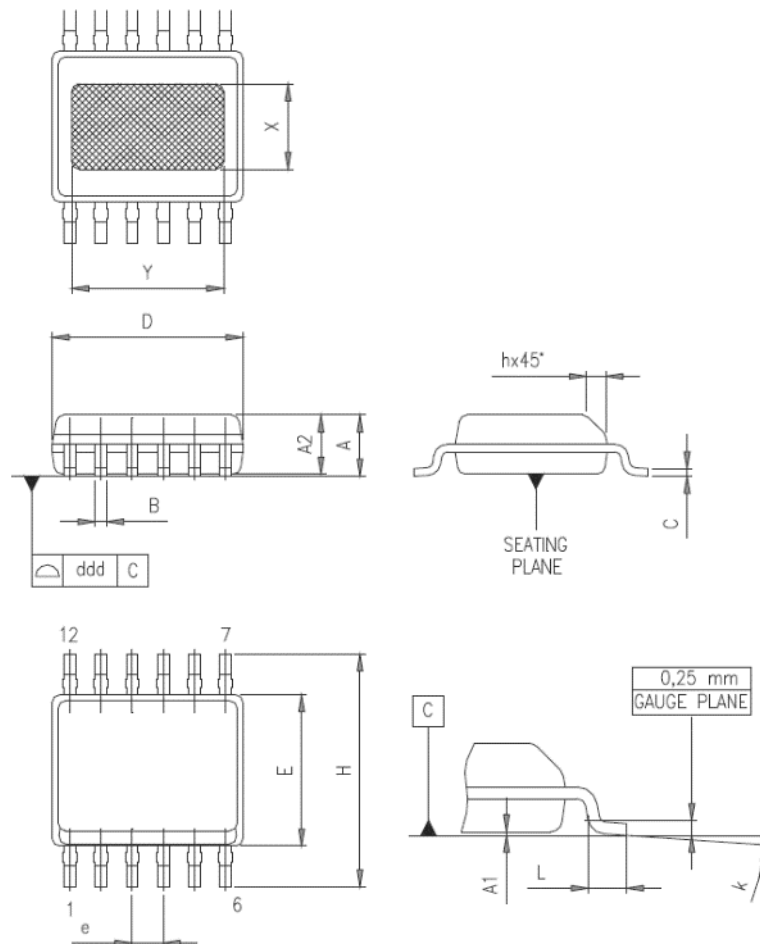


Table 18. PowerSSO-12 package mechanical data

Symbol	Millimeters		
	Min	Typ.	Max
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
b	0.230		0.410
c	0.190		0.250
D	4.800		5.000

Symbol	Millimeters		
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	2.200		2.800
Y	2.900		3.500
ddd			0.100

7.2 SO-8 package information

Figure 53. SO-8 package dimension

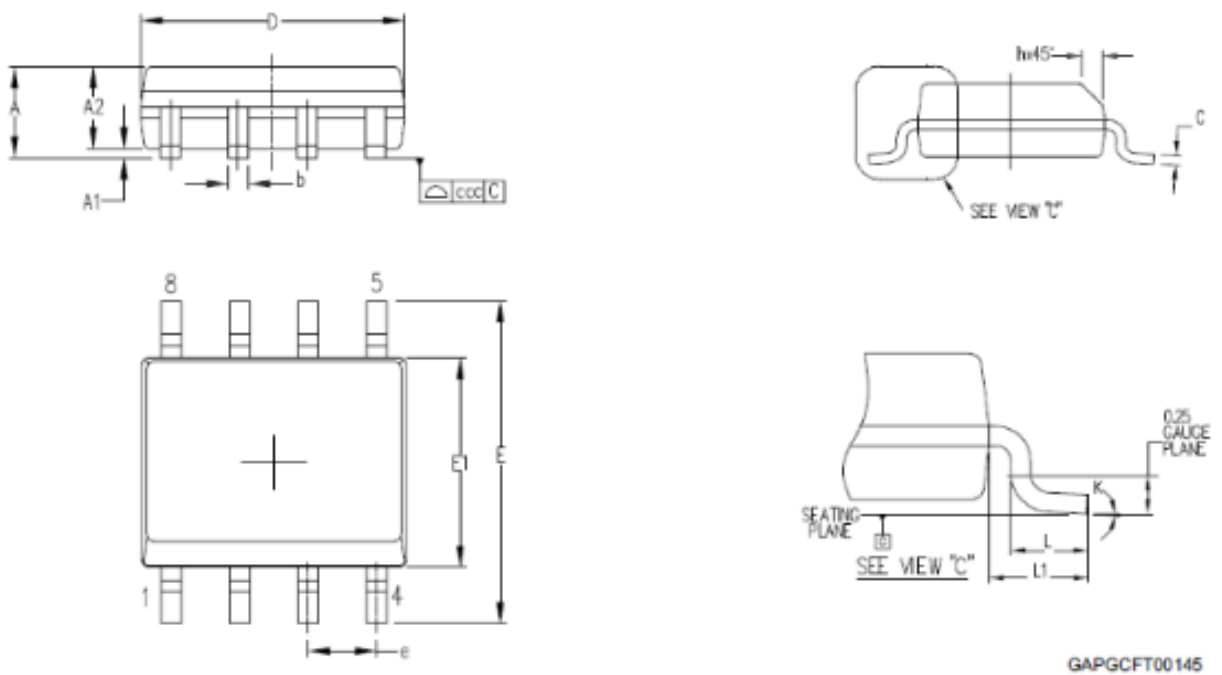
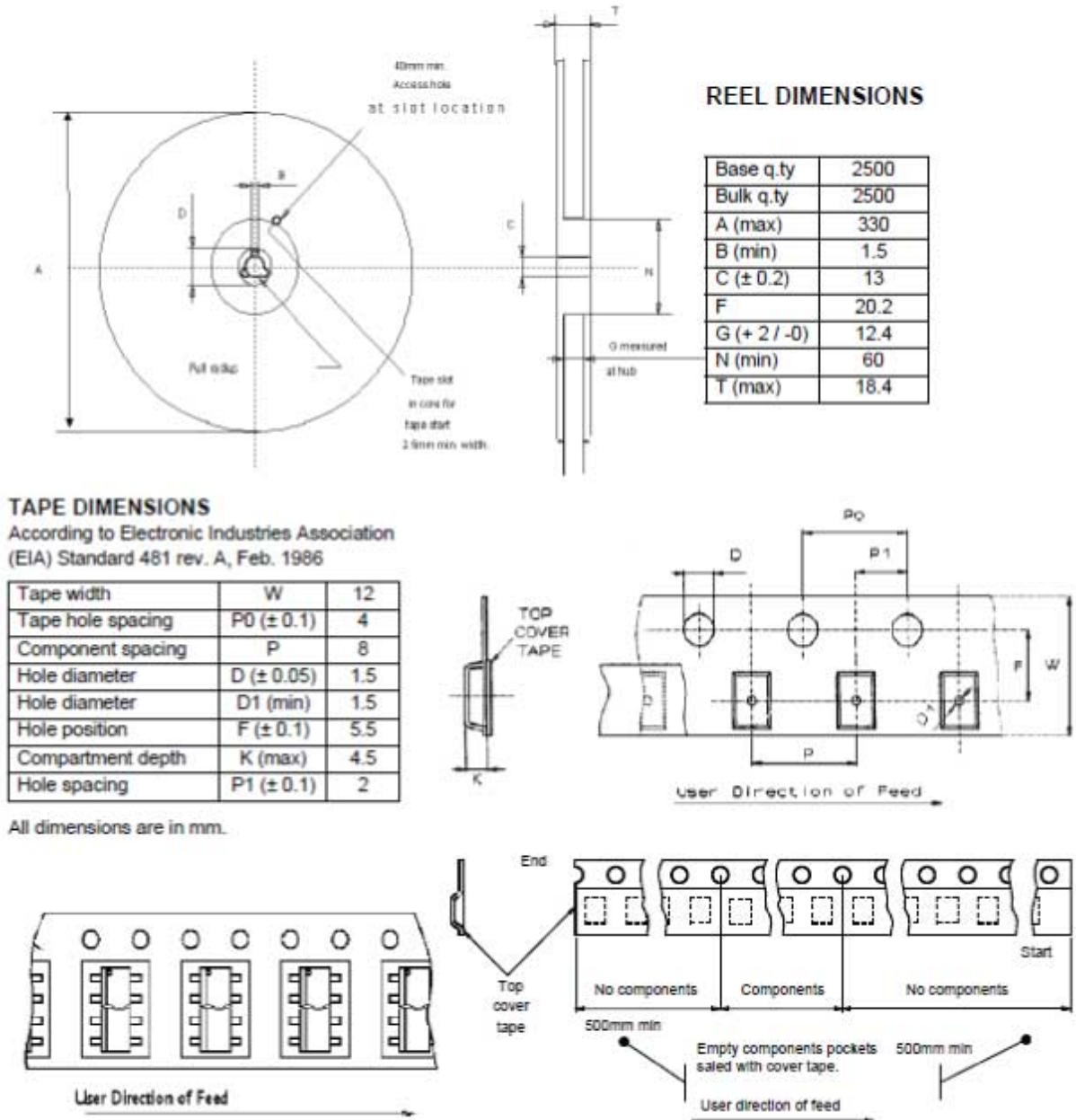


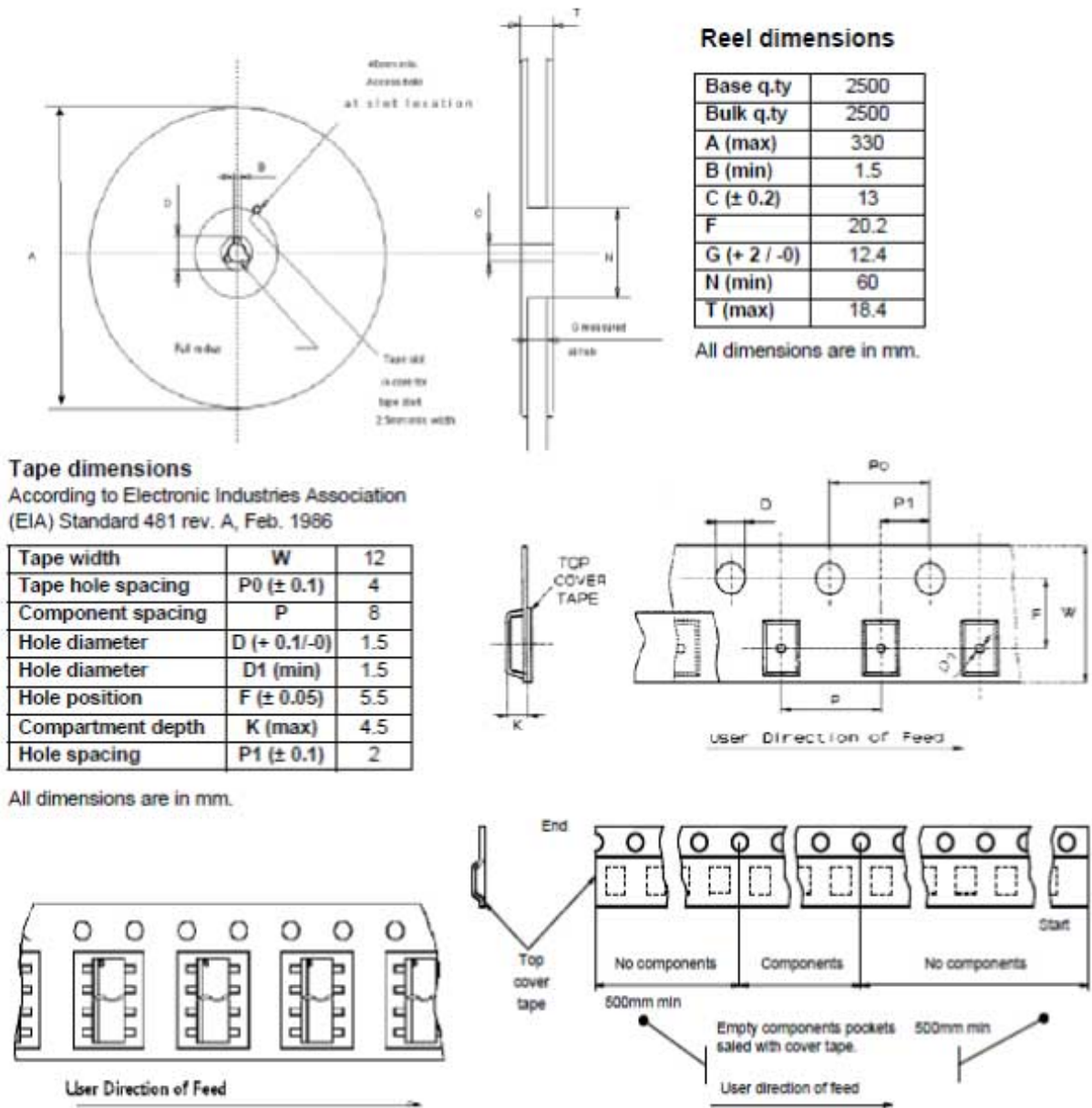
Table 19. SO-8 package mechanical data

Symbol	Millimeters		
	Min	Typ.	Max
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D ⁽¹⁾	4.80	4.90	5.00
E	5.80	6.00	6.20

Symbol	Millimeters		
E1 ⁽²⁾	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

7.3 PowerSSO-12 packaging information
Figure 54. PowerSSO-12 tape and reel shipment (suffix "TR")


7.4 SO-8 packaging information
Figure 55. SO-8 tape and reel shipment (suffix "TR")


8 Order codes

Order codes					
Order code			L99VR01		
Package	Tape & reel		SO-8	L99VR01STR	
			PowerSSO-12	L99VR01JTR	
P/N	Enable	Reset	Autonomous watchdog	Advanced thermal warning	Ishort CTRL
L99VR01STR	X	X	-	-	-
L99VR01JTR	X	X	X	X	X

Revision history

Table 20. Document revision history

Date	Version	Changes
02-Mar-2021	1	Initial release
13-Apr-2021	2	Updated Table 11. Thermal warning and protection (only for L99VR01J) ; Section 2.4 Electrical characteristics curves.

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