4.2 Primary PHY Registers

The primary PHY registers are accessed via the SMI bus. An index is used to access individual primary registers. Primary PHY register indexes are shown in Table 4-2, "PHY Control and Status Registers". Additional read-only advanced registers are indirectly accessible via the Advanced Register Address Port and Advanced Register Read Data Port. Section 4.3, "Advanced PHY Registers," on page 53 provides detailed information regarding the advanced registers.

Note 1: All unlisted register index values are not supported and should not be addressed.

2: The NASR (Not Affected by Software Reset) designation is only applicable when the PHY Soft Reset (RESET) bit of the Basic Control Register is set.

TABLE 4-2: PHY CONTROL AND STATUS REGISTERS

Index (In Decimal)	Register Name
0	Basic Control Register
1	Basic Status Register
2	PHY Identifier 1 Register
3	PHY Identifier 2 Register
4	Auto Negotiation Advertisement Register
5	Auto Negotiation Link Partner Ability Register
6	Auto Negotiation Expansion Register
7	Auto Negotiation Next Page TX Register
8	Auto Negotiation Next Page RX Register
9	Master/Slave Control Register
10	Master/Slave Status Register
15	Extended Status Register
16	Link Control Register
17	10/100 Mode Control/Status Register
18	10/100 Special Modes Register
19	Extended Mode Control/Status Register
20	Advanced Register Address Port
21	Advanced Register Read Data Port
27	Control / Status Indications Register
29	Interrupt Source Flags Register
30	Interrupt Mask Register
31	PHY Special Control / Status Register

4.2.1 BASIC CONTROL REGISTER

Index (In Decimal): 0 Size: 16 bits

Bits	Description	Type	Default
15	**PHY Soft Reset (RESET)** 1 = PHY software reset. This bit is self-clearing. When setting this bit, do not set other bits in this register. The configuration is set from the register bit values as described in Section 3.6.2, "Software Reset," on page 22. **Note:** The PHY will be in the normal mode after a PHY software reset.	R/W SC	0b
14	**Loopback** 0 = normal operation 1 = loopback mode	R/W	0b
13	**Speed Select[0]** Together with Speed Select[1], sets speed per the following table: [Speed Select1][Speed Select 0] 00 = 10Mbps 01 = 100Mbps 10 = 1000Mbps 11 = Reserved **Note:** Ignored if the Auto-Negotiation Enable bit of this register is 1.	R/W	Note 4-1
12	**Auto-Negotiation Enable** 0 = disable auto-negotiate process 1 = enable auto-negotiate process (overrides the Speed Select[0], Speed Select[1], and Duplex Mode bits of this register)	R/W	Note 4-1
11	**Power Down** 0 = normal operation 1 = General power down mode **Note:** Auto-Negotiation Enable must be cleared before setting this bit.	R/W	0b
10	**Isolate** 0 = normal operation 1 = electrical isolation of PHY from RGMII	R/W	0b
9	**Restart Auto-Negotiate** 0 = normal operation 1 = restart auto-negotiate process **Note:** Bit is self-clearing.	R/W SC	0b
8	**Duplex Mode** 0 = half duplex 1 = full duplex **Note:** Ignored if the Auto-Negotiation Enable bit of this register is 1.	R/W	Note 4-1
7	**RESERVED**	RO	-
6	**Speed Select[1]** See description for Speed Select[0] for details.	RO	Note 4-1
5:0	**RESERVED**	RO	-

Note 4-1 The default is determined by the CONFIG[3:2] pins as described in Section 3.8.1.2.3, "Configuration Bits Impacted by the Mode of Operation," on page 26“

4.2.2 BASIC STATUS REGISTER

Index (In Decimal): 1 Size: 16 bits

Bits	Description	Type	Default
15	**100BASE-T4** 0 = no T4 ability 1 = T4 able	RO	0b
14	**100BASE-TX Full Duplex** 0 = no TX full duplex ability 1 = TX with full duplex	RO	1b
13	**100BASE-TX Half Duplex** 0 = no TX half duplex ability 1 = TX with half duplex	RO	1b
12	**10BASE-T Full Duplex** 0 = no 10Mbps with full duplex ability 1 = 10Mbps with full duplex	RO	1b
11	**10BASE-T Half Duplex** 0 = no 10Mbps with half duplex ability 1 = 10Mbps with half duplex	RO	1b
10	**100BASE-T2 Full Duplex** 0 = PHY not able to perform full duplex 100BASE-T2 1 = PHY able to perform full duplex 100BASE-T2	RO	0b
9	**100BASE-T2 Half Duplex** 0 = PHY not able to perform half duplex 100BASE-T2 1 = PHY able to perform half duplex 100BASE-T2	RO	0b
8	**Extended Status** 0 = no extended status information in register 15 1 = extended status information in register 15	RO	1b
7:6	**RESERVED**	RO	-
5	**Auto-Negotiate Complete** 0 = auto-negotiate process not completed 1 = auto-negotiate process completed	RO	0b
4	**Remote Fault** 0 = no remote fault 1 = remote fault condition detected	RO/LH	0b
3	**Auto-Negotiate Ability** 0 = unable to perform auto-negotiation function 1 = able to perform auto-negotiation function	RO	1b
2	**Link Status** 0 = link is down 1 = link is up	RO/LL	0b
1	**Jabber Detect** 0 = no jabber condition detected 1 = jabber condition detected	RO/LH	0b
0	**Extended Capabilities** 0 = does not support extended capabilities registers 1 = supports extended capabilities registers	RO	1b

4.2.3 PHY IDENTIFIER 1 REGISTER

Index (In Decimal): 2 Size: 16 bits

Bits	Description	Type	Default
15:0	**PHY ID Number** Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively. OUI=00800Fh	R/W	0007h

4.2.4 PHY IDENTIFIER 2 REGISTER

Index (In Decimal): 3 Size: 16 bits

Bits	Description	Type	Default
15:10	**PHY ID Number** Assigned to the 19th through 24th bits of the OUI.	R/W	C0h
9:4	**Model Number** Six-bit manufacturer's model number.	R/W	0Eh
3:0	**Revision Number** Four-bit manufacturer's revision number.	R/W	Note 4-2

Note 4-2 The default value of this field will vary dependent on the silicon revision number.

4.2.5 AUTO NEGOTIATION ADVERTISEMENT REGISTER

Index (In Decimal): 4 Size: 16 bits

Bits	Description	Type	Default
15	**Next Page** 0 = no next page ability 1 = next page capable **Note:** This device does not support next page ability.	R/W	0b
14	**RESERVED**	RO	-
13	**Remote Fault** 0 = no remote fault 1 = remote fault detected	R/W	0b
12	**RESERVED**	RO	-

Bits	Description	Type	Default
11	**Asymmetric Pause** 0 = Asymmetrical pause direction is not supported by MAC 1 = Asymmetrical pause direction is supported by MAC	R/W	0b
10	**Pause Operation (PAUSE)** 0 = Pause operation is not supported by MAC 1 = Pause operation is supported by MAC	R/W	Note 4-3
9	**RESERVED**	RO	-
8	**100BASE-TX Full Duplex** 0 = no TX full duplex ability 1 = TX with full duplex	R/W	Note 4-4
7	**100BASE-TX** 0 = no TX ability 1 = TX able	R/W	Note 4-4
6	**10BASE-T Full Duplex** 0 = no 10Mbps with full duplex ability 1 = 10Mbps with full duplex	R/W	Note 4-4
5	**10BASE-T** 0 = no 10Mbps ability 1 = 10Mbps able	R/W	Note 4-4
4:0	**Selector Field** 00001 = IEEE 802.3	R/W	00001b

Note 4-3 The default is determined by the CONFIG1 pin as described in Section 3.8.1.2.1, "Configuring the SMI Address (CONFIG[1:0])," on page 25

Note 4-4 The default is determined by the CONFIG[3:2] pins as described in Section 3.8.1.2.3, "Configuration Bits Impacted by the Mode of Operation," on page 26.

4.2.6 AUTO NEGOTIATION LINK PARTNER ABILITY REGISTER

Index (In Decimal): 5 Size: 16 bits

Bits	Description	Type	Default
15	**Next Page** 0 = no next page ability 1 = next page capable	RO	0b
14	**Acknowledge** 0 = link code word not yet received 1 = link code word received from partner	RO	0b
13	**Remote Fault** 0 = no remote fault 1 = remote fault detected	RO	0b
12:11	**RESERVED**	RO	-
10	**Pause Operation (PAUSE)** 0 = Pause Operation is not supported by remote MAC 1 = Pause Operation is supported by remote MAC	RO	0b

Bits	Description	Type	Default
9	**100BASE-T4** 0 = no T4 ability 1 = T4 able **Note:** This PHY does not support T4 ability.	RO	0b
8	**100BASE-TX Full Duplex** 0 = no TX full duplex ability 1 = TX with full duplex	RO	0b
7	**100BASE-TX** 0 = no TX ability 1 = TX able	RO	0b
6	**10BASE-T Full Duplex** 0 = no 10Mbps with full duplex ability 1 = 10Mbps with full duplex	RO	0b
5	**10BASE-T** 0 = no 10Mbps ability 1 = 10Mbps able	RO	0b
4:0	**Selector Field** 00001 = IEEE 802.3	RO	00001b

4.2.7 AUTO NEGOTIATION EXPANSION REGISTER

Index (In Decimal): 6 Size: 16 bits

Bits	Description	Type	Default
15:5	**RESERVED**	RO	-
4	**Parallel Detection Fault** 0 = no fault detected by parallel detection logic 1 = fault detected by parallel detection logic	RO/LH	0b
3	**Link Partner Next Page Able** 0 = link partner does not have next page ability 1 = link partner has next page ability	RO	0b
2	**Next Page Able** 0 = local device does not have next page ability 1 = local device has next page ability	RO	0b
1	**Page Received** 0 = new page not yet received 1 = new page received	RO/LH	0b
0	**Link Partner Auto-Negotiation Able** 0 = link partner does not have auto-negotiation ability 1 = link partner has auto-negotiation ability	RO	0b

4.2.8 AUTO NEGOTIATION NEXT PAGE TX REGISTER

Index (In Decimal): 7 Size: 16 bits

Bits	Description	Type	Default
15	**Next Page** 0 = no next page ability 1 = next page capable	R/W	0b
14	**RESERVED**	RO	-
13	**Message Page** 0 = unformatted page 1 = message page	R/W	1b
12	**Acknowledge 2** 0 = device cannot comply with message 1 = device will comply with message	R/W	0b
11	**Toggle** 0 = previous value was HIGH 1 = previous value was LOW	RO	0b
10:0	**Message Code** Message/Unformatted Code Field	RW	00 0000 0001b

4.2.9 AUTO NEGOTIATION NEXT PAGE RX REGISTER

Index (In Decimal): 8 Size: 16 bits

Bits	Description	Type	Default
15	**Next Page** 0 = no next page ability 1 = next page capable	RO	0b
14	**Acknowledge** 0 = Link code word not yet received from partner 1 = Link code word received from partner	RO	0b
13	**Message Page** 0 = unformatted page 1 = message page	RO	1b
12	**Acknowledge 2** 0 = device cannot comply with message 1 = device will comply with message	RO	0b
11	**Toggle** 0 = previous value was HIGH 1 = previous value was LOW	RO	0b
10:0	**Message Code** Message/Unformatted Code Field	RO	000 0000 0000b