

### PROTECTION PRODUCTS

#### Description

The LC05-6 has been specifically designed to protect sensitive components which are connected to high-speed telecommunications lines from over voltages caused by **lightning**, electrostatic discharge (**ESD**), and electrical fast transients (**EFT**).

The device is in a JEDEC SO-16 NB package. It is designed to provide metallic surge protection for two tip and ring line pairs. The low capacitance topology means signal integrity is preserved on high-speed lines. The high surge capability (2000W,  $t_p=8/20\mu s$ ) makes the LC05-6 suitable for telecommunications systems operating in harsh transient environments.

The LC05-6 is designed to meet the lightning surge requirements of Bellcore GR-1089 (intra-building), ITU K.20, and IEC 61000-4-5. The features of the LC05-6 are ideal for protecting T1/E1 transceivers in WAN applications.

#### Features

- ◆ Transient protection for high-speed data lines to **Bellcore GR 1089  $I_{pp}=100A$  (2/10 $\mu s$ )**  
**ITU K.20  $I_{pp}=40A$  (5/310 $\mu s$ )**  
**IEC 61000-4-2 (ESD) >25kV**  
**IEC 61000-4-4 (EFT) 40A (5/50ns)**  
**IEC 61000-4-5 (Lightning) 100A (8/20 $\mu s$ )**
- ◆ Protects two tip and ring line pairs
- ◆ Low capacitance for high-speed interfaces
- ◆ High surge capability
- ◆ Low clamping voltage
- ◆ Solid-state silicon avalanche technology

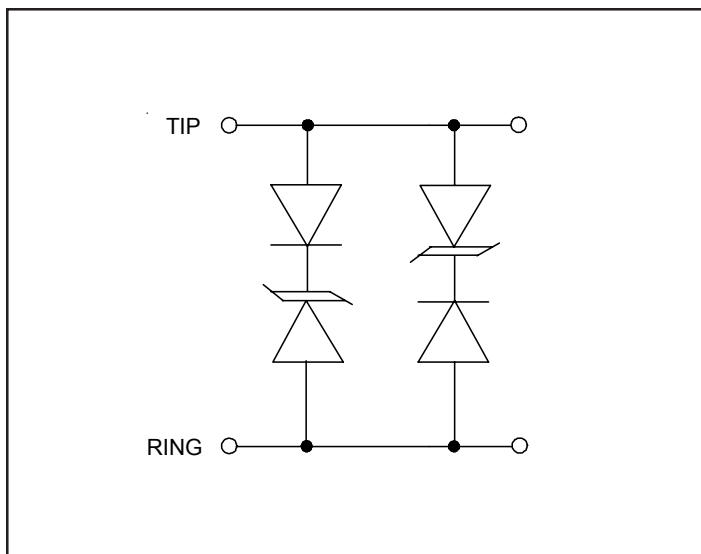
#### Mechanical Characteristics

- ◆ JEDEC SO-16 package
- ◆ RoHS/WEEE Compliant
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking : Part number, date code, logo
- ◆ Packaging : Tube or Tape and Reel per EIA 481

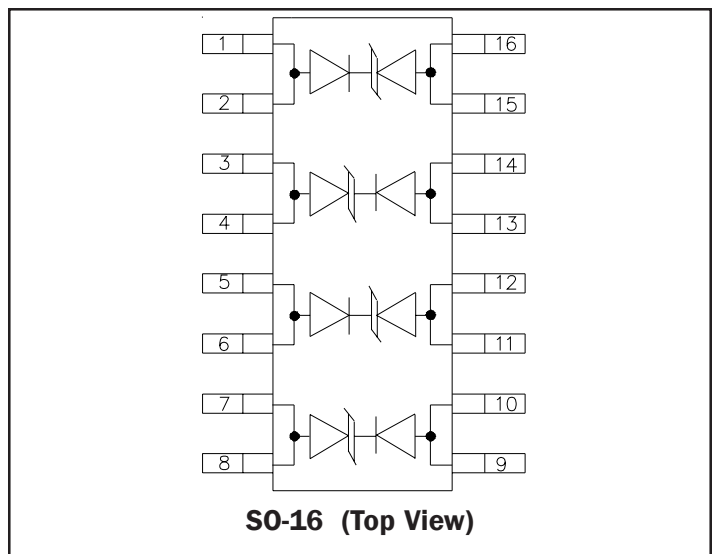
#### Applications

- ◆ T1/E1 Line Cards
- ◆ Base Stations
- ◆ WAN Equipment
- ◆ CSU/DSU
- ◆ Multiplexers
- ◆ Routers
- ◆ ISP Equipment
- ◆ Customer Premise Equipment

#### Circuit Diagram



#### Schematic & PIN Configuration



**PROTECTION PRODUCTS**
**Absolute Maximum Rating**

Rating	Symbol	Value	Units
Peak Pulse Power ( $t_p = 8/20\mu s$ )	$P_{pk}$	2000	Watts
Peak Pulse Current ( $t_p = 8/20\mu s$ )	$I_{pp}$	100	A
Lead Soldering Temperature	$T_L$	260 (10 sec.)	$^{\circ}C$
Operating Temperature	$T_J$	-55 to +125	$^{\circ}C$
Storage Temperature	$T_{STG}$	-55 to +150	$^{\circ}C$

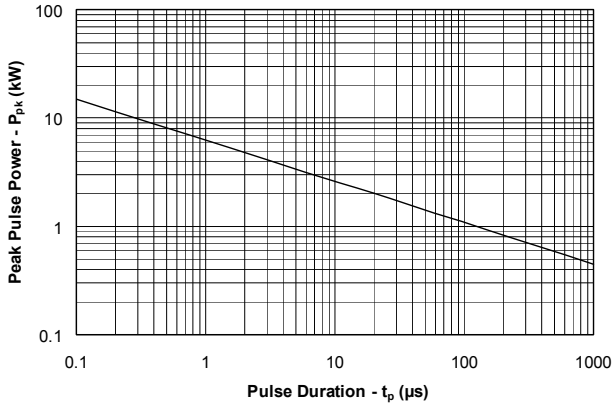
**Electrical Characteristics**

LC05-6						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	$V_{RWM}$				6	V
Reverse Breakdown Voltage	$V_{BR}$	$I_t = 1mA$	6.8			V
Reverse Leakage Current	$I_R$	$V_{RWM} = 6V, T=25^{\circ}C$			15	$\mu A$
		$V_{RWM} = 3V, T=25^{\circ}C$			2	$\mu A$
Clamping Voltage	$V_C$	$I_{pp} = 10A,$ $t_p = 10/1000\mu s$			12.5	V
Clamping Voltage	$V_C$	$I_{pp} = 50A,$ $t_p = 8/20\mu s$			15	V
Clamping Voltage	$V_C$	$I_{pp} = 100A,$ $t_p = 8/20\mu s$			20	V
Junction Capacitance	$C_J$	Each Line $V_R = 0V, f = 1MHz$			15	pF

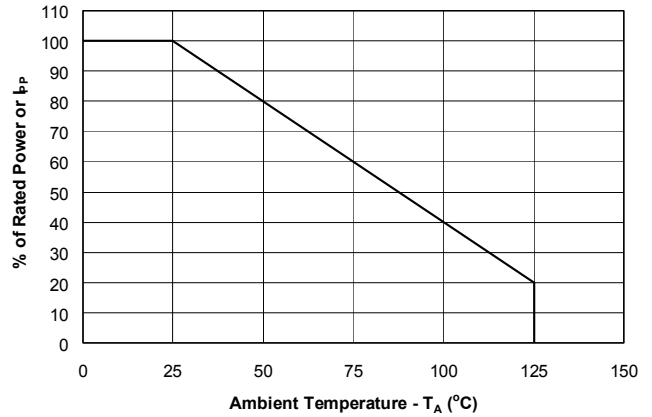
**PROTECTION PRODUCTS**

**Typical Characteristics**

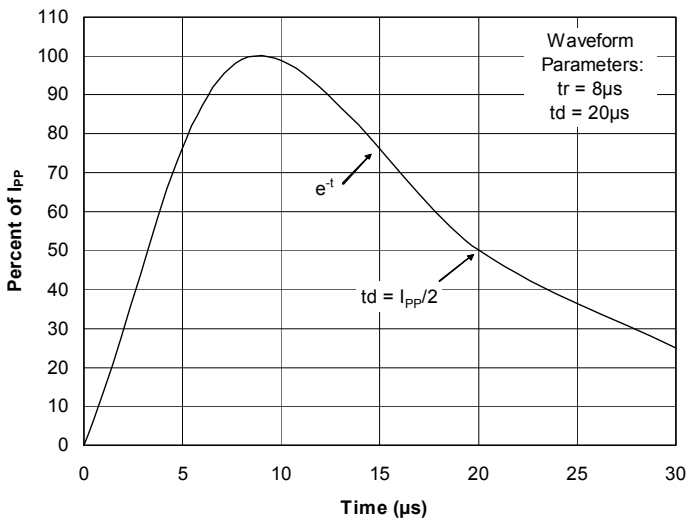
**Non-Repetitive Peak Pulse Power vs. Pulse Time**



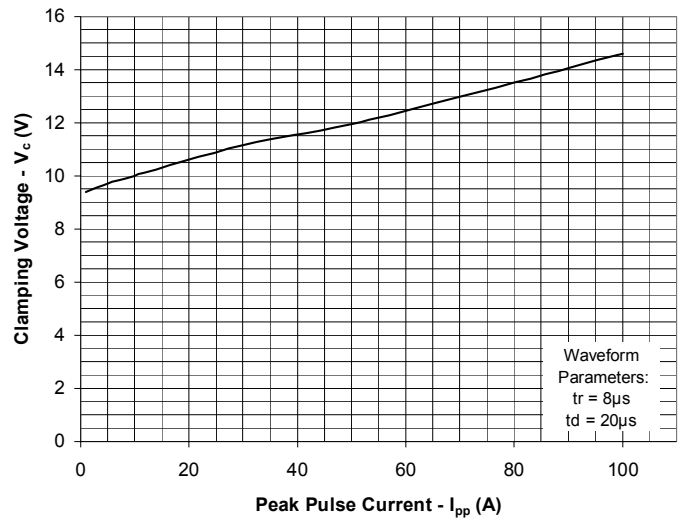
**Power Derating Curve**



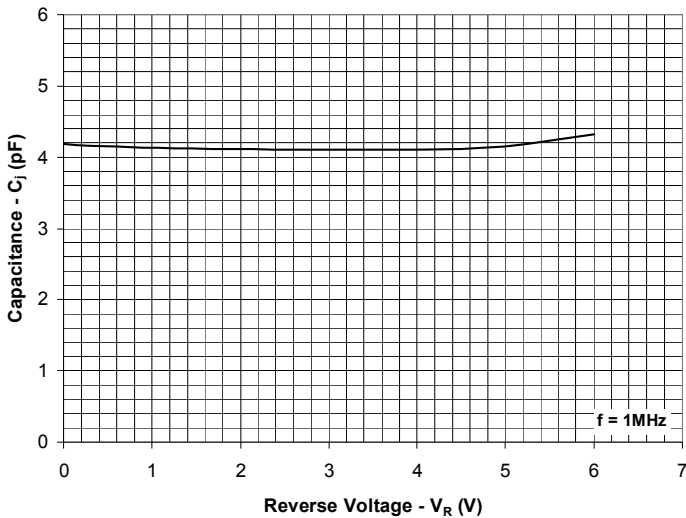
**Pulse Waveform**



**Clamping Voltage vs. Peak Pulse Current**



**Capacitance vs. Reverse Voltage**



**PROTECTION PRODUCTS**

**Applications Information**

**Device Connection Options for Protection of Two High-Speed Line Pairs**

The LC05-6 is designed to protect four high-speed data lines (two differential pairs) from transient over-voltages which result from lightning and ESD. Protection of two line pairs is achieved by connecting the device as follows: Pins 1-4 are connected to line 1 of the first pair (i.e. Tip 1) and pins 13-16 are connected to line 2 of the first pair (i.e. Ring 1). Pins 5-8 are connected to line 1 of the second pair (i.e. Tip 2) and pins 9-12 are connected to line 2 of the second pair (i.e. Ring 2). All pins should be connected for best results. Minimize parasitic inductance in the protection circuit path by keeping the trace length between the protected line and the LC05-6 as short as possible.

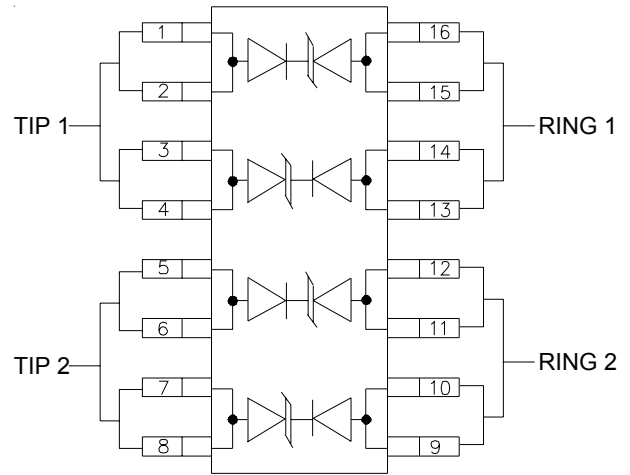
**T1/E1 Linecard Protection**

A typical T1/E1 linecard protection circuit is shown in Figure 2. The LC05-6 is connected between Tip and Ring on the transmit and receive line pairs. It provides protection to metallic (line-to-line) lightning and ESD surges. It is designed to meet the intra-building requirements of Bellcore GR-1089. This design takes advantage of the isolation of the transformer to suppress common mode surges. To complete the protection circuit, the SRDA05-4 (or SRDA3.3-4 for 3.3V supplies) is employed as the IC side protection element. This device helps prevent the transceiver from latching up by providing fine clamping of transients that are coupled through the transformer.

**Matte Tin Lead Finish**

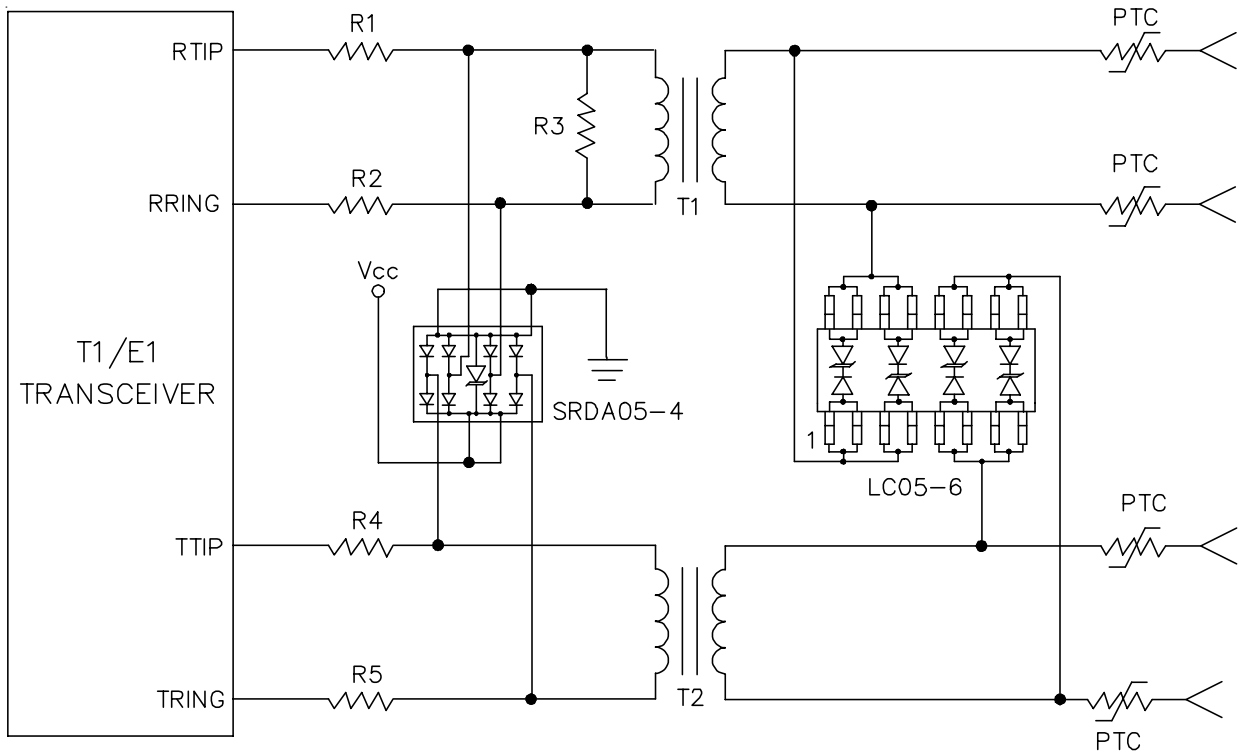
Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

**Figure 1 - Connection for Differential (Line-to-Line) Protection of two Tip/Ring Line Pairs**



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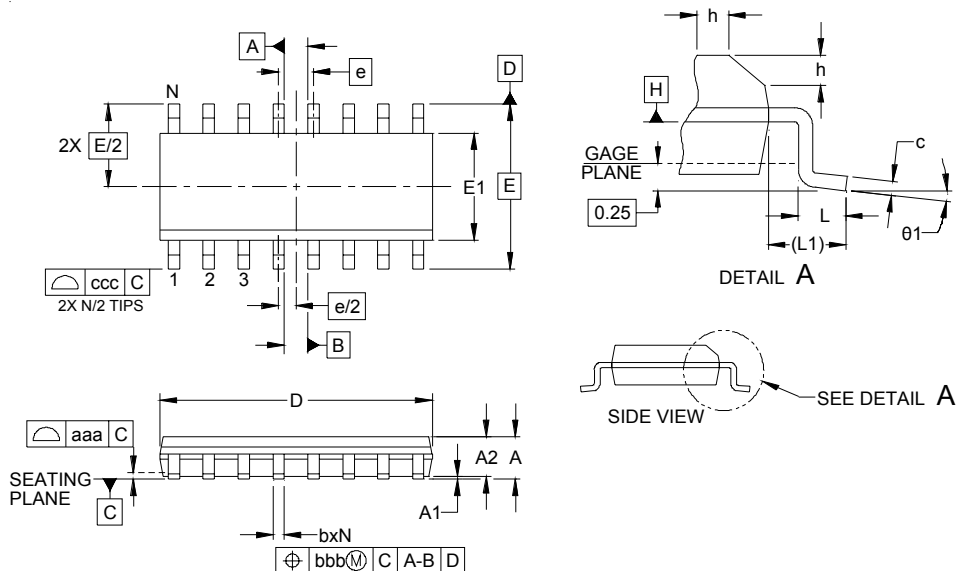
Typical Applications



**Figure 2 - T1/E1 Line Card Protection**

PROTECTION PRODUCTS

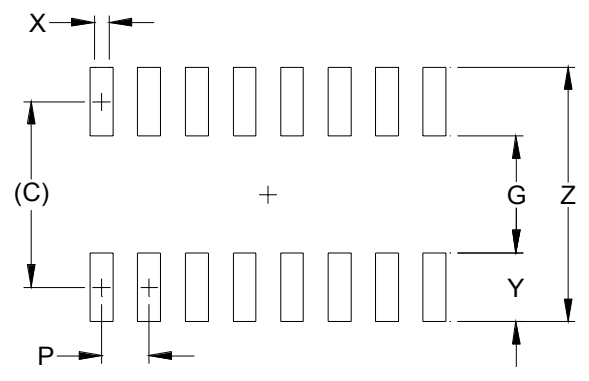
Outline Drawing - S0-16



DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.386	.390	.394	9.80	9.90	10.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	16			16		
theta1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
  2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
  3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
  4. REFERENCE JEDEC STD MS-012, VARIATION AC.

Land Pattern - S0-16



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
  2. REFERENCE IPC-SM-782A, RLP NO. 304A.