LCDA12C-8 and LCDA15C-8
Low Capacitance TVS Diode Array For Multi-mode Transceiver Protection

PROTECTION PRODUCTS

Description

The LCDAxxC-8 has been specifically designed to protect sensitive components which are connected to data and transmission lines from over voltages caused by electrostatic discharge **(ESD)**, electrical fast transients **(EFT)**, and **lightning**.

The low capacitance array configuration of the LCDAxxC-8 allows the user to protect eight high-speed data or I/O lines. They may be used on systems operating from 5 to 15 Volts. The high surge capability (500W, tp=8/20µs) makes the LCDAxxC-8 suitable for telecommunications systems operating in harsh transient environments. The low inductance construction minimizes voltage overshoot during high current surges.

The features of the LCDAxxC-8 are ideal for protecting multi-protocol transceivers in WAN applications such as Frame Relay systems, routers, and switches.

Features

- Transient protection for high-speed data lines to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 0.5kV, 12A (8/20µs)
- Protects eight I/O lines
- Low capacitance for high-speed interfaces
- High surge capability
- Low clamping voltage
- Solid-state silicon avalanche technology

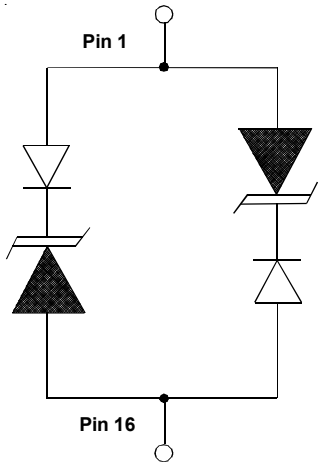
Mechanical Characteristics

- JEDEC SO-16 package
- Molding compound flammability rating: UL 94V-0
- Marking : Part number, date code, logo
- Packaging : Tape and Reel per EIA 481

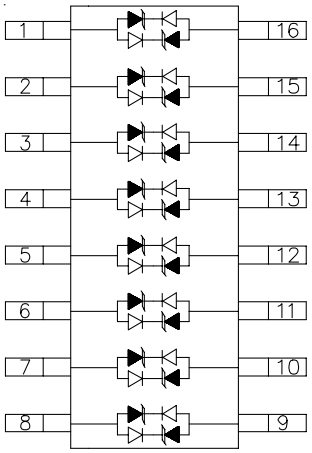
Applications

- Multi-Mode Transceiver Protection
- WAN Equipment:
  - CSU/DSU
  - Multiplexers
  - Routers
  - ISP Equipment
  - Customer Premise Equipment
- Protection for any of the following interfaces:
  - RS-232 (V.28)
  - RS-422 (V.11, X.21)
  - RS-449 (V.11/V.10)

Circuit Diagram



Schematic & PIN Configuration



SO-16 (Top View)

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (t_p = 8/20µs)	P_{pk}	500	Watts
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics

LCDA12C-8

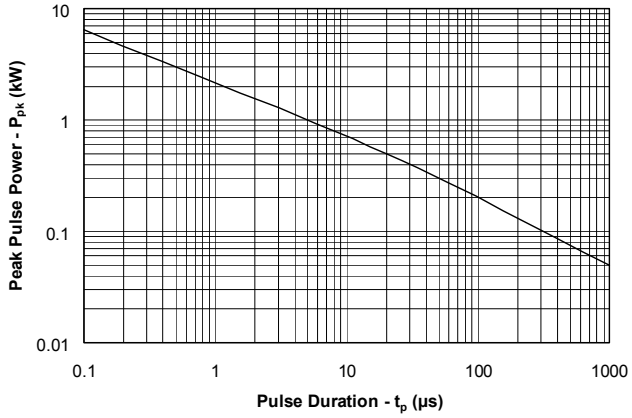
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				12	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	13.3			V
Reverse Leakage Current	I_R	V_{RWM} = 12V, T=25°C			5	µA
Clamping Voltage	V_C	I_{PP} = 5A, t_p = 8/20µs			19	V
Clamping Voltage	V_C	I_{PP} = 20A, t_p = 8/20µs			26.6	V
Peak Pulse Current	I_{PP}	t_p = 8/20µs			20	A
Junction Capacitance	C_j	Between I/O pins and Ground V_R = 0V, f = 1MHz		8	15	pF

LCDA15C-8

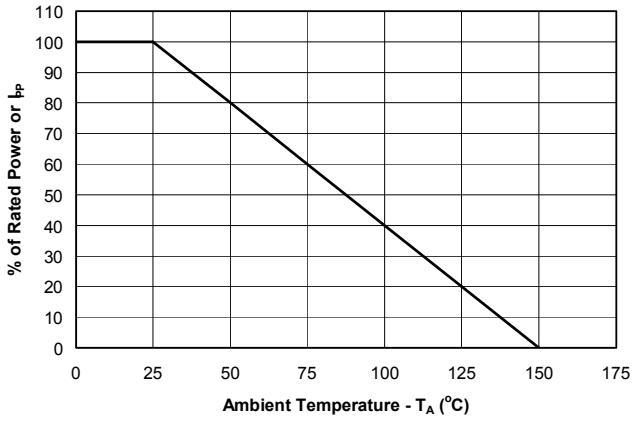
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				15	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	16.7			V
Reverse Leakage Current	I_R	V_{RWM} = 15V, T=25°C			5	µA
Clamping Voltage	V_C	I_{PP} = 1A, t_p = 8/20µs			24	V
Clamping Voltage	V_C	I_{PP} = 15A, t_p = 8/20µs			33	V
Peak Pulse Current	I_{PP}	t_p = 8/20µs			15	A
Junction Capacitance	C_j	Between I/O pins and Ground V_R = 0V, f = 1MHz		8	15	pF

Typical Characteristics

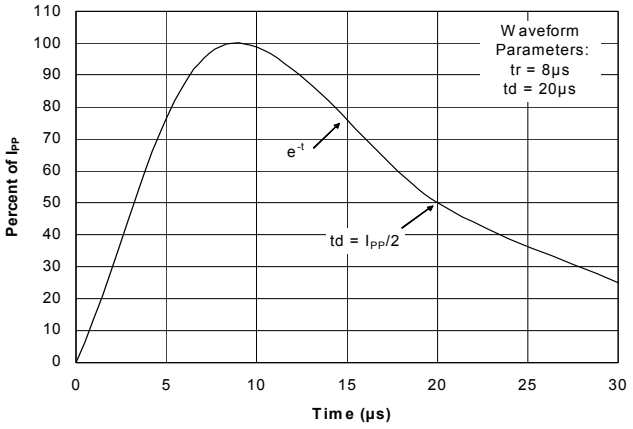
Non-Repetitive Peak Pulse Power vs. Pulse Time



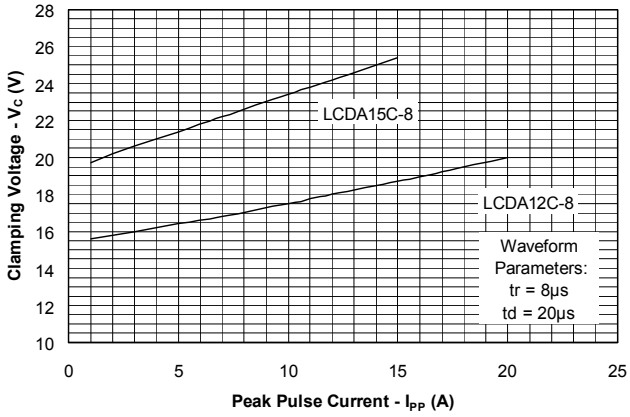
Power Derating Curve



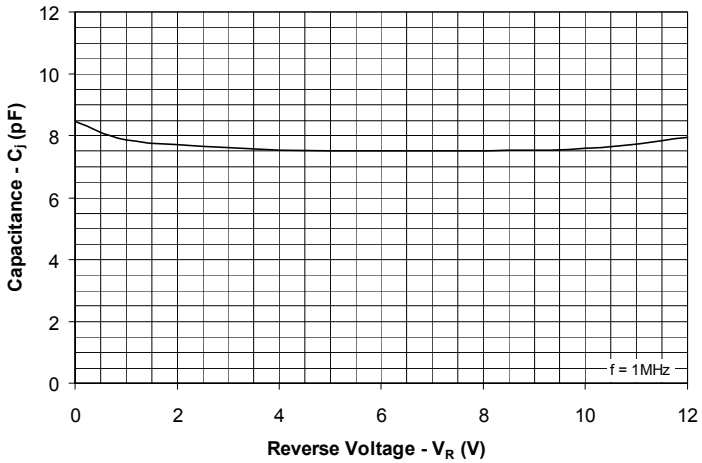
Pulse Waveform



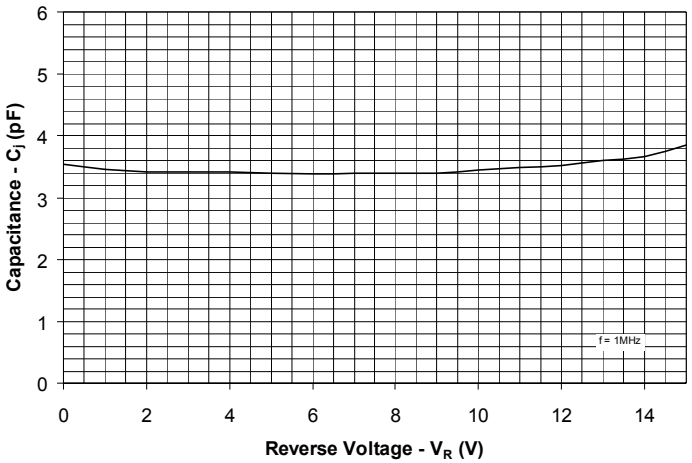
Clamping Voltage vs. Peak Pulse Current



LCDA12C-8 Capacitance vs. Reverse Voltage



LCDA15C-8 Capacitance vs. Reverse Voltage

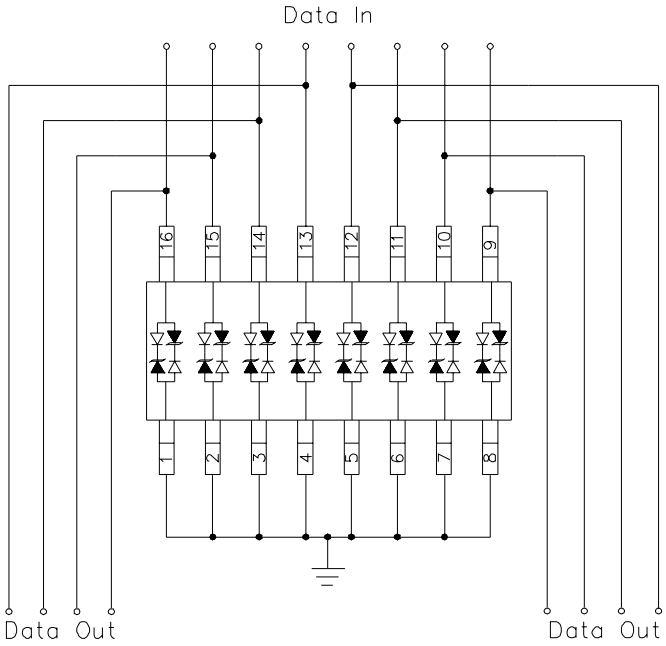


Applications Information

Device Connection Options for Protection of Eight High-Speed Data Lines

The LCDAxxC-8 may be configured to protect up to eight I/O lines operating between 5 and 15V. It may be used to protect the most popular serial data interface standard lines making it ideal for use in equipment utilizing multi-mode transceivers. The LCDAxxC-8 is symmetrical so the data lines may be connected at pins 1-8 or 9-16. Pins 9-16 or 1-8 are connected to ground as shown. For best results, these pins should be connected directly to a ground plane on the board. The path length should be kept as short as possible to minimize parasitic inductance.

Device Connection



Multi-Mode Transceiver Protection

The LCDAxxC-8 may be used to protect multi-mode transceiver I/O lines with external connections. The LCDAxxC-8 adds a maximum loading capacitance of 15pF with a working voltage of 12V or 15V. This allows the transceiver to safely operate in all modes without clipping or degradation of the signal.
With proper design and layout, the transceiver port can be protected to >15kV (HBM per IEC 61000-4-2).

Circuit Board Layout Recommendations for Suppression of ESD.

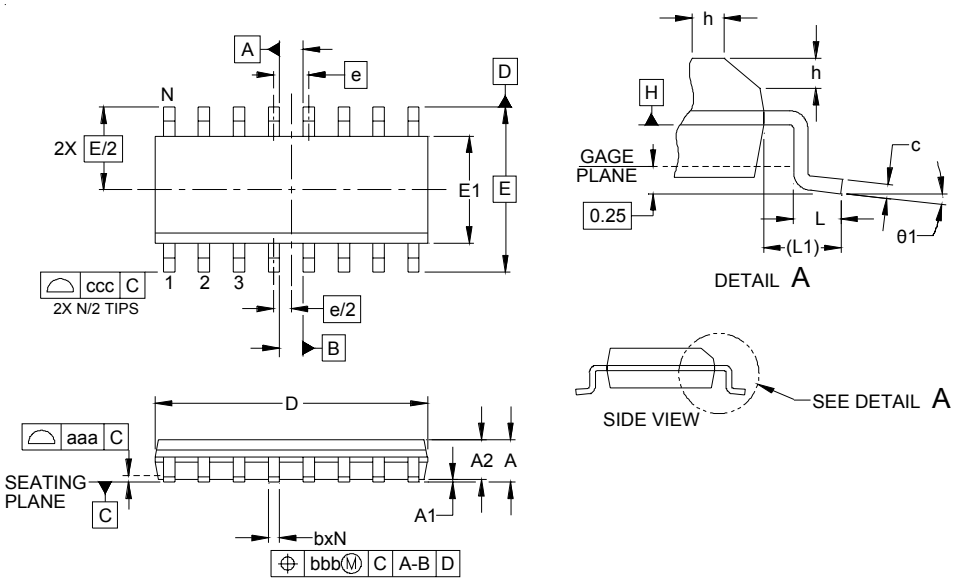
Good circuit board layout is critical for the suppression of fast rise-time transients such as ESD. The following guidelines are recommended:

- Place the LCDAxxC-8 near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the LCDAxxC-8 and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Outline Drawing - SO-16

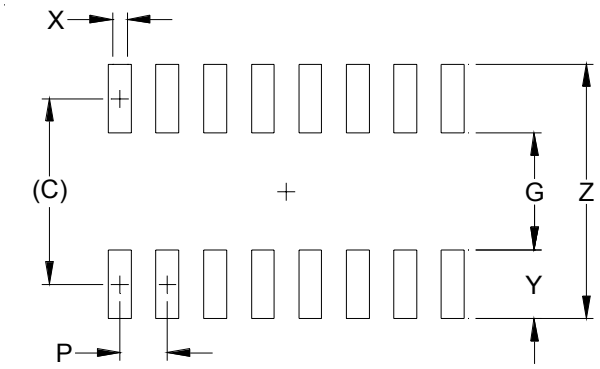


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.386	.390	.394	9.80	9.90	10.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	16			16		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AC.

Land Pattern - SO-16



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 304A.