HiperLCS Family

Integrated LLC Controller, High-Voltage Power MOSFETs and Drivers

Product Highlights

Features

- LLC half-bridge power stage incorporating controller, high and low-side gate drives, and high-voltage power MOSFETs
  - Eliminates up to 30 external components
- High maximum operating frequency of 1 MHz
  - Nominal steady-state operation up to 500 kHz
  - Dramatically reduces magnetics size and allows use of SMD ceramic output capacitors
- Precise duty symmetry balances output rectifier current, improving efficiency
  - 50% ±0.3% typical at 300 kHz
- Comprehensive fault handling and current limiting
  - Programmable brown-in/out thresholds and hysteresis
  - Undervoltage (UV) and overvoltage (OV) protection
  - Programmable over-current protection (OCP)
  - Short-circuit protection (SCP)
  - Over-temperature protection (OTP)
- Programmable dead-time for optimized design
- Programmable burst mode maintains regulation at no-load and improves light load efficiency
- Programmable soft-start time and delay before soft-start
- Accurate programmable minimum and maximum frequency limits
- Single package designed for high-power and high-frequency
  - Reduces assembly cost and reduces PCB layout loop areas
  - Simple single clip attachment to heat sink
  - Staggered pin arrangement for simple PC board routing and high-voltage creepage requirements
- Paired with HiperPFS PFC product gives complete, high efficiency, low part count PSU solutions

Applications

- High-efficiency power supplies (80 PLUS Silver, Gold and Platinum)
- LCD TV power supplies
- LED street and area lighting
- Printer power supplies
- Audio amplifier

Description

The HiperLCS™ is an integrated LLC power stage incorporating a multi-function controller, high-side and low-side gate drivers, plus two power MOSFETs in a half-bridge configuration. Figure 1 shows a simplified schematic of a HiperLCS based power stage where the LLC resonant inductor is integrated into the transformer.

The variable frequency controller provides high-efficiency by switching the power MOSFETs at zero voltage (ZVS), eliminating switching losses.

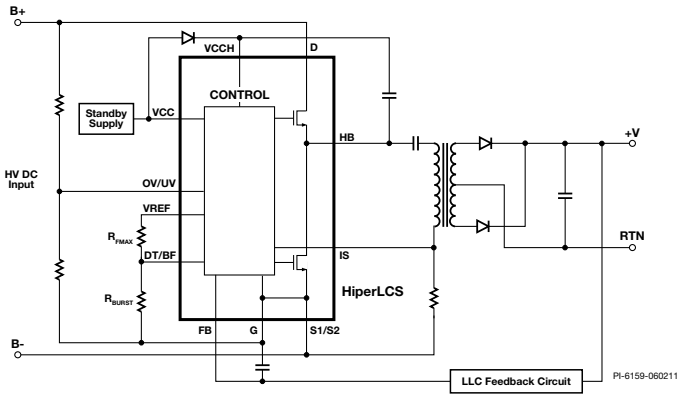


Figure 1. Typical Application Circuit – LCD TV and PC Main Power Supply.

Output Power Table

Product	Maximum Practical Power[1]
LCS700HG/LG	110 W
LCS701HG/LG	170 W
LCS702HG/LG	220 W
LCS703HG/LG	275 W
LCS705HG/LG	350 W
LCS708HG/LG	440 W

Table 1. Output Power Table.

Notes:
1. Maximum practical power is the power the part can deliver when properly mounted to a heat sink and a maximum heat sink temperature of 90 °C.

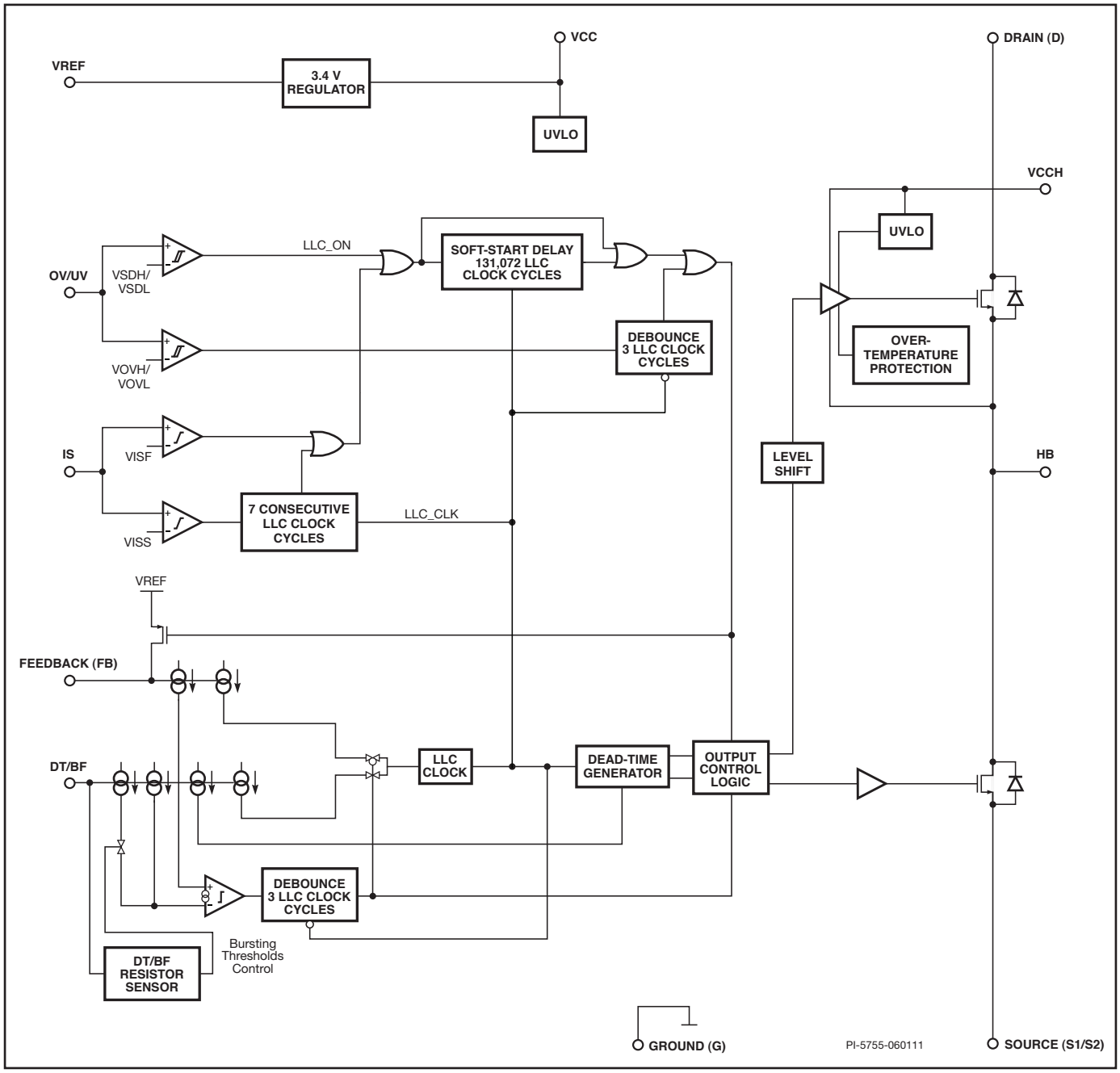


Figure 2. Block Diagram.

Pin Functional Description

VCC Pin
IC power pin. In a typical application, VCC is connected to the 12 V system standby supply via a 5 Ω resistor. This resistor helps provide filtering and improves noise immunity.

Note: The system standby supply return should be connected to the B- bus and not to the GROUND pin.

VREF Pin
3.4 VREF pin. An internal voltage reference network used as a voltage source for FEEDBACK pin and DT/BF pin pull-up resistor.

GROUND (G) Pin
G is the return node for all analog small signals. All small signal pin bypass capacitors must be returned to this pin through short traces, with the exception of the D-S high-voltage bypass capacitor, and the VCCH bypass capacitor. It is internally connected to the SOURCE pins to provide a star connection. **Do not connect the GROUND pin to the SOURCE pins, nor to the B- bus, in the PCB layout**.

OV/UV Pin
Overvoltage/Undervoltage pin. B+ is sensed by this pin through a resistor divider. The OV/UV pin implements brown-in, brown-out, and overvoltage lockout with hysteresis. Pulling this pin down to ground will implement a remote-off function.

FEEDBACK (FB) Pin
Current fed into this pin determines LLC switching frequency; higher current programs higher switching frequency. The pin V-I characteristic resembles a diode to ground during normal switching. An RC network between the VREF pin and FEEDBACK pin determines the minimum operating frequency, start-up frequency, soft-start time, and delay before start-up.

DEAD-TIME/BURST FREQUENCY (DT/BF) Pin
A resistor divider from VREF to ground programs dead-time, maximum switching frequency at start-up, and burst-mode threshold frequencies.

CURRENT-SENSE (IS) Pin
The CURRENT-SENSE pin is used for sensing transformer primary current, to detect overload and fault conditions, through a current sense resistor or a capacitive divider plus sense resistor circuit. It resembles a reverse diode to ground, and does not require a rectifier circuit for preventing negative pulses from reaching the pin, provided the reverse current is limited to <5 mA.

SOURCE (S1), (S2) Pins
SOURCE pins of internal low-side MOSFET. These should be connected together on the PCB, and connected to the B- from the PFC bulk capacitor or input high-voltage DC return.

HB Pin
This is the output of the half-bridge connected MOSFETs (Source of high-side MOSFET, Drain of low-side MOSFET), to be connected to the LLC power train (transformer primary and series resonant capacitor).

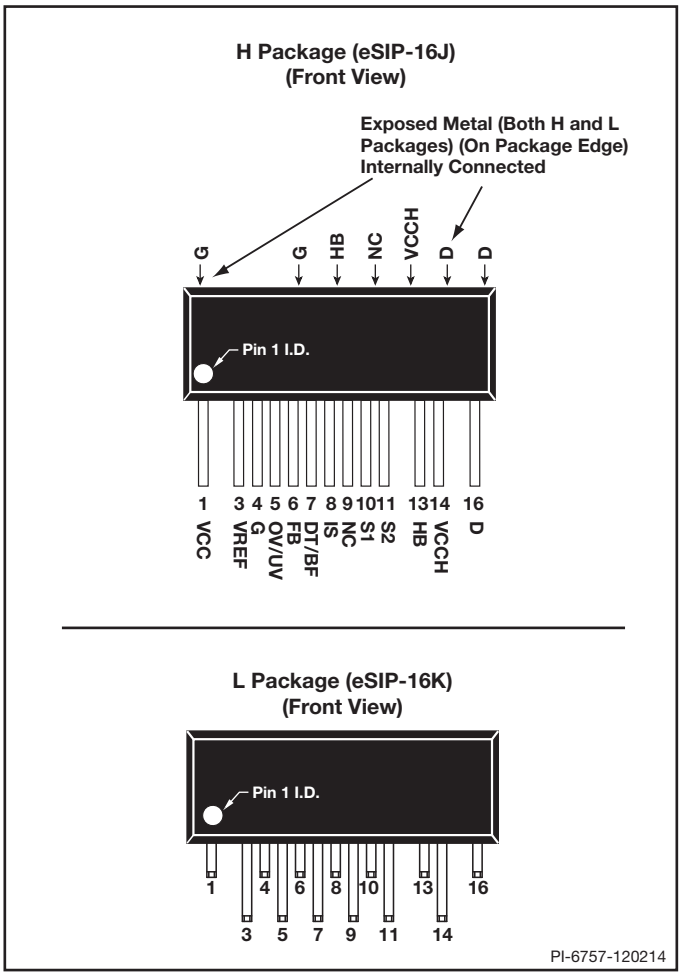


Figure 3. Pin Numbering and Designation.

VCCH Pin
Floating bootstrap supply pin for the LLC high-side driver. This pin is referenced to the HB pin, which in turn is internally connected to the SOURCE pin of the high-side MOSFET. A bypass/storage capacitor between VCCH and HB pins, and a boot strap diode with a series resistor from the standby supply, are required. The storage capacitor is refreshed every time the lower MOSFET turns on or its body diode conducts.

DRAIN (D) Pin
DRAIN pin of the internal high-side MOSFET. This connects to the B+ from the PFC bulk capacitor or input high-voltage DC bus.

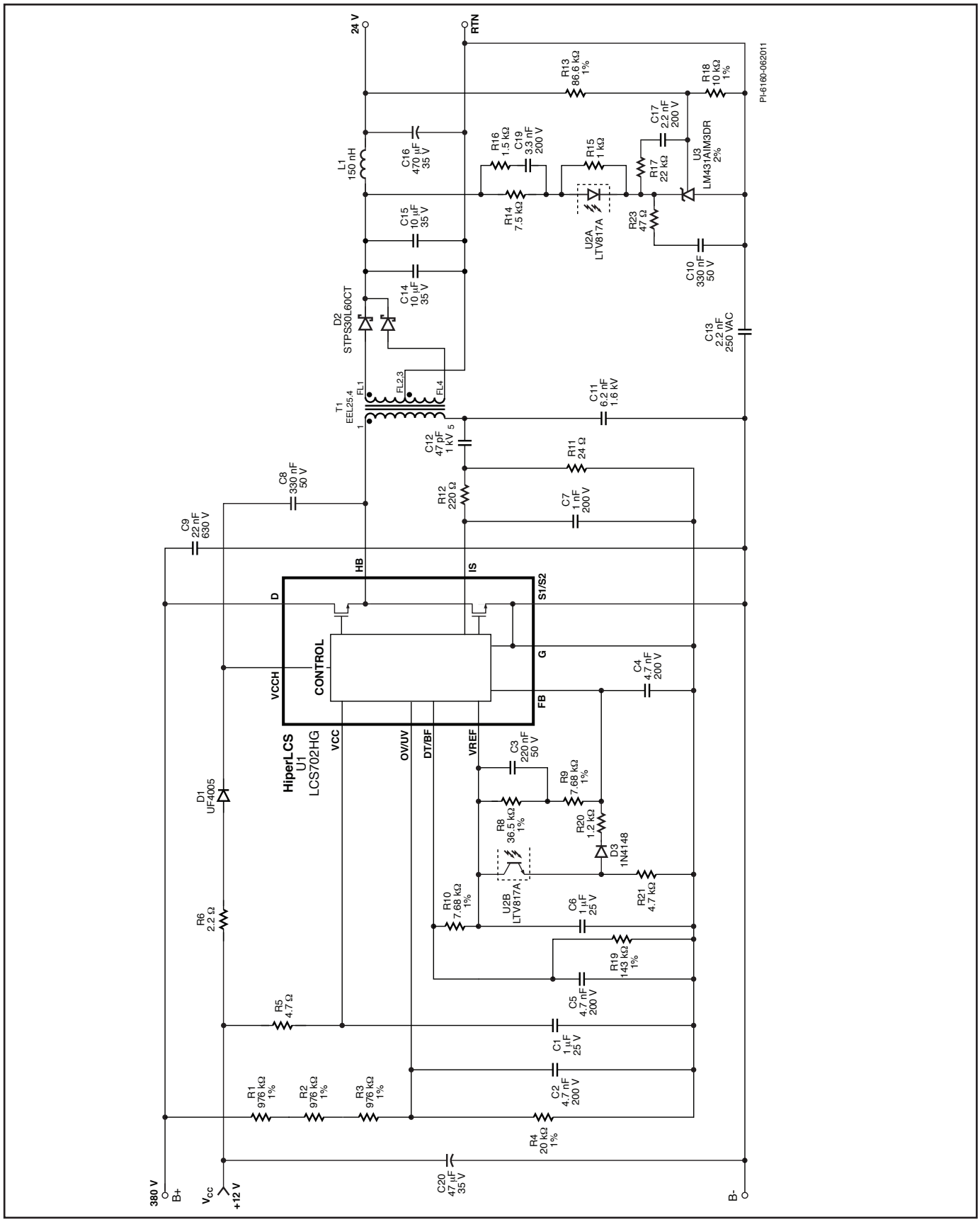


Figure 4. 150 W Laser-Jet Printer Power Supply.

HiperLCS Basic Operation

The HiperLCS is designed for half-bridge LLC converters, which are high-efficiency resonant, variable frequency converters. The HiperLCS is an LLC controller chip with built-in drivers and half-bridge MOSFETs.

LLC converters require a fixed dead-time between switching half-cycles. The dead-time, maximum frequency at start-up, and burst threshold frequencies, are programmed with a resistor divider on the DT/BF pin from the VREF to the GROUND pins.

The FEEDBACK (FB) pin is the frequency control input for the feedback loop. Frequency is proportional to FEEDBACK pin current. The FEEDBACK pin V-I characteristic resembles a diode to ground.

Burst Mode

If the frequency commanded by the FEEDBACK pin current exceeds the upper burst threshold frequency (f_{STOP}, I_{STOP}) programmed by the resistor divider on the DT/BF pin, the output MOSFETs will turn off, and will resume switching when the current drops below the value which corresponds to the frequency equal to the lower burst threshold frequency (f_{START}, I_{START}). As a first approximation, burst mode control resembles a hysteretic controller where the frequency ramps from f_{START} to f_{STOP}, stops and repeats. An external component network connected from the VREF pin to the FEEDBACK pin determines the minimum and start-up FEEDBACK pin currents, and thus the minimum and start-up switching frequencies. A soft-start capacitor in this network determines soft-start timing.

The VREF pin provides a nominal 3.4 V as a reference for this FEEDBACK pin external network and other functions. Maximum current from this pin must be ≤4 mA.

The Dead-Time/Burst Frequency (DT/BF) pin also has a diode-to-ground V-I characteristic. A resistor divider from VREF to GROUND programs dead-time, maximum start-up switching frequency (f_{MAX}), and the burst threshold frequencies. The current flowing from the resistor divider to the DT/BF pin determines f_{MAX}. The ratio of the resistors selects from 3 discrete, burst threshold frequency ratios, which are fixed fractions of f_{MAX}.

The OV/UV pin senses the high-voltage B+ input through a resistor divider. It implements brown-in, brown-out, and OV with hysteresis. The ratios of these voltages are fixed; the user must select the resistor divider ratio such that the brown-in voltage is below the minimum nominal bulk (input) voltage regulation set-point to ensure start-up, and the OV (lower) restart voltage is above the maximum nominal bulk voltage set-point, to ensure that the LCS will restart after a voltage swell event that triggers the OV upper threshold. If different brown-in to brown-out to OV ratios are required, external circuitry needs to be added to the resistor divider.

VCC Pin UVLO

The VCC pin has an internal UVLO function with hysteresis. The HiperLCS will not start until the voltage exceeds the VCC start threshold $V_{UVLO(+)}$. HiperLCS will turn off when the VCC drops to the VCC Shutdown Threshold $V_{UVLO(-)}$.

VCCH Pin UVLO

The VCCH pin is the supply pin for the high-side driver. It also has a UVLO function similar to the VCC pin, with a threshold lower than the VCC pin. This is to allow for a VCCH voltage that is slightly lower than VCC because the VCCH pin is fed by a bootstrap diode and series current-limiting resistor from the VCC supply.

Start-Up and Auto-Restart

Before start-up the FEEDBACK pin is internally pulled up to the VREF pin to discharge the soft-start capacitor and to keep the output MOSFETs off. When start-up commences the internal pull-up transistor turns off, the soft-start capacitor charges, the outputs begin switching at f_{MAX}, the FEEDBACK pin current diminishes, the switching frequency drops, and the PSU output rises. When the output reaches the voltage set-point, the optocoupler will conduct, closing the loop and regulating the output.

Whenever the VCC pin is powered up, the DT/BF pin goes into high impedance mode for 500 μs in order to sense the voltage divider ratio and select the Burst Threshold. This setting is stored until the next VCC recycle. The DT/BF pin then goes into normal mode, resembling a diode to ground, and the sensed current continuously sets the f_{MAX} frequency. The burst threshold frequencies are fixed fractions of f_{MAX}. The internal oscillator runs the internal counters at f_{MAX} whenever the FEEDBACK pin internal pull-up is on.

When a fault is detected on the IS, OV/UV, or VCC pin (UVLO), the internal FEEDBACK pin pull-up transistor turns on for 131,072 clock cycles, to discharge the soft-start capacitor completely, then a restart is attempted. The first power-up after a VCC recycle only waits 1024 cycles, including the condition where the OV/UV pin rises above the brown-in voltage for the first time, after VCC is powered up.

Remote-Off

Remote-off can be invoked by pulling down the OV/UV pin to ground, or by pulling up the IS pin to >0.9 V. Both will invoke a 131,072 cycle restart cycle. VCC can also be pulled down to shut the device off, but when it is pulled up, the FEEDBACK pin is pulled up to the VREF pin to discharge the soft-start capacitor for only 1024 f_{MAX} clock cycles. If this scheme is used, the designer must ensure that the time the VCC is pulled down, plus 1024 cycles, is sufficient to discharge the soft-start capacitor, or if not, that the resulting lower starting frequency is high enough so as not to cause excessive primary currents that may cause the over-current protection to trip.

Current Sense

The IS pin senses the primary current. It resembles a reverse diode to the GROUND pin. It is tolerant of negative voltages provided the negative current is limited to <5 mA. Therefore it must be connected to the current sense resistor (or primary capacitive voltage divider + sense resistor) via a series current limiting resistor of >220 Ω. Thus it can accept an AC waveform and does not need a rectifier or peak detector circuit. If the IS pin senses a nominal positive peak voltage of 0.5 V for 7 consecutive cycles, an auto-restart will be invoked. The IS pin also has a second, higher threshold at nominally 0.9 V, which will invoke an auto-restart with a single pulse. The minimum pulse width requirement for detection of both voltage thresholds is nominally 30 ns. i.e. the thresholds have to be exceeded for >30 ns for proper detection.

Over-Temperature Shutdown

The HiperLCS has latching OTP. VCCH must be cycled to resume operation once the unit drops down below the OTP threshold.

Basic Layout Guidelines

The HiperLCS is a high-frequency power device and requires careful attention to circuit board layout in order to achieve maximum performance.

The bypass capacitors need to be positioned and laid out carefully to minimize trace lengths to the pins they serve. SMD components are recommended for minimum component and trace stray inductance.

Table 2 describes the recommended bypass capacitor values for pins that require filtering/bypassing. The table lists the pins in the order of most to least sensitive. The bypass capacitor of the pin at the top of the list being the most sensitive, receives higher priority in bypass capacitor positioning to minimize trace lengths, than the bypass capacitor of the pin below it. Noise entering the two most sensitive pins on the list, namely the FEEDBACK and DT/BF pins, will cause duty cycle, and dead-time imbalance, respectively.

Figure 5 and Figure 6 show two alternate schemes for routing ground traces for optimum performance. Figure 5 shows a layout footprint for the LCS with oval pads. These allow a trace to be passed between pins 3 and 5, directly connecting the ground systems for the bypass capacitors located on each side of the IC.

Figure 6 shows an LCS layout footprint with round pads that do not allow traces to be routed between them due to insufficient space. In this case, a jumper (JP1, a 1206 size 0 Ω resistor) is used to connect the ground systems together and allow a connection for pin 3 to be routed under JP1 to the optocoupler.

Transformer T1 is a source of both high di/dt signals and dv/dt noise. The first can couple magnetically to sensitive circuitry, while the second can inject noise via electrostatic coupling. Electrostatic noise coupling can be reduced by grounding the transformer core, but it is not economically feasible to reduce the stray magnetic field around the transformer without drastically reducing its efficiency. Sensitive traces and components (such as the optocoupler) should be located away from the transformer to avoid noise pickup.

Pin	Returned to Pin	Recommended Value	Notes
FEEDBACK (FB)	GROUND	4.7 nF (at 250 kHz)	Increase value proportionally for lower nominal frequency (e.g. 10 nF at 100 kHz). Forms a pole with FEEDBACK pin input impedance which is part of feedback loop characteristic. Must not introduce excessive phase shift at expected gain crossover frequency. Noise entering FEEDBACK pin will cause duty cycle imbalance.
DEAD-TIME/BURST FREQUENCY (DT/BF)	GROUND	4.7 nF	Time constant of this capacitor and the source impedance of the resistors connected to DT/BF pin must be <100 µs. Noise entering DT/BF pin will cause dead time imbalance.
CURRENT SENSE (IS)	GROUND	1 nF (at 250 kHz)	Value changes proportionally with nominal LLC stage operating frequency. Forms an RC low pass filter with recommended 220 Ω series resistor. Must not attenuate AC signal of primary current sense.
VCC	GROUND	1 µF ceramic	
VREF	GROUND	1 µF ceramic	
VCCH	HB	0.1 µF - 0.47 µF	Bootstrap capacitor. Provides instantaneous current for high-side driver for turning on high-side MOSFET. Time constant formed with boost-strap current limiting resistor (in series with bootstrap diode), delays VCCH UVLO for a few switching cycles at start-up and during burst mode operation for the first switching cycles
DRAIN (DC Bus)	S1, S2	10-22 nF SMD ceramic minimum, plus 22-100 nF through-hole	Total of 22 nF per amp of nominal primary RMS current. SMD part must be located directly at the IC and connected close, with short traces. This prevents ringing of D-S during hard-switching (loss of ZVS) transients. It also reduces high-frequency EMI.
OV/UV	GROUND	4.7 nF	

Table 2. Bypass Capacitor Table in Order of Importance.

Figure 7 shows a an example of preferred routing for the optocoupler and traces connected to the FEEDBACK pin. The optocoupler is spaced away from the transformer, reducing noise pickup. The optocoupler output trace (from pin 3) is also routed to increase the distance between it and "active" components and traces, such as T1 and the hot side of capacitor C12. Resistor R20 is located close to U1 rather than optocoupler U2, so that any noise picked up on the optocoupler trace is filtered by the combination of R20 and C4 before it gets to the FEEDBACK pin on U1. C4 is placed directly adjacent to the FEEDBACK pin of U1 (pin 4).

VCCH is connected to the standby supply through a high-voltage ultrafast diode and a 2.2 Ω resistor connected in series. This diode resistor network charges the VCCH bypass/storage capacitor whenever the internal LLC low-side MOSFET is on. The resistor limits the peak instantaneous charging current. See R6 and D1 in Figure 8.

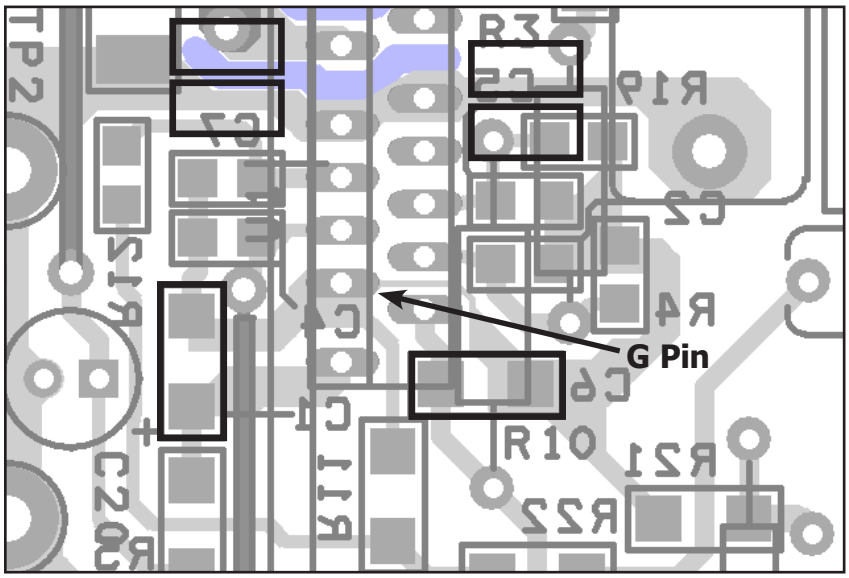


Figure 5. Placement of Bypass Capacitors on Signal Pins of IC.

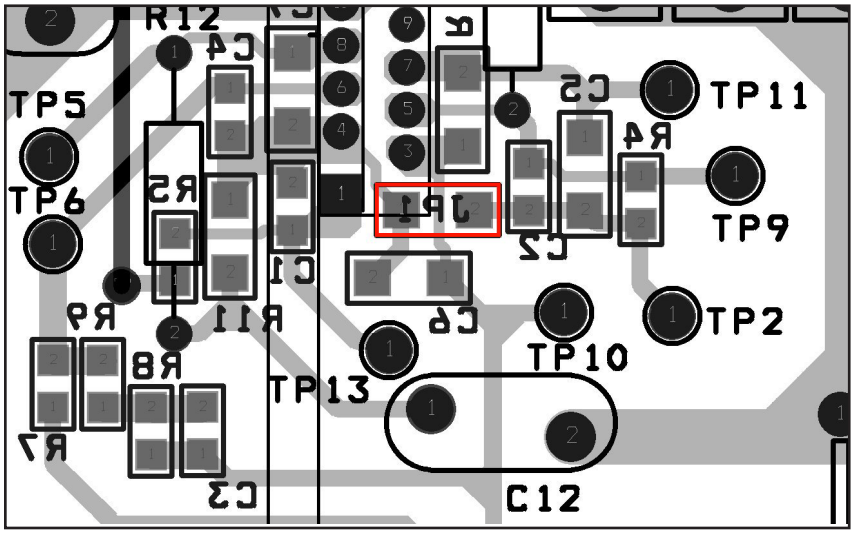


Figure 6. Alternate Layout for LCS Footprint using Round Pads with Jumper Connecting Two Grounds Highlighted.

Small Signal Bypass Capacitors

Please refer to Figure 5 Note the location of the small signal bypass capacitors (highlighted) for the FEEDBACK, DT/BF, IS, VREF, OV/UV and VCC pins, which allow short traces to their pin connections and to the GROUND pin. Note that there is no connection between the GROUND pin and the SOURCE pin or the B- bus on the printed circuit board.

VCCH Bypass Capacitor

Please refer to Figure 8. Note the location of the VCCH capacitor (highlighted) which allows short connections to the HB pin and the VCCH pin.

Drain to Source High-Voltage Bypass Capacitor

Please refer to Figure 9. Note the location of the B+ to B- high-voltage bypass capacitors (highlighted) placed at the IC, minimizing the PCB trace length to the D and S pins.

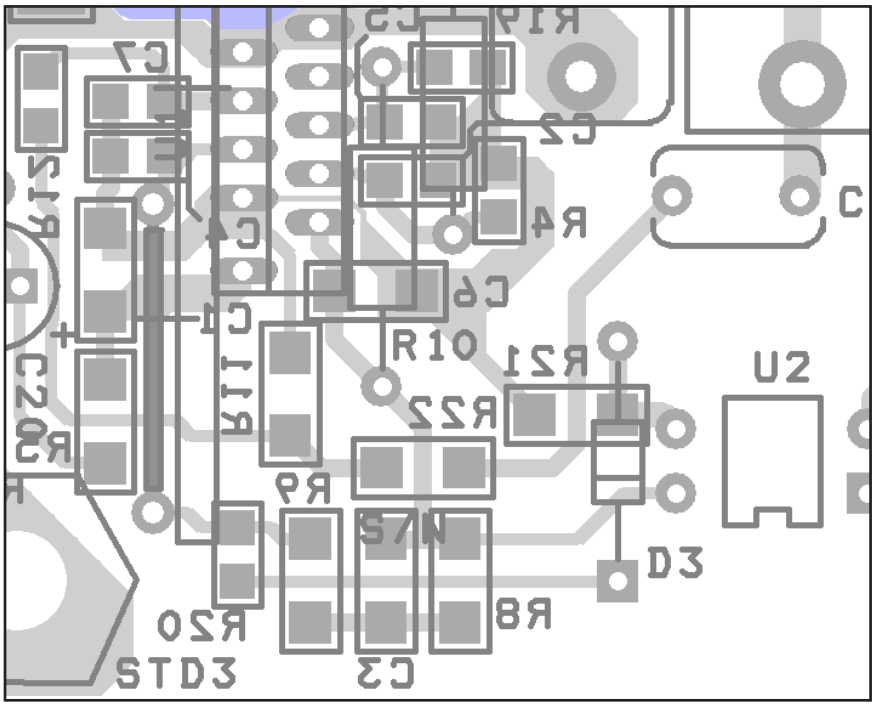


Figure 7. Preferred Routing of Optocoupler and Traces to FEEDBACK Pin.

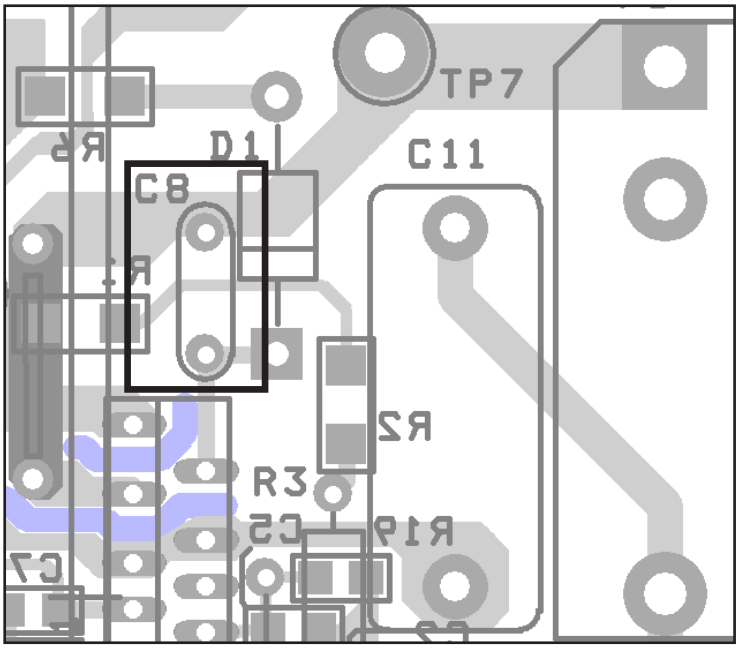


Figure 8. Placement of VCCH Capacitor.

Bootstrap Circuit and HB Node Layout

Please refer to Figure 10. Note the location of the bootstrap diode, capacitor, resistor, and the HB trace routing. The objective is to keep them away from the small signal components and traces, such as the feedback optocoupler. Do not unnecessarily increase the area of the PCB traces on this node, because it will increase the dv/dt (capacitive) coupling to low-voltage circuits.

Transformer Secondary

The transformer secondary pins, output diodes, and main output capacitors should be positioned close together and routed with short thick traces. This is **critical** for secondary current symmetry and to minimize output diode inverse voltage stress. The use of ceramic capacitors allows placement between the transformer secondary pins and the output rectifier, producing a very tight layout. See Figure 11. The secondary winding halves should be inter-twined together before they are wound on the bobbin. This minimizes the leakage inductance between them and greatly improves current symmetry and minimizes output diode inverse voltage stress. For a 2-output design the half-windings of a given output need to be intertwined.

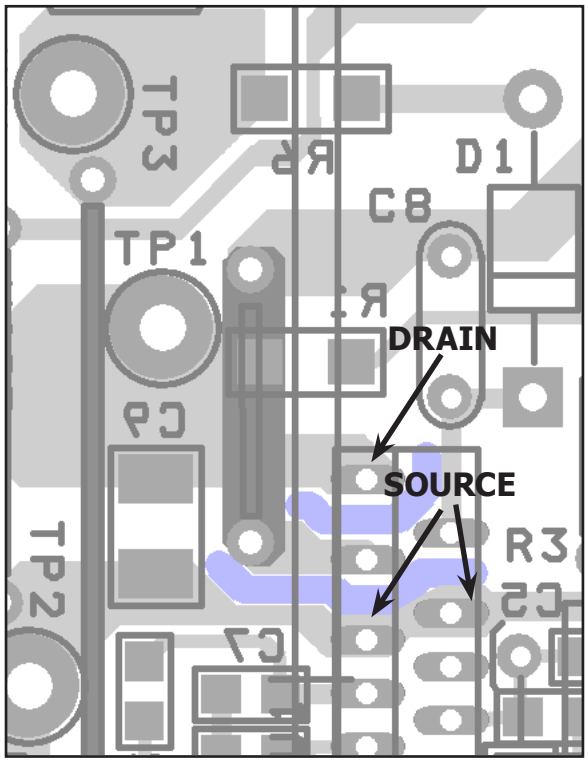


Figure 9. Placement of B+ and B- High-Voltage Bypass Capacitors.

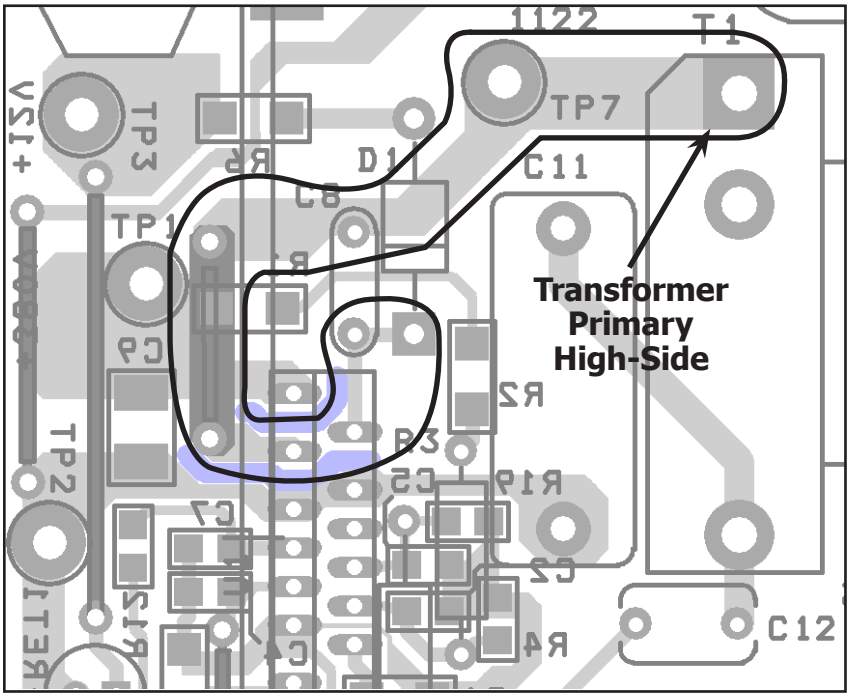


Figure 10. Placement of Boot Strap Diode, Capacitor, Resistor and the High-Voltage Trace Routing.

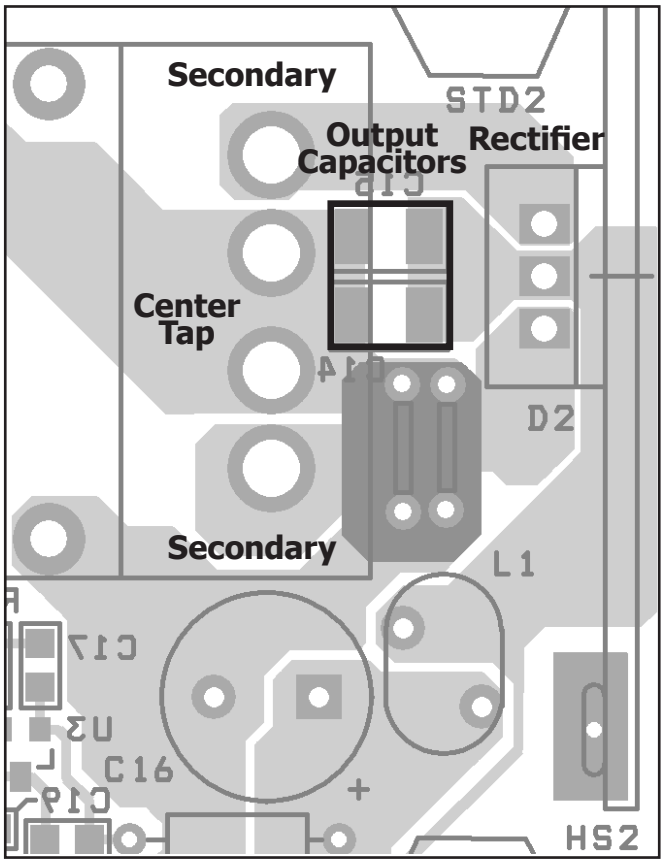


Figure 11. Placement of Capacitors Between Transformer Secondary Pins and the Output Rectifier to minimize and Equalize Loop Areas.

Key Design Details

The LLC converter is a variable frequency resonant converter. As input voltage decreases, the frequency must decrease in order to maintain output regulation. To a lesser extent, as load reduces the frequency must increase. When the converter is operating at the series resonant frequency, the frequency changes very little with load. The minimum operating frequency required occurs at brownout (minimum input voltage), at full load.

Operating Frequency Selection

For lowest cost, and smallest transformer size with the least amount of copper, the recommended nominal operating frequency is ~250 kHz. This allows the use of low-cost ceramic output capacitors in place of electrolytic capacitors, especially at higher output voltages (≥12 V). If the core and bobbin used exhibits too much leakage inductance for 250 kHz, operation at 180 kHz also results in excellent performance. For optimal efficiency at 250 kHz, AWG #44 (0.05 mm) Litz is recommended for the primary, and AWG #42 (0.07 mm) for the secondary winding. Thicker gauge lower cost Litz can be used at the expense of increased copper loss and lower efficiency. Litz gauge (AWG #38 or 0.1 mm) is optimal for very low frequencies (60-70 kHz), requires much larger transformers and greater lengths of Litz wire.

For nominal operating frequencies even as low as 130 kHz, the use of PC44 or equivalent core material is recommended for reduced losses. For a given transformer design, shifting the frequency up (by substituting a smaller resonant capacitor), will reduce core loss (due to reduced AC flux density B_{AC}) and increase copper loss. Core loss is a stronger function of flux density than of frequency. The increased frequency increases copper loss due to eddy current losses.

Nominal operating frequencies >300 kHz start to lose significant efficiency due to increased eddy current losses in the copper, and due to the fact that a more significant percentage of time is spent on the primary slew time (ZVS transition time) which erodes the percentage of time that power is transferred to the secondary.

Resonant Tank and Transformer Design

Please refer to the Application Note AN-55 for guidance on using the PIXls HiperLCS spreadsheet which assists in the entire design process.

Primary Inductance

The optimal powertrain design for the HiperLCS uses a primary inductance that results in minimal loss of ZVS at any steady-state condition. Some loss of ZVS during non-steady-state conditions is acceptable. Reducing primary inductance produces higher magnetizing current which increases the range of ZVS operation, but the increased magnetizing current increases losses and reduces efficiency.

The calculation of the primary inductance to be used for a first-pass design is based on device size, rated load, minimum input voltage, and desired operating frequency. It is provided in the PIXls spreadsheet. L_{PRI} is the primary inductance of an integrated transformer (high leakage inductance), or in the case of the use of an external series inductance, the sum of this inductance and the transformer primary inductance.

Leakage Inductance

The parameter K_{RATIO} is a function of leakage inductance:

$$K_{RATIO} = \frac{L_{PRI}}{L_{RES}} - 1$$

The recommended K_{RATIO} is from 2.5 - 7. This determines the acceptable range of leakage inductance.

L_{RES} is the leakage inductance in an integrated transformer; if a separate series inductor is used, it is the sum of this inductance and the leakage inductance of the transformer.

A low K_{RATIO} (high leakage inductance) may not be capable of regulation at the minimum input voltage, and may show increased transformer copper losses due to the leakage flux. A high K_{RATIO} (low leakage inductance) will have high peak and RMS currents at low-line, and require a lower primary inductance to achieve ZVS operation over a suitably wide range, which increases the resonant circulating current, reducing efficiency.

The core and bobbin designs available to the designer may limit the adjustability of leakage inductance. Fortunately, excellent performance can be achieved over a relatively wide range of leakage inductance values.

The K_{RATIO} directly affects the frequency range that the LLC needs to operate in order to maintain regulation over the input voltage range. Increasing K_{RATIO} increases this frequency range, lowering f_{MIN}.

A low f_{MIN} is only a potential problem for low frequency designs which typically run at higher nominal B_{AC}. This may allow the core to reach saturation when operating at f_{MIN}. Operating at f_{MIN} occurs when the input voltage is at a minimal (input brown-out).

For a design with a separate resonant inductor, running the inductance on the low side of the range (K_{RATIO} = 7), minimizes the size and cost of the inductor.

Adjusting Leakage Inductance

Sectioned bobbins (separated primary and secondary) are commonly used for LLC converters. Increasing or decreasing both primary and secondary turns (while maintaining turns ratio) will change the leakage inductance proportionally to the square of primary turns.

If the leakage inductance is too high, one possible solution is to use a 3-section bobbin, where the secondary is in the middle section, and the primary winding is split into 2 halves connected in series.

Lastly, if the leakage inductance is too low an external inductor may be added.

Resonant Frequency

The series resonant frequency is a function of L_{RES} and C_{RES}, the resonant capacitor. For any given value of L_{RES}, the value of C_{RES} can be adjusted for the desired series resonant frequency f_{RES}. For best efficiency the resonant frequency is set close to the target operating frequency at nominal input voltage.

Operating Frequency and Frequency Ratio

The operating to resonant frequency ratio f_{RATIO} is defined as:

$$f_{RATIO} = \frac{f_{SW}}{f_{RES}}$$

f_{RATIO} = 1 signifies the converter is operating at the series resonant frequency.

The main determinant of f_{RATIO} is the transformer turns ratio. Increasing primary turns lowers f_{RATIO} for a given input and output voltage.

The recommended f_{RATIO} at nominal input voltage is 0.92 – 0.97. Operating at resonance often yields the highest efficiency for the resonant powertrain if output rectifier selection is ignored. However, operating slightly below resonance (which puts the rectifiers in discontinuous conduction mode), allows the use of lower voltage diodes or synchronous MOSFETs, which have lower losses, increasing overall efficiency. This is because at high-line, when the converter needs to operate above resonance, the rectifiers operate less deeply in continuous mode, reducing the magnitude of their current commutation, reducing their stray inductance voltage spikes. (The stray inductance is comprised of the leakage inductance between secondary phases and the stray inductance in the connections to the rectifiers and output capacitors).

Conversely, operating at a very low f_{RATIO} (<0.8) results in higher RMS and peak currents. In some cases, this may result in an optimal design because it allows the use of lower voltage rating, lower V_F rectifier as they do not operate in continuous conduction mode even at high-line, results in no voltage spikes enabling a lower voltage rating.

An LLC half-bridge converter will operate at resonance when this equation is true:

$$\frac{\frac{V_{IN}}{2}}{V_{OUT}} = n_{EQ}$$

Where n_{EQ} is the transformer equivalent circuit turns ratio. Note that the n_{EQ} of an integrated transformer is lower than its physical turns ratio N_{PRI} / N_{SEC}. The secondary turns is that of each half-secondary. V_{OUT} in the above equation is equal to output voltage + diode drop. The divisor "2" is due to the half-bridge configuration – each half-cycle conducts half the input voltage to each secondary half.

Note that if the resonant capacitor or inductance value is changed, both switching frequency and resonant frequency change, but f_{RATIO} changes little.

For a given design, the input voltage at which the LLC operates at resonance is $V_{INPUT(RESONANCE)}$. Below this voltage, the LLC operates at a lower frequency (below resonance). Thus for the recommended f_{RATIO} ≈ 0.95 at nominal input voltage, $V_{INPUT(RESONANCE)}$ will be slightly higher than the nominal voltage.

For a design with a variable nominal input voltage (e.g. no PFC pre-regulator), it is recommended that the initial turns ratio be set so that $V_{INPUT(RESONANCE)}$ is at about halfway between maximum and minimum input voltage. For a design with a variable output voltage (e.g. constant current regulated output), it is recommended that the initial turns ratio be set to operate the LLC at resonance at a point halfway between minimum and maximum output voltages.

Dead-Time Selection

The vast majority of designs using HiperLCS, regardless of power and operating frequency, work very well with a dead-time of between 290 and 360 ns. Designs that require a low $V_{BROWNOUT}$ tend to require shorter dead-times.

The dead-time setting is a compromise between low-line / full load (low frequency), and minimum-load / high-line (high- frequency) conditions. Low-line / full load operation has short optimal dead-times, while minimum load / high-line has long optimal dead-times.

A dead-time setting that is longer than optimal for low-line / full load operation, exhibiting partial loss of ZVS, is acceptable if the condition does not occur during steady-state operation – i.e. appears only during transient conditions, such as hold-up time. Operation with loss of ZVS during steady-state operation leads to high internal power dissipation and should be avoided.

A dead-time setting that is shorter than optimal for high-line / minimum-load operation, will tend to cause the feedback sign to invert and force the HiperLCS to enter burst mode. This is acceptable if the resulting burst mode operation is acceptable (i.e. repetition rate does not produce audible noise and if the large signal transients, wherein the HiperLCS enters and exits burst mode, is acceptable). Note that with a PFC pre-regulated front end, a load dump (e.g. 100% to 1% load step) will exhibit a transient input voltage condition only temporarily (e.g. Input voltage to LLC stage will increase from 380 V to 410 V and relatively slowly return to 380 V). Note also that the Burst Threshold frequency setting is another variable available to the designer to tune burst mode.

OV/UV Pin

The HiperLCS OV/UV pin which monitors the input (B+) voltage, has a brown-out shutdown threshold ($V_{SD(L)}$) of nominally 79% of the brown-in (turn-on) threshold ($V_{SD(H)}$), which in turn, is nominally 2.4 V. The overvoltage (OV) lockout shutdown threshold ($V_{OV(H)}$) is nominally 131% of the brown-in start-up threshold, and the OV restart point ($V_{OV(L)}$) at nominally 126%. The ratios of these thresholds are fixed and selected for maximum utility in a design with a PFC pre-regulator front-end with a fixed output voltage set-point. The resistor divider ratio has to be selected so that brown-in point is always below the PFC output set-point, and so that the OV restart (lower) threshold, is always above it, including component tolerances.

During hold-up time, the voltage will drop from the nominal value, down to the brown-out threshold, whereby the HiperLCS will stop switching.

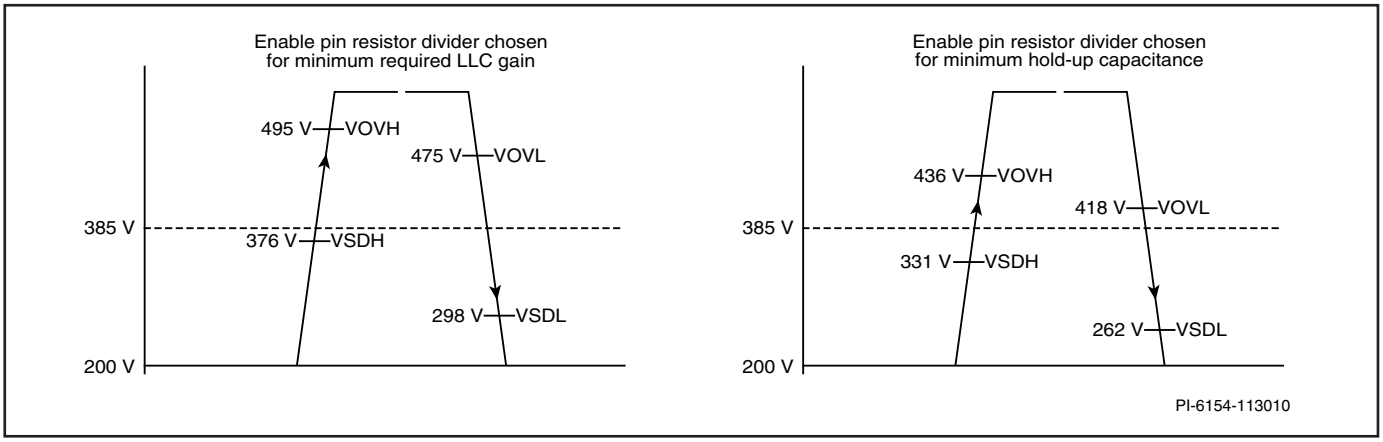


Figure 14. OV/UV Pin Voltage Thresholds, at Minimum and Maximum Divider Ratios, for 385 V Nominal Input Voltage.

If the input voltage is variable (e.g. no PFC pre-regulator), and the variation is greater than 24%, the OV threshold should be increased with external circuitry on the resistor divider. External circuitry is also needed if $V_{BROWNOUT}$ needs to be reduced below the default ratio.

In the example in the left-hand side of Figure 14 the resistor divider is set so that brown-in threshold is 376 V, just under the V_{PFC} set-point of 385 V. The OV shutdown threshold is 495 V, which gives adequate margin against the device max V_{DS} rating of 530 V. This minimizes required minimum LLC gain, and minimizes the peak current at brown-out. In the example on the right of Figure 14, the OV restart threshold is set to 418 V, just above V_{PFC}. This maximizes hold-up time for a given bulk capacitor value.

The OV/UV pin has an integrated 5 MΩ pull-down to detect pin-open fault conditions.

The recommended pull-down resistor value for the OV/UV pin divider is 20 kΩ – 22 kΩ. A very large resistor value will cause the pin pull-down current to affect accuracy, and a small value will increase power loss.

DT/BF Pin

The DT/BF pin senses the voltage divider ratio by entering into a high-impedance mode for 500 µs after VCC is applied. It senses the pin voltage, before the HiperLCS starts switching. See Figure 15.

There are 3 discrete Burst Threshold settings that can be selected. (This determines the burst start and stop switching frequencies, see Table 3).

For proper selection, set the ratio of R_{BURST} to R_{FMAX} as per Table 3.

The Burst Threshold setting is stored until VCC is powered down. After the Burst Threshold detection, the DT/BF pin operates in normal mode, sinking current, resembling a diode to ground, with a Thevenin equivalent circuit of nominally 0.66 V and

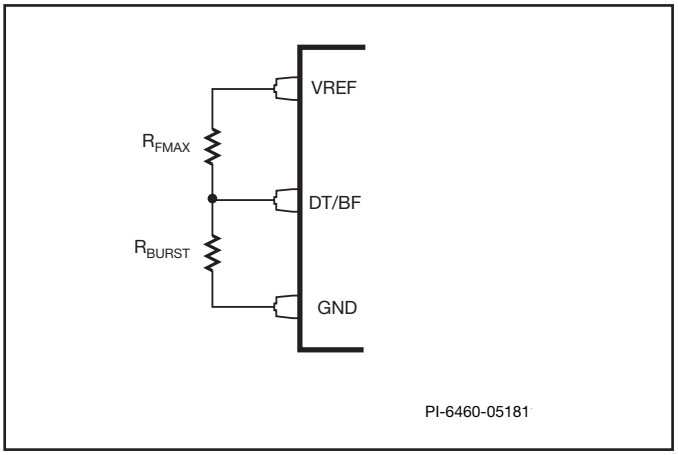


Figure 15. DT/BF Pin Divider.

1.1 kΩ. The current from the resistor divider into the pin, determines the dead-time and the maximum frequency f_{MAX}. The relationship between dead-time and f_{MAX} is fixed and approximated by:

$$f_{MAX}(kHz) = \frac{270000}{Dead-Time(ns)}$$

The relationship between DT/BF pin current and f_{MAX}, and switching frequency vs. FEEDBACK pin current (which has the same characteristic), is show in Figure 16.

The burst mode start and stop frequency thresholds are fixed fractions of f_{MAX}, which depend on the Burst Threshold setting, as set by the resistor divider ratio on the DT/BF pin.

Burst Threshold	R_{BURST} / R_{FMAX}
1	19
2	9
3	5.67

Table 3. Burst Threshold Selection Table.

Burst Threshold Setting	f_{START}/f_{MAX}	f_{STOP}/f_{MAX}
1	7/16	8/16
2	6/16	7/16
3	5/16	6/16

Table 4. Nominal Burst Start and Stop Frequencies as Ratios of f_{MAX}.

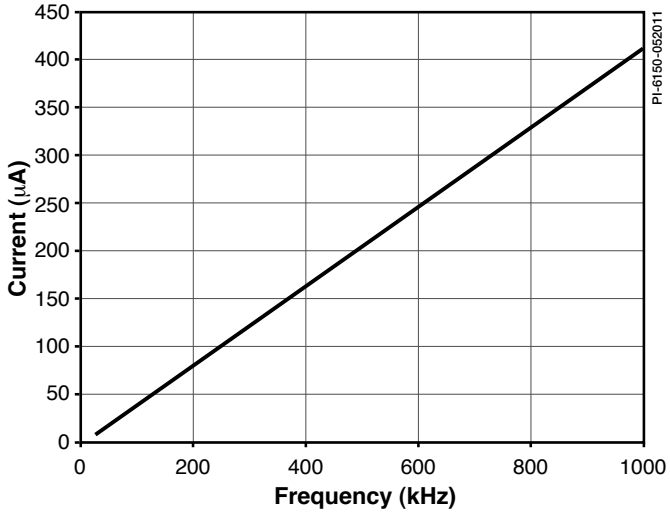


Figure 16. FEEDBACK Pin and DT/BF Pin Current vs. Frequency.

For example, if BT2 is selected, and f_{MAX} is 800 kHz, then f_{START} = 300 kHz, and f_{STOP} = 350 kHz. If during normal operation the load is reduced and the frequency rises to 350 kHz, the switching will stop. This causes the output voltage to drop and the feedback loop to decrease the FEEDBACK pin current. When the current decreases to a value which corresponds to 300 kHz, switching will commence, and the cycle will repeat. During start-up mode, however, the outputs can switch at a frequency between f_{STOP} and f_{MAX} (250 kHz and 800 kHz in the above example). Start-up mode is exited once the switching frequency drops below f_{STOP}, and the HiperLCS will subsequently enter burst mode if the feedback loop attempts to produce a switching frequency >f_{STOP}.

f_{MAX} is the frequency at which the internal counters run when the HiperLCS is in the off-state of the auto-restart cycle, or in the power-up delay before switching.

The minimum recommended dead-time is 275 ns, and thus the maximum f_{MAX} setting is 1 MHz.

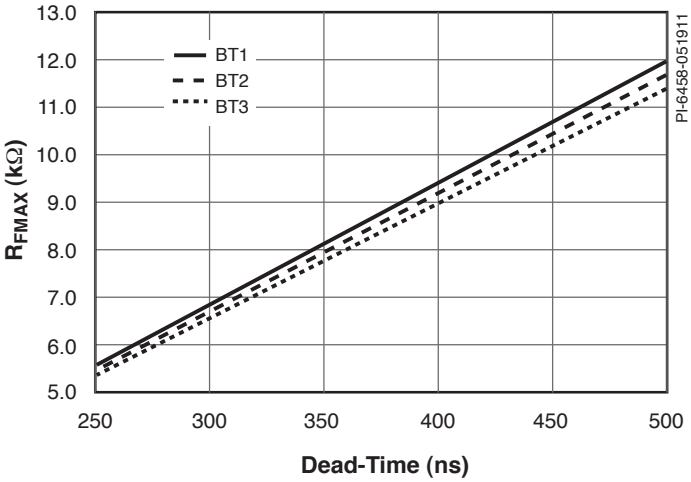


Figure 17. R_{FMAX} vs. Dead-Time, for the 3 Different Burst Threshold Settings.

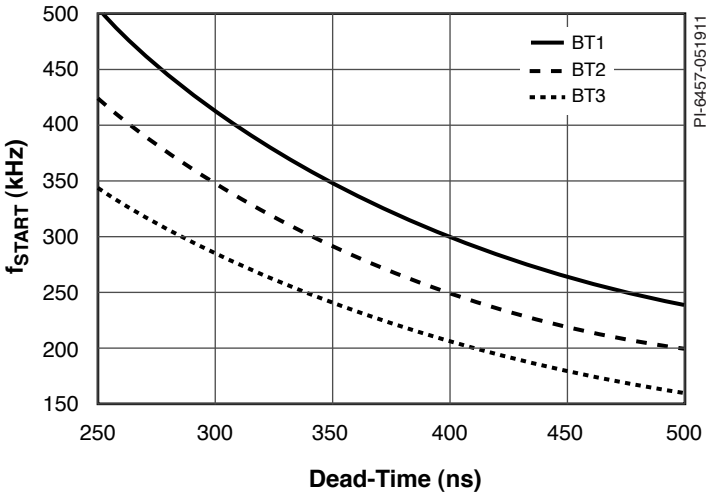


Figure 18. f_{START} (Lower Burst Threshold Frequency) vs. Dead-Time Setting for Different Burst Threshold Settings (BT1, BT2, BT3).

Burst Threshold Setting	f_{STOP} / f_{START}
1	1.14
2	1.17
3	1.20

Table 5. Ratio of f_{STOP}/f_{START} vs. Burst Threshold Selection.

To simplify the selection of R_{FMAX}, see the selection curves in Figure 17. The f_{STOP} to f_{START} ratio is fixed, and dependent on the Burst Threshold setting (see Table 5).

As a first approximation, during burst mode, the frequency ramps from f_{START} to f_{STOP}; then switching stops, and then the cycle repeats.

FEEDBACK Pin

The FEEDBACK pin is the voltage regulation FEEDBACK pin. It has a nominal Thevenin equivalent circuit of 0.65 V and 2.5 kΩ. In normal operation, it sinks current. During the off-period of auto-restart, and during the clocked delay before start-up, it pulls up internally to V_{REF} in order to discharge the soft-start capacitor. The current entering the pin determines switching frequency. Higher current yields higher frequency and thus reduces LLC output voltage. In a typical application an optocoupler connected to the VREF pin pulls up on the FEEDBACK pin, via a resistor network. The optocoupler is configured to source increasing FEEDBACK pin current, as the output rises. The resistor network between the optocoupler, FEEDBACK pin, and VREF pin, determine the minimum and maximum FEEDBACK pin current (and thus the minimum and maximum operating frequency), that the optocoupler can command as it goes from cutoff to saturation. This network also contains the soft-start timing capacitor, C_{START} (Figure 19).

The minimum frequency as set by this network must be lower than the frequency required by the powertrain at minimum input voltage. In Figure 19 this is determined by the sum of R_{FMIN} and R_{START}. The FEEDBACK pin current is determined by these two resistors when the optocoupler is cut off. C_{START} can be ignored during normal operation.

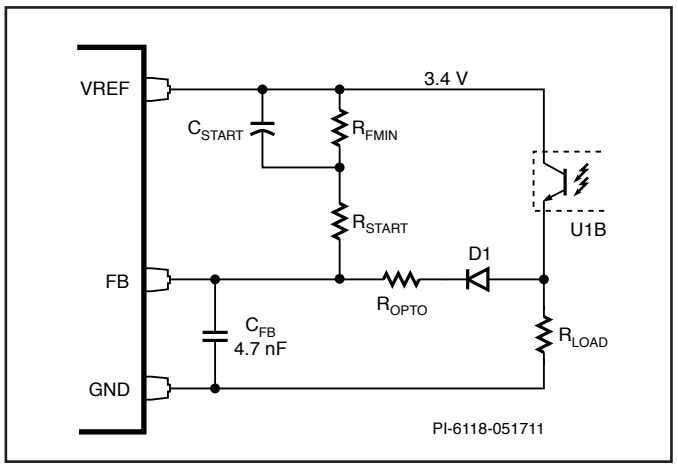


Figure 19. Feedback Network Shown with Additional Load Resistor.

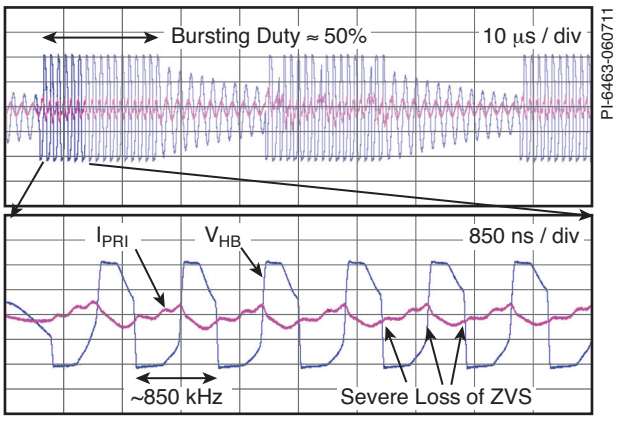


Figure 20. Bursting at f_{MAX} Causes High Internal Dissipation Due to Loss of ZVS and Should be Avoided.

Do not confuse R_{START}, which determines start-up frequency, and f_{START}, which is the burst mode start (lower) threshold frequency.

The FEEDBACK pin current at start-up is determined by the value of R_{START} because the voltage on C_{START} will be zero. For minimum start-up peak currents, this current should match or slightly exceed the DT/BF pin current so that start-up switching frequency begins at f_{MAX}. The resulting value of R_{START} will be approximately 10% lower than the value of the pull-up resistor on the DT/BF pin. The frequency will slide down as C_{START} charges. If R_{START} is smaller than that which provides start-up at f_{MAX}, it will create an additional delay before start-up switching. Please see the PIXIs HiperLCS spreadsheet.

Resistor R_{LOAD} provides a load on the optocoupler, and speeds up the large signal transient response during burst mode. The recommended value is ~4.7 kΩ. Diode D1 prevents R_{LOAD} from loading R_{FMIN} when the optocoupler is cut off. Diode D1 can be omitted and a combination of resistor values found to achieve the desired f_{MIN} but the resulting tolerances will be poor. Resistor R_{OPTO} will improve the ESD and surge immunity of the PSU. It also improves burst mode output ripple voltage. Its maximum value must be such that the FEEDBACK pin current is equal to the DT/BF pin current when the optocoupler is in saturation and the FEEDBACK pin is at 2.0 V (please see PIXIs HiperLCS spreadsheet). This is to ensure that if the HiperLCS does not exit start-up mode, because the feedback loop did not allow the switching frequency to drop below f_{STOP}, then it can regulate at light load by bursting at f_{MAX}. Note however bursting at f_{MAX} can lead to high internal dissipation due to loss of ZVS and should be avoided. See Figure 20.

Capacitor C_{START} should be sized at the minimum possible value that exhibits a 7 consecutive-cycle peak current at start-up that is just below the peak current measured at brown-out and full load. A larger value will slow down start-up and will make it more likely that f_{STOP} is not reached. This can prevent exiting start-up mode when the HiperLCS is powered up at high-line and minimum load, and may subsequently cause the HiperLCS to burst at f_{MAX} instead of between f_{START} and f_{STOP}.

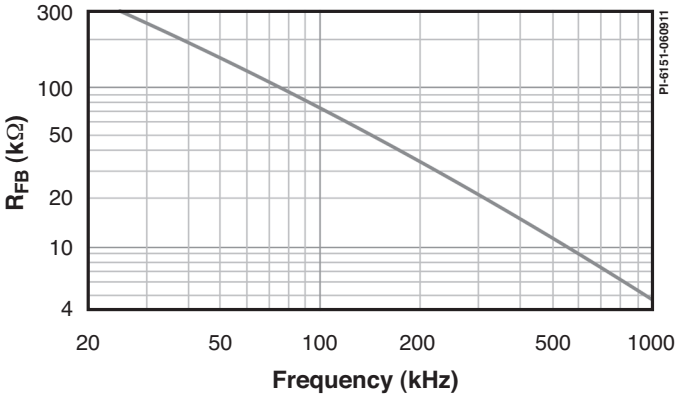


Figure 21. VREF to FB External Resistance vs. Frequency.

In order to calculate R_{FMIN} and R_{START}, use the following equation which describes nominal resistance from FEEDBACK pin to VREF pin, vs. frequency:

$$R_{FB} = \frac{3574}{f^{(0.6041 + 0.1193 \times LOG(f))}}$$

Where R_{FB} is in kΩ and f is in kHz.
To calculate the minimum R_{START}, which produces start-up at f_{MAX}, use the above equation with f = f_{MAX} from the equation relating dead-time and f_{MAX}.

To set f_{MIN}, use the above equation with f = f_{MIN} × 0.93. Where 0.93 is to ensure that, despite the worst case frequency tolerance of -7%, the frequency can go below f_{MIN}, guaranteeing regulation at $V_{BROWNOUT}$.

Using the resulting calculated value for R_{FB}, calculate R_{FMIN}:

$$R_{FMIN} = R_{FB} - R_{START}$$

The sum of R_{FMIN} and R_{START} determines f_{MIN}.

It should be noted that the 4.7 nF decoupling capacitor, C_{FB} (see Figure 19), in conjunction with the 2.5 kΩ input resistance presented by the FEEDBACK pin, form a pole in the LLC transfer function. This can add significant phase lag to the feedback loop. A typical value for a 250 kHz design with a 3 kHz crossover frequency is 4.7 nF. To prevent loop instability, the value of the 4.7 nF capacitor should not be increased arbitrarily. At the other extreme, insufficient FEEDBACK pin bypass capacitance or poor layout may cause duty cycle asymmetry.

Start-Up and Auto-Restart

At start-up and during the off-state of the auto-restart cycle, the FEEDBACK pin is internally pulled up to the VREF pin. This keeps the output MOSFETs off and discharges the soft-start capacitor, in preparation for soft-start.

At start-up, this state remains for 1024 clock cycles at frequency f_{MAX}. During the off-state of auto-restart, or if the OV/UV or IS pin is triggered while the VCC remains above its UVLO threshold, this state remains for 131,072 clock cycles.

After 1024 or 131,072 cycles (as the case may be), the HiperLCS turns off the internal pull-up transistor, the soft-start capacitor begins to charge, the output MOSFETs switch at f_{MAX}, current in the FEEDBACK pin diminishes, the frequency begins to drop, and the PSU output rises.

For example, for f_{MAX} = 800 kHz, the start-up delay after VCC power-up is 1.3 ms. If IS, or the OV/UV pin are tripped, auto-restart is invoked, with a restart delay of 164 ms.

The FEEDBACK pin has a current limit equal to the current flowing into the DT/BF pin. This limits the maximum current that charges the soft-start capacitor at start-up. If R_{START} is smaller than that which allows the FEEDBACK pin current to match the DT/BF pin current at start-up, an additional delay is introduced. C_{START} will charge at the current limit, and switching will only commence when the FEEDBACK pin voltage drops below 2.0 V. Thus the designer can add an additional start-up delay if desired.

As the soft-start capacitor continues to charge, the current through R_{START} and thus the FEEDBACK pin decreases, reducing switching frequency. The output voltage climbs; and when the feedback loop closes, the optocoupler conducts and starts controlling the switching frequency thus the output voltage.

Remote-Off

Remote-off can be invoked by pulling down the OV/UV pin to ground, or by pulling up the IS pin to >0.9 V. Both will invoke a 131,072 cycle restart cycle. VCC can also be pulled down to shut the device off, but when it is pulled up, the FEEDBACK pin is pulled up to the VREF pin to discharge the soft-start capacitor for only 1024 f_{MAX} clock cycles. If this scheme is used, the designer must ensure that the time the VCC is pulled down, plus 1024 cycles, is sufficient to discharge the soft-start capacitor, or if not, that the resulting lower starting frequency is high enough so as not to cause excessive primary currents that may cause the over-current protection to trip.

IS Pin

The IS pin has 2 thresholds: nominally 0.5 V and 0.9 V. The IS pin can tolerate small negative voltages and currents, and thus does not need a peak detector or rectifier circuit. The pin has a reverse-biased diode to ground equivalent circuit, and can tolerate a maximum negative current of 5 mA. The primary current is sampled by a primary, B- referenced current sense resistor, or by a capacitor current divider + current sense resistor combination circuit. In order to limit the negative current to 5 mA, a current limiting resistor between the sense resistor and the IS pin is necessary, with a minimum value of 220 Ω. Using the minimum value maximizes the IS pin bypass capacitor value and thus pin noise rejection, for a given RC pole frequency. The IS pin will invoke a restart if it sees 7 consecutive pulses >0.5 V. It will also invoke a restart if a single pulse exceeds 0.9 V. The minimum pulse detection time is nominally 30 ns – i.e. the pulses must be higher than the threshold voltage for >30 ns.

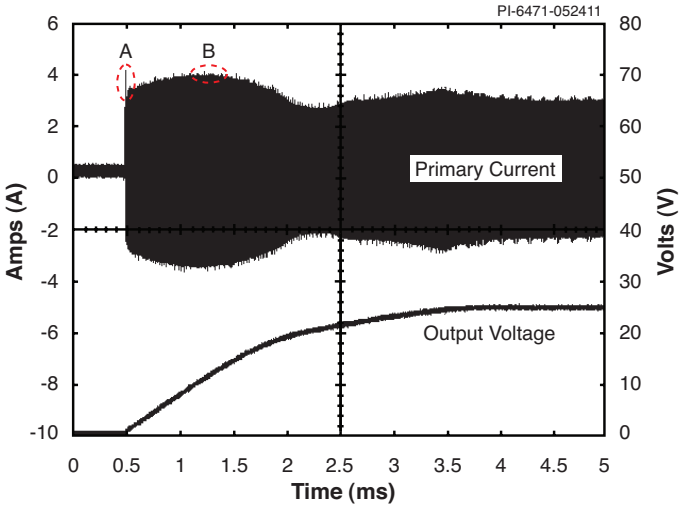


Figure 22. Typical Start-up Waveform. Observe Initial Current Spike 'A' to Ensure it is Below the 1-Cycle Current Limit. A Higher f_{MAX} Reduces it. Size the Soft-Start Capacitor so that the Peak of 'B' is just Below the Peak Current at $V_{BROWNOUT}$ at Full Load.

The "capacitive divider" circuit in Figure 23 reduces power dissipation and improves efficiency over a simple current sense resistor circuit. The two capacitors, main resonant capacitor C11, and sense capacitor C12, form a current divider. The portion of the primary current routed through C12 is

$$\frac{C12}{C11 + C12}.$$

Consequently, the voltage at the IS pin is equal to

$$I_P \times \frac{C12}{C11 + C12} \times R11,$$

where I_P is the primary current flowing from the HB pin through the transformer primary. The current in the sense capacitor passes through sense resistor R11. Resistor R11 is the main means for tuning current limit. The signal on R11, an AC voltage, passes through low-pass filter R12 and C7, to the IS pin. Note that R11 is returned to the GROUND pin and not to SOURCE pin.

The recommended series resistor value of 220 Ω and the bypass capacitor form a low-pass filter, and its time constant must not cause significant attenuation of the current sense signal at the nominal operating frequency. The effect of the attenuation is greatest for the first pulse in the start-up current waveform, and can also affect proper shutdown during short-circuit testing, which typically trips the 7-cycle current limit. Place a close-coupled probe across the IS pin bypass capacitor and compare the waveform to the primary current.

Burst Mode Operation and Tuning

Burst mode will produce a typical waveform such as in Figure 24. During the burst pulse train, the switching frequency rises from f_{START} to f_{STOP}.

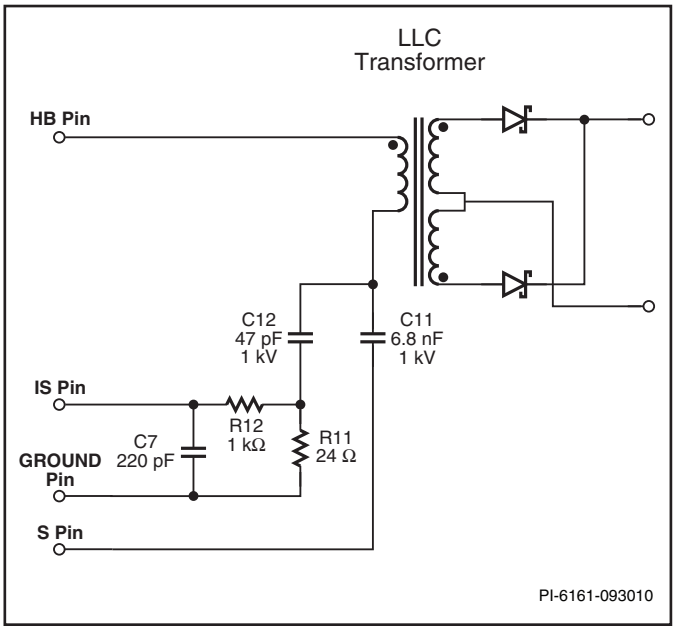


Figure 23. Capacitive Divider Current Sense Circuit.

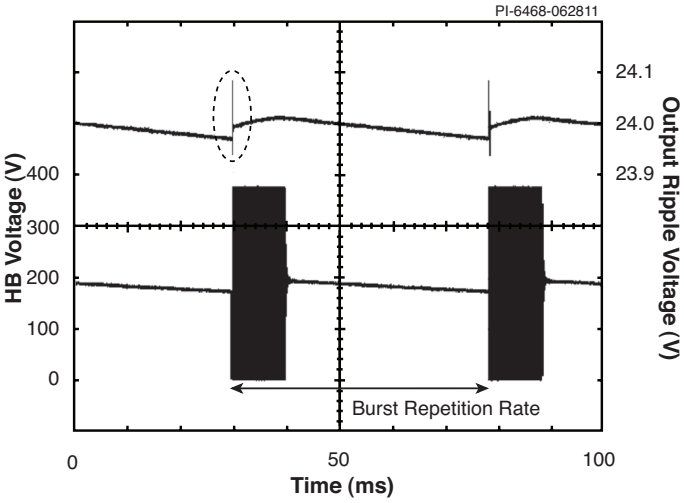


Figure 24. Typical Waveform of Burst Mode. 24 V / 150 W HiperLCS Design at Zero Load. The Initial Spike (circled) Size is Dependent on Post-Filter Electrolytic Capacitor ESR.

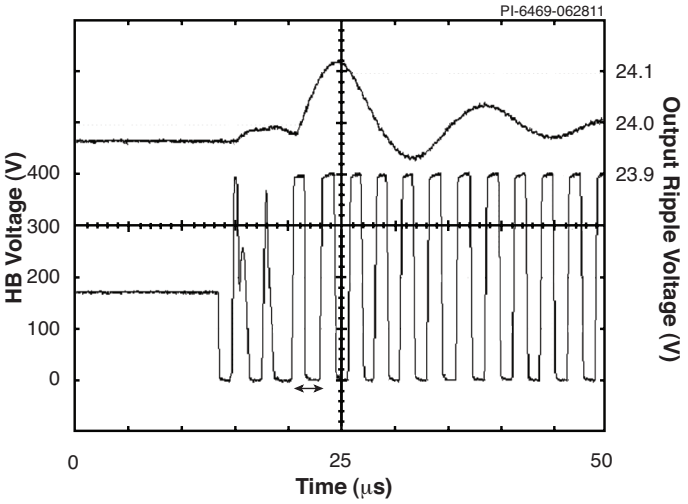


Figure 25. Zoom in of First Few Switching Cycles of Burst Pulse Train of Figure 24. The First 2 Cycles Show That the High-Side Driver has not Turned on yet. The Switching Frequency of the First Few Cycles is f_{START}, 335 kHz in This Case. The Ringing on the Output is from the Output Filter.

If the initial output ripple spike at the beginning of the burst pulse train is ignored, the output ripple somewhat resembles a sawtooth. See the output ripple waveform in Figure 24. When the HiperLCS is switching, the output rises. When it stops switching, the output falls. The top of the sawtooth is where the burst pulse train ends, because the feedback loop has commanded a frequency = f_{STOP}. The bottom of the sawtooth is where the burst pulse train begins, because the feedback loop has commanded a frequency = f_{START}. As such, the burst mode control resembles a hysteretic controller, where the top and bottom of the sawtooth are fixed by the feedback loop gain. The downward slope of the sawtooth is merely the output capacitors discharging into the load, with dv/dt:

$$I = C \times \frac{dv}{dt}$$

Where I = load current. C is the total output capacitance.

The upward slope of the sawtooth is dependent on the difference between the current delivered by the powertrain, and the current drawn by the load. For a given design, the upward slope increases with input voltage.

The burst repetition rate (frequency) then increases with load. When the load reaches a point where the powertrain can regulate at a frequency <f_{STOP}, the bursting will stop. When the load current decreases (from heavy load), frequency increases, and when it reaches f_{STOP}, bursting will commence.

In a typical design, f_{START} must be chosen to be at least 20-40% higher than the nominal switching frequency. Figure 18 shows the relationship between f_{START} and dead-time, and Table 5 the ratio of f_{STOP} to f_{START} vs. Burst Threshold setting number). In some cases the designer may choose to change dead-time slightly in order to change f_{START} and f_{STOP}. Some designs may only enter burst mode at zero load and an input voltage above nominal.

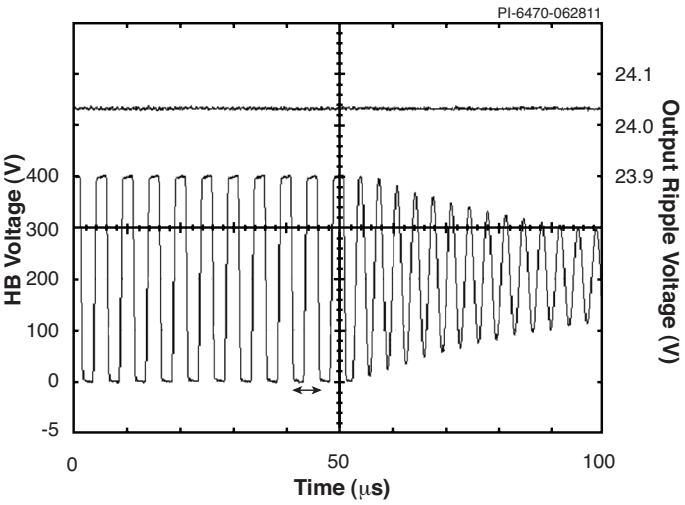


Figure 26. Zoom in of Last Few Switching Cycles of Burst Pulse Train of Figure 24. The Switching Frequency of the Last Few Cycles is f_{STOP}, 383 kHz in This Case (arrow). The Ringing in V_{HB} After Switching Stops, is the Primary Inductance Ringing with the MOSFET Capacitance.

Higher f_{START} will decrease the load threshold at which bursting begins, increase the input voltage threshold and decrease the output ripple in burst mode, but will increase the burst repetition rate, which may introduce audible noise in some combinations of line and load. The choice of f_{START} will affect the large signal transient response where the HiperLCS goes in and out of burst mode.

Absolute Maximum Ratings[6]

Instantaneous Repetitive D or HB Current[5] .....
.....V_{CC}, V_{CCH} = 11.5 V, T_J = 25 °C
LCS700..... .....5.2 A
LCS701..... ..... 7.7 A
LCS702..... ..... 10.3 A
LCS703 ..... 12.9 A
LCS705..... ..... 19.3 A
LCS708..... ..... 30.9 A
Instantaneous Repetitive D or HB Current[5] .....
..... V_{CC}, V_{CCH} = 11.5 V, T_J = 125 °C
LCS700..... .....4.2 A
LCS701..... .....6.2 A
LCS702..... .....8.3 A
LCS703 ..... 10.4 A
LCS705..... ..... 15.6 A
LCS708..... ..... 24.9 A
DRAIN Pin Voltage D[1] .....-1.3 V to 530 V
Half-bridge Voltage, HB[1].....-1.3 V to D + 0.5 V
Half-bridge Voltage Slew Rate, HB ..... 10 V/ns SUPPLY
Pin Voltage, VCC[1], VCCH[2] .....-0.3 V to 17.5 V
G Pin Voltage[1] ..... -0.3 V to 0.3 V
IS Pin Voltage[3] .....-0.65 to VREF + 0.3 V
DT/BF and FEEDBACK Pin Voltages[3]..... -0.3 to VREF + 0.3 V
OV/UV Pin Voltage[3].....-0.3 to VCC + 0.3 V
Pin Current (VREF, OV/UV, DT/BF, FEEDBACK, IS)..... ..... ±100 mA
Junction Temperature ..... -40 °C to 150 °C[7]
Storage Temperature .....-65 °C to 150 °C
Lead Temperature[4] ..... 260 °C
ESD Rating (JESD22-A114-B, HBM) ..... 2 kV

Notes:
1. Voltage referenced to S.
2. Voltage referenced to HB.
3. Voltage referenced to G.
4. 1/16 inch from case for 5 seconds.
5. One-cycle peak current can exceed repetitive maximum current for $t < 460$ ns if $T_J < 100$ °C and drain voltage ≤ 400 VDC.
6. The absolute maximum voltage rating for all pins is as specified. This is an absolute maximum condition which must not be exceeded. Voltages between the maximum operating condition and this absolute maximum rating condition should be infrequent and short in duration (e.g. as in a temporary fault condition). These conditions are not intended as a guarantee of the reliability of the product up to the absolute maximum rating, but as a guideline for the level of maximum applied voltage beyond which there is a risk of immediate damage to the product.
7. The Absolute Maximum Junction Temperature is the temperature beyond which device damage (latent or otherwise) may occur.

Thermal Resistance

Junction to Case Thermal Resistance[1,3]:
LCS700 (θ_{JC}).....7.6 °C/W
LCS701 (θ_{JC})..... .....7.0 °C/W
LCS702 (θ_{JC})..... ..... 6.6 °C/W
LCS703 (θ_{JC}) ..... 6.2 °C/W
LCS705 (θ_{JC})..... ..... 5.9 °C/W
LCS708 (θ_{JC})..... ..... 5.5 °C/W
Junction to heat sink Thermal Resistance[1,2]:
LCS700 (θ_{JH})..... .....10.1 °C/W
LCS701 (θ_{JH})..... 9.5 °C/W
LCS702 (θ_{JH})..... ..... 9.1 °C/W
LCS703 (θ_{JH})..... ..... 8.7 °C/W
LCS705 (θ_{JH})..... ..... 8.4 °C/W
LCS708 (θ_{JH})..... ..... 8.0 °C/W
Hottest Junction to OT Sensor Thermal Offset[1,2,4]:
LCS700 (ΔT_{J-OT})..... 4.6 °C/W
LCS701 (ΔT_{J-OT})..... ..... 4.0 °C/W
LCS702 (ΔT_{J-OT})..... ..... 3.5 °C/W
LCS703 (ΔT_{J-OT}) ..... 3.2 °C/W
LCS705 (ΔT_{J-OT})..... ..... 2.8 °C/W
LCS708 (ΔT_{J-OT})..... ..... 2.5 °C/W

Notes:
1. Both power switches each dissipating half the total power.
2. Mounted to an aluminum heat sink with uniform coverage of Thermalloy thermal paste. Mounting clip with normal force > 30 N applied to the center of the package.
3. Junction to case thermal resistance is based on hottest junction, case temperature measured at center of package back surface.
4. Temperature difference between hottest junction and over-temperature sensor.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 °C to 125 °C[D] V_{CC} = 12 V, V_{CCH} = 12 V (Unless Otherwise Specified)		Min	Typ	Max	Units
Half-Bridge							
OFF-State Current	I_{DSS}	Measured from D to HB or from HB to S T_J = 100 °C, V_{CC} = 12 V, V_{CCH} = 12 V, V_D = 424 V	LCS700			60	µA
			LCS701			60	
			LCS702			65	
			LCS703			80	
			LCS705			120	
			LCS708			200	
Breakdown Voltage	BV_{DSS}	V_{CC} = 12 V, V_{CCH} = 12 V, 250 mA, T_J = 25 °C Measured from D to HB or from HB to S		530			V

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 °C to 125 °C(D) V_{CC} = 12 V, V_{CCH} = 12 V (Unless Otherwise Specified)		Min	Typ	Max	Units
Half-Bridge (cont.)							
Breakdown Voltage Temperature Coefficient	$BV_{DSS(TC)}$	Measured from D to HB or from HB to S			0.2		V/°C
ON-State Resistance	$R_{DS(ON)}$	Measured from D to HB or from HB to S V_{CC} = 12 V, V_{CCH} = 12 V, T_J = 25 °C	LCS700, I = 0.8 A		1.53	1.82	Ω
			LCS701, I = 1.2 A		1.00	1.24	
			LCS702, I = 1.6 A		0.74	0.92	
			LSC703, I = 2.0 A		0.60	0.73	
			LCS705, I = 3.0 A		0.40	0.49	
			LCS708, I = 4.8 A		0.26	0.31	
ON-State Resistance	$R_{DS(ON)}$	Measured from D to HB or from HB to S V_{CC} = 12 V, V_{CCH} = 12 V, T_J = 100 °C	LCS700, I = 0.8 A		2.15	2.63	Ω
			LCS701, I = 1.2 A		1.42	1.78	
			LCS702, I = 1.6 A		1.05	1.33	
			LCS703, I = 2.0 A		0.85	1.06	
			LCS705, I = 3.0 A		0.58	0.71	
			LCS708, I = 4.8 A		0.36	0.45	
Half-Bridge Capacitance	C_{HB}	Effective half-bridge capacitance. V_{HB} swinging from 0 V to 400 V or 400 V to 0 V, See Note A	LCS700		134		pF
			LCS701		201		
			LCS702		268		
			LCS703		335		
			LCS705		503		
			LCS708		804		
Diode Forward Voltage	V_{FWD}	Measured from HB to D or from S to HB T_J = 125 °C	LCS700, I = 0.8 A		1.15		V
			LCS701, I = 1.2 A		1.15		
			LCS702, I = 1.6 A		1.15		
			LSC703, I = 2.0 A		1.15		
			LCS705, I = 3.0 A		1.15		
			LCS708, I = 4.8 A		1.15		
Power Supply							
VCC Supply Voltage Range	V_{CC}	See Note C		11.4	12	15	V
VCCH Supply Voltage Range	V_{CCH}	See Note C		11.4	12	15	V
Start-Up Current	$I_{CC(OFF)}$	Undervoltage lockout state: V_{CC} = 7 V			120	170	µA
Inhibit Current	$I_{CC(INHIBIT)}$	V_{CC} = 12 V, OV/UV < $V_{SD(L)}$			450	650	µA
VCC Operating Current	$I_{CC(ON)}$	Typical at V_{CC} = 12 V Maximum at V_{CC} = 15 V Measured at 300 kHz, HB Open and V_D = 15 V	LCS700		2.8	5.2	mA
			LCS701		3.3	5.8	
			LCS702		3.8	6.5	
			LCS703		4.2	7.1	
			LCS705		5.4	8.8	
			LCS708		7.4	11.8	
VCCH Operating Current	$I_{CCH(ON)}$	Typical at V_{CCH} = 12 V Maximum at V_{CCH} = 15 V Measured at 300 kHz, HB Open and V_D = 15 V	LCS700		2.4	4.6	mA
			LCS701		2.9	5.2	
			LCS702		3.3	5.8	
			LSC703		3.7	6.4	
			LCS705		4.8	7.9	
			LCS708		6.8	10.7	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 °C to 125 °C(D) V_{CC} = 12 V, V_{CCH} = 12 V (Unless Otherwise Specified)	Min	Typ	Max	Units
VCCH Supply Undervoltage Lockout						
VCC Start Threshold	$V_{UVLO(+)}$	Device exits UVLO state when V_{CC} exceeds UVLO+, T_J = 0 to 100 °C	10	10.5	11.4	V
VCC Shutdown Threshold	$V_{UVLO(-)}$	Device enters UVLO state when V_{CC} falls below UVLO+, T_J = 0 to 100 °C	9.1	9.5	10.5	V
VCC Start-Up/ Shutdown Hysteresis	$V_{UVLO(HYST)}$	T_J = 0 to 100 °C	0.7	1.0	1.2	V
VCCH Start Threshold	$V_{UVLO(H+)}$	Driver exits UVLO state when V_{CCH} exceeds UVLOH+	8.2	8.5	8.9	V
VCCH Shutdown Threshold	$V_{UVLO(H-)}$	Driver enters UVLO state when V_{CCH} falls below UVLOH-	7.2	7.5	7.9	V
VCCH Start-Up/Shutdown Hysteresis	$V_{UVLO(H)HYST}$		0.8	1.0	1.2	V
High-Voltage Supply Undervoltage/Overvoltage Enable						
OV/UV Overvoltage Shutdown Threshold	$V_{OV(H)}$	Overvoltage assertion threshold	129	131	133	% of $V_{SD(H)}$
OV/UV Overvoltage Recovery Threshold	$V_{OV(L)}$	Overvoltage de-assertion threshold	124	126	128	% of $V_{SD(H)}$
OV/UV Undervoltage Start Threshold	$V_{SD(H)}$	Undervoltage de-assertion threshold	2.35	2.40	2.45	V
OV/UV Undervoltage Shutdown Threshold	$V_{SD(L)}$	Undervoltage assertion threshold	77	79	81	% of $V_{SD(H)}$
OV/UV Pin Input Resistance	$R_{IN(OVUV)}$	OV/UV pin resistance to G T_J = 25 °C	4.0	5.0	6.0	MΩ
OV/UV Pin Input Resistance Temperature Coefficient	$R_{IN(OVUVTC)}$			-0.4		%/°C
Reference						
Reference Voltage	V_{REF}	I_{REF} = 4 mA	3.20	3.40	3.50	V
Current Source Capability of VREF Pin	I_{REF}				4	mA
V_{REF} Capacitance	C_{REF}	Required external coupling on VREF pin	1			µF
LLC Oscillator						
Frequency Range	F_{RANGE}		25		1000	kHz
Accuracy of Minimum Frequency Limit	$F_{MIN(ACC)}$	R_{FB} = 37.9 kΩ to V_{REF}, 180 kHz	-5.0		5.0	%
	$F_{MIN(ACL)}$	R_{FB} = 154 kΩ to V_{REF}, 48 kHz T_J = 25 °C	-7.5		7.5	
Accuracy of Maximum Frequency Limit	$F_{MAX(ACC)}$	I_{FB} = $I_{DT/BF}$, R_{FMAX} = 12.5 kΩ, F_{MAX} = 510 kHz, T_J = 0 to 100 °C	-7.5		7.5	%
Duty Balance	D_{LLC}	Duty symmetry of the half-bridge waveform, C_{FB} = 4.7 nF, $C_{DT/BF}$ = 4.7 nF, 250 kHz Use recommended layout	49		51	%
Dead-Time[B]	t_D	R_{FMAX} = 7 kΩ, R_{BURST} = 39.6 kΩ		330		ns
DT/BF Control Current Range	$I_{DT/BF}$		30		430	µA

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 °C to 125 °C[D] V_{CC} = 12 V, V_{CCH} = 12 V (Unless Otherwise Specified)	Min	Typ	Max	Units
LLC Oscillator (cont.)						
I_{FB} Threshold to Stop LLC Switching	I_{STOP1}	Threshold applies after exiting soft-start mode for burst setting BT1		52.0		% of $I_{DT/BF}$
	I_{STOP2}	Threshold applies after exiting soft-start mode for burst setting BT2		46.0		
	I_{STOP3}	Threshold applies after exiting soft-start mode for burst setting BT3		39.0		
I_{FB} Threshold Hysteresis	$I_{BURST(HYST)}$	I_{START} is $I_{BURST(HYST)}$ below I_{STOP}	5	6.8	8	% of $I_{DT/BF}$
DT/BF Voltage to Program Burst Setting	V_{BT1}	Required $V_{DT/BF}$ at start-up to enable burst setting BT1	93.5	95	96.3	% of V_{REF}
	V_{BT2}	Required $V_{DT/BF}$ at start-up to enable burst setting BT2	88.5	90	91.3	
	V_{BT3}	Required $V_{DT/BF}$ at start-up to enable burst setting BT3	83.5	85	86.3	
Time Constant for the Combination of R_{FMAX}, R_{BURST} and the Decoupling Cap on DT/BF	$RC_{DT/BF}$	This time constant must be less than the specified maximum to ensure correct setting of burst mode.			100	µs
Feedback Current Maximum	I_{FB}	Determines the maximum control frequency that can be set by I_{FB}		100		$\%I_{DT/BF}$
Feedback Control Current Range	I_{FB}	I_{FB} is limited by the current into DT/BF	15		430	µA
Feedback Virtual Voltage	V_{FB}	FB input appears as $R_{IN(FB)}$ in series with V_{FB}, 30 µA < I_{FB} < $I_{DT/BF}$		0.65		V
Feedback Input Resistance	$R_{IN(FB)}$	FB input appears as $R_{IN(FB)}$ in series with V_{FB}, 30 µA < I_{FB} < $I_{DT/BF}$		2.5		kΩ
Feedback Input Resistance During Soft-Start	$R_{FB(SS)}$	FB input appears as $R_{FB(SS)}$ in series with V_{REF} during the soft-start delay interval or when OV/UV < V_{SD} or OV/UV > V_{OV}		750		Ω
Over-Current Protection						
Fast Over-Current Fault Voltage Threshold[4]	$V_{IS(F)}$		0.855	0.905	0.955	V
Slow Over-Current Fault Voltage Threshold	$V_{IS(S)}$	7 LLC clock cycle debounce	0.455	0.505	0.555	V
Over-Current Fault Pulse Width	t_{IS}	Minimum time V_{IS} exceeds $V_{IS(F)}$/$V_{IS(S)}$ per cycle to trigger fault protection		30		ns
Over-Temperature Protection						
Over-Temperature Shutdown Threshold[A]	T_{OT}			125		°C

NOTES:
A. Guaranteed by design.
B. Typical apparent dead-time at the HB pin under resonant ZVS conditions.
C. VCC/VCCH operating range to achieve power capabilities specified in data sheet power table.
D. Operation possibly limited by over-temperature shutdown.

Typical Performance Characteristics

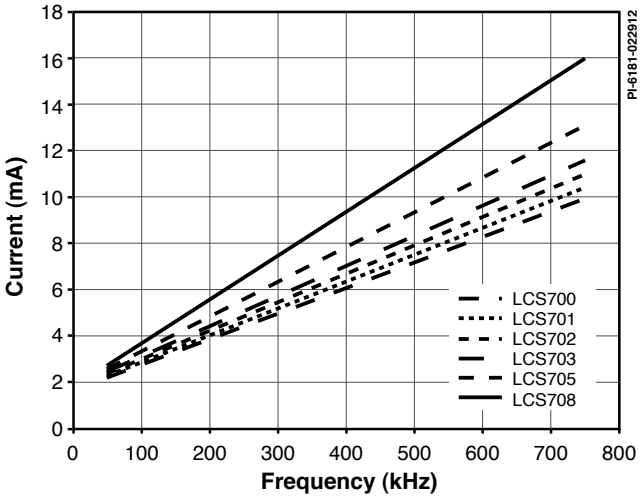


Figure 27. V_{CC} Current vs. Frequency.

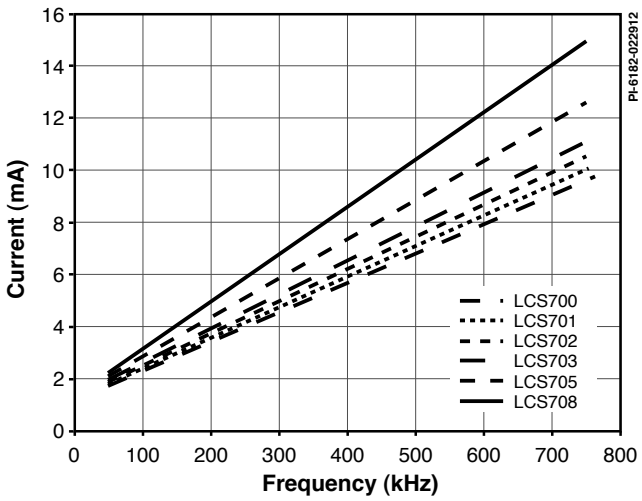


Figure 28. V_{CCH} Current vs. Frequency.

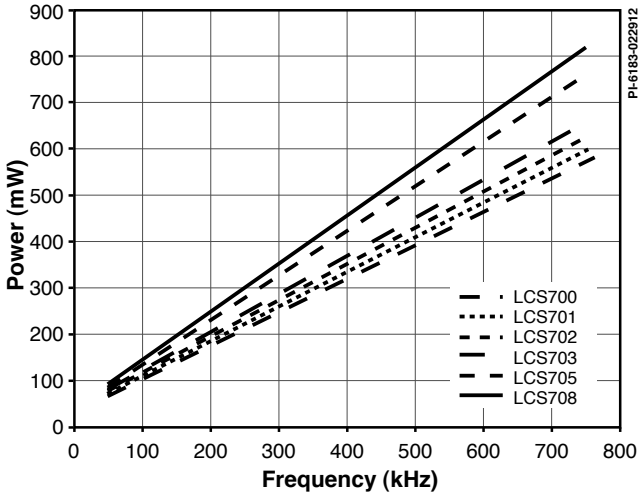


Figure 29. Control Power vs. Frequency.

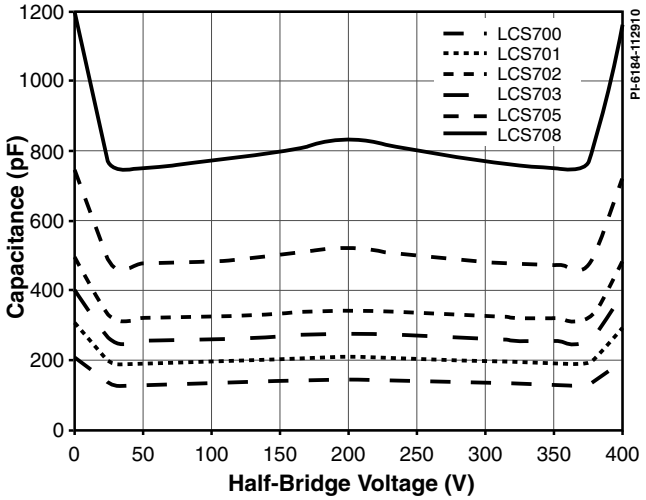


Figure 30. Half-Bridge Small Signal Capacitance vs. Half-Bridge Voltage.

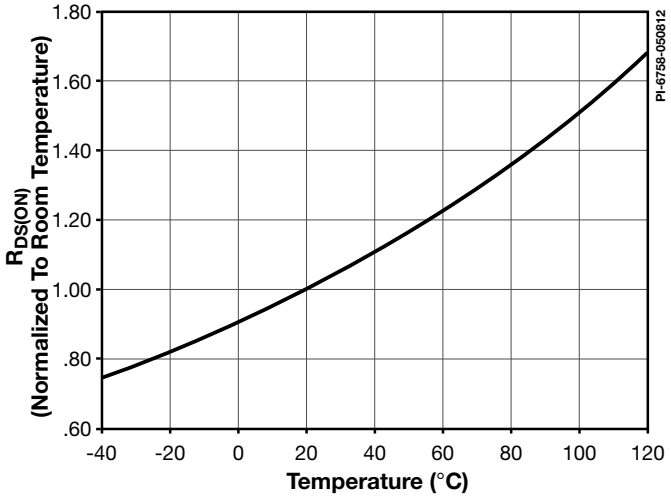


Figure 31. Normalized $R_{DS(ON)}$ vs. Temperature.

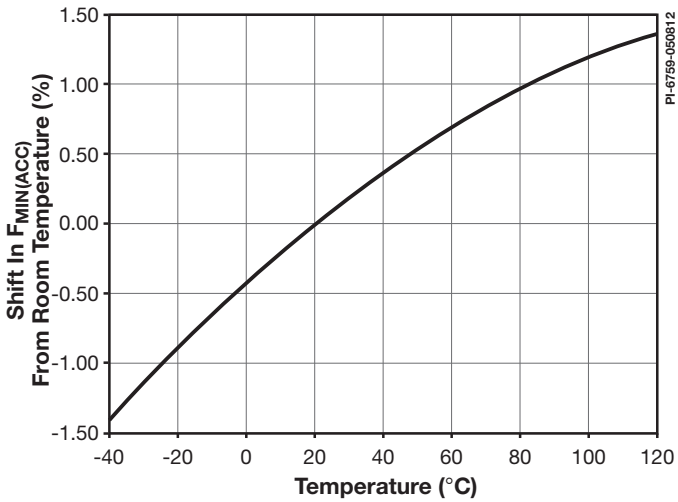


Figure 32. Typical $F_{MIN(ACC)}$ Shift vs. Temperature.

Typical Performance Characteristics

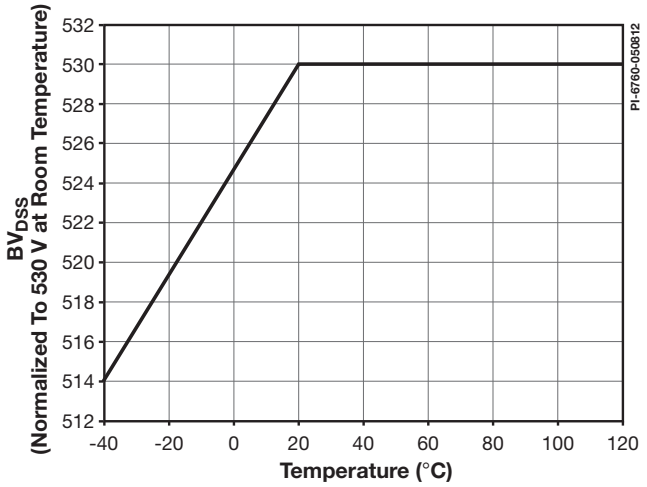


Figure 33. Normalized BV_{DSS} vs. Temperature.

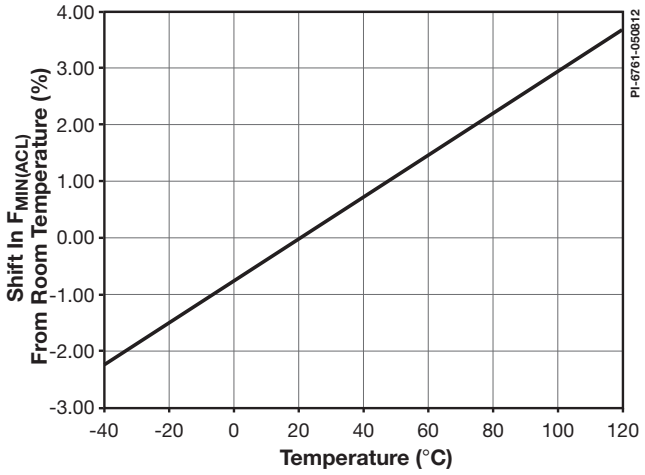


Figure 34. Typical $F_{MIN(ACL)}$ vs. Temperature.

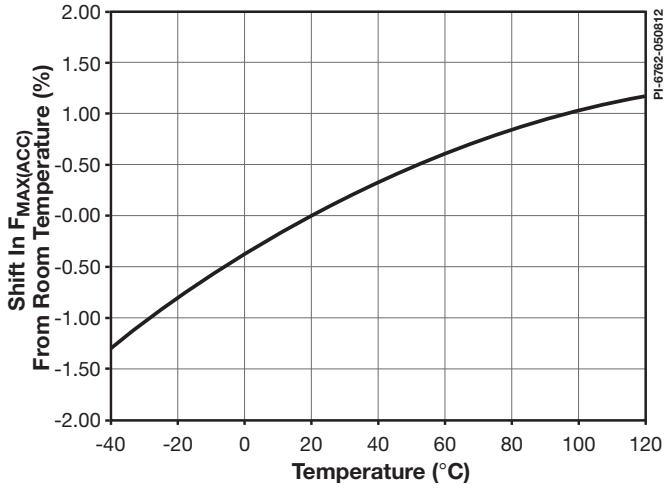


Figure 35. Typical $F_{MAX(ACC)}$ vs. Temperature.

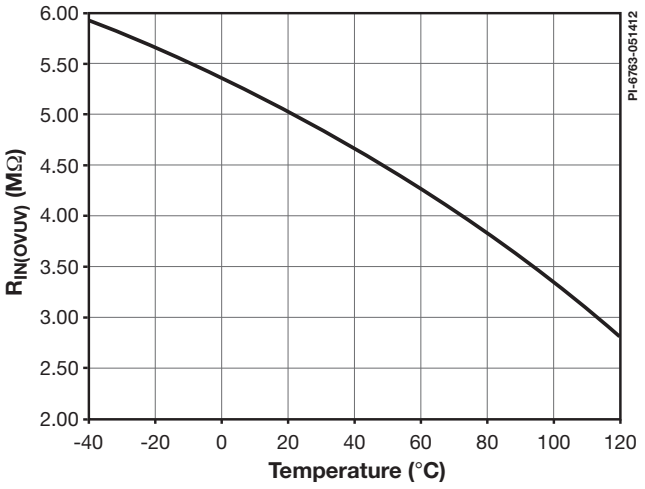


Figure 36. Typical $R_{IN(OVUV)}$ vs. Temperature.

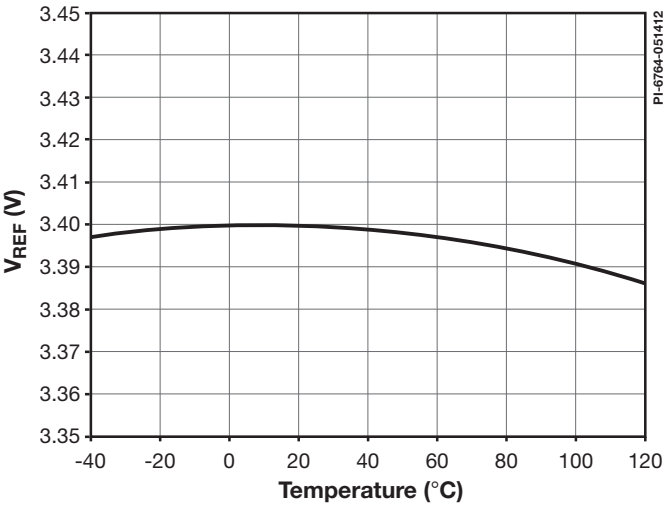


Figure 37. Typical V_{REF} vs. Temperature.

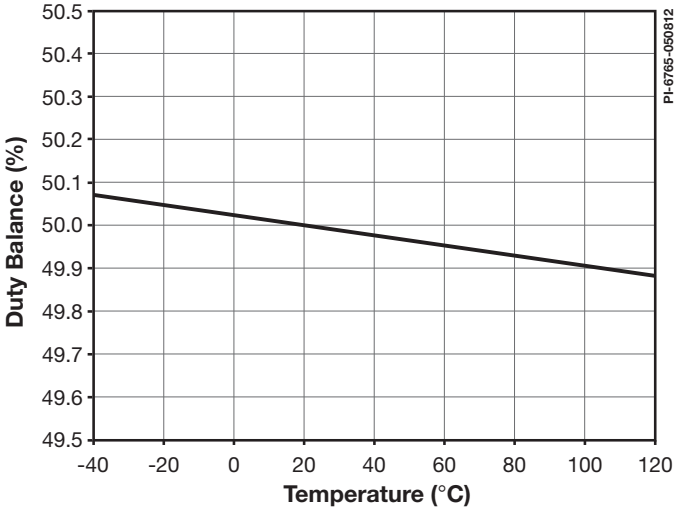


Figure 38. Typical Duty Balance vs. Temperature.

Typical Performance Characteristics

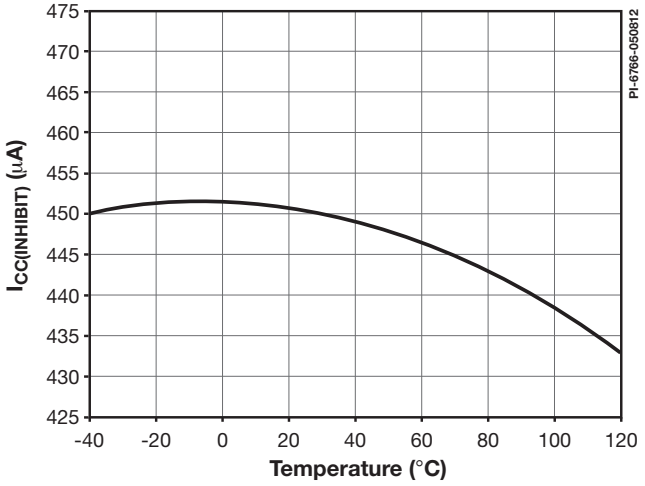


Figure 39. Typical $I_{CC(INHIBIT)}$ vs. Temperature.

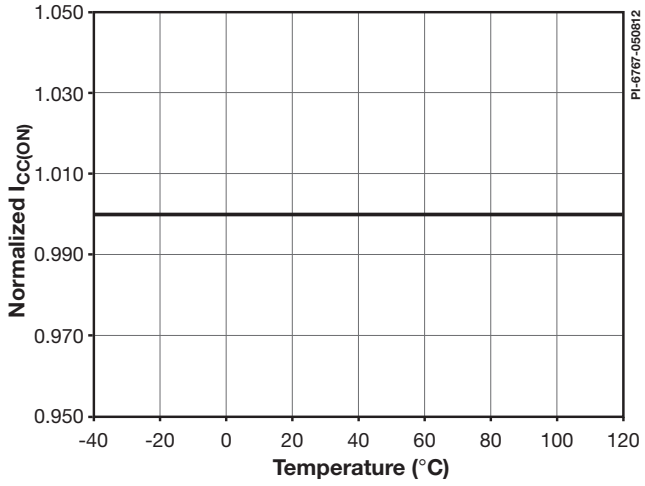


Figure 40. Normalized $I_{CC(ON)}$ vs. Temperature.

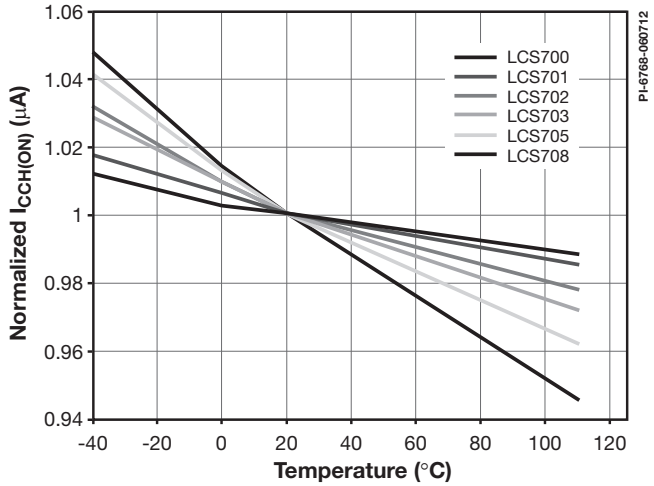


Figure 41. Typical $I_{CCH(ON)}$ vs. Temperature (Normalized to Room Temperature).

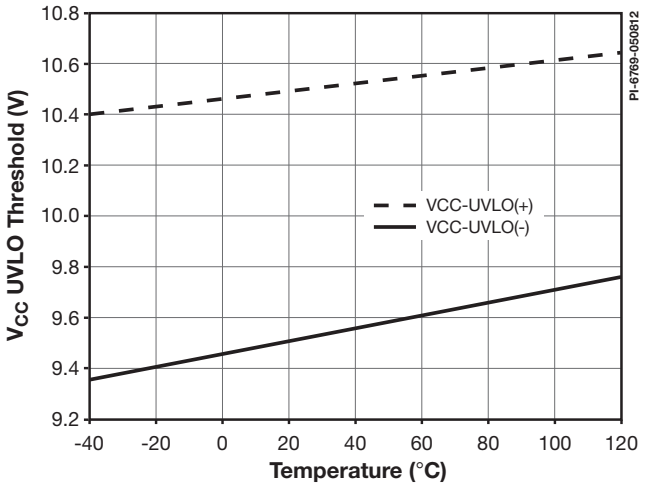


Figure 42. Typical V_{CC} UVLO vs. Temperature.

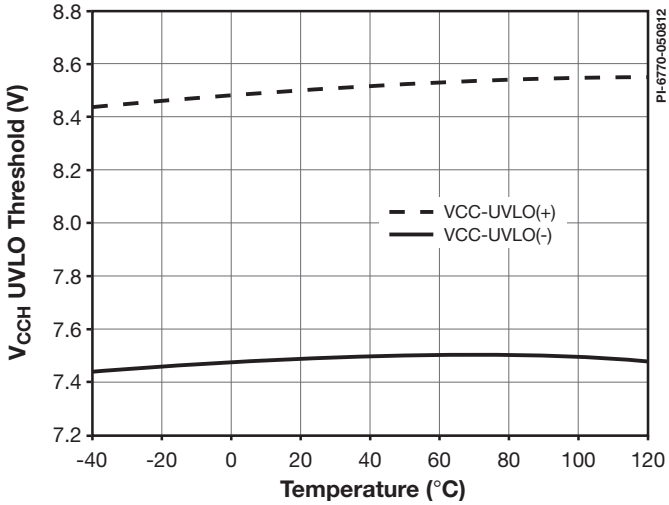
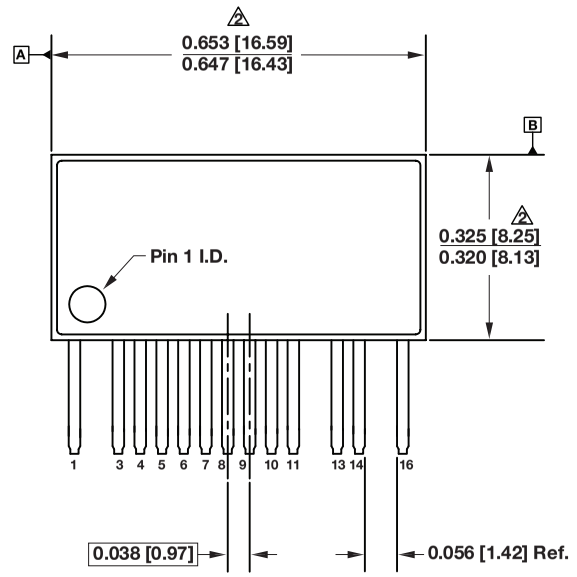
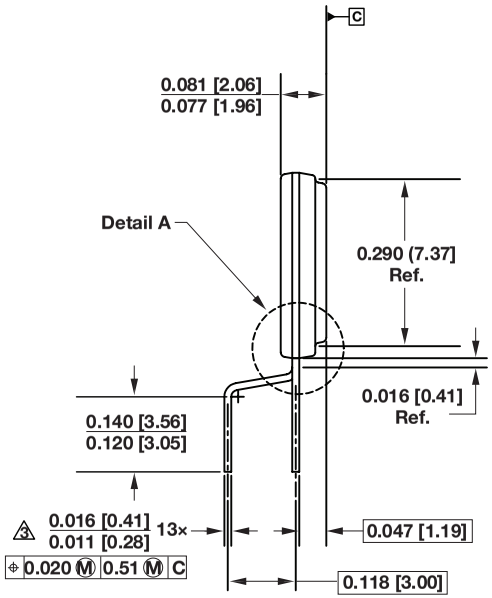


Figure 43. Typical V_{CCH} UVLO vs. Temperature.

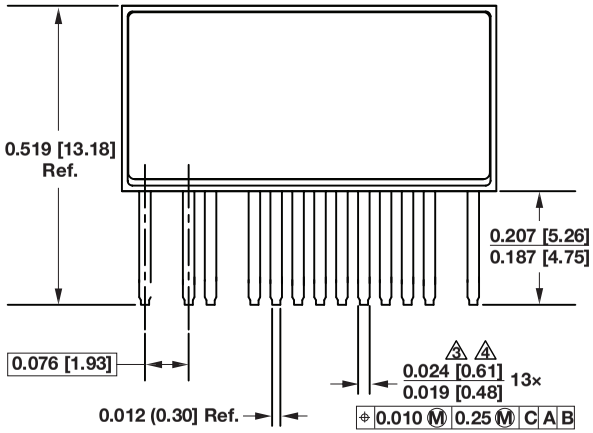
eSIP-16J (H Package)



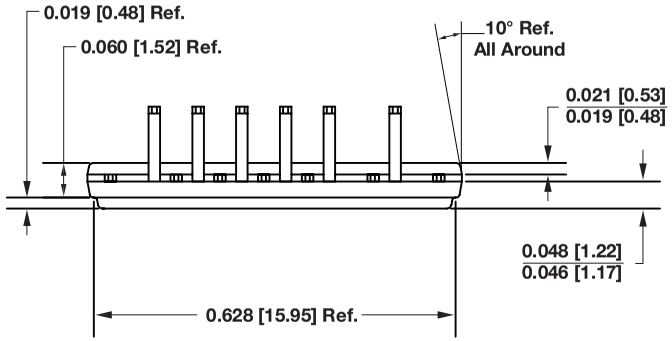
FRONT VIEW



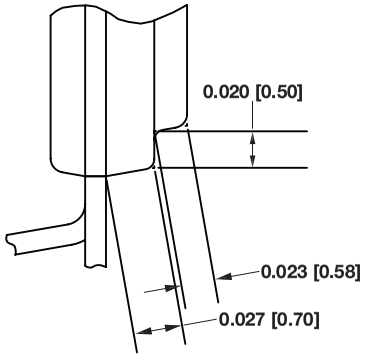
SIDE VIEW



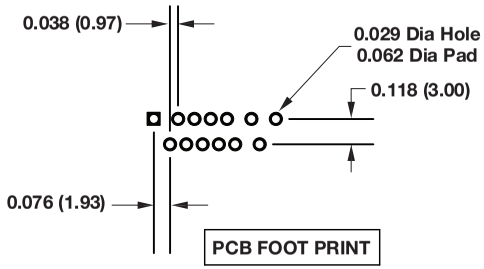
BACK VIEW



END VIEW



Detail A (Scale = 9×)



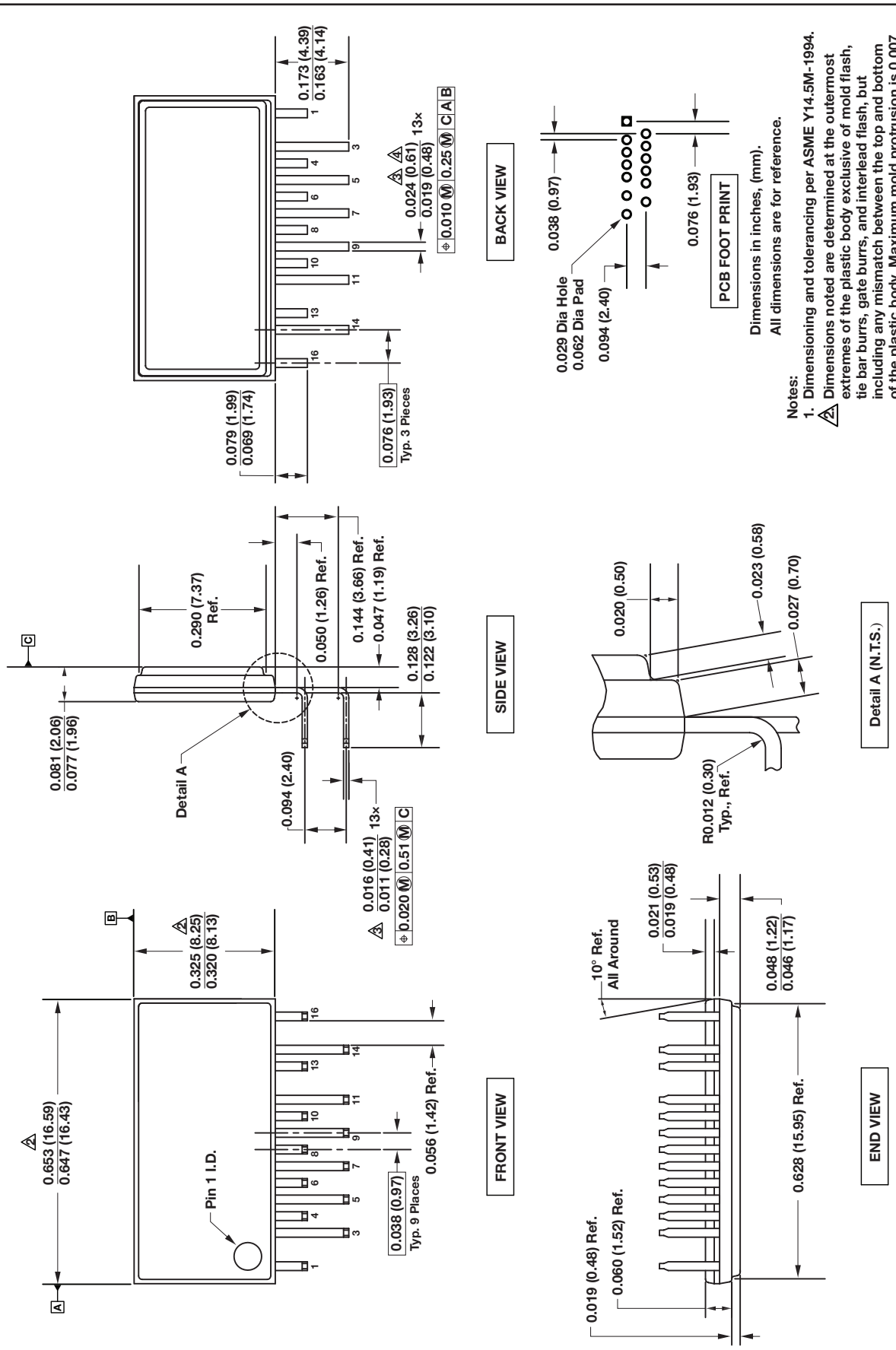
PCB FOOT PRINT

Dimensions in inches, (mm).
All dimensions are for reference.

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include interlead flash or protrusions.
5. Controlling dimensions in inches [mm].

PI-6632-120211

eSIP-16K (L Package)

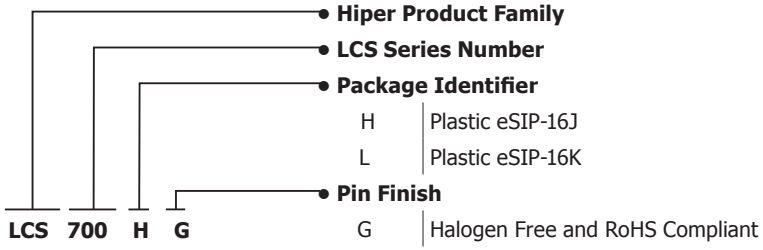


Dimensions in inches, (mm).
All dimensions are for reference.

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include interlead flash or protrusions.
5. Controlling dimensions in inches (mm).

PI-6454-020212

Part Ordering Information



Revision	Notes	Date
B	Initial Release.	06/20/11
C	Added L bend parts.	02/12
C1	Removed backside metal H package option.	06/12
D	Not implemented.	
E	Overmold change, extended temperature change.	06/12
E	Updated $BV_{DSS(TC)}$ unit, Junction Temperature range and added Note 7.	08/30/12
E	Corrected error in Figure 3.	12/02/14
F	Updated with new Brand Style.	06/15
G	Added LG package parts for LCS705 and LCS708.	05/17