

200 mA very low quiescent current linear regulator IC



DFN4 1x1



SOT23-5L

Features

- Input voltage from 1.5 to 5.5 V
- Ultra low dropout voltage (200 mV typ. at 200 mA load)
- Very low quiescent current (20 μ A typ at no load, 0.03 μ A typ in off mode)
- Output voltage tolerance: $\pm 0.5\%$ (A version) or $\pm 2.0\%$ @ 25 °C (standard version)
- 200 mA guaranteed output current
- High PSRR (80 dB@1 kHz, 50 db@100 kHz)
- Wide range of output voltages available on request: from 0.8 V up to 5.0 V in 50 mV step
- Logic-controlled electronic shutdown
- Internal soft-start
- Optional output voltage discharge feature
- Compatible with ceramic capacitor $C_{OUT} = 0.47\ \mu$ F
- Internal current limit and thermal protections
- Available in DFN4 1x1 and SOT23-5L packages
- Operating temperature range: -40 °C to 125 °C

Applications

- Mobile phones
- Tablets
- Digital still cameras (DSC)
- Cordless phones and similar battery-powered systems
- Portable media players

Maturity status link

[LD39020](#)

Description

The [LD39020](#) high accuracy voltage regulator provides 200 mA of maximum current from an input voltage ranging from 1.5 V to 5.5 V, with a typical dropout voltage of 200 mV.

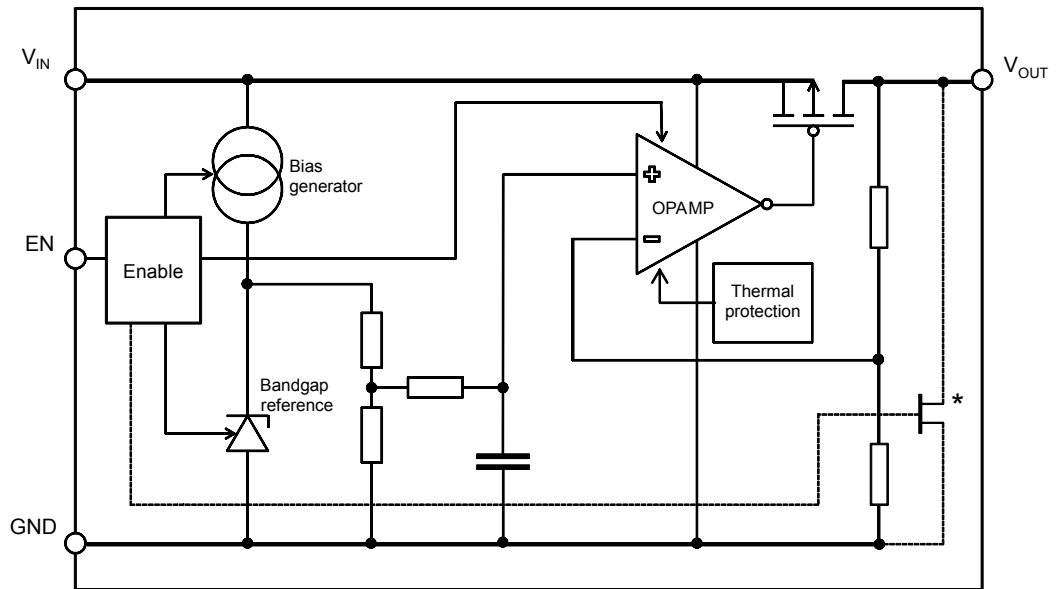
It is available in DFN4 1x1 and SOT23-5L packages, allowing the maximum space saving.

The device is stabilized with a ceramic capacitor on the output. The ultra low drop voltage, low quiescent current and low noise features, together with the internal soft-start circuit, make the [LD39020](#) suitable for low power battery-operated applications.

An enable logic control function puts the [LD39020](#) in shutdown mode allowing a total current consumption lower than 0.1 μ A. Constant current and thermal protection are provided.

1 Diagram

Figure 2. Block diagram



AM13852V1

Note: The output discharge MOSFET is optional.

2 Pin configuration

Figure 3. Pin connection (top view)

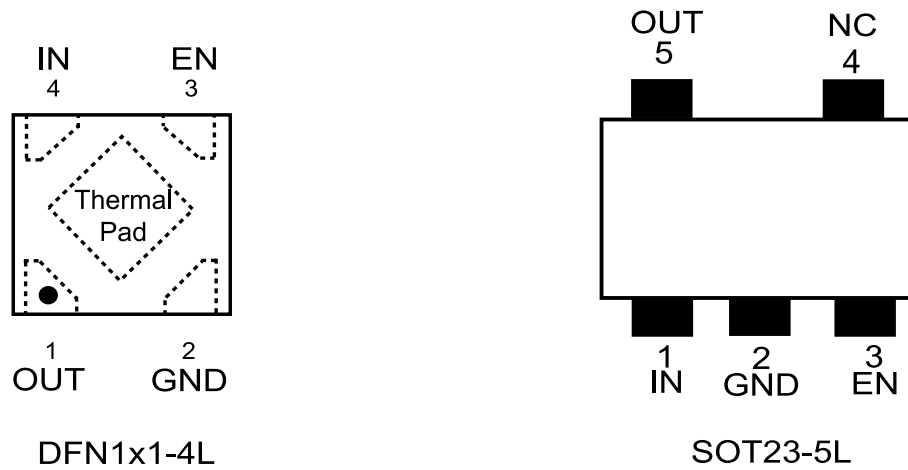
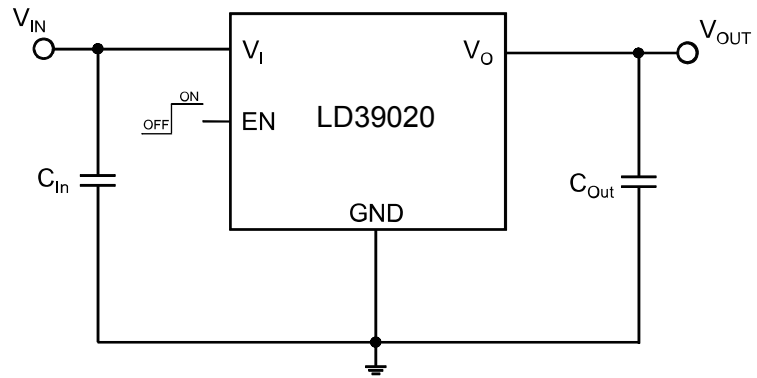


Table 1. Pin description

Pin DFN4 1x1	Pin SOT23-5L	Symbol	Function
1	5	OUT	Output voltage
2	2	GND	Common ground
3	3	EN	Enable pin logic input: Low = shutdown, High = active
4	1	IN	Input voltage
Thermal pad	-	GND	Connect to GND on the PCB
-	4	NC	Not internally connected

3 Typical application

Figure 4. Typical application circuits



4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input voltage	- 0.3 to 7	V
V_{OUT}	Output voltage	- 0.3 to $V_{IN} + 0.3$	V
V_{EN}	Enable input voltage	- 0.3 to 7	V
I_{OUT}	Output current	Internally limited	mA
P_D	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	- 40 to 150	°C
T_{OP}	Operating junction temperature range	- 40 to 125	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient, DFN4 1x1	250	°C/W
R_{thJC}	Thermal resistance junction-case, SOT23-5L	81	°C/W
R_{thJA}	Thermal resistance junction-ambient, SOT23-5L	255	°C/W

Table 4. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD Protection voltage	HBM	4	kV
		MM	400	V
		CDM	500	V

5 Electrical characteristics

$T_J = 25\text{ }^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$, $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, unless otherwise specified.

Table 5. Electrical characteristics for LD39020T, LD39020DT

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		1.5		5.5	V
V_{OUT}	V_{OUT} accuracy	$I_{OUT} = 1\text{ mA}$, $T_J = 25\text{ }^\circ\text{C}$	-2		2	%
		$I_{OUT} = 1\text{ mA}$, $-40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$	-3		3	%
ΔV_{OUT}	Static line regulation ⁽¹⁾	$V_{OUT(NOM)} + 1\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $I_{OUT} = 10\text{ mA}$		0.02		%/V
		$-40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$			0.2	
ΔV_{OUT}	Static load regulation	$I_{OUT} = 0\text{ mA to } 200\text{ mA}$		10		mV
		$-40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$			0.01	%/mA
V_{DROP}	Dropout voltage	$I_{OUT} = 30\text{ mA}$, $V_{OUT} = 2.8\text{ V}$		35		mV
		$I_{OUT} = 200\text{ mA}$, $V_{OUT} = 2.8\text{ V}$ $-40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$		200	350	
e_N	Output noise voltage	10 Hz to 100 kHz, $I_{OUT} = 10\text{ mA}$		45		$\mu\text{V}_{RMS}/V_{OUT}$
SVR	Supply voltage rejection	$V_{IN} = V_{OUT(NOM)} + 1\text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.2\text{ V}$ Freq. = 1 kHz $I_{OUT} = 30\text{ mA}$		80		dB
		$V_{IN} = V_{OUT(NOM)} + 1\text{ V} \pm V_{RIPPLE}$, $V_{RIPPLE} = 0.2\text{ V}$ Freq. = 100 kHz, $I_{OUT} = 30\text{ mA}$		55		
I_Q	Quiescent current	$I_{OUT} = 0\text{ mA}$		20	40	μA
		$I_{OUT} = 200\text{ mA}$		100		
$I_{Standby}$	Standby current	V_{IN} input current in OFF MODE: $V_{EN} = \text{GND}$		0.03	1	μA
I_{SC}	Short circuit current	$R_L = 0$	250	350		mA
R_{ON}	Output voltage discharge MOSFET	(only on LD39020DT)		100		Ω
V_{EN}	Enable input logic low	$V_{IN} = 1.5\text{ V to } 5.5\text{ V}$ $-40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$			0.4	V
	Enable input logic high	$V_{IN} = 1.5\text{ V to } 5.5\text{ V}$ $-40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$	1			
I_{EN}	Enable pin input current	$V_{EN} = V_{IN}$			100	nA
T_{ON} ⁽²⁾	Turn on time			100		μs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T _{SHDN}	Thermal shutdown			160		°C
	Hysteresis			20		
C _{OUT}	Output capacitor	Capacitance see Figure 18. Stability area vs. (C _{OUT} , ESR)	0.47		22	μF

1. Not applicable for $V_{out(nom)} > 4.5\text{ V}$
2. Turn-on time is time measured between the enable input just exceeding V_{EN} high value and the output voltage just reaching 95 % of its nominal value

$T_J = 25\text{ °C}$, $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$, $C_{IN} = C_{OUT} = 1\text{ μF}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, unless otherwise specified.

Table 6. Electrical characteristics for LD39020AT, LD39020ADT

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{IN}	Operating input voltage		1.5		5.5	V
V _{OUT}	V _{OUT} accuracy	$I_{OUT} = 1\text{ mA}$, $T_J = 25\text{ °C}$	-0.5		0.5	%
		$I_{OUT} = 1\text{ mA}$, $-40\text{ °C} < T_J < 125\text{ °C}$	-1.5		1.5	%
ΔV _{OUT}	Static line regulation ⁽¹⁾	$V_{OUT(NOM)} + 1\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $I_{OUT} = 10\text{ mA}$		0.02		%/V
		$-40\text{ °C} < T_J < 125\text{ °C}$			0.2	
ΔV _{OUT}	Static load regulation	$I_{OUT} = 0\text{ mA}$ to 200 mA		10		mV
		$-40\text{ °C} < T_J < 125\text{ °C}$			0.01	%/mA
V _{DROP}	Dropout voltage	$I_{OUT} = 30\text{ mA}$, $V_{OUT} = 2.8\text{ V}$		35		mV
		$I_{OUT} = 200\text{ mA}$, $V_{OUT} = 2.8\text{ V}$ $-40\text{ °C} < T_J < 125\text{ °C}$		200	350	
e _N	Output noise voltage	10 Hz to 100 kHz, $I_{OUT} = 10\text{ mA}$		45		μV _{RMS} / V _{OUT}
SVR	Supply voltage rejection	$V_{IN} = V_{OUT(NOM)} + 1\text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.2\text{ V}$ Freq. = 1 kHz $I_{OUT} = 30\text{ mA}$		80		dB
		$V_{IN} = V_{OUT(NOM)} + 1\text{ V} \pm V_{RIPPLE}$, $V_{RIPPLE} = 0.2\text{ V}$ Freq. = 100 kHz, $I_{OUT} = 30\text{ mA}$		55		
I _Q	Quiescent current	$I_{OUT} = 0\text{ mA}$		20	40	μA
		$I_{OUT} = 200\text{ mA}$		100		
I _{Standby}	Standby current	V _{IN} input current in OFF MODE: V _{EN} = GND		0.03	1	μA
I _{SC}	Short circuit current	R _L = 0	250	350		mA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{ON}	Output voltage discharge MOSFET	(only on LD39020ADT)		100		Ω
V_{EN}	Enable input logic low	$V_{IN} = 1.5\text{ V to }5.5\text{ V}$ $-40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$			0.4	V
	Enable input logic high	$V_{IN} = 1.5\text{ V to }5.5\text{ V}$ $-40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$	1			
I_{EN}	Enable pin input current	$V_{EN} = V_{IN}$			100	nA
$T_{ON}^{(2)}$	Turn on time			100		μs
T_{SHDN}	Thermal shutdown			160		$^\circ\text{C}$
	Hysteresis			20		
C_{OUT}	Output capacitor	Capacitance see Figure 18. Stability area vs. (C_{OUT}, ESR)	0.47		22	μF

1. Not applicable for $V_{out(nom)} > 4.5\text{ V}$
2. Turn-on time is time measured between the enable input just exceeding V_{EN} high value and the output voltage just reaching 95 % of its nominal value

6 Application information

6.1 Soft-start function

The LD39020 has an internal soft start circuit. By increasing the startup time up to 100 μs , without the need of any external soft start capacitor, this feature is able to keep the regulator inrush current at startup under control.

6.2 Output discharge function

The LD39020 integrates a MOSFET connected between V_{OUT} and GND. This transistor is activated when the EN pin goes to low logic level and has the function to quickly discharge the output capacitor when the device is disabled by the user.

The device is available with or without auto-discharge feature.

See [Table 10. DFN4 1x1 order code](#) for more details.

6.3 Input and output capacitors

The LD39020 requires external capacitors to assure the regulator control loop stability.

Any good quality ceramic capacitor can be used but, the X5R and the X7R are suggested since they guarantee a very stable combination of capacitance and ESR overtemperature.

Locating the input/output capacitors as closer as possible to the relative pins is recommended.

The LD39020 requires an input capacitor with a minimum value of 1 μF .

This capacitor must be located as closer as possible to the input pin of the device and returned to a clean analog ground.

The control loop of the LD39020 is designed to work with an output ceramic capacitor.

This capacitor must meet the requirements of minimum capacitance and equivalent series resistance (ESR), as shown in [Figure 18. Stability area vs. \(\$C_{\text{OUT}}\$, ESR\)](#). To assure stability, the output capacitor must maintain its ESR and capacitance in the stable region, over the full operating temperature range.

The LD39020 shows stability with a minimum effective output capacitance of 220 nF.

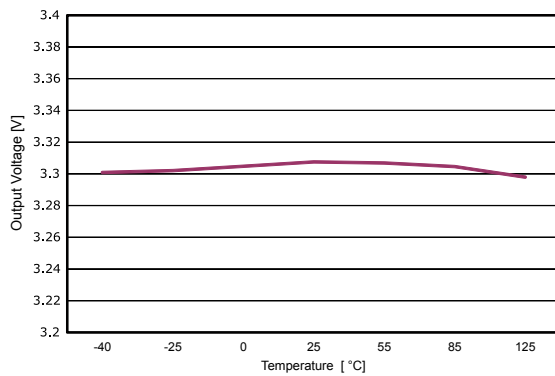
However, to keep stability in all operating conditions (temperature, input voltage and load variations), a minimum output capacitor of 0.47 μF is recommended.

The suggested combination of 1 μF input and output capacitors offers a good compromise among the stability of the regulator, optimum transient response and total PCB area occupation.

7 Typical characteristics

($C_{IN} = C_{OUT} = 1 \mu F$, V_{EN} to V_{IN} , $T_J = 25^\circ C$ unless otherwise specified)

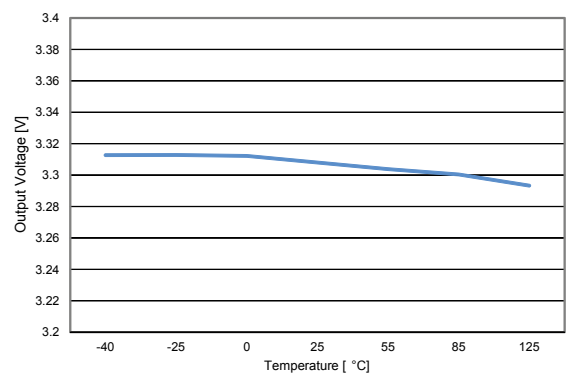
Figure 5. Output voltage vs. temperature
($I_{OUT} = 1 \text{ mA}$)



$V_{IN} = 4.3 \text{ V}$, $I_{OUT} = 1 \text{ mA}$

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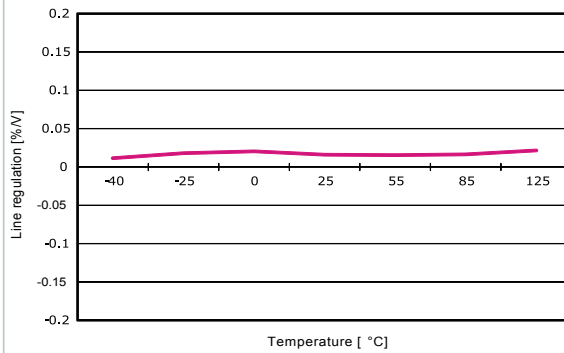
Figure 6. Output voltage vs. temperature
($I_{OUT} = 200 \text{ mA}$)



$V_{IN} = 4.3 \text{ V}$, $I_{OUT} = 200 \text{ mA}$

AM13856V1

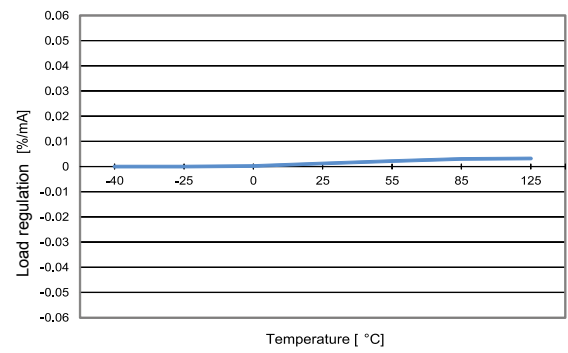
Figure 7. Line regulation vs. temperature



$V_{IN} = 4.3 \text{ V to } 5.5 \text{ V}$, $I_{OUT} = 10 \text{ mA}$

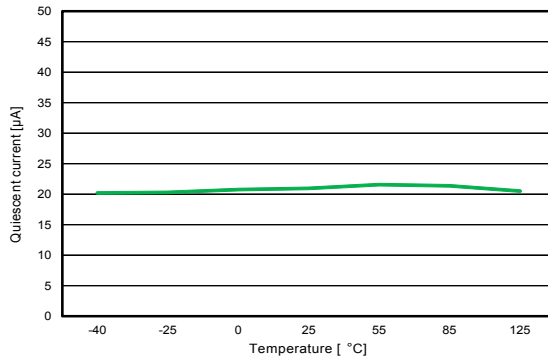
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Figure 8. Load regulation vs. temperature

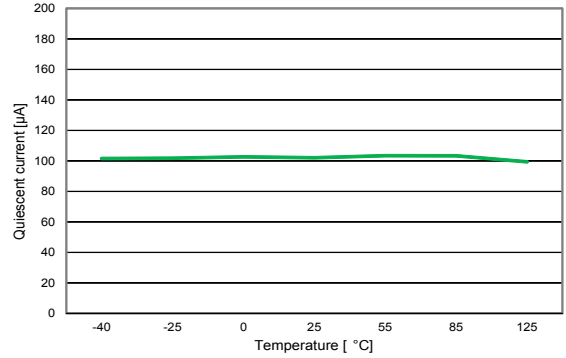


$V_{IN} = 4.3 \text{ V}$, $I_{OUT} = 0 \text{ to } 200 \text{ mA}$

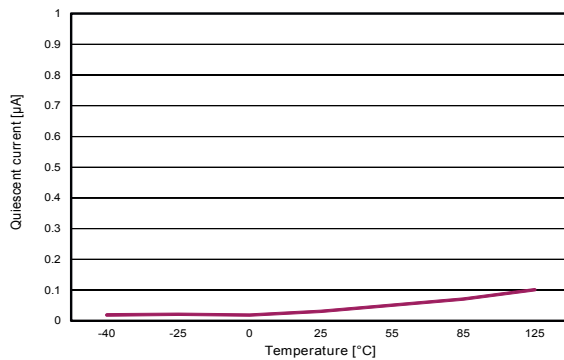
AM13858V1

Figure 9. Quiescent current vs. temperature
 ($I_{OUT} = 0 \text{ mA}$)

 $V_{IN} = 4.3 \text{ V}, I_{OUT} = 0 \text{ mA}$

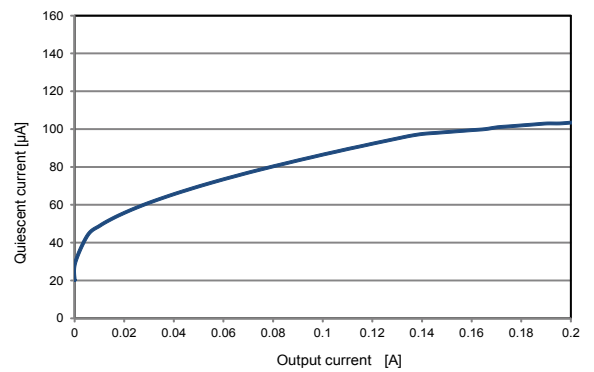
AM13859V1

Figure 10. Quiescent current vs. temperature
 ($I_{OUT} = 200 \text{ mA}$)

 $V_{IN}=4.3\text{V}, I_{OUT}=200\text{mA}$

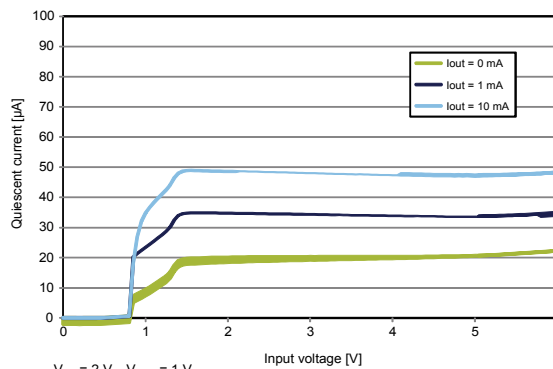
AM13860V1

Figure 11. Shutdown current vs. temperature

 $V_{IN} = 4.3 \text{ V}, V_{EN} = \text{GND}$

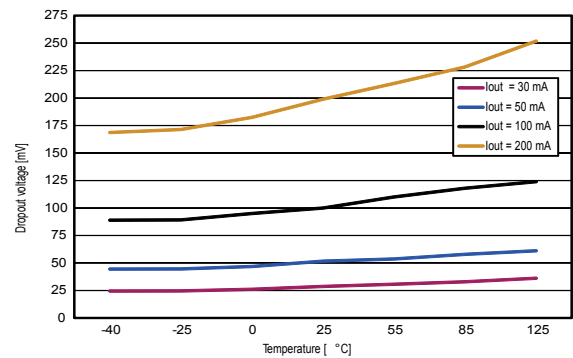
AM13861V1

Figure 12. Quiescent current vs. load current

 $V_{IN}=2\text{V}, V_{OUT}=1\text{V}$

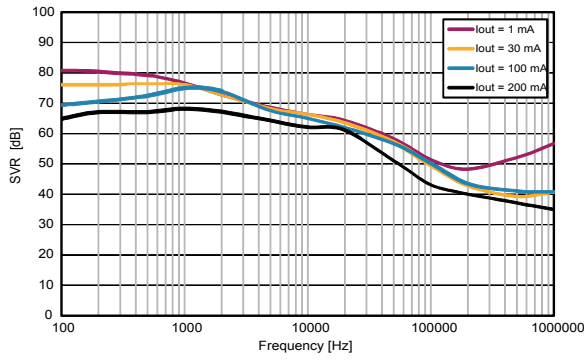
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Figure 13. Quiescent current vs. input voltage

 $V_{IN} = 2 \text{ V}, V_{OUT} = 1 \text{ V}$

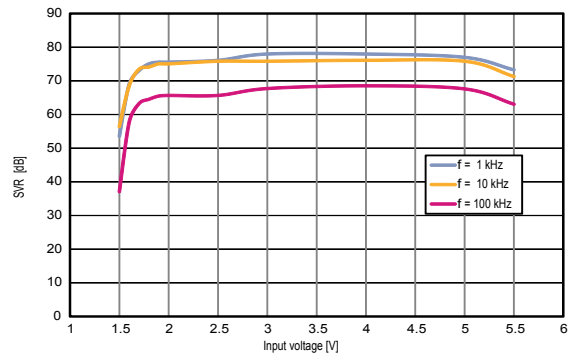
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Figure 14. Dropout voltage vs. temperature


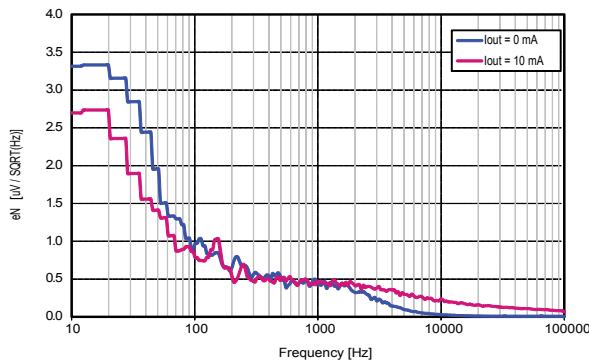
AM13864V1

Figure 15. Supply voltage rejection vs. frequency

 $V_{IN} = 2\text{ V} \pm 200\text{ mV}$, $V_{OUT} = 1\text{ V}$, $C_{OUT} = 1\text{ }\mu\text{F}$

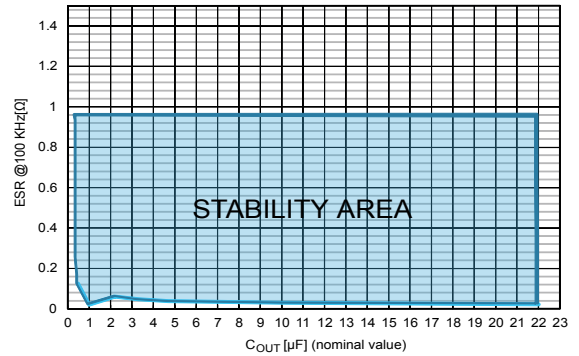
AM13865V1

Figure 16. Supply voltage rejection vs. input voltage

 $I_{OUT} = 30\text{ mA}$, $V_{OUT} = 1\text{ V}$, $C_{OUT} = 1\text{ }\mu\text{F}$

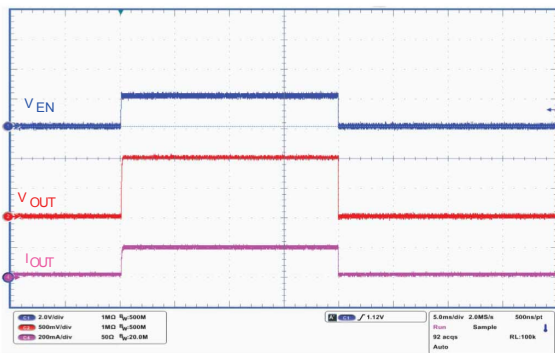
AM13866V1

Figure 17. Output noise spectral density

 $V_{IN} = 2.0\text{ V}$, $V_{OUT} = 1.0\text{ V}$, $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$

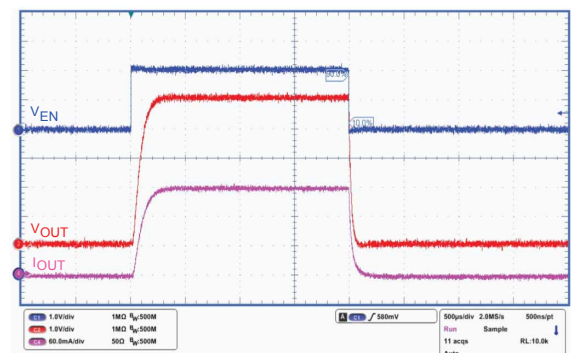
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Figure 18. Stability area vs. (C_{OUT}, ESR)

 V_{IN} from 2 to 5.5 V, I_{OUT} from 0 to 300 mA, $C_{IN} = 1\text{ }\mu\text{F}$

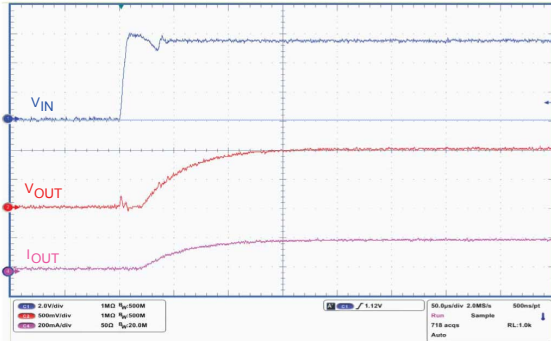
AM13868V1

Figure 19. Enable startup ($V_{OUT} = 1\text{ V}$)

 $V_{IN} = 2\text{ V}$, $V_{EN} = 0\text{ V to } V_{IN}$, $I_{OUT} = 0.2\text{ A}$, $V_{OUT} = 1\text{ V}$, $T_r = 5\text{ }\mu\text{s}$

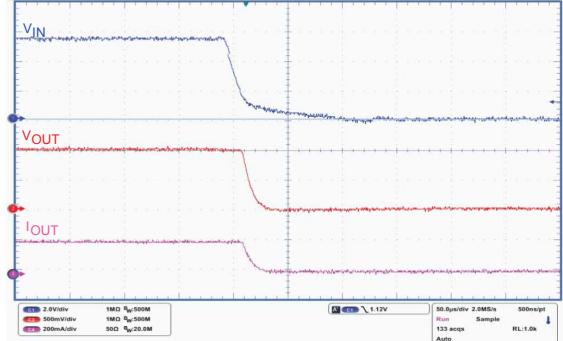
AM13869V1

Figure 20. Enable startup ($V_{OUT} = 5\text{ V}$)

 $V_{IN} = 5.5\text{ V}$, $V_{EN} = 0\text{ V to } 2\text{ V}$, $I_{OUT} = 0.2\text{ A}$, $V_{OUT} = 5\text{ V}$, $T_r = 5\text{ }\mu\text{s}$

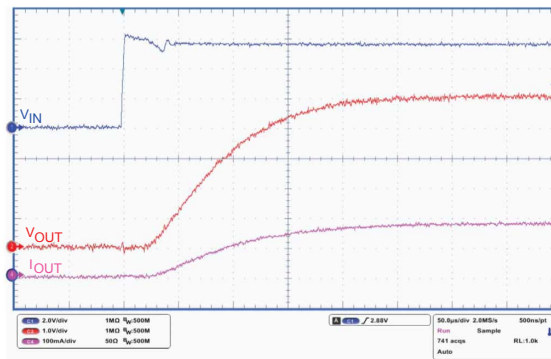
AM13870V1

Figure 21. Turn-on time ($V_{OUT} = 1\text{ V}$)

 $V_{IN} = V_{EN} = \text{from } 0\text{ V to } 5.5\text{ V}, I_{OUT} = 0.2\text{ A}, V_{OUT} = 1\text{ V}, T_r = 5\text{ }\mu\text{s}$

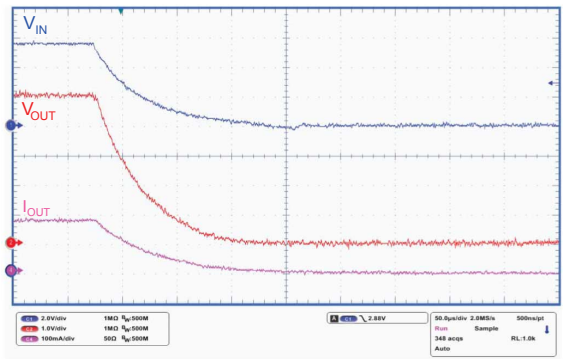
AM13871V1

Figure 22. Turn-off time ($V_{OUT} = 1\text{ V}$)

 $V_{IN} = V_{EN} = \text{from } 5.5\text{ V to } 0\text{ V}, I_{OUT} = 0.2\text{ A}, V_{OUT} = 1\text{ V}, T_r = 5\text{ }\mu\text{s}$

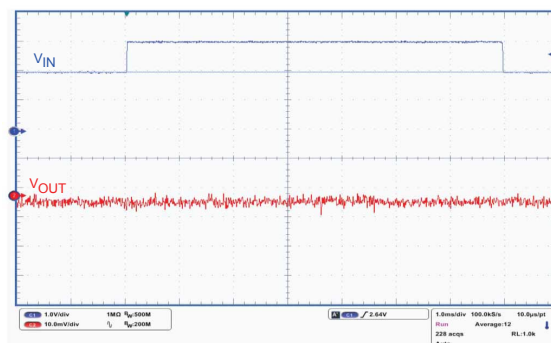
AM13872V1

Figure 23. Turn-on time ($V_{OUT} = 5\text{ V}$)

 $V_{IN} = V_{EN} = \text{from } 0\text{ V to } 5.5\text{ V}, I_{OUT} = 0.2\text{ A}, V_{OUT} = 5\text{ V}, T_r = 5\text{ }\mu\text{s}$

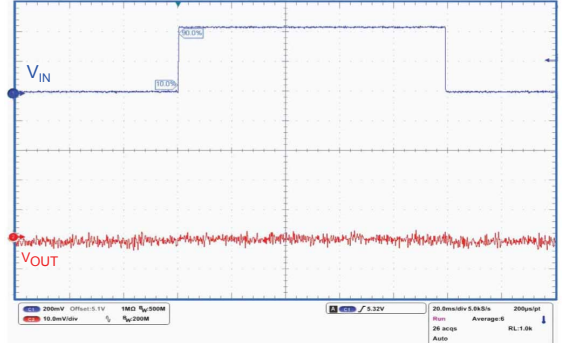
AM13873V1

Figure 24. Turn-off time ($V_{OUT} = 5\text{ V}$)

 $V_{IN} = V_{EN} = \text{from } 5.5\text{ V to } 0\text{ V}, I_{OUT} = 0.2\text{ A}, V_{OUT} = 5\text{ V}, T_r = 5\text{ }\mu\text{s}$

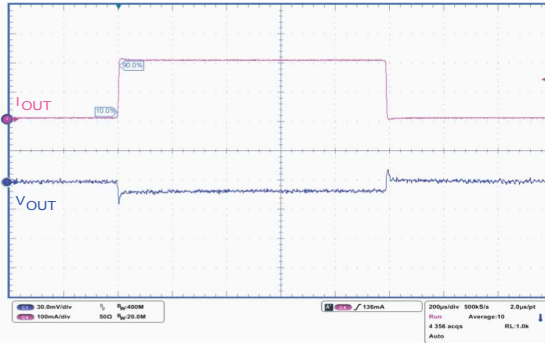
AM13874V1

Figure 25. Line transient ($V_{OUT} = 1\text{ V}$)

 $V_{IN} = V_{EN} = \text{from } 2\text{ V to } 3\text{ V}, I_{OUT} = 10\text{ mA}, V_{OUT} = 1\text{ V}, T_r = T_f = 5\text{ }\mu\text{s}$

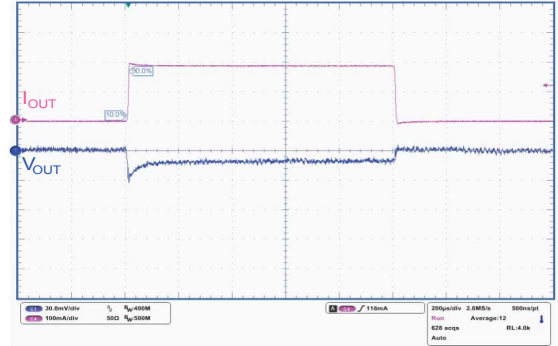
AM13875V1

Figure 26. Line transient ($V_{OUT} = 5\text{ V}$)

 $V_{IN} = V_{EN} = \text{from } 5.1\text{ V to } 5.5\text{ V}, I_{OUT} = 10\text{ mA}, V_{OUT} = 5\text{ V}, T_r = T_f = 5\text{ }\mu\text{s}$

AM13876V1

Figure 27. Load transient ($V_{OUT} = 1\text{ V}$)

 $V_{IN} = V_{EN} = 2\text{ V}$, $I_{OUT} = \text{from } 0 \text{ to } 0.2\text{ A}$, $V_{OUT} = 1\text{ V}$, $t_r = t_f = 5\text{ }\mu\text{s}$

AM13877V1

Figure 28. Load transient ($V_{OUT} = 5\text{ V}$)

 $V_{IN} = V_{EN} = 5.5\text{ V}$, $I_{OUT} = \text{from } 0 \text{ to } 0.2\text{ A}$, $V_{OUT} = 5\text{ V}$, $t_r = t_f = 5\text{ }\mu\text{s}$

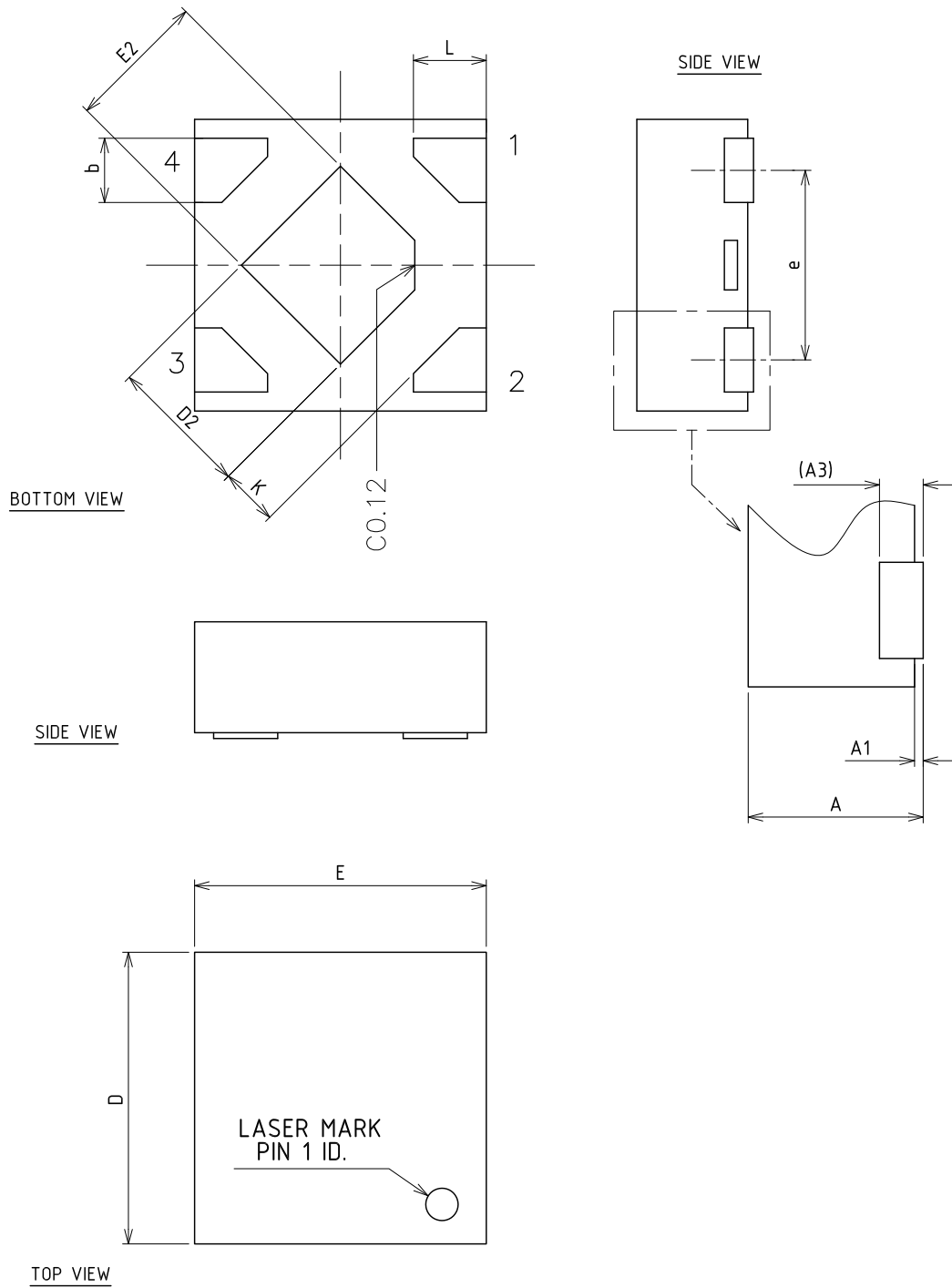
AM13878V1

8 **Package information**

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK®** packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

8.1 DFN4 1x1 package info

Figure 29. DFN4 1x1 package outline

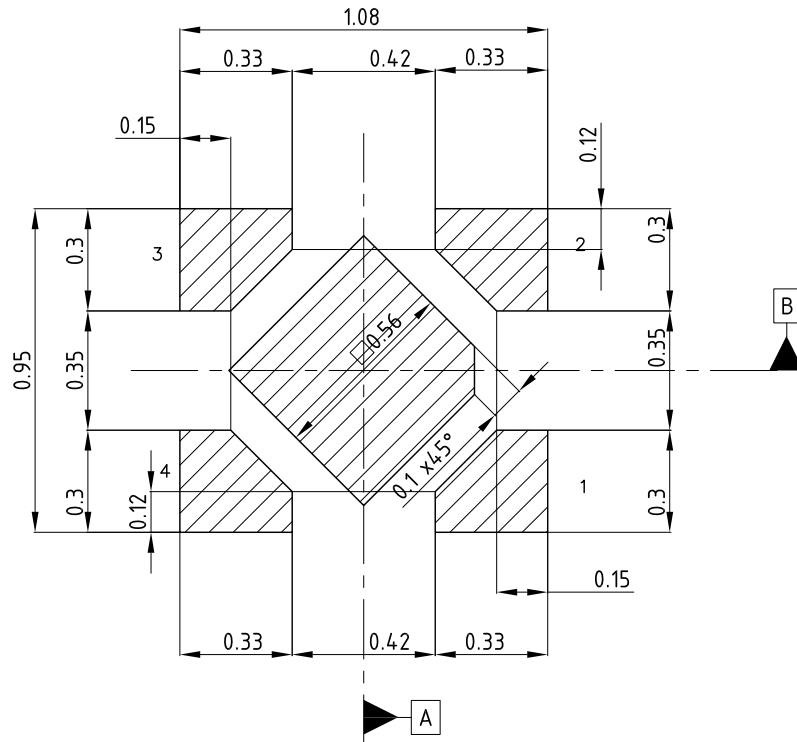


8405587_A

Table 7. DFN4 1x1 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.34	0.37	0.40
A1	0	0.02	0.05
A3		0.10	
b	0.17	0.22	0.27
D	0.95	1.00	1.05
D2	0.43	0.48	0.53
E	0.95	1.00	1.05
E2	0.43	0.48	0.53
e		0.65	
L	0.20	0.25	0.30
K	0.15		

Figure 30. DFN4 1x1 recommended footprint

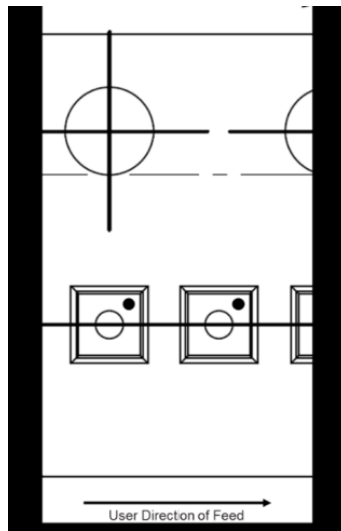


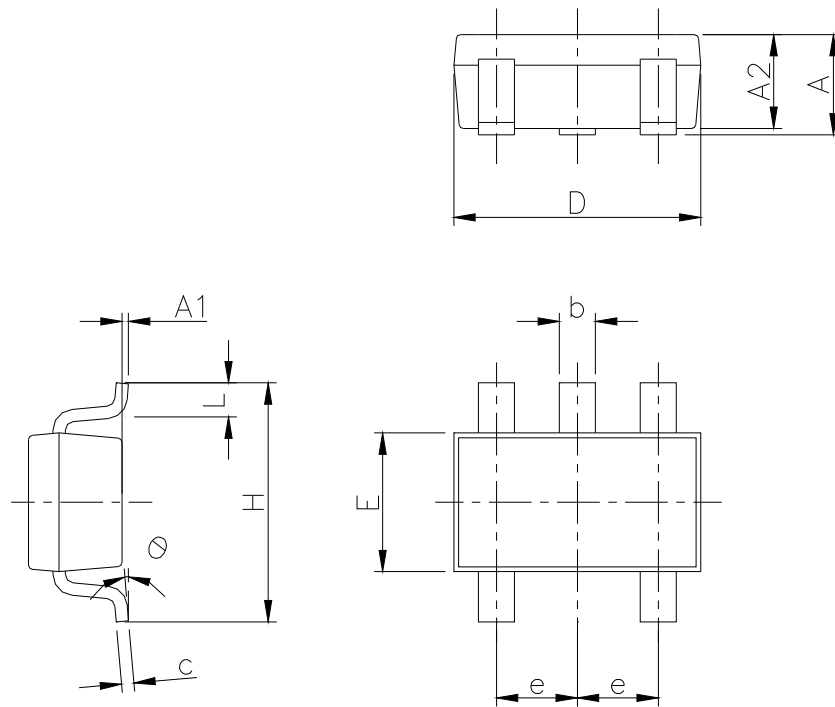
Notes:

- 1) This footprint is able to ensure insulation up to 10 Vrms (according to CEI IEC 664-1)
- 2) The device must be positioned within $\oplus 0.02$ A B

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Figure 33. DFN4 1x1 orientation

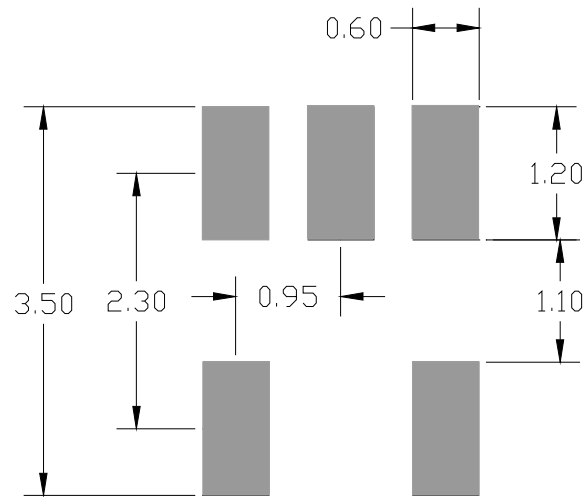


8.2 SOT23-5L mechanical data
Figure 34. SOT23-5L package outline


7049676_k

Table 8. SOT23-5L package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.90		1.45
A1	0		0.15
A2	0.90		1.30
b	0.30		0.50
c	0.09		0.20
D		2.95	
E		1.60	
e		0.95	
H		2.80	
L	0.30		0.60
θ	0°		8°

Figure 35. SOT23-5L recommended footprint


Note: Dimensions are in mm

8.3 SOT23-5L packing information

Figure 36. SOT23-5L tape and reel outline

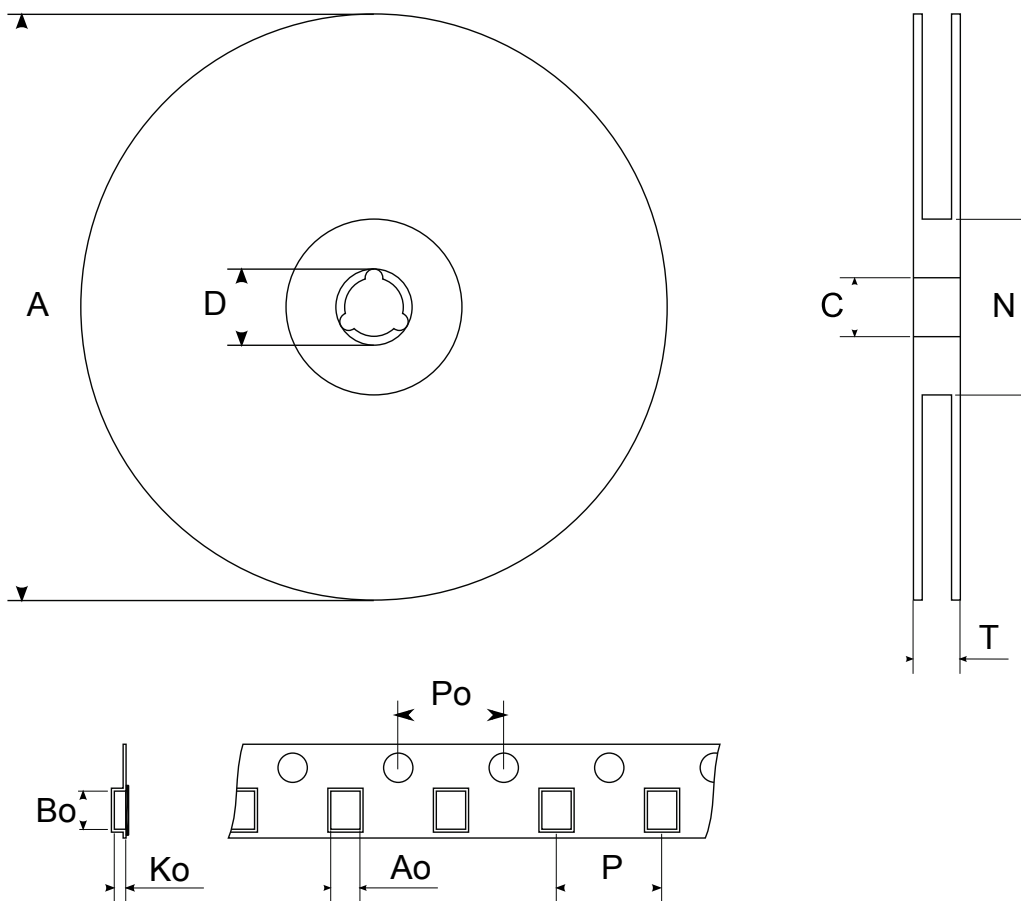


Table 9. SOT23-5L tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			180
C	12.8	13.0	13.2
D	20.2		
N	60		
T			14.4
Ao	3.13	3.23	3.33
Bo	3.07	3.17	3.27
Ko	1.27	1.37	1.47
Po	3.9	4.0	4.1
P	3.9	4.0	4.1

9 Order code

Table 10. DFN4 1x1 order code

Order code	Output voltage (V)	Auto-discharge	Tolerance (%)	Marking
LD39020ADTPU08R	0.8	Yes	0.5	A1
LD39020DTPU08R			2	08
LD39020ADTPU11R	1.1	Yes	0.5	A4
LD39020DTPU11R			2	11
LD39020ADTPU13R	1.3	Yes	0.5	AP
LD39020DTPU13R			2	13
LD39020ADTPU15R ⁽¹⁾	1.5	Yes	0.5	A6
LD39020DTPU15R			2	15
LD39020ADTPU18R	1.8	Yes	0.5	A7
LD39020DTPU18R			2	18
LD39020ATPU185R	1.85	No	0.5	BR
LD39020TPU185R			2	CR
LD39020ADTPU21R	2.1	Yes	0.5	A9
LD39020DTPU21R ⁽¹⁾			2	21
LD39020ADTPU25R	2.5	Yes	0.5	AA
LD39020DTPU25R			2	25
LD39020ADTPU27R ⁽¹⁾	2.7	Yes	0.5	AB
LD39020DTPU27R ⁽¹⁾			2	27
LD39020ADTPU28R	2.8	Yes	0.5	AC
LD39020DTPU28R ⁽¹⁾			2	28
LD39020ADTPU30R	3	Yes	0.5	AF
LD39020DTPU30R			2	30
LD39020ADTPU31R ⁽¹⁾	3.1	Yes	0.5	AG
LD39020DTPU31R			2	31
LD39020ATPU32R	3.2	No	0.5	BH
LD39020TPU32R			2	CH
LD39020ADTPU33R	3.3	Yes	0.5	AJ
LD39020DTPU33R			2	33
LD39020ATPU33R		No	0.5	BJ
LD39020TPU33R			2	CJ
LD39020ADTPU40R ⁽¹⁾	4	Yes	0.5	AL
LD39020DTPU40R			2	40
LD39020ADTPU47R ⁽¹⁾	4.7	Yes	0.5	AM
LD39020DTPU47R			2	47

1. Available on request.

Table 11. SOT23-5L order code

Order code	Output voltage (V)	Auto-discharge	Tolerance (%)	Marking
LD39020ADM30R	3.0	Yes	0.5	AD30

Revision history

Table 12. Document revision history

Date	Revision	Changes
04-Dec-2013	1	Initial release.
02-Apr-2014	2	Updated Table 10: "DFN4 1x1 order codes"..
05-Jun-2015	3	Added SOT23-5L package. Modified features and description in cover page. Updated Section 7: "Pin configuration" and Table 3: "Thermal data". Added Section 13.2: "SOT23-5L package information" and Section 13.3: "SOT23-5L packing information". Minor text changes.
03-Jul-2015	4	Updated package name from DFN1x1-4L to DFN4 1x1. Updated note in Table 11: "SOT23-5L order code". Minor text changes.
07-Jan-2019	5	Added Figure 31. DFN4 1x1 tape outline , Figure 32. DFN4 1x1 reel outline and Figure 33. DFN4 1x1 orientation . Updated Section 9 Order code .

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