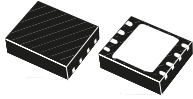


500 mA, high performance low dropout linear regulator



DFN8 (3 x 3 mm)

Features

- Input voltage range: 2.7 V to 6.5 V
- Very low output voltage noise: $13 \mu\text{V}_{\text{RMS}}/\text{V}_{\text{OUT}}$
- Low quiescent current: 48 μA typical
- 500 mA guaranteed output current
- Fast start-up time: 50 μs
- High PSRR: 65 dB at 100 Hz
- -40 °C to 125 °C ambient operative temperature range
- Very low dropout: 190 mV at max. I_{OUT}
- Adjustable (from 1.25 V to 6 V) or fixed output voltage on request (from 1.0 V to 4.3 V)
- Stable with low ESR capacitor: min. 2 μF
- Current limit and thermal protections
- DFN8 (3 x 3 mm) standard for industrial

Application

- Low noise POL
- Wireless communication
- Industrial applications

Maturity status link
LDLN050

Description

The [LDLN050](#) is a 500 mA LDO regulator, designed to be used in several environments. The [LDLN050](#) has a very low-resistance pass element (PMOS) that is even very fast during the turn-on.

Thanks to its low-noise design, the [LDLN050](#) can be used to supply noise sensitive circuits such as sensors, MCUs and wireless ICs in industrial applications.

The LDO low current consumption (typically 48 μA) is also used on battery-supplied applications.

On the adjustable version, the output voltage can be set to any desired value between 1.25 V and 6 V. Fixed voltage versions, between 1.0 V and 4.3 V (with 0.1 V step) can be provided upon request.

On the fixed voltage versions only, an external capacitor can be connected to C_{NR} pin to further reduce the noise on the regulated output voltage.

The [LDLN050](#) is available in DFN8 (3 x 3 mm) package.

1 Diagram

Figure 1. Block diagram, adjustable version

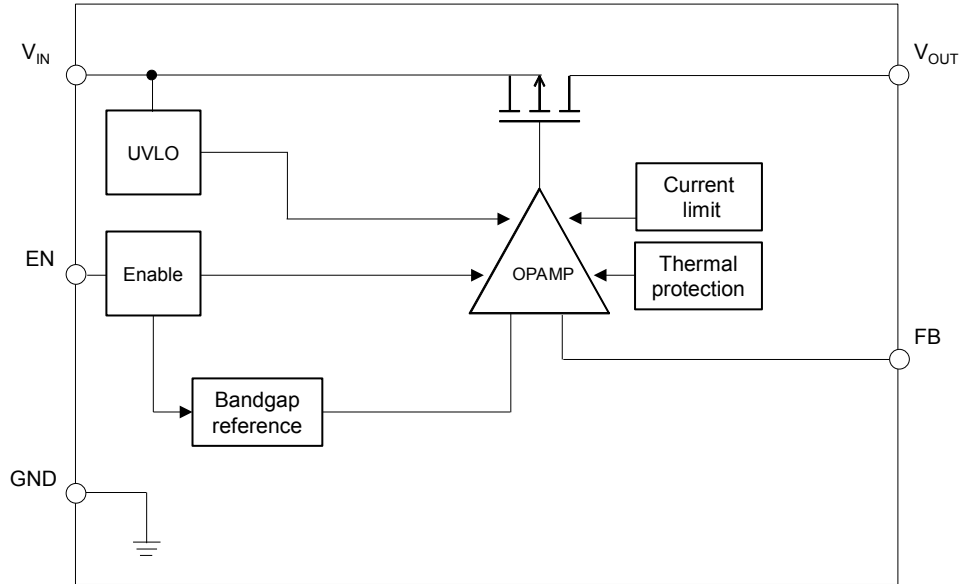
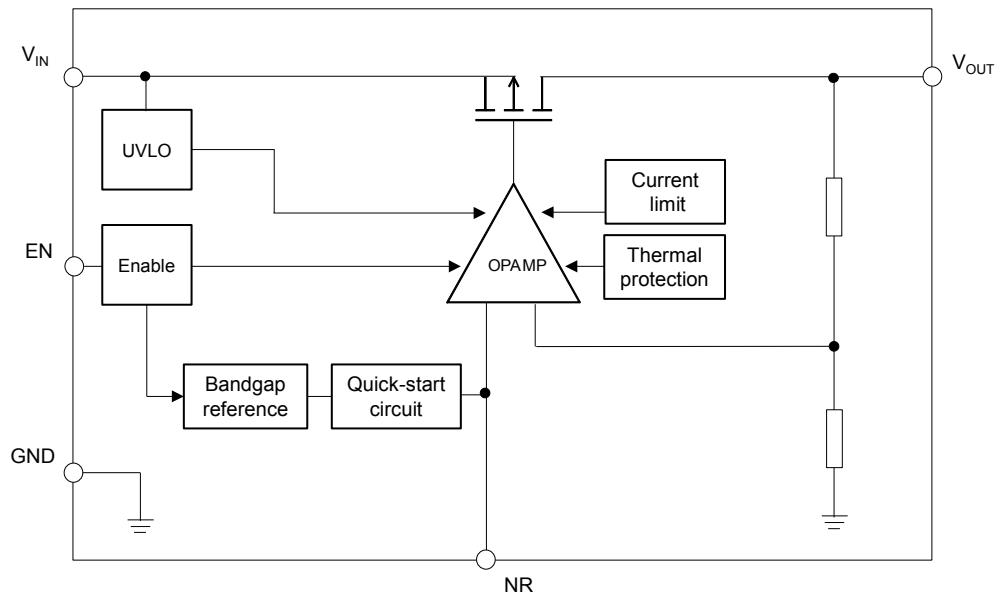


Figure 2. Block diagram, fixed version



2 Pin configuration

Figure 3. Pin connection, DFN8 – 3 x 3 (top view)

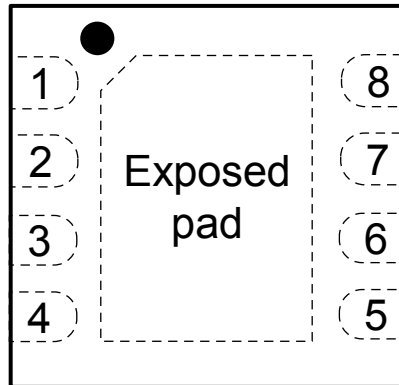


Table 1. Pin description

Pin	Symbol	Function
1	OUT	Output pin
2	N.C.	Not internally connected
3	FB (ADJ) NR (FIXED)	Feedback pin on adjustable version Noise reduction on fixed version
4	GND	Ground connection
5	EN	Enable pin logic input: Low=shutdown, High=active This pin is not internally pulled up. Don't leave floating.
6	N.C.	Not internally connected
7	N.C.	Not internally connected
8	IN	Input pin
Exp. Pad.	Exposed thermal Pad	Must be connected to GND

3 Typical application diagram

Figure 4. Typical application circuit for adjustable version

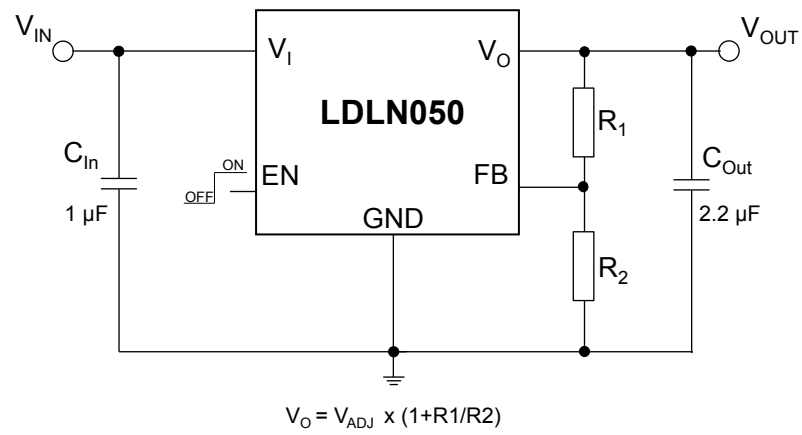
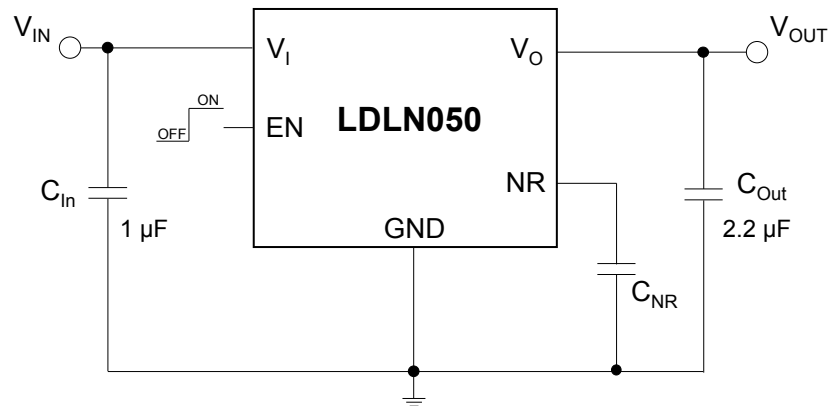


Figure 5. Typical application circuit for fixed output version



4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input voltage pin	-0.3 to 7	V
V_{EN}	Enable pin	-0.3 to $V_{IN} + 0.3$	V
V_{OUT}	DC output voltage	-0.3 to $V_{IN} + 0.3$	V
V_{FB}	Feedback pin	-0.3 to 1.6	V
I_{OUT}	Output current	Internally limited	A
P_{DIS}	Maximum Power dissipation	Refer to Table 3. Thermal data	W
T_{ST}	Storage temperature range	-55 to 150	°C
T_j	Operating Junction temperature range	-40 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 3. Thermal data

Symbol	Parameter	DFN8 3x3 mm	Unit
R_{thJA}	Thermal resistance junction-ambient	51	°C/W
Ψ_{J-T}	Thermal characterization parameter junction to top of package	2.4	°C/W

Note: JEDEC 2S2P (4L) board as per JESD 51-7 with two thermal vias.

Table 4. Electrostatic discharge

Symbol	Parameter	DFN8 3x3	Unit
HBM	Human Body Model	+/-2000	V

5 Electrical characteristics

If not differently specified, $T_J = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, typical values refer to $T_J = +25\text{ }^{\circ}\text{C}$, $V_{IN} = V_{OUT} + 0.5\text{ V}$ or 2.7 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 10\text{ nF}$.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage ⁽¹⁾		2.7		6.5	V
V_{ADJ}	Reference voltage for Adj	$T_{AMB} = 25\text{ }^{\circ}\text{C}$	1.196	1.208	1.22	V
V_{OUT}	Output voltage range		V_{ADJ}		6	V
	Output voltage accuracy ⁽¹⁾	$1\text{ mA} < I_{OUT} < 500\text{ mA}$ $V_{OUT} + 0.5\text{ V} < V_{IN} < 6.5\text{ V}$ $V_{OUT} > 2.2\text{ V}$	-2		2	%
		$1\text{ mA} < I_{OUT} < 500\text{ mA}$ $V_{OUT} + 0.5\text{ V} < V_{IN} < 6.5\text{ V}$ V_{OUT} up to 2.2 V	-3		3	%
	Line regulation ⁽¹⁾	$V_{OUT} + 0.5\text{ V} < V_{IN} < 6.5\text{ V}$		0.02		%/V
	Load Regulation	$0.5\text{ mA} < I_{OUT} < 500\text{ mA}$		0.005		%/mA
V_{DO}	Dropout Voltage ⁽²⁾	$I_{OUT} = 500\text{ mA}$		190	500	mV
I_{LIM}	Output current limit	$V_{OUT} = 0.9 \times V_{OUTNOM}$, $V_{IN} = V_{OUTNOM} + 0.9\text{ V}$, $V_{IN} > 2.7\text{ V}$	800			mA
I_{GND}	Ground pin current	$I_{OUT} = 10\text{ mA}$		48	65	μA
		$I_{OUT} = 500\text{ mA}$		70	120	
I_{SHDN}	Shutdown current	$V_{EN} = 0\text{ V}$			1	μA
I_{FB}	Feedback pin current (Adj)	$V_{OUTNOM} = 1.2\text{ V}$	-0.5		0.5	μA
P_{SRR}	Power supply rejection ration	$V_{IN} = 4.3\text{ V}$ $V_{OUT} = 3.3\text{ V}$ $C_{NR} = 10\text{ nF}$ $I_{OUT} = 100\text{ mA}$	F = 100 Hz	65		dB
			F = 1 KHz	47		
			F = 10 KHz	45		dB
			F = 100 KHz	38		
V_{NOISE}	Output noise	BW = 10 Hz to 100 KHz, $V_{OUT} = 2.8\text{ V}$, $C_{NR} = 10\text{ nF}$		$13 \times V_{OUT}$		μV_{RMS}
		BW = 10 Hz to 100 KHz, $V_{OUT} = 2.8\text{ V}$, no CNR		$25 \times V_{OUT}$		μV_{RMS}
T_{STR}	Start-up time $V_{OUT} = 10\%$ to 90%	Without CNR		45		μsec
		CNR = 1 nF		45		
		CNR = 10 nF		50		
		CNR = 47 nF		50		
$V_{EN} (H)$	Enable input logic level High		1.2			V
$V_{EN} (L)$	Enable input logic level Low				0.4	V
I_{EN}	Enable pin current (EN = H)	$V_{EN} = V_{IN} = 6.5\text{ V}$		0.03	1	μA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
UVLO	Undervoltage lockout	V_{IN} rising	1.9	2.2	2.65	V
V_{HYS}	UVLO Hysteresis	V_{IN} falling		0.07		V
T_{op}	Operating ambient temperature range		-40		125	°C
T_{SD}	Thermal shutdown temperature	High temp threshold		165		°C
		Thermal hysteresis		20		

1. Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7 V, whichever is greater.

2. Input voltage = $V_{OUTNOM} - 100$ mV. This specification does not apply to $V_{OUTNOM} < 2.8$ V.

6 Typical characteristics

$C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 2.2 \mu\text{F}$, $V_{EN} = V_{IN} = 3.8 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$, $T_j = 25 \text{ }^\circ\text{C}$ unless otherwise specified.

Figure 6. Output voltage vs. temperature ($I_{OUT} = 1 \text{ mA}$)

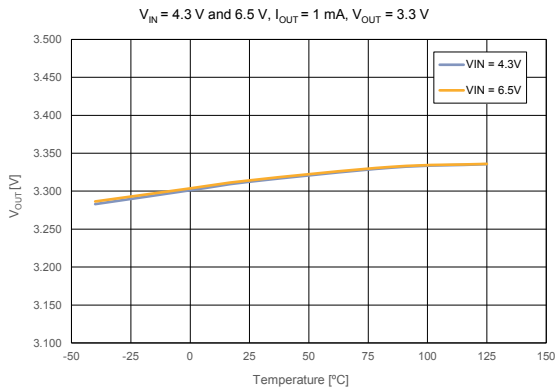


Figure 7. Output voltage vs. temperature ($I_{OUT} = 500 \text{ mA}$)

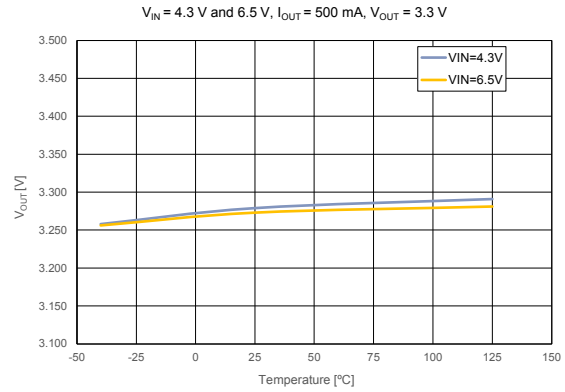


Figure 8. Line regulation vs. temperature

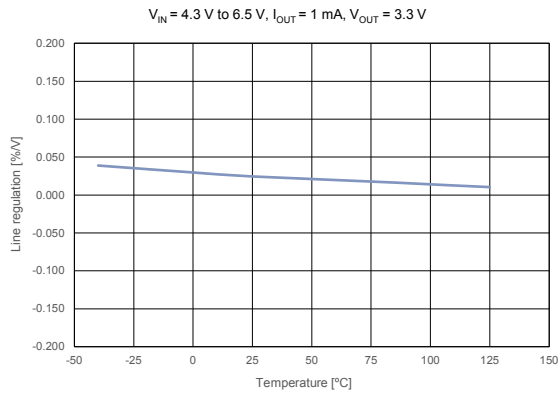


Figure 9. Load regulation vs. temperature

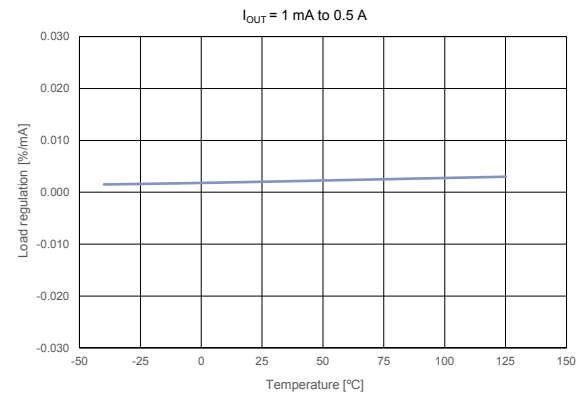


Figure 10. Quiescent current vs. temperature

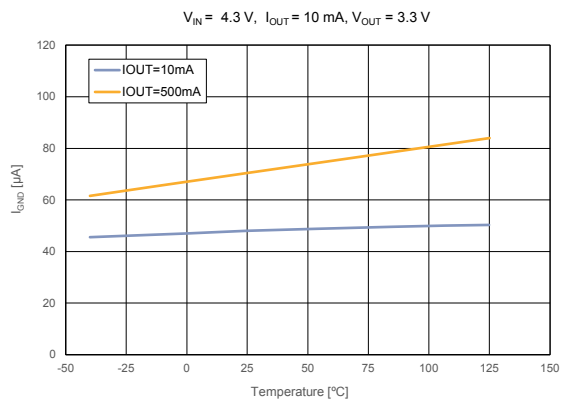


Figure 11. Quiescent current vs. load current

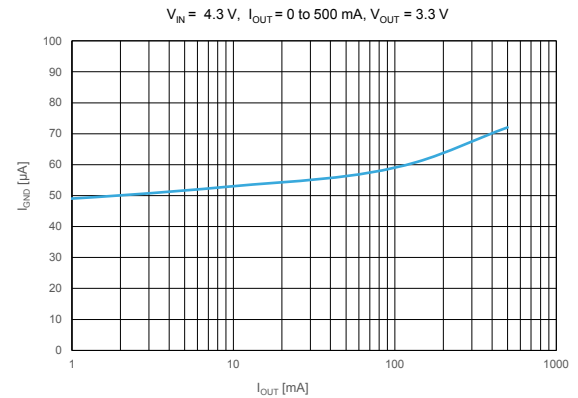


Figure 12. Supply current vs. input voltage

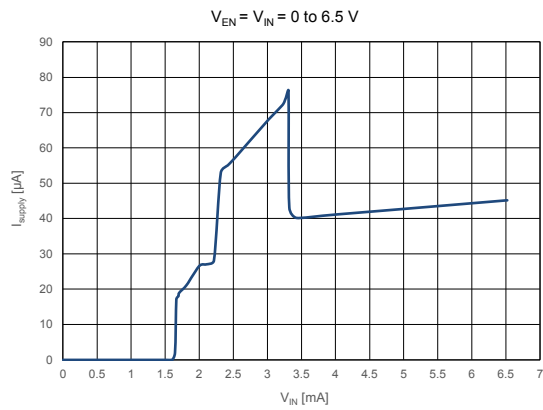


Figure 13. Off-state current vs. temperature

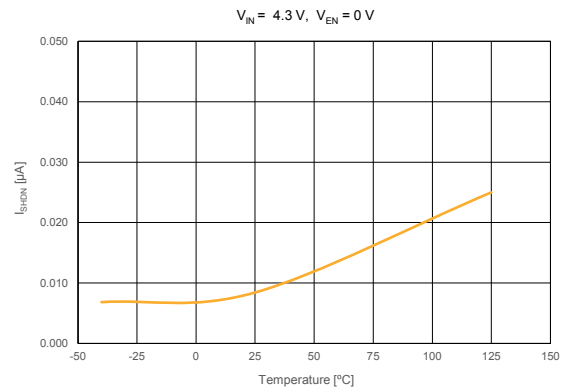


Figure 14. Dropout voltage vs. temperature

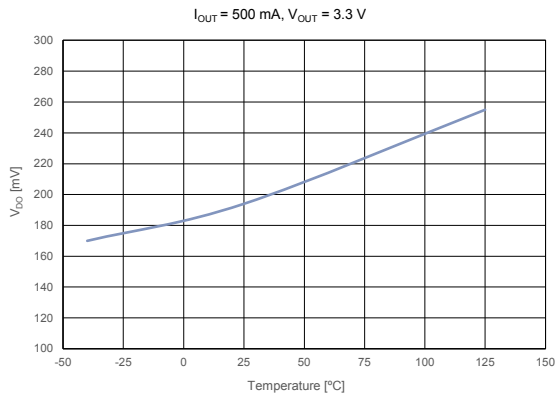


Figure 15. Dropout voltage vs. load current

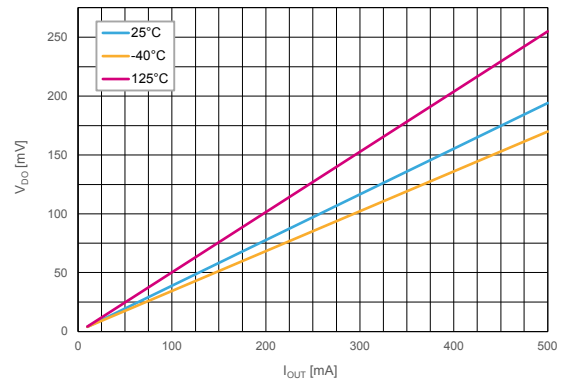


Figure 16. Short circuit current vs. temperature

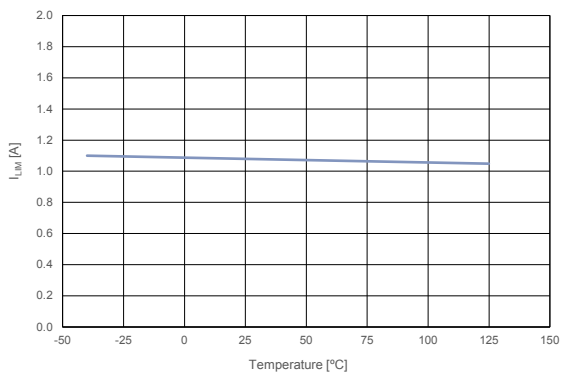


Figure 17. Enable thresholds vs. temperature

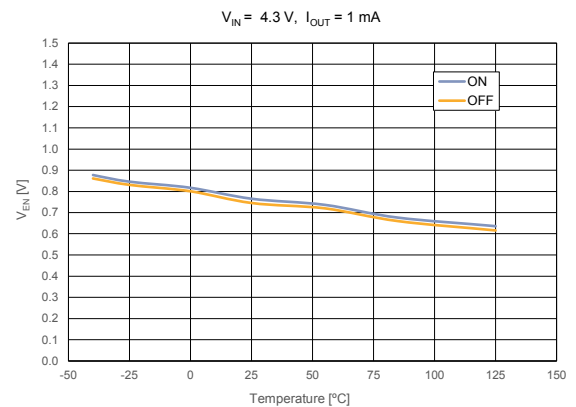


Figure 18. UVLO thresholds vs. temperature

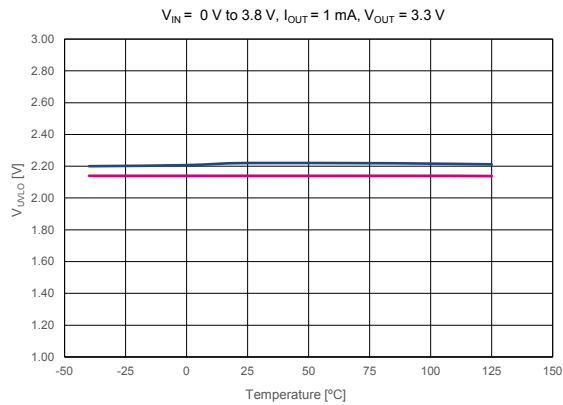


Figure 19. Enable pin current vs. temperature

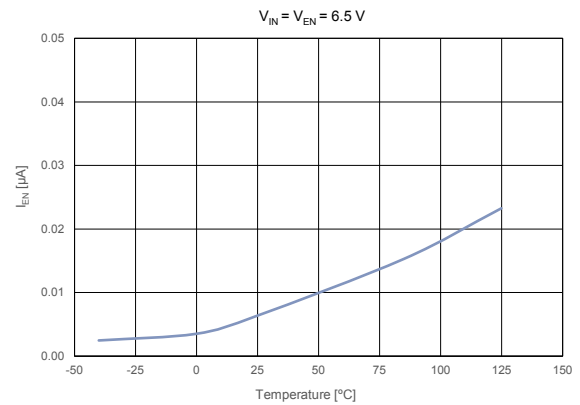


Figure 20. PSRR vs. Frequency (no C_{NR})

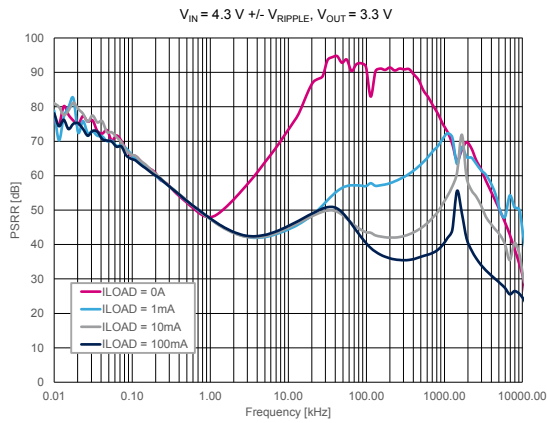


Figure 21. PSRR vs. frequency ($C_{NR} = 10 \text{ nF}$)

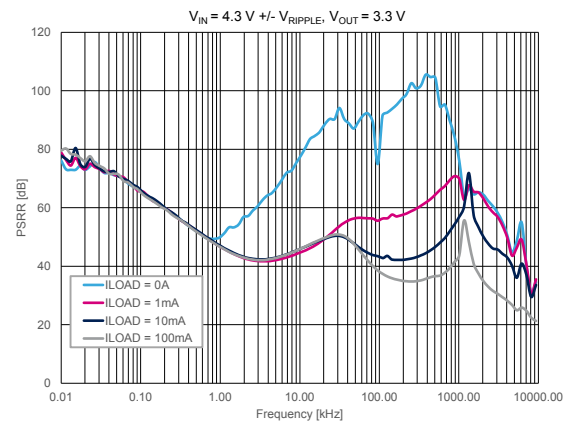


Figure 22. Output noise spectrum ($C_{NR} = 10 \text{ nF}$)

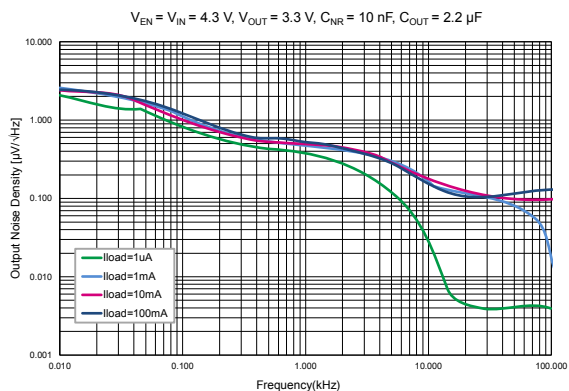


Figure 23. Output noise spectrum vs. C_{NR}

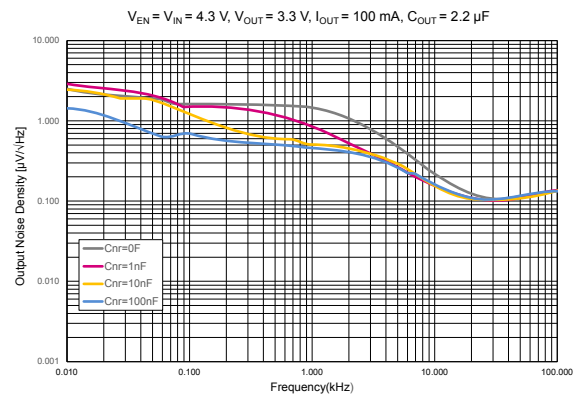


Figure 24. Line transient

V_{IN} from 3.8 V to 4.8 V, $I_{OUT} = 1\text{ mA}$, $T = 25^\circ\text{C}$, $C_{IN} = 500\text{ nF}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 10\text{ nF}$

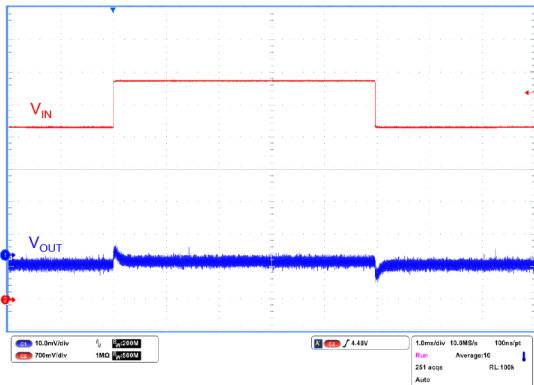


Figure 25. Load transient

I_{OUT} from 1 mA to 500 mA, $C_{IN} = 500\text{ nF}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 10\text{ nF}$, $t_t = 5\text{ }\mu\text{s}$

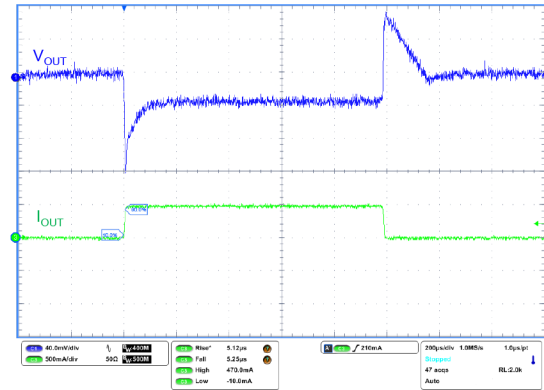


Figure 26. Startup transient

$V_{IN} = V_{EN}$ from 0 V to 5.5 V and back, $I_{OUT} = 1\text{ mA}$, $t_{RISE} = 500\text{ }\mu\text{s}$, $C_{NR} = 10\text{ nF}$, $V_{OUT} = 3.3\text{ V}$

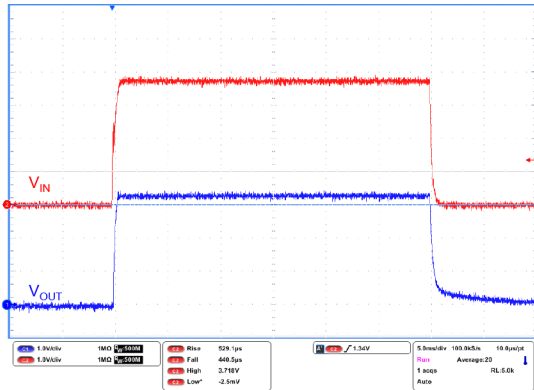


Figure 27. Enable startup ($C_{NR} = 1\text{ nF}$)

$V_{EN} = 0$ to 3.8 V, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 500\text{ nF}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 1\text{ nF}$, $t_t = 1\text{ }\mu\text{s}$, $V_{OUT} = 3.3\text{ V}$

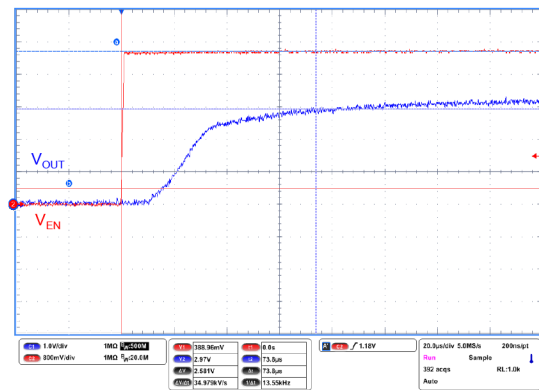


Figure 28. Enable startup ($C_{NR} = 2.2\text{ nF}$)

$V_{EN} = 0$ to 3.8 V, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 500\text{ nF}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 2.2\text{ nF}$, $t_t = 1\text{ }\mu\text{s}$, $V_{OUT} = 3.3\text{ V}$

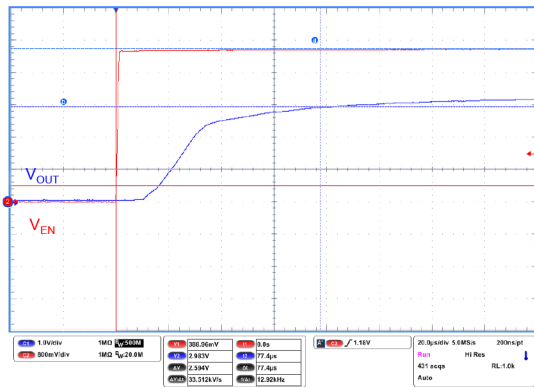


Figure 29. Enable startup ($C_{NR} = 10\text{ nF}$)

$V_{EN} = 0$ to 3.8 V, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 500\text{ nF}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 10\text{ nF}$, $t_t = 1\text{ }\mu\text{s}$, $V_{OUT} = 3.3\text{ V}$

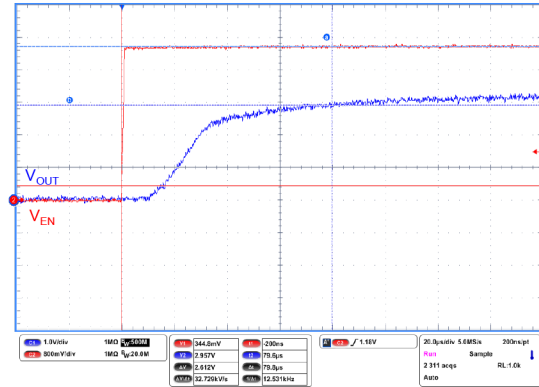


Figure 30. Enable startup ($C_{NR} = 47 \text{ nF}$)

$V_{EN} = 0 \text{ to } 3.8 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $C_{IN} = 500 \text{ nF}$, $C_{OUT} = 2.2 \text{ }\mu\text{F}$, $C_{NR} = 47 \text{ nF}$, $t_r = 1 \text{ }\mu\text{s}$, $V_{OUT} = 3.3 \text{ V}$

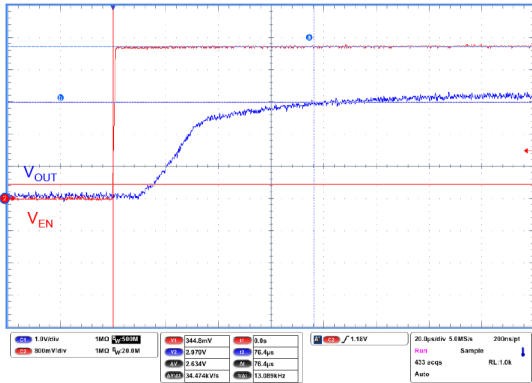
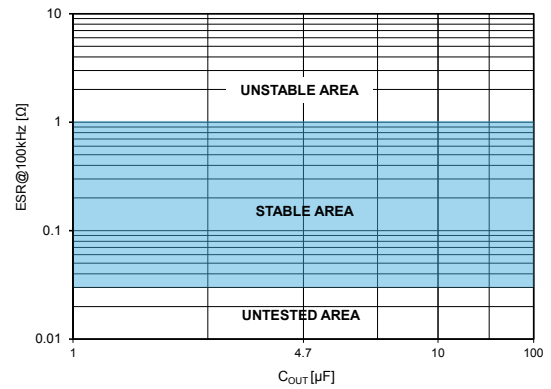


Figure 31. Tested stability area

$V_{EN} = V_{IN} = \text{from } 3.8 \text{ V to } 6.5 \text{ V}$, $I_{OUT} = \text{from } 0 \text{ mA to } 0.5 \text{ A}$, $T = 25 \text{ }^\circ\text{C}$, $C_{IN} = 500 \text{ nF}$, $C_{NR} = 10 \text{ nF}$, $V_{OUT} = 3.3 \text{ V}$



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 DFN8 3 x 3 package information

Figure 32. DFN8 3x3 package drawing outline

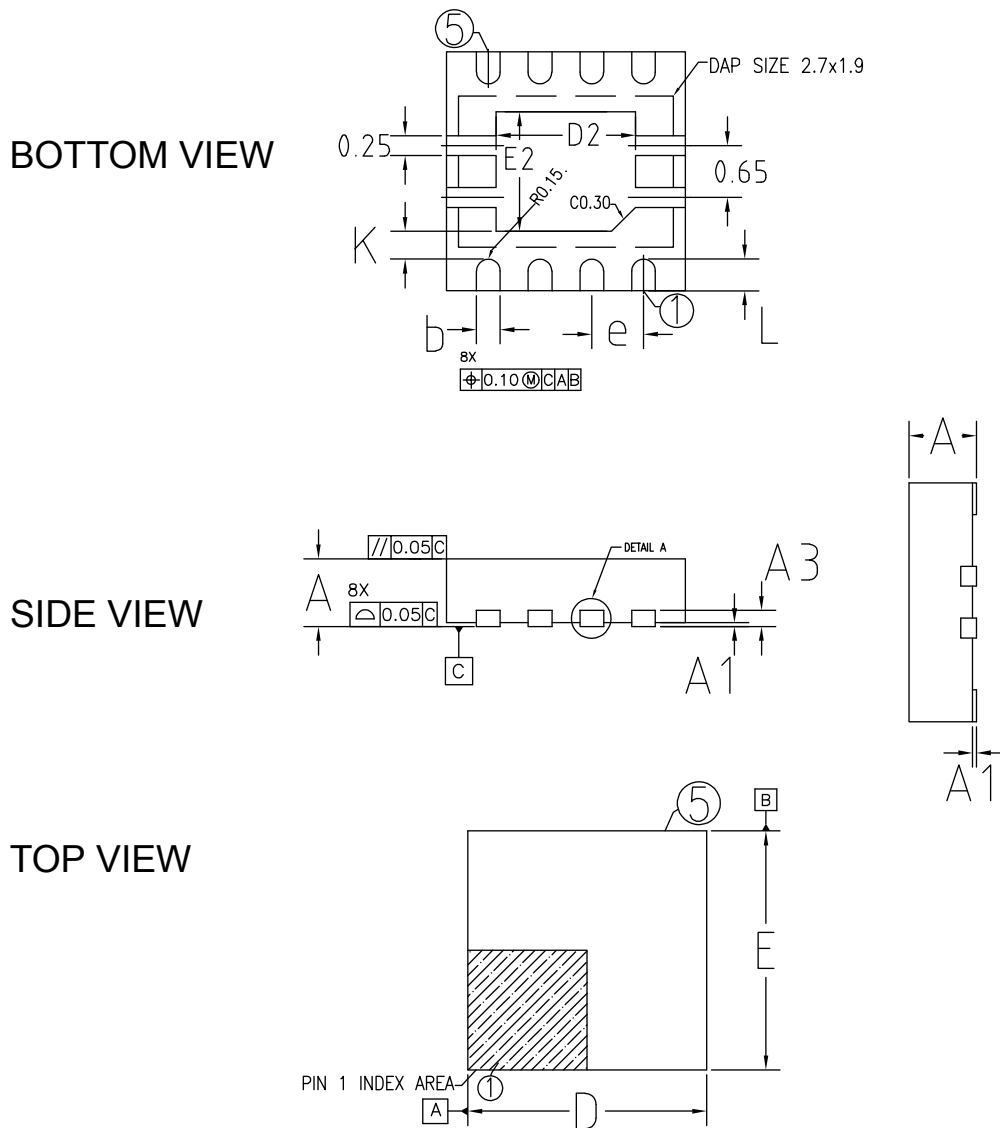
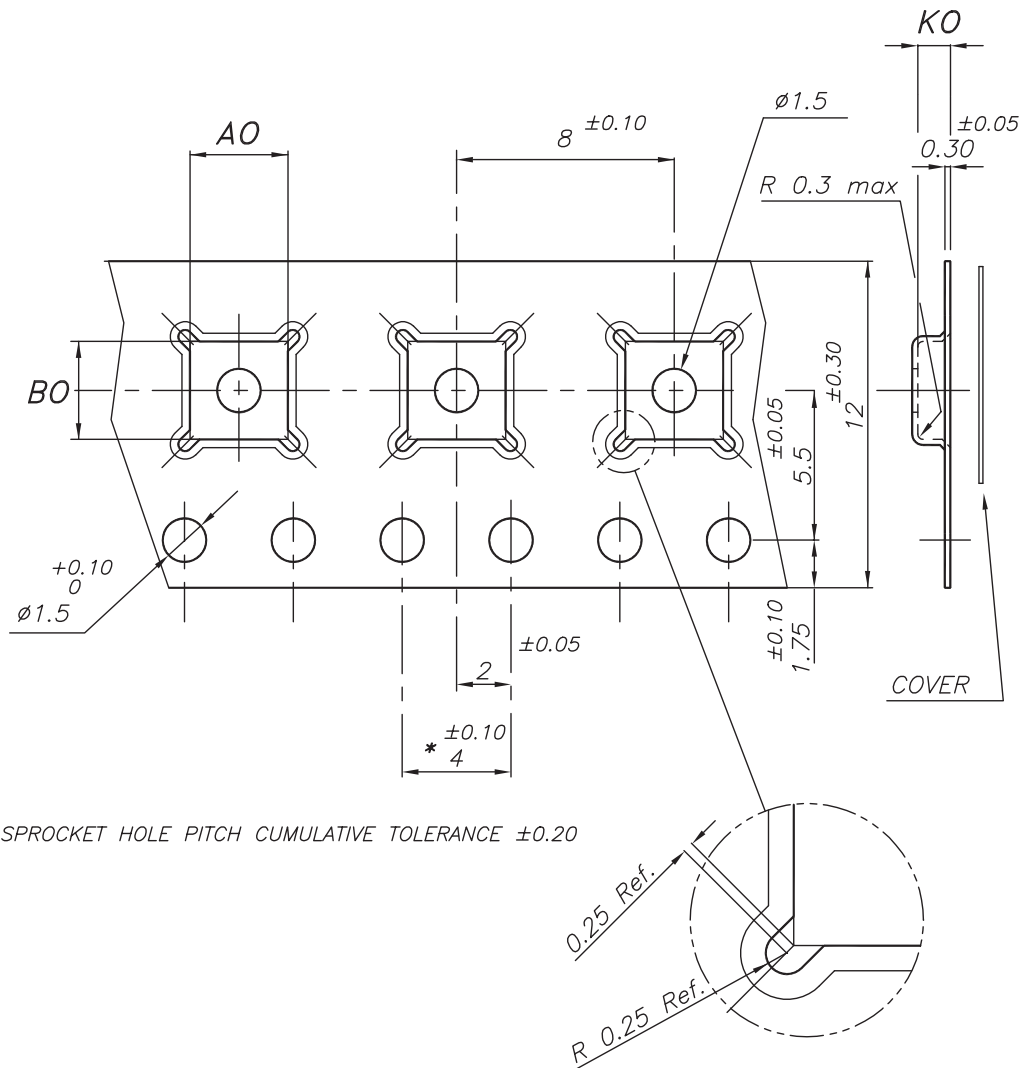


Table 6. DFN8 3x3 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.85	0.90
A1	0.00		0.05
A3	0.203 Ref.		
b	0.25	0.30	0.35
D	2.95	3.00	3.05
D2	1.65	1.75	1.85
e	0.65 BSC		
E	2.95	3.00	3.05
E2	1.40	1.50	1.60
L	0.30	0.40	0.50
K	0.35 Ref.		
N	8		

7.2 DFN8 (3 x 3 mm) package information

Figure 33. DFN8-3x3 tape outline

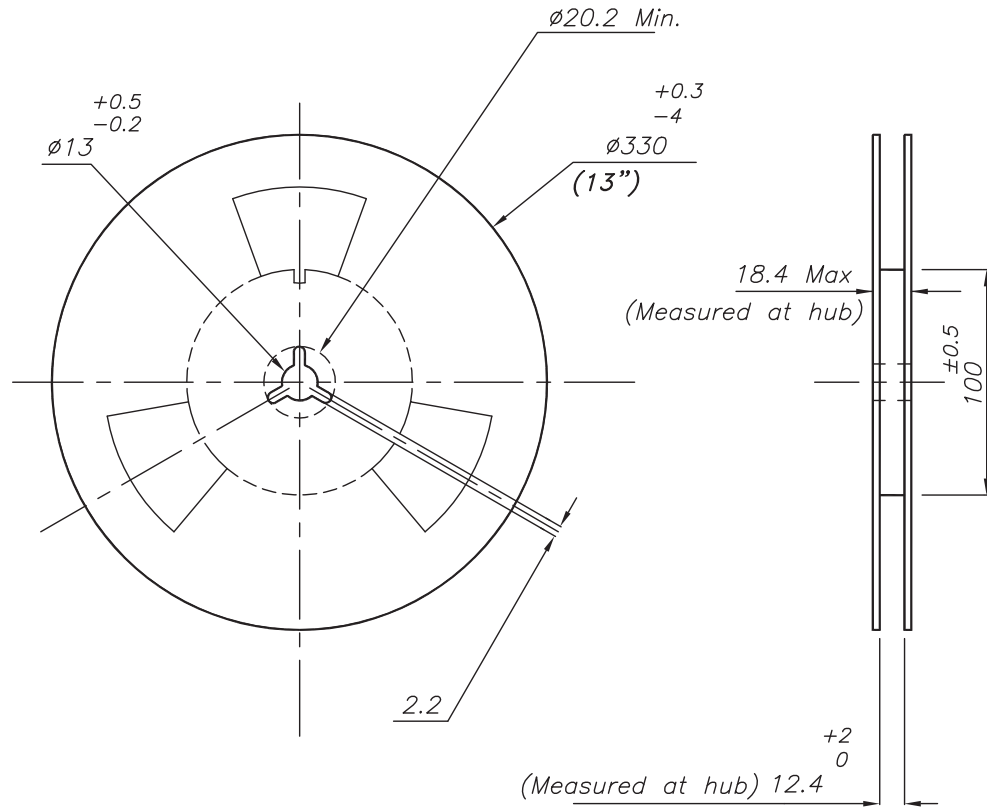


* - 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.20

Table 7. DFN8-3x3 tape mechanical data

Dim.	mm	
	Value	
Ao	3.30 ±0.10	
Bo	3.30 ±0.10	
Ko	1.10 ±0.10	

Figure 34. DFN8-3x3 reel outline



8 Ordering information

Table 8. Order code

Order codes	DFN8 3x3		
	Marking	Grade	Output voltage
LDLN050PU33R	LI5033	Industrial	3.3 V

Revision history

Table 9. Document revision history

Date	Revision	Changes
10-Jan-2019	1	Initial release.
13-Jun-2019	2	Added new order code LDLN050PU33 in Table 9. Order code and new package mechanical data Figure 33. DFN8 3x3 package drawing outline - option B.
07-Sep-2021	3	Updated figure, features, applications and description on the cover page. Updated Section 7.1 DFN8 3 x 3 package information and Table 8. Order code
13-Sep-2021	4	Updated features on the cover page.

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