Le87100
PLC Differential Line Driver
Line Driver BD870 Series

Preliminary Datasheet

Microsemi
Power Matters.™

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Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

In revision 2.0, electrical specifications are updated in Table 1, page 6.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Overview

The Le87100 device is a single-channel differential amplifier designed to drive PLC high-power signals. The Le87100 device contains a pair of wide-band amplifiers designed with Microsemi's HV15 bipolar SOI process for high-power output with low-power consumption.

Line driver gain is set externally to the device. The device can be powered from a single high-voltage supply or from dual supplies.

The device can be programmed to one of three preset bias levels to optimize power and performance. In addition, the line driver features a power down state, which forces low-power and high-impedance mode for receive transmissions or for idle operations.

The control pins respond to input levels that can be generated with a standard GPIO, but are tolerant of higher voltage logic levels.

The Le87100 device is available in a 16-pin (4 mm x 4 mm) QFN package with an exposed pad for enhanced thermal conductivity.

2.1 Features

- High-power differential output
  - Delivers signal strengths up to 15.5 dBm
  - Operates up to 13.2 V from a single supply or up to ±6.6 V from dual power supplies
  - Drive capability up to 400 mA from a single 12 V supply
  - High output impedance when disabled for a TDM operation
- User settable gain and bandwidth
  - Bandwidth up to 100 MHz
- Class AB operation
- Four operational states, low power operation
- Thermal shutdown circuitry
- Miniature 4 x 4 mm thermally enhanced package
- RoHS compliant
- Pin-compatible with industry standard line drivers

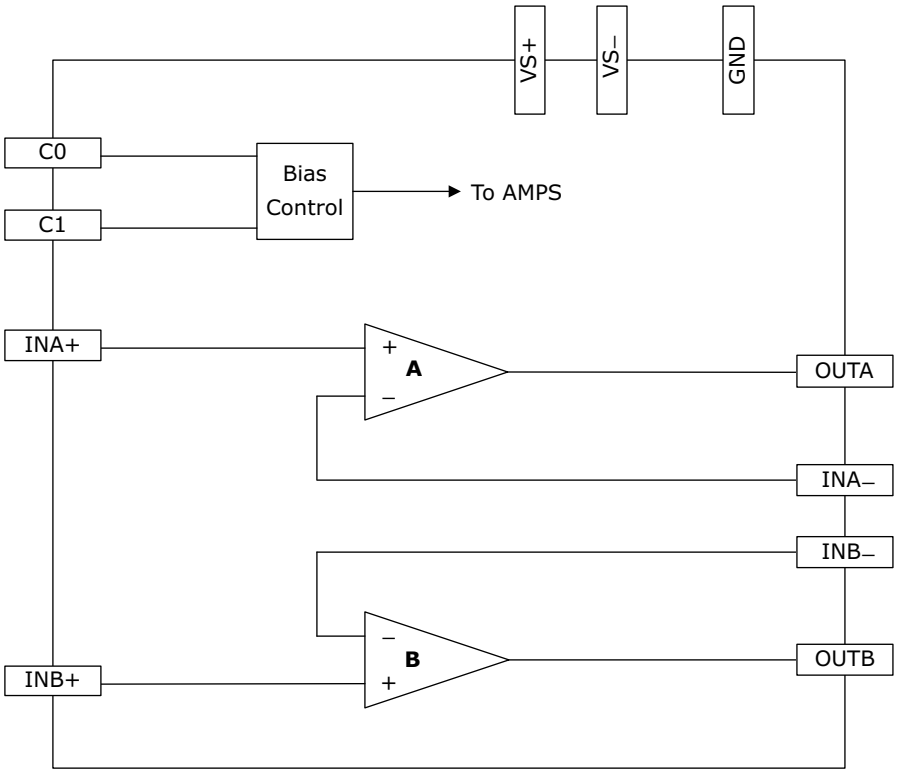
2.2 Target Applications

- Power Line Communications (PLC)
- G.HN, EOC HomePlug AV2

2.3 Block Diagram

The following figure shows the Le87100 block diagram.

Figure 1 • **Line Driver Block Diagram**



3 Functional Descriptions

3.1 Applications

The Le87100 device contains a pair of wide-band high-power current-feedback amplifiers. The external RFA and RFB resistors close the feedback loop for each amplifier. The Le87100 device is designed with the specification of RF = 1 KΩ and AV = 16. An RFA or RFB value of 1000 Ω provides a 3 dB bandwidth of ~180 MHz. In general, a lower RFA or RFB value provides a greater bandwidth and a higher RFA or RFB value provides a narrower bandwidth. If the line driver is in high-impedance when disabled, it provides a better PLC half-duplex operation.

Note: Amplifiers configured in a current-feedback arrangement exhibit some amount of gain peaking before roll-off. The higher the bandwidth, the more peaking.

The RG resistor sets the gain of both amplifiers, using the following formula:

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AV = [(RFA + RFB)/RG] + 1
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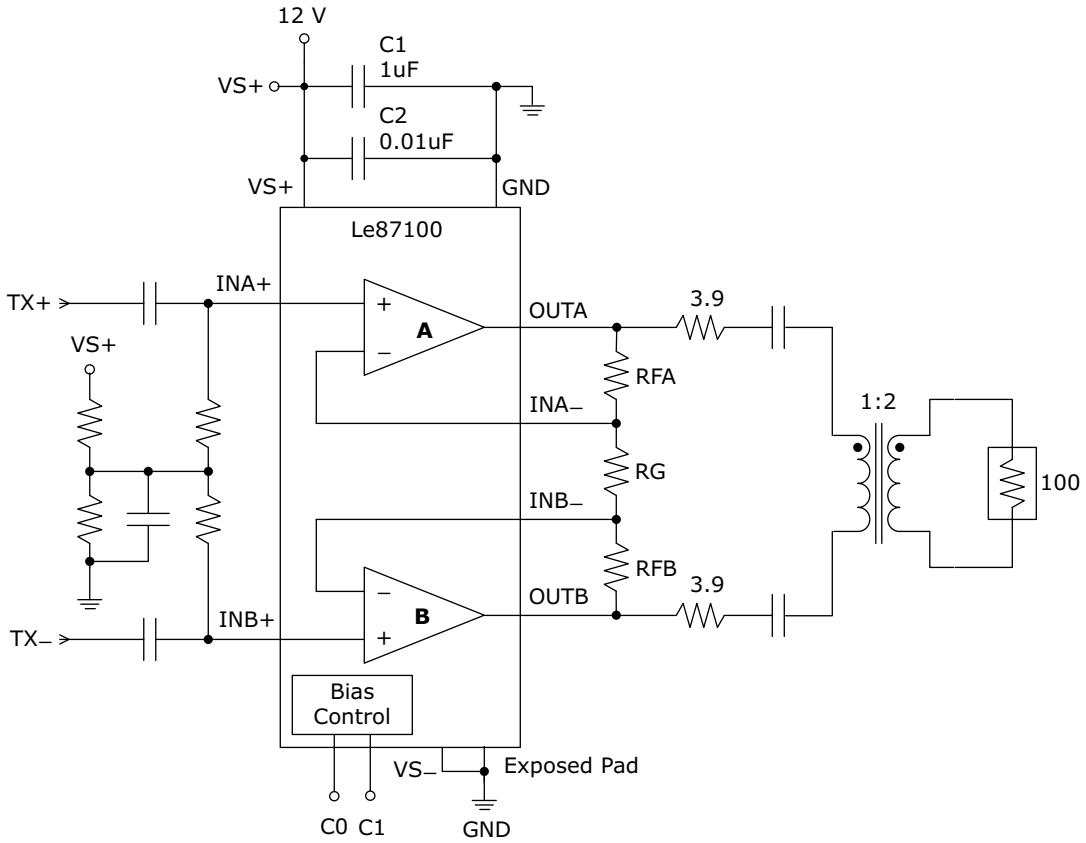
The resistor network on the INA+ and INB+ inputs sets a common-mode bias for the inputs. This bias should be set at the midpoint of VS+.

3.1.1 Block Diagram

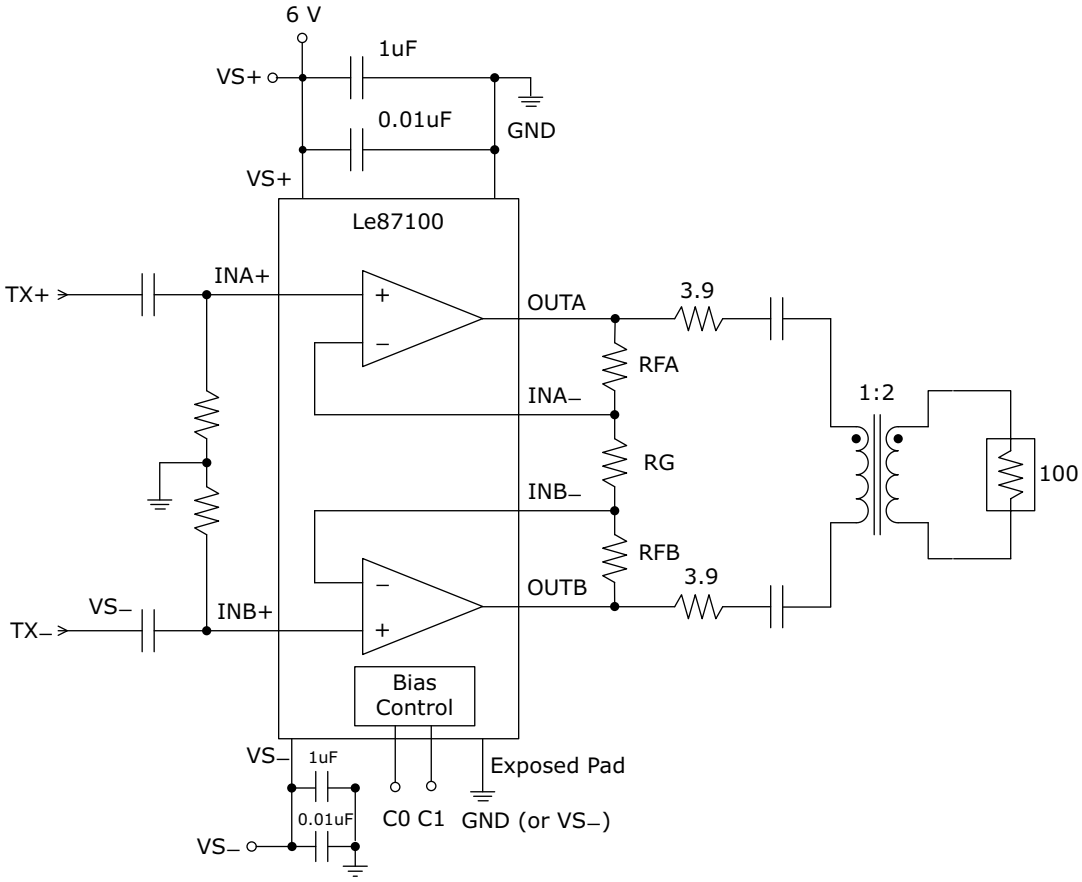
The following figure shows a typical PLC application circuit for transmission of 15.5 dBm to the line. This circuit uses a single VS supply.

Figure 2 • **Typical Application Circuit - Single Supply**



The following figure shows the typical application circuit using dual VS supplies. The resistor network on the INA+ and INB+ inputs sets a common-mode bias for the inputs.

Figure 3 • **Typical Application Circuit - Dual Supplies**



3.1.1.1 Input Considerations

The driving source impedance should be less than 100 nH to avoid any ringing or oscillation.

3.1.1.2 Output Driving Considerations

The internal metalization is designed to drive 200 mArms sinusoidal current and there is no current limit mechanism. It is recommended that series resistors are used to drive lines.

If a DC current path exists between the two outputs, DC current can flow through the outputs. To avoid the DC current flow, the most effective solution is to place DC blocking capacitors in series with the outputs.

3.1.1.3 Protection

The line driver has thermal shutdown protection. Amplifiers turn off and outputs appear as high-impedance if the silicon temperature rises above the TSD temperature.

3.1.1.4 Power Supplies and Component Placement

The power supply should be well bypassed with decoupling placed close to the Le87100 device.

4 Electrical Specifications

This section provides the DC characteristics, AC characteristics, and recommended operating conditions of the Le87100 device.

Typical Conditions: VS+ = 12 V and T_A = 25 °C

VS– = GND, RF = 1000 Ω, and RG = 133 R. For more information, see Figure 4, page 7.

The following table shows the electrical specifications, full bias.

Table 1 • **Electrical Specifications**

Symbol	Parameter Description	Condition	Min	Typical	Max	Unit
I_{VS+}	Quiescent Supply Current	Full Bias	27	32	37	mA
I_{VS+}	Quiescent Supply Current	Medium Bias	19	23	27	mA
I_{VS+}	Quiescent Supply Current	Low Bias	12	17	20.5	mA
I_{VS+}	Quiescent Supply Current	Power Down	0.8	1.2	1.8	mA
V_{IH}	Input High Voltage		2.0	3.3	5.5	V
V_{IL}	Input Low Voltage		–0.3	0	0.8	V
I_{IH}[1]	Input High Current	C0, C1 = 3.3 V	–150	–90	–30	µA
I_{IL}[1]	Input Low Current	C0, C1 = 0 V	–1.5	1	–1.5	µA
I_B[2]	Input at mid-supply voltage		–7	2	7	µA
I_B[2]	Input DM mismatch		–0.5	0	0.5	µA
I_B[2]	–Input at mid-supply voltage		–90	–30	55	µA
I_B[2]	–Input DM mismatch		–35	0	35	µA
I_B[2]	–Input CM		–90	–30	55	µA
e_N	Input Noise Voltage	f > 1 MHz		6		nV/$\sqrt{Hz}$
i_N	+Input Noise Current	f > 1 MHz		13		pA/$\sqrt{Hz}$
i_N	–Input Noise Current	f > 1 MHz		50		pA/$\sqrt{Hz}$
V_O[2]	Output Voltage	VS = ±6 V, R_{Load} > 1000 Ω	±4.85	±5.0		V
V_O[2]	Output Voltage	VS = ±6 V, R_{Load} = 29 R; Linear		±4.6		V
V_O[2]	Output Voltage	VS = ±6 V, R_{Load} = 29 R; Driven to rail	±4.2	±4.7		V
V_O[2]	Slew Rate	V_O = –5 to 5 V		1200		V/µs
MTPR		2 MHz to 50 MHz, 25 KHz, PLINE = 15.5 dBm, PAR = 15 dB		–43		dBc
MTPR-OFF		2 MHz to 50 MHz, 25 KHz, PLINE = 15.5 dBm, PAR = 15 dB		–55		dBc
I_O	Output Current	Linear Output Current	±300	±400		mA
BW	Bandwidth, –3 dB	RF = 1000 Ω, RG = 133 Ω, AV = 16		180		MHz

Table 1 • **Electrical Specifications *(continued)***

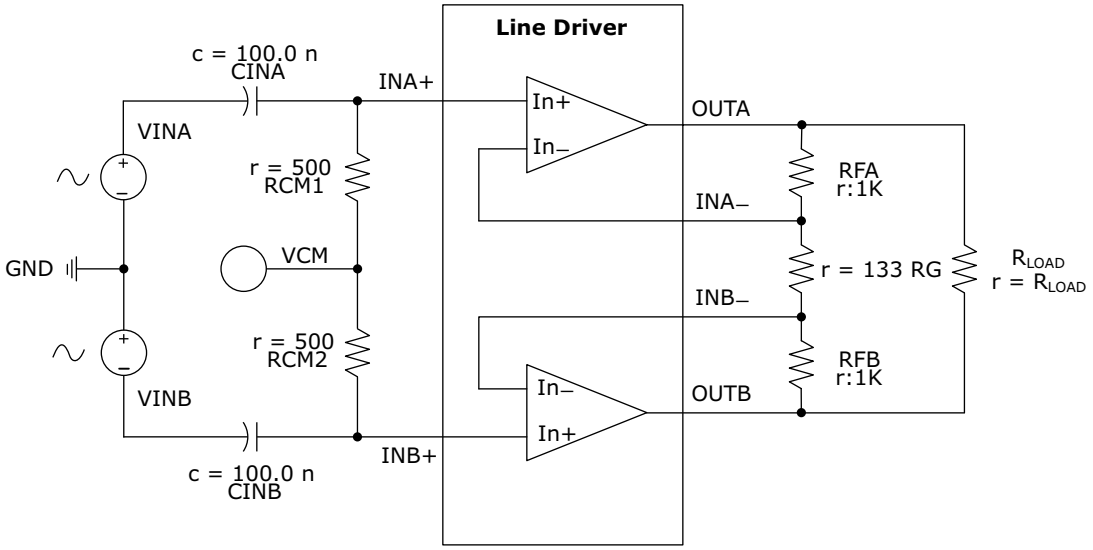
Symbol	Parameter Description	Condition	Min	Typical	Max	Unit
THD[2]	Total Harmonic Distortion	f = 200 kHz, V_O = 12 Vp-p, R_{LOAD} >= 350 Ω		–88	–67	dBc
THD[2]	Total Harmonic Distortion	f = 200 kHz, V_O = 12 Vp-p, R_{LOAD} = 29 Ω		–72	–68	dBc
THD[2]	Total Harmonic Distortion	f = 4 MHz, V_O = 12 Vp-p, R_{LOAD} = > 350 Ω		–64	–58	dBc
THD[2]	Total Harmonic Distortion	f = 4 MHz, V_O = 12 Vp-p, R_{LOAD} = 29 Ω		–51	–48	dBc
TSD	Thermal Shutdown			170		°C

1. Positive current flows out of pin.
2. Guaranteed by design and device characterization.

Note: The line driver can survive a permanent short circuit on the line.

The following figure shows the basic test circuit.

Figure 4 • **Basic Test Circuit**



4.1 Operational States

Logic input control pins have internal pull-down resistors. By default, the line driver powers-up in the full bias state.

The following table lists the operational state control.

Table 2 • **Operational State Control**

C1	C0	Device State
0	0	Full bias
0	1	Medium bias
1	0	Low bias
1	1	Power down

The line driver is active for transmission in full, medium, and low bias states. These states are different only in the level of bias current applied to amplifiers, allowing the user to select the lowest amount of power required to achieve the desired linearity.

The amplifier outputs are set for high-impedance in the power-down state.

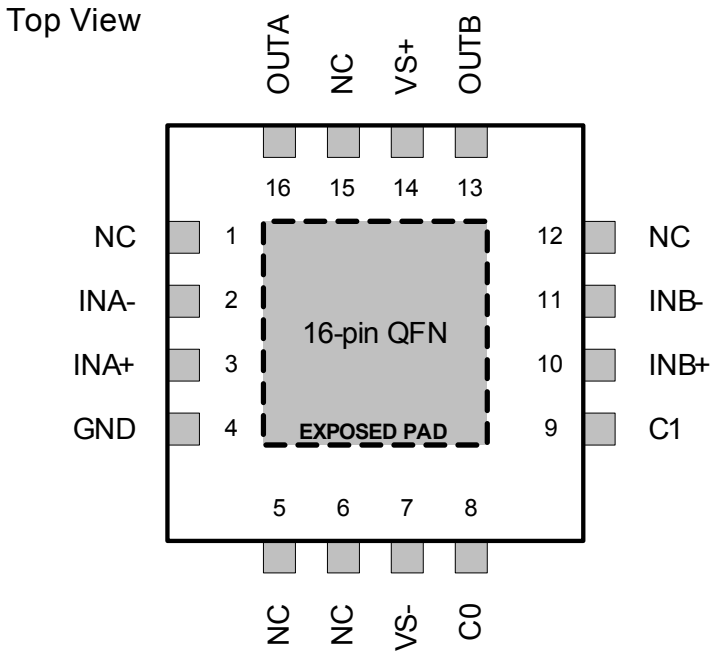
5 Pin Descriptions

The Le87100 device has 16 pins, which are described in this section.

5.1 Connection Diagram

The following illustration represents the pin diagram for the Le87100 device, as seen from top of the package.

Figure 5 • **Connection Diagram**



Note: The device incorporates an exposed die pad on the underside of its package. The pad acts as a heat sink and must be connected to a copper plane through the thermal plane for proper heat dissipation. It is electrically isolated and may be connected to GND or VS–.

5.1.1 Pin Description

The following table shows the functional pin descriptions for the Le87100 device.

Table 3 • **Pin Descriptions**

Pin	Pin Name	Type	Description
1, 5, 6, 12, 15	NC		No connects, no internal connection
2	INA–	Input	Amplifier A negative input
3	INA+	Input	Amplifier A positive input
4	GND	Ground	Low noise analog ground
7	VS–	Power	Negative power supply. Connect to GND if single supply.
8, 9	C0, C1	Inputs	Control inputs
10	INB+	Input	Amplifier B positive input
11	INB–	Input	Amplifier B negative input
13	OUTB	Output	Amplifier B output
14	VS+	Power	Positive power supply
16	OUTA	Output	Amplifier A output
Exposed Pad			The exposed pad must be connected to a thermal plane, it is electrically isolated and can be connected to GND or VS–.

6 Package Information

6.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings.

Table 4 • **Absolute Maximum Ratings**

Names	Range
Storage temperature	–65 °C ≤ TA ≤ 150 °C
Operating junction temperature	–40 °C ≤ TJ ≤ 150 °C[1]
VS+ to GND	–0.3 V to 13.3 V
VS- to GND	–6.6 V to 0.3 V
Continuous driver output current	VS+ to VS–
Control inputs C0/1	–0.3 V to VS+
Maximum device power dissipation, continuous [2] - TA = 85 °C, PD	1.0 W
Junction to ambient thermal resistance [2, 3], θJA	52 °C/W
Junction to board thermal resistance [2], θJB	26 °C/W
Junction to case bottom (exposed pad) thermal resistance, θJC (BOTTOM)	14.6 °C/W
Junction-to-top characterization parameter [2], ψJT	3.1 °C/W
ESD immunity (Human Body Model)	JESD22 class 2 compliant
ESD immunity (Charge Device Model)	JESD22 class IV compliant

1. Continuous operation above 145 °C junction temperature may degrade device reliability.
2. For more information, see "Thermal Resistance".
3. No air flow.

6.1.1 Thermal Resistance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad should be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to larger internal copper planes.

6.1.2 Package Assembly

The green package devices are assembled with enhanced, environment-friendly materials that have no lead, halogens, or antimony. The leads possess a matte tin plating that is compatible with conventional board assembly processes or newer lead-free board assembly processes.

Refer to IPC/JEDEC J-Std-020 for recommended peak soldering temperature and solder reflow temperature profile.

6.1.3 Operating Ranges

Microsemi guarantees the performance of this device over the –40 °C to 85 °C temperature range by conducting electrical characterization and a single insertion production test coupled with periodic sampling. These procedures comply with the Telcordia GR-357-CORE generic requirements for assuring the reliability of components used in telecommunications equipment.

The following table shows the operating ranges.

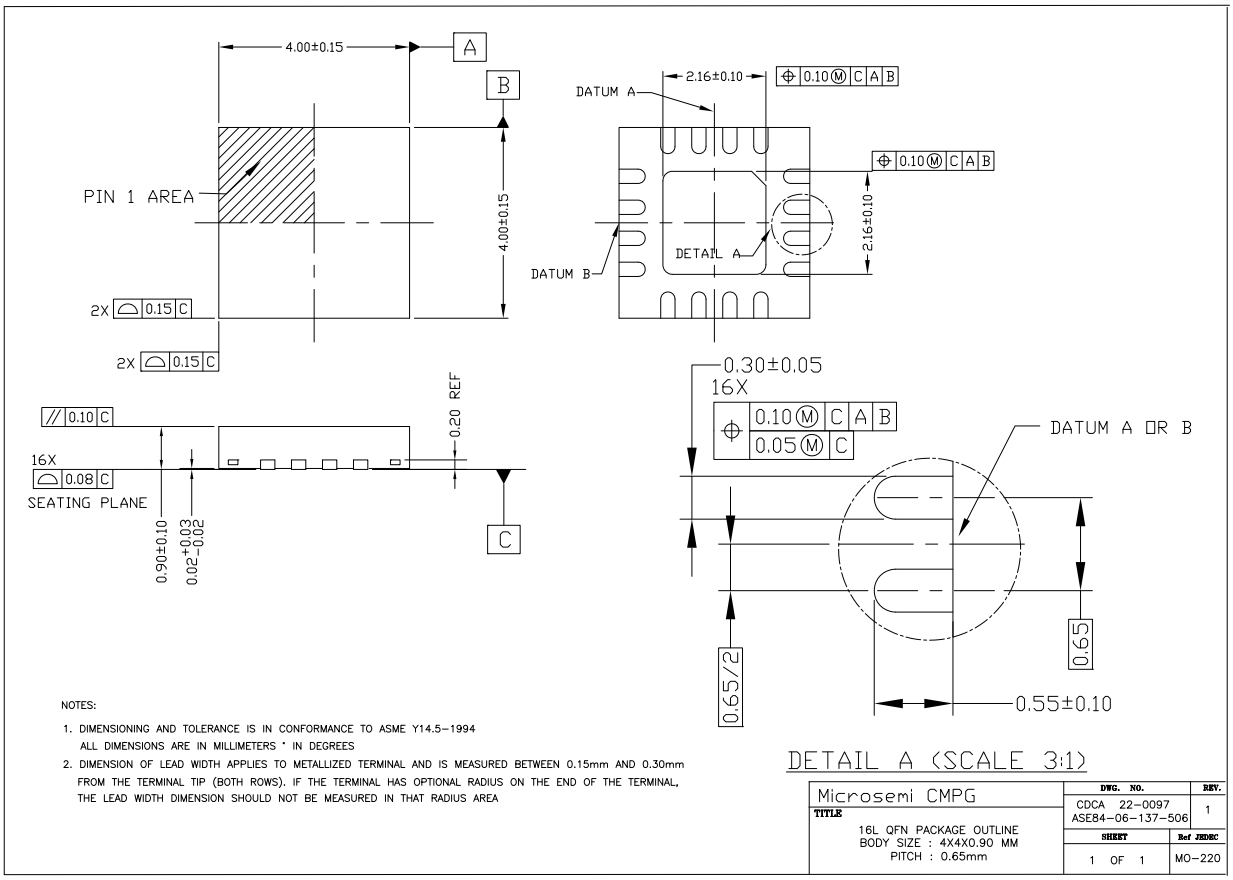
Table 5 • **Operating Ranges**

Name	Unit	Range
Ambient temperature	T_A	–40 °C to 85 °C
Single power supply operation	VS+ with respect to GND, VS– tied to GND: Typical usage	8 V to 12 V, 12 V to ±10%
Dual power supply operation	VS+/VS– with respect to GND: Typical usage	±4 V to ±6 V, ±6 V to ±10%

6.2 Physical Dimension - 16-Pin Diagram

The following illustration shows the package drawing for the Le87100 device. The drawing presents the top, bottom, and side views of the device.

Figure 6 • **Package Drawing**



Note: Packages may have mold tooling markings on the surface, that vary with the tool used in manufacturing. These markings have no impact on the form, fit, or function of the device.