Document ID# 152633 Version 3 July 2016

Features

- Operations to 86 MHz
- High Voltage Gain – 25 dB
- Class AB Operation
- Enable/Disable Control
- Capable of Driving Line Impedances Between 50 Ω to 200 Ω
- Low Power Operation
- 16-pin, 4x4 mm QFN Package
- RoHS Compliant

Applications

- Power Line Communications
- Home Networking
- HPNA
- G.hn

Description

The Le87511 is a single channel differential amplifier designed to work in home network G.hn power line communication systems.

The Le87511 contains a pair of wideband amplifiers designed with Microsemi's HV30 Bipolar SOI process for low power consumption.

The line driver gain is fixed internally. The amplifiers are powered from a single supply.

The device can be programmed to one-of-four preset Bias levels to optimize power and performance. In addition, the line driver features a Disable state which forces a low-power, high impedance mode for receive transmissions.

The control pins respond to input levels that can be generated with a standard GPIO.

The Le87511 is available in a 16-pin (4 mm x 4 mm) QFN package with exposed pad for enhanced thermal conductivity.

Ordering Information

Le87511NQC	16-pin QFN Green Pkg.	Tray
Le87511NQCT	16-pin QFN Green Package	Tape and Reel

The green package is Halogen free and meets RoHS 2 Directive 2011/65/EU of the European Council to minimize the environmental impact of electrical equipment.

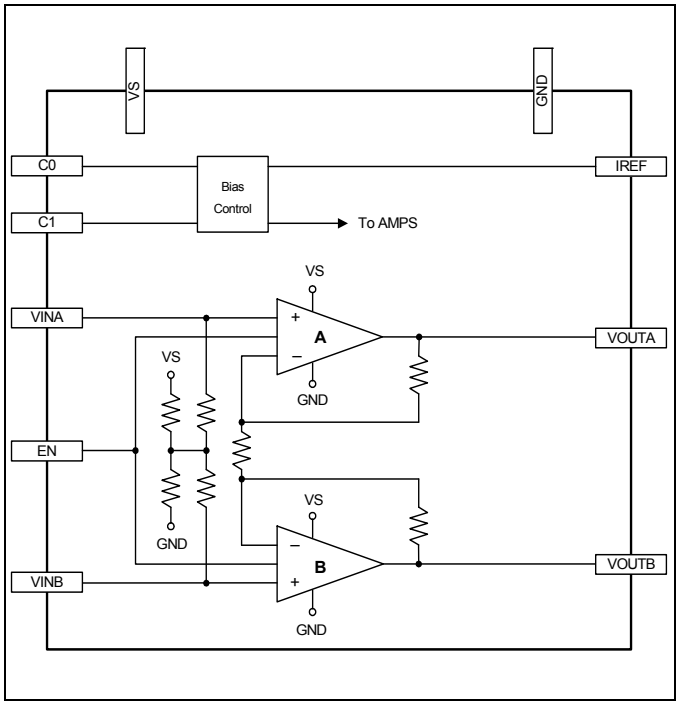

Figure 1 - Block Diagram

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Pin Diagram

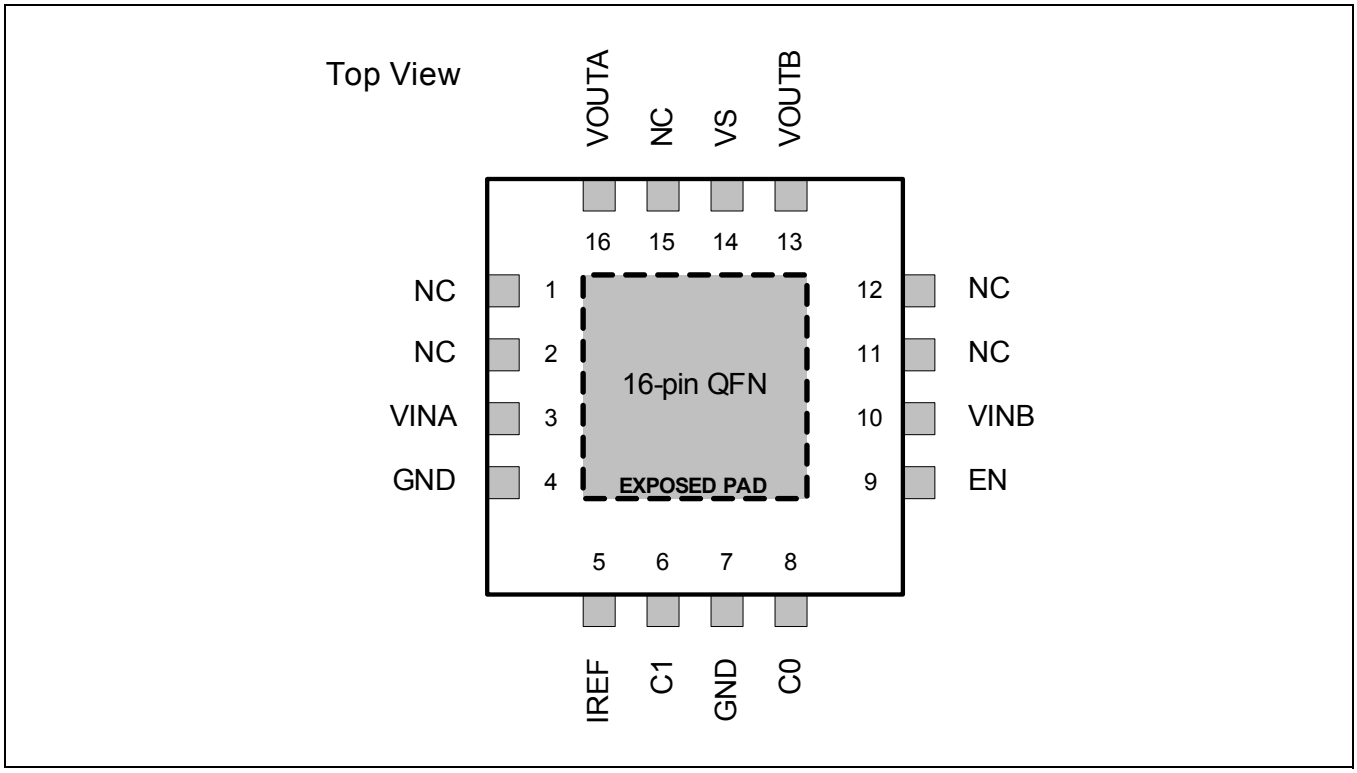


Figure 2 - Pin Diagram

Note 1: Pin 1 is marked for orientation.

Note 2: The device incorporates an exposed die pad on the underside of its package. This pad must be connected to GND. The pad acts as a heat sink and must be connected to a copper plane through thermal vias for proper heat dissipation.

Pin Description

Pin #	Pin Name	Type	Description
1, 2, 11, 12, 15	NC		No connects, no internal connection
3	VINA	Input	Amplifier A input
4, 7	GND	Ground	Low noise analog ground
5	IREF	Input	Device Internal Reference Current. Connect a resistor to GND.
6, 8	C1, C0	Inputs	Control inputs, sets operation state when channel enabled
9	EN	Input	Enable/Disable control
10	VINB	Input	Amplifier B input
13	VOUTB	Output	Amplifier B output
14	VS	Power	Power supply
16	VOUTA	Output	Amplifier A output
	Exposed Pad	Ground	Low noise analog ground. This pad must be connected to GND.

Table 1 - Pin Descriptions

Absolute Maximum Ratings

Stresses above the values listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage Temperature	$-65°C \le T_A \le +150°C$
Operating Junction Temperature	$-40°C \le T_J \le +150°C$[1]
VS to GND	–0.3 V to +22 V
Driver inputs VINA/B	VS to GND
Control inputs C0/1, EN	–0.3 V to +4.0 V
Maximum device power dissipation, continuous (2) - T_A = 85°C, P_D	1.0 W
Junction to ambient thermal resistance (2,3), θ_{JA}	52.0 °C/W
Junction to board thermal resistance (2), θ_{JB}	26.0 °C/W
Junction to case bottom (exposed pad) thermal resistance, θ_{JC} (BOTTOM)	14.6 °C/W
Junction-to-top characterization parameter (2), ψ_{JT}	3.1 °C/W
ESD Immunity (Human Body Model)	JESD22 Class 2 compliant
ESD Immunity (Charge Device Model)	JESD22 Class IV compliant

Notes:

1. *Continuous operation above 145°C junction temperature may degrade device reliability.*
2. *See "Thermal Resistance".*
3. *No air flow.*

Thermal Resistance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to larger internal copper planes.

Package Assembly

The green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes.

Refer to IPC/JEDEC J-Std-020 for recommended peak soldering temperature and solder reflow temperature profile.

Operating Ranges

Microsemi guarantees the performance of this device over the -40°C to +85°C temperature range by conducting electrical characterization and a single insertion production test coupled with periodic sampling. These procedures comply with the Telcordia GR-357-CORE Generic Requirements for Assuring the Reliability of Components Used in Telecommunications Equipment

Ambient temperature	T_A	-40°C to +85°C
Power Supply	VS with respect to GND: Typical usage	+12 V to +20 V, +17.5 V

Device Specifications

VS = +17.5 V. Device in Enable, Bias Level 3 state using the Basic Test Circuit (Figure 3), unless otherwise specified.

Typical Conditions*:* T_A = 25°C.

Min/Max Parameters*:* Guaranteed across process variation and T_A = -40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	Notes
Power							
I_{VS}	Quiescent Supply Current	VINA/B floating				mA	
		Enable, Bias Level 3		21.8	27.4		
		Enable, Bias Level 2		19.1	24.1		
		Enable, Bias Level 1		16.4	20.8		
		Enable, Bias Level 0		13.7	17.5		
		Disable State		1.0			
P_{VS}	Supply Power	TX 16 dBm with R_{LINE} = 100 Ω (see Figure 4)		940		mW	1
		Disable, Full signal on line		60			
		Disable, Quiescent		15			
Control Input (C0/1, EN) Characteristics							
V_{IH}	Input High Voltage		2.0			V	
V_{IL}	Input Low Voltage				0.8	V	
Channel Input (VINA/B) Characteristics							
V_{IPK}	Input Signal Peak				0.75	V_{PKD}	1
Z_I	Differential Input Impedance	VINA – VINB at 2 MHz	10			kΩ	1
Channel Output (VOUTA/B) Characteristics							
V_O	Output Voltage	R_{LOAD} = 50 Ω, VS ≥17.5 V				V	
		Positive Swing		16			
		Negative Swing		2			
		Differential Swing	13.35				1
I_O	Output Current		270			mA	1
Z_O	Disabled Output Impedance	Differential	400	2300		Ω	

Table 2 - Electrical Specifications

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	Notes
Channel Dynamic Characteristics							
	Voltage Gain	VOUT/VIN at 1 MHz		25 17.78		dB V/V	
	Bandwidth	-3 dB	86			MHz	1
	Gain Flatness	to 80 MHz	-1.5		1	dB	1
Noise	Input Referred Noise	at VIN			12.5	nV/$\sqrt{Hz}$	1
MTPR	Multi Tone Power Ratio	+16 dBm, 2–30 MHz +16 dBm, 30–86 MHz -5 dBm, 2–86 MHz	50 20 50			dBc	1, 3
	Switching Time	Enable/Disable states			1	µs	1
TSD	Thermal Shutdown Temperature Hysteresis			170 20		°C	

Notes:
1. Guaranteed by design and device characterization.
2. The line driver can survive a permanent short circuit on the line.
3. Tested using the Typical Application Circuit (Figure 4), VS ≥17.5 V.

Table 2 - Electrical Specifications

Test Circuit

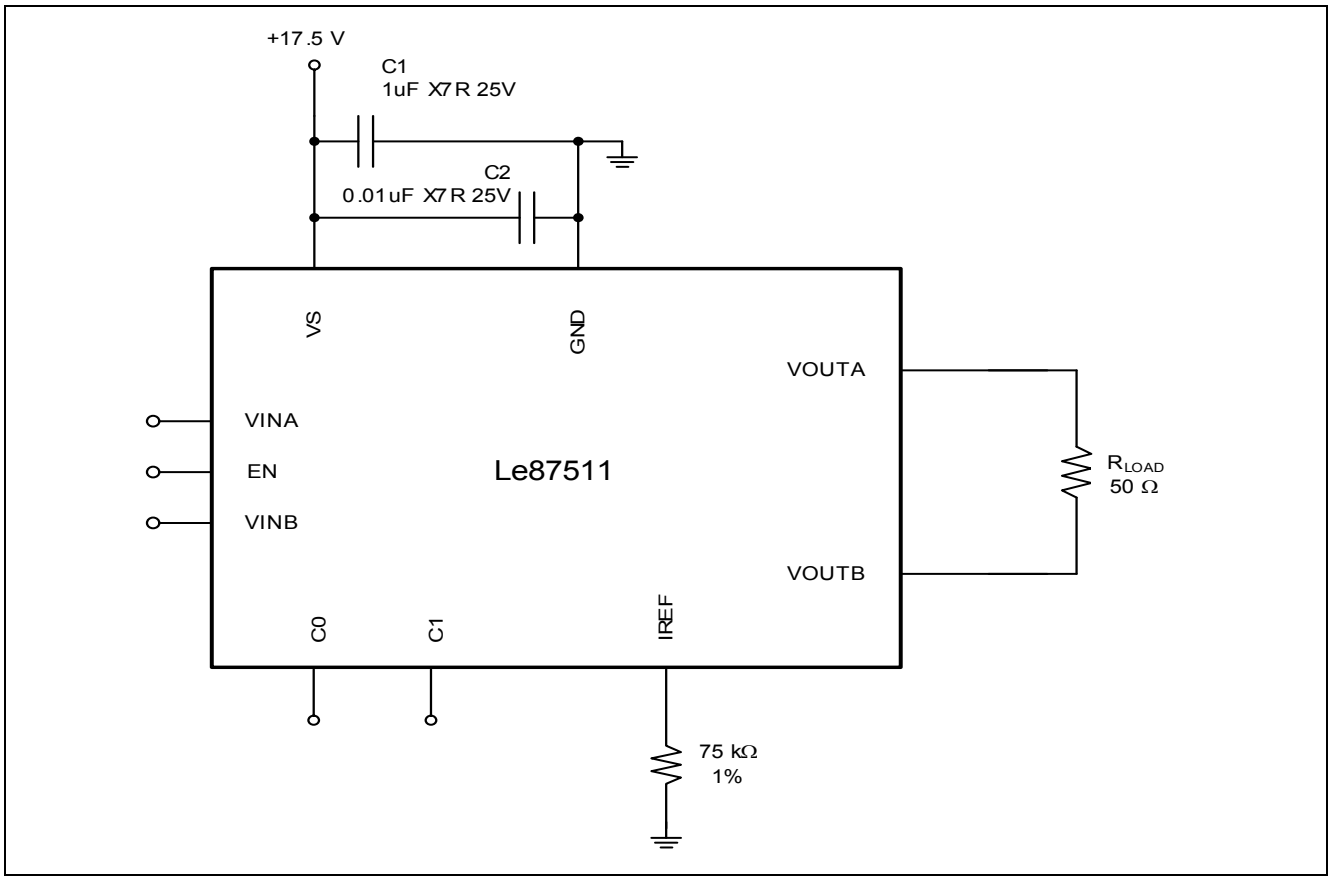


Figure 3 - Basic Test Circuit

Operation States

Operation state control is depicted in Table 3.

Logic input control pins have internal pull-down resistors. By default, the line driver will power-up in the Disable State with EN = 0.

EN	C1	C0	Device State
1	0	0	Enable TX – Bias Level 3 (Highest)
1	0	1	Enable TX – Bias Level 2
1	1	0	Enable TX – Bias Level 1
1	1	1	Enable TX – Bias Level 0 (Lowest)
0	X	X	Disable/RX
X = Don't care			

Table 3 - Operation State Control

The EN pin is used to rapidly switch the line driver between Enable/Disable states.

Enable States

Enable TX is used for transmit time periods. Bias current is applied to the amplifiers and the line driver provides gain from VIN to VOUT. When the amplfier bias current is increased, the amplifier operates with improved linearity, but also higher power.

Control pins C1/C0 are used to select 1 of 4 bias current levels during transmit This allows the user to make an appropriate trade-off between power and performance.

Pin IREF is used to connect a low-tolerance resistor between the pin and ground. This resistor reduces bias current variation in the line driver. This resistor can be varied from its nominal value to allow further adjustment of the amplifier bias currents.

Disable State

Disable/RX is used during receive time periods. The line driver amplifiers are powered-down and amplifier outputs are high-impedance. Gain-setting resistors remain in place and present a differential impedance at the output pins.

During Disable/RX, a full power signal on the line will not be distorted by the high-impedance line driver.

Applications

The Le87511 integrates a high-power line driver amplifier designed for low distortion for signals up to 86 MHz.

A typical application interface circuit is shown in Figure 4.

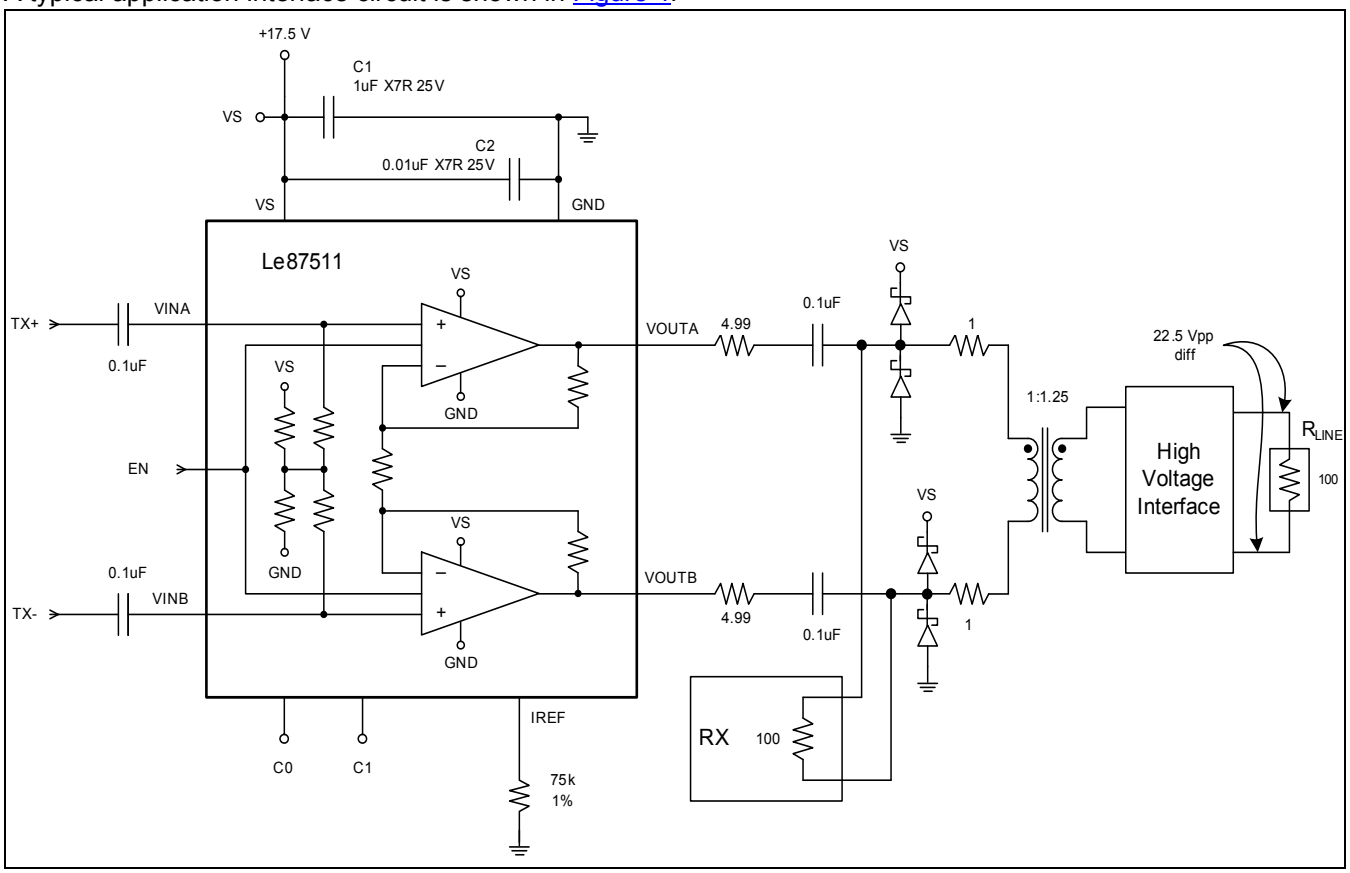


Figure 4 - Typical Application Circuit

The amplifiers have identical positive gain connections with common-mode rejection. Any DC input errors are duplicated and create common-mode rather than differential line errors.

Output Driving Considerations

The internal metallization is designed to drive 200 mA_{RMS} sinusoidal current and there is no current limit mechanism. Driving lines without a series resistor is not recommended.

If a DC current path exists between the two outputs, a DC current can flow through the outputs. To avoid DC current flow, the most effective solution is to place DC blocking capacitors in series with the output as shown in Figure 4.

Protection

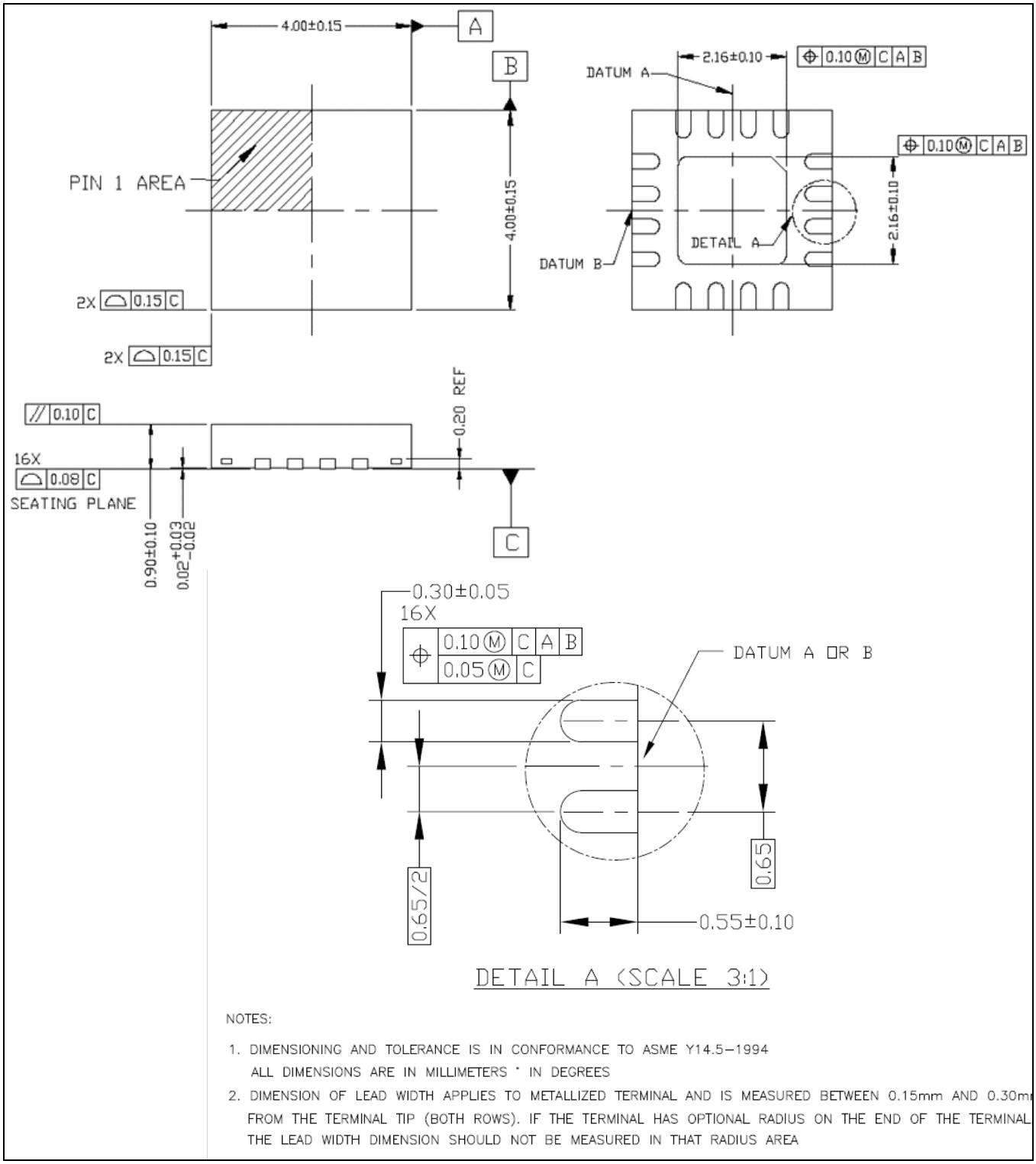
The line driver is designed to operate with various protection components. Figure 4 shows a pair of schottky diodes providing voltage clamping. To maintain stability, the capacitance of these diodes should be less than 30 pF.

Power Supplies and Component Placement

The power supply should be well bypassed with decoupling placed close to the Le87511.

Physical Dimensions

16-Pin QFN



Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.