LM202802-M-C-300

PIN Diode Limiter
2 - 8 GHz

Rev. V1

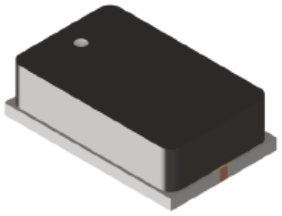
Features

- Surface Mount Limiter in 8 mm x 5 mm x 2.5 mm Package
- Incorporates NIP & PIN Limiter Diodes
- Higher Average Power Handling than Plastic: 45 dBm
- Lower Insertion Loss: 1.4 dB
- Lower Flat Leakage Power: 20 dB
- RoHS* Compliant

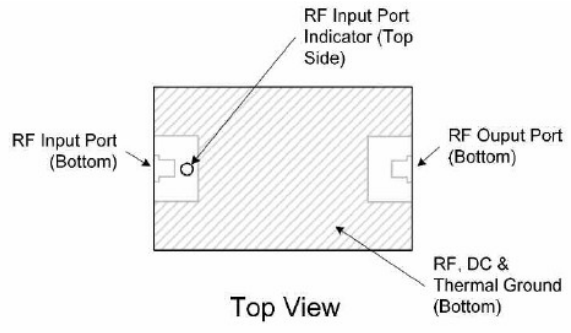
Description

The LM202802-M-C-300 Surface Mount PIN Diode Limiter Module is a surface mount, passive 2-stage power limiter. It is manufactured using a proven hybrid manufacturing process incorporating silicon NIP and PIN diodes integrated onto a ceramic substrate. This low profile, surface mount component offers superior small and large signal performance. This product is designed to minimize small signal insertion loss for very low receiver noise figure and high isolation for low flat leakage power for effective receiver protection from 2 - 8 GHz.

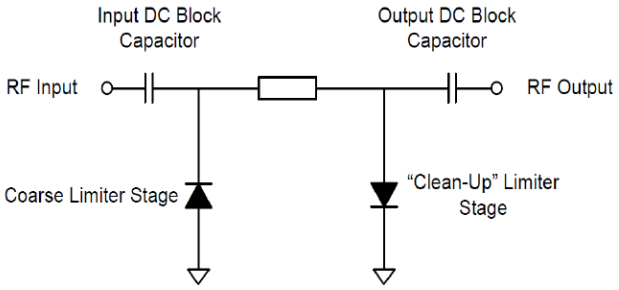
The design incorporates a silicon NIP coarse limiter diode and a silicon PIN clean-up stage diode to provide broadband microwave performance from 2 - 8 GHz. The NIP and PIN diode configuration eliminates the need to include an RF choke to complete the DC bias return path. The very low thermal resistance (NIP diode: <20ºC/W, PIN diode: <90ºC/W, junction to the bottom surface of the package) enables the limiter to safely and reliably handle RF CW incident power levels of 45 dBm and RF peak incident power levels of 53 dBm (1 µs RF pulse width, 0.1% duty cycle). The low PIN and NIP diodes' series resistances (<1.5 Ω) provide low flat leakage power (<22 dBm) and the thin I layer of the output stage provides low spike leakage energy (<0.5 Ergs) for superior LNA protection. No external control signals are required.



Pin Out



Limiter Schematic



Ordering Information

Part Number	Package
LM202802-M-C-300-T	tube packaging
LM202802-M-C-300-R	250 or 500 piece reel
LM202802-M-C-300-W	waffle packaging
LM202802-M-C-300-E	RF evaluation board

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

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Electrical Specifications: Freq. = 2 - 8 GHz, P_{IN} = 0 dBm, T_A = +25°C, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	2 GHz ≤ F ≤ 8 GHz, P_{IN} = -10 dBm	dB	-	1.2	1.4
Return Loss	2 GHz ≤ F ≤ 8 GHz, P_{IN} = -10 dBm	dB	13	15	-
Input 1 dB Compression Point	2 GHz ≤ F ≤ 8 GHz	dBm	7	8	10
2ND Harmonic	P_{IN} = -10 dBm F_0 = 2.0 GHz	dBc	-	-50	-45
Peak Incident Power	RF Pulse Width = 1 µs, duty cycle = 0.1%	dBm	-	-	53
CW Incident Power	2 GHz ≤ F ≤ 8 GHz	dBm	-	-	45
Flat Leakage Power	P_{IN} = 50 dBm, RF pulse width = 1 µs, duty cycle = 0.1%	dBm	-	20	22
Spike Leakage Energy	P_{IN} = 60 dBm peak, RF pulse width = 1 µs, duty cycle = 0.1%	erg	-	0.3	0.5
Recovery Time	50% falling edge of RF pulse to 1 dB IL, P_{IN} = 50 dBm peak, RF pulse width = 1 µs, duty cycle = 0.1%	µs	-	1.5	2.0

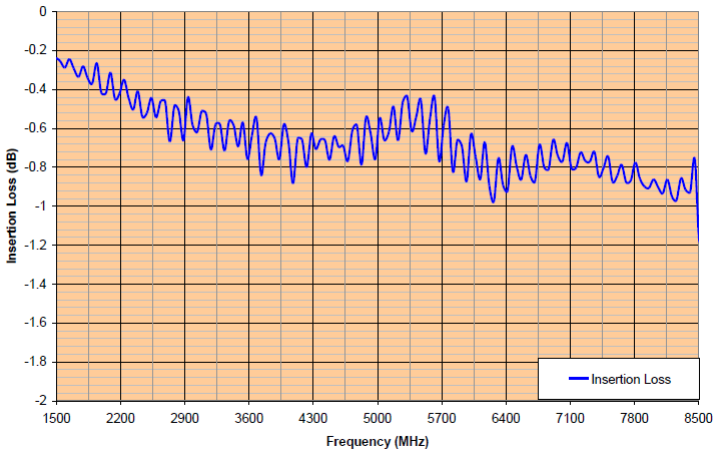
Absolute Maximum Ratings[1,2]

Parameter	Absolute Maximum
RF CW Incident Power @ +85°C, Source & Load VSWR <1.2:1 Derate linearly t 0 W @ T_C = +150°C[3]	45 dBm
RF Peak Incident Power @ +85°C, Source & Load VSWR <1.2:1 Derate linearly t 0 W @ T_C = +150°C[3]	53 dBm
Thermal Resistance Junction to bottom surface of package	25°C/W
Junction Temperature	+175°C
Operating Temperature	-65°C to +125°C
Storage Temperature	-65°C to +150°C
Assembly Temperature	260°C for 30 seconds

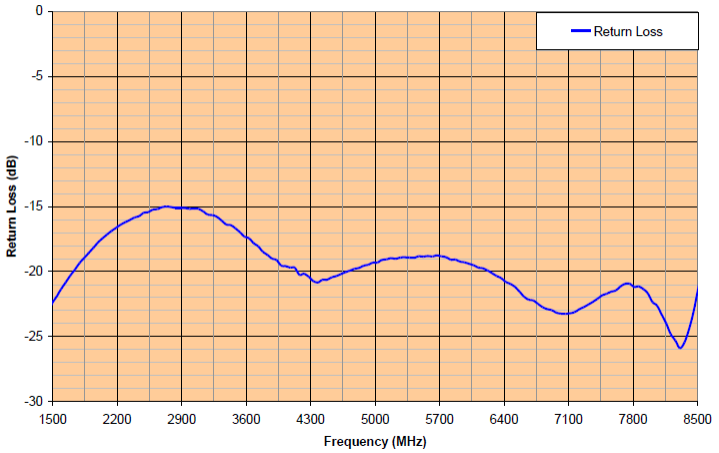
1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. MACOM does not recommend sustained operation near these survivability limits.
3. T_C is defined as the temperature of the bottom surface of the package.

Typical Performance Curves

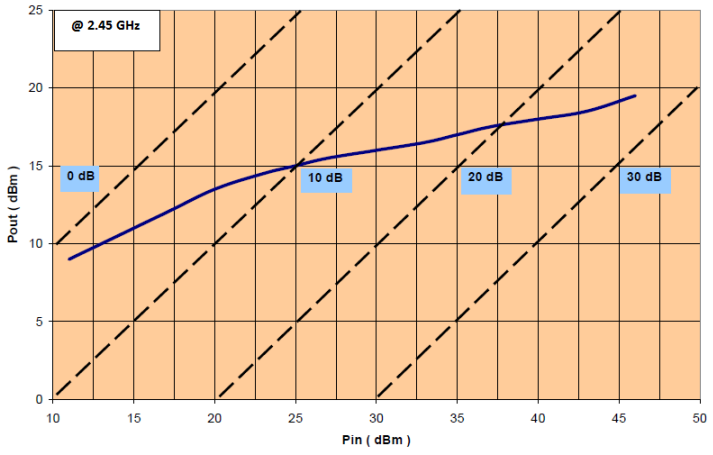
Insertion Loss vs. Frequency



Return Loss vs. Frequency



CW Output Power vs. CW Input Power



Handling Procedures

Please observe the following precautions to avoid damage:

Static and Moisture Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 0 (HBM) devices.

The moisture sensitivity level rating for this device is MSL 1.

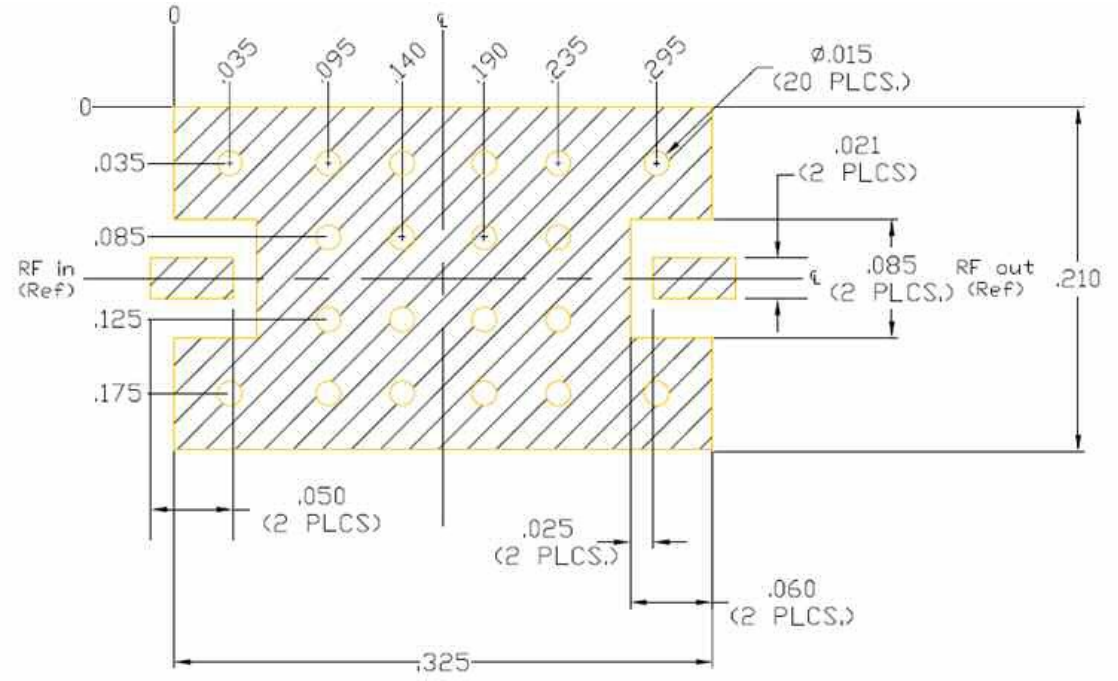
Environmental Capabilities

This limiter is capable of meeting the environmental requirements of MIL-STD-750 and MIL-STD-202.

Assembly Instructions

LM202802-M-C-300 may be placed onto circuit boards with pick and place manufacturing equipment from tube or tape-reel dispensing. The devices are attached to the circuit board using conventional solder re-flow or wave soldering procedures with RoHS type or Sn63/Pb37 type solders per Table 1 and Graph 1 Time-Temperature recommended profile.

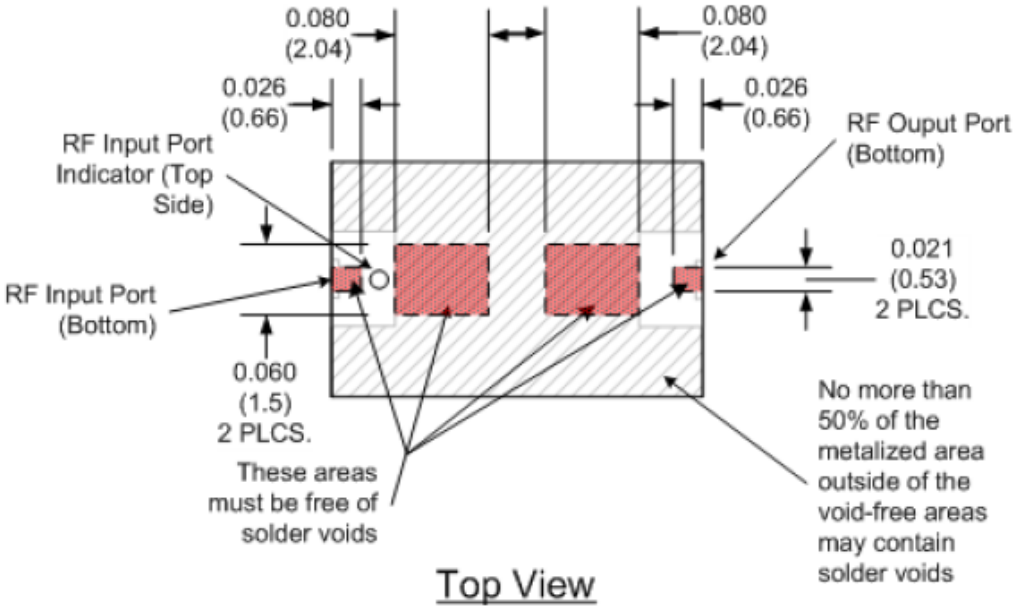
RF Circuit Solder Footprint, case style 300 (CS300)



Recommended RF circuit is Rogers R04350B, 10 mils thick.
The hatched metal area on circuit side of device is RF, DC and thermal grounded. Vias should be solid copper fill and gold plated for optimum heat transfer from backside of switch module through circuit vias to metal thermal ground.

Criteria for Proper Mounting on PCB

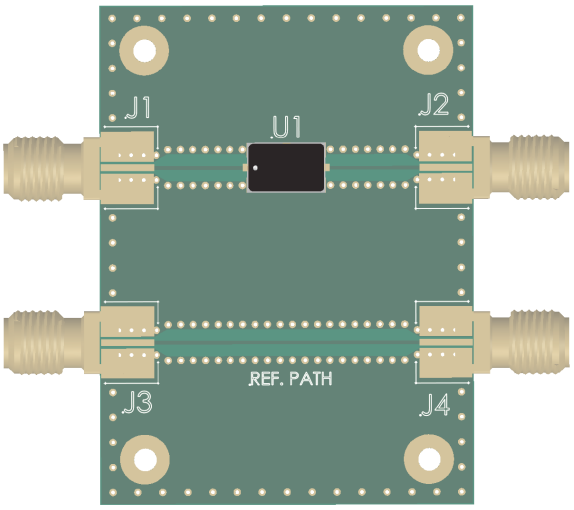
When a large signal is incident upon the input of the LM202802-M-C-300, the impedance of the coarse limiter diodes is forced to a low value by the charge which is injected into these diodes by the combination of the current from the internal detector stage and the large RF voltage initially present across these diodes. As the impedance of these diodes decreases, an increasingly large impedance mismatch with the impedance of the transmission line to which the limiter is connected is created. Ultimately, the impedance of the coarse limiter diodes is reduced to a few ohms or less. This mismatch creates a standing wave, with a current maximum and voltage minimum located at the position of the coarse limiter diodes. While the large majority of the input signal power is reflected back to its source due to the impedance mismatch, the significant RF current that flows at the current maximum causes Joule heating to occur in the coarse limiter diodes. In order to maintain the junction temperature of these diodes below their maximum rated value, there must be a path with minimal thermal resistance from the coarse diodes to the external system heat sink. Also, there must be a minimal electrical resistance and inductance between the underside of the limiter module package and the system ground in order to achieve maximum RF isolation between the input and the output of the limiter module.



Dimensions in inches (mm).

For these reasons, it is imperative that there are no voids in the electrical and thermal paths directly under the coarse limiter diodes. Care must be taken when mounting the LM202802-M-C-300 to avoid voids in the solder joint in the area along the lengthwise axis of the package, under and between the filled vias in the AlN substrate of the module which are shown in the diagram (above). It is also important to ensure no solder voids exist between the limiter module RF ports and the PCB to which the limiter module is attached. No greater than 50 % of the remaining metalized area on the bottom of the package may contain solder voids.

Limiter Evaluation Board Layout



The evaluation board for the LM202802-M-C-300 limiter is shown above. This evaluation board comprises two sections: the evaluation circuit for the limiter module; and, a reference transmission line.

The limiter module is mounted in position U1. Its RF input is connected to J1 and its output port is connected to J2, via two 50-Ω microstrip transmission lines.

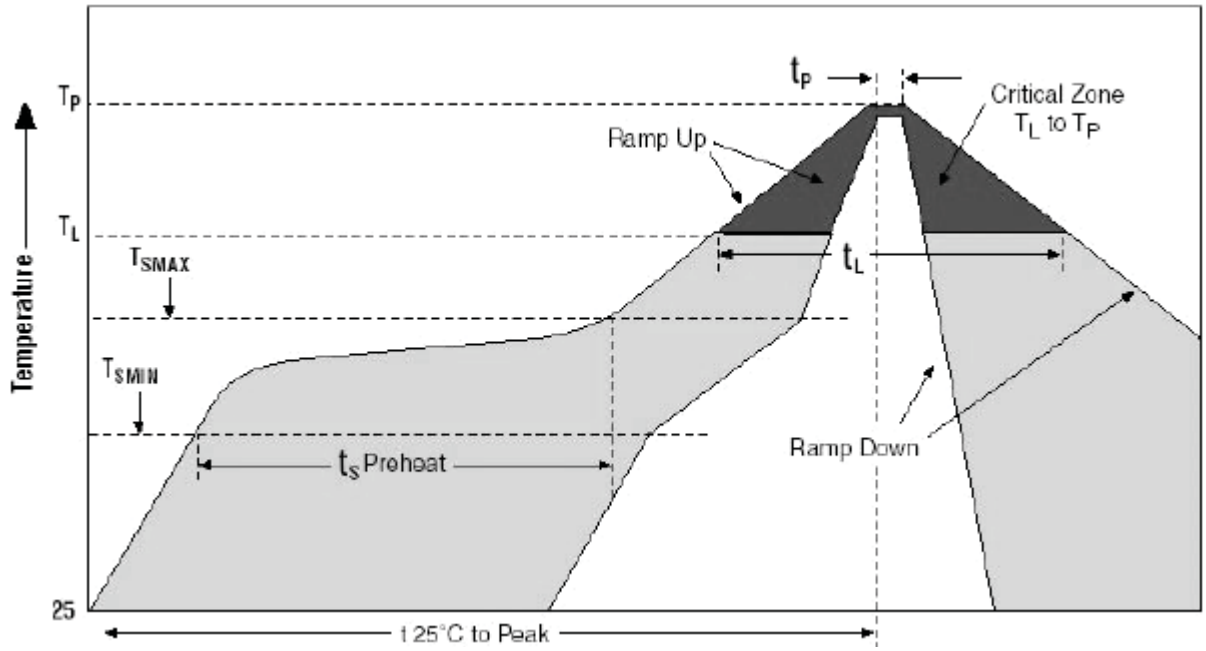
The reference path 50-Ω microstrip transmission line structure can be utilized to determine the insertion loss of the transmission line structures connected between J1 and the limiter module input, as well as between the limiter module output and J2, so that their respective insertion losses may be subtracted from the total insertion loss measured between J1 and J2. This enables the resolution of the insertion loss of the limiter module only.

The evaluation board is supplied mounted on a heat sink. The maximum RF input power specified in the Absolute Maximum Ratings table must not be exceeded.

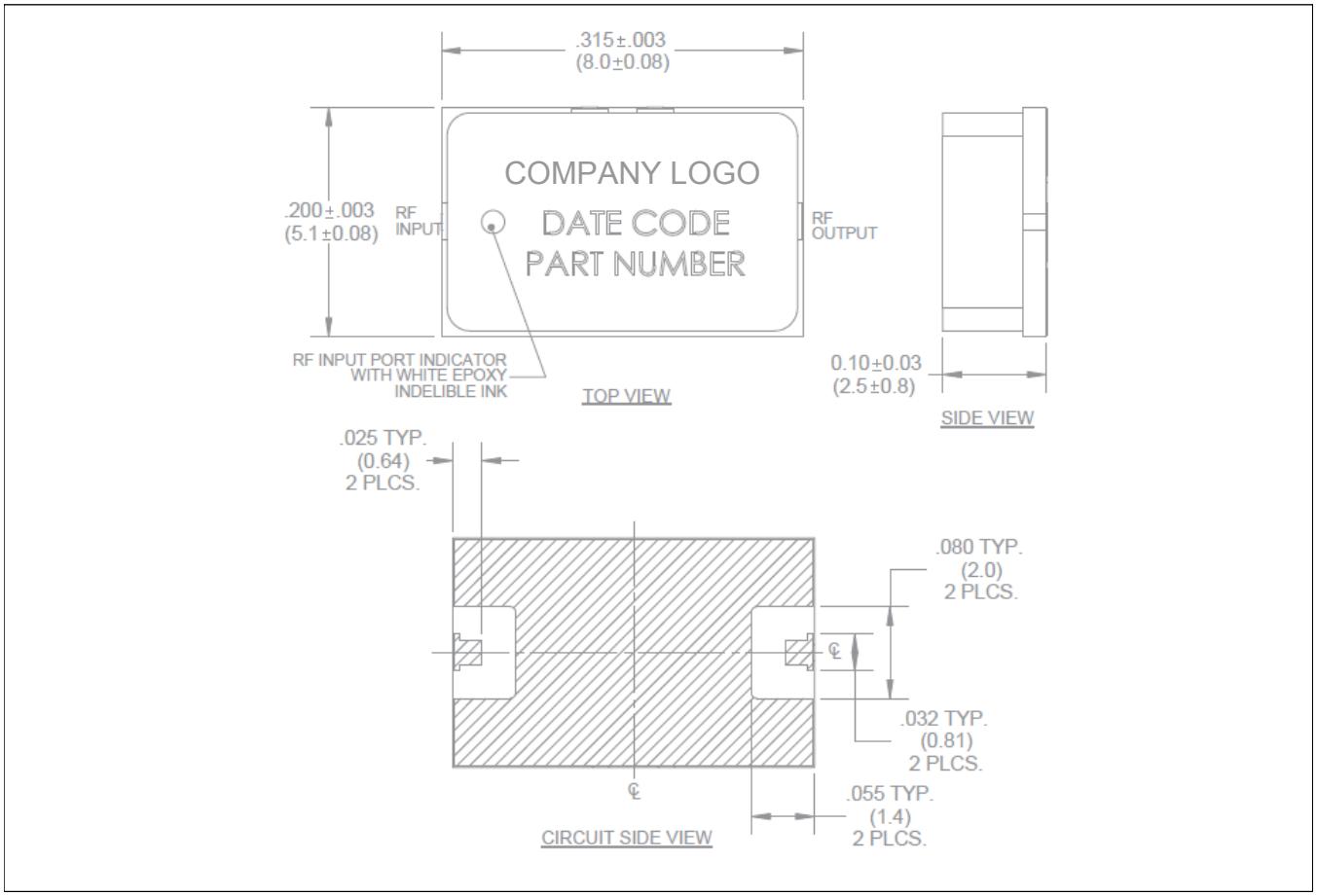
Table 1: Time-Temperature Profile for Sn 60 / Pb 40 or RoHS Type Solders

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (TL to TP)	3°C/second maximum	3°C/second maximum
Preheat - Temperature Minimum (TSMIN) - Temperature Maximum (TSMAX) - Time (Minimum to maximum) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
TSMAX to TL - Ramp-up Rate	—	3°C/second maximum
Time Maintained above: - Temperature (TL) - Time (tL)	183°C 60-150 seconds	217°C 60-150 seconds
Peak Temperature (TP)	225 +0 / -5°C	245 +0 / -5°C
Time within 5°C of actual Peak Temperature (TP)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second maximum	6°C/second maximum
Time 25°C to Peak Temperature	6 minutes maximum	8 minutes maximum

Graph1: Solder Re-Flow Time-Temperature Function



Outline Drawing, Case Style 300 (CS300)



The hatched metal area on circuit side of device is RF, DC and thermal grounded.
Dimensions are in inches (mm)
Substrate Material: 20 mil thick Alumina Nitride (ALN)
RF Cover: Black Ceramic
Top Side and Backside Metallization: 100 µ IN. typical plated over Ti-Pd.