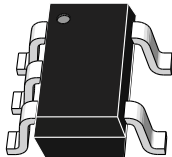


Tiny, low power, 16 V single operational amplifier for cost-optimized systems



SOT23-5

Features

- Low power consumption: 235 μA typ. at 5 V
- Supply voltage: 3 V to 16 V
- Gain bandwidth product: 900 kHz typ.
- Offset voltage: 3 mV maximum
- Low input bias current: 1 pA typ.
- High tolerance to ESD: 4 kV
- Wide temperature range: $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Rail-to-Rail input and output
- SOT23-5 package

Applications

- Industrial and automotive signal conditioning
- Active filtering
- Power savings in power-conscious applications
- Medical instrumentation
- High impedance sensors
- Easy interfacing with high impedance sensors

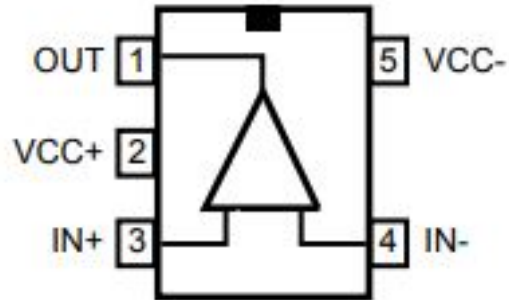
Description

The **LMC7101** operational amplifier benefits from STMicroelectronics® 16 V CMOS technology to offer state-of-the-art accuracy and performance in the smallest industrial packages. The **LMC7101** offers an outstanding speed/power consumption ratio, 900 kHz gain bandwidth product while consuming only 250 μA at 16 V. Such features make the **LMC7101** ideal for sensor interfaces and industrial signal conditioning. The wide temperature range and high ESD tolerance ease use in harsh automotive applications.

Product status link	
LMC7101	
Related products	
See TSX631	for reduced power consumption (45 μA , 200 kHz)
See TSX921	for higher gain bandwidth products (10 MHz)

1 Pinout information

Figure 1. Pin connections (top view)



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage ⁽¹⁾		18	V
V_{id}	Differential input voltage ⁽²⁾		$\pm V_{CC}$	
V_{in}	Input voltage ⁽³⁾		$(V_{CC-}) - 0.2$ to $(V_{CC+}) + 0.2$	
I_{in}	Input current ⁽⁴⁾		10	mA
T_{stg}	Storage temperature		-65 to 150	°C
T_j	Maximum junction temperature		150	
R_{thja}	Thermal resistance junction-to-ambient ⁽⁵⁾⁽⁶⁾	SOT23-5	250	°C/W
ESD	HBM: human body model ⁽⁷⁾		4	kV
	MM: machine model ⁽⁸⁾		200	V
	CDM: charged device model ⁽⁹⁾		1.5	kV
	Latch-up immunity		200	mA

1. All voltage values, except the differential voltage are with respect to the network ground terminal.
2. The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.
3. $V_{CC} - V_{in}$ must not exceed 18 V, V_{in} must not exceed 18 V
4. Input current must be limited by a resistor in series with the inputs.
5. R_{th} are typical values.
6. Short-circuits can cause excessive heating and destructive dissipation.
7. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
8. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
9. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3 to 16	V
V_{icm}	Common-mode input voltage range	$(V_{CC-}) - 0.1$ to $(V_{CC+}) + 0.1$	
T_{oper}	Operating free-air temperature range	-40 to 125	°C

3 Electrical characteristics

Table 3. Electrical characteristics at $V_{CC+} = 3.3\text{ V}$ with $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T_{amb} = 25\text{ }^{\circ}\text{C}$, and $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	$T = 25\text{ }^{\circ}\text{C}$			3	mV
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			5	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$		1		$\mu\text{V}/^{\circ}\text{C}$
I_{ib}	Input bias current, $V_{out} = V_{CC}/2$	$T = 25\text{ }^{\circ}\text{C}$		1	100 ⁽¹⁾	pA
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$		1	200 ⁽¹⁾	
I_{io}	Input offset current, $V_{out} = V_{CC}/2$	$T = 25\text{ }^{\circ}\text{C}$		1	100 ⁽¹⁾	
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$		1	200 ⁽¹⁾	
CMR1	Common mode rejection ratio, $\text{CMR} = 20 \log(\Delta V_{ic}/\Delta V_{io})$, $V_{ic} = -0.1\text{ V}$ to $V_{CC} - 1.5\text{ V}$, $V_{out} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$	$T = 25\text{ }^{\circ}\text{C}$	63	80		dB
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	59			
CMR2	Common mode rejection ratio, $\text{CMR} = 20 \log(\Delta V_{ic}/\Delta V_{io})$, $V_{ic} = -0.1\text{ V}$ to $V_{CC} + 0.1\text{ V}$, $V_{out} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$	$T = 25\text{ }^{\circ}\text{C}$	47	66		dB
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	45			
A_{vd}	Large signal voltage gain, $V_{out} = 0.5\text{ V}$ to $(V_{CC} - 0.5\text{ V})$, $R_L > 1\text{ M}\Omega$	$T = 25\text{ }^{\circ}\text{C}$	85			
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	83			
V_{OH}	High-level output voltage, $V_{OH} = V_{CC} - V_{out}$	$T = 25\text{ }^{\circ}\text{C}$			70	mV
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			100	
V_{OL}	Low-level output voltage	$T = 25\text{ }^{\circ}\text{C}$			70	
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			100	
I_{out}	I_{sink} , $V_{out} = V_{CC}$	$T = 25\text{ }^{\circ}\text{C}$	4.3	5.3		mA
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	2.5			
	I_{source} , $V_{out} = 0\text{ V}$	$T = 25\text{ }^{\circ}\text{C}$	3.3	4.3		
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	2.5			
I_{CC}	Supply current, per channel, $V_{out} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$	$T = 25\text{ }^{\circ}\text{C}$		220	300	μA
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			350	
AC performance						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	600	800		kHz
F_u	Unity gain frequency			690		
ϕ_m	Phase margin			55		Degrees
G_m	Gain margin			9		dB
SR	Slew rate	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $V_{out} = 0.5\text{ V}$ to $V_{CC} - 0.5\text{ V}$		1		$\text{V}/\mu\text{s}$
e_n	Equivalent input noise voltage density	$f = 1\text{ kHz}$		55		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		29		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{e_n}	Low-frequency peak-to-peak input noise	Bandwidth, $f = 0.1$ to 10 Hz		16		μV_{pp}
THD+N	Total harmonic distortion + noise	Follower configuration, $f_{in} = 1$ kHz, $R_L = 100$ k Ω , $V_{icm} = (V_{CC} - 1.5 \text{ V})/2$, BW = 22 kHz, $V_{out} = 1$ V $_{pp}$		0.004		%

1. Guaranteed by design

Table 4. Electrical characteristics at $V_{CC+} = 5$ V with $V_{CC-} = 0$ V, $V_{icm} = V_{CC}/2$, $T_{amb} = 25$ °C, and $R_L = 10$ k Ω connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	$T = 25$ °C			3	mV
		-40 °C < $T < 125$ °C			5	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < $T < 125$ °C		1		$\mu\text{V}/^\circ\text{C}$
ΔV_{io}	Long-term input offset voltage drift	$T = 25$ °C ⁽¹⁾		5		nV/ $\sqrt{\text{month}}$
I_{ib}	Input bias current, $V_{out} = V_{CC}/2$	$T = 25$ °C		1	100 ⁽²⁾	pA
		-40 °C < $T < 125$ °C		1	200 ⁽²⁾	
I_{io}	Input offset current, $V_{out} = V_{CC}/2$	$T = 25$ °C		1	100 ⁽²⁾	pA
		-40 °C < $T < 125$ °C		1	200 ⁽²⁾	
CMR1	Common mode rejection ratio, CMR = $20 \log (\Delta V_{ic}/\Delta V_{io})$, $V_{ic} = -0.1$ V to $V_{CC} - 1.5$ V, $V_{out} = V_{CC}/2$, $R_L > 1$ M Ω	$T = 25$ °C	66	84		dB
		-40 °C < $T < 125$ °C	63			
CMR2	Common mode rejection ratio, CMR = $20 \log (\Delta V_{ic}/\Delta V_{io})$, $V_{ic} = -0.1$ V to $V_{CC} + 0.1$ V, $V_{out} = V_{CC}/2$, $R_L > 1$ M Ω	$T = 25$ °C	50	69		dB
		-40 °C < $T < 125$ °C	47			
A_{vd}	Large signal voltage gain, $V_{out} = 0.5$ V to $(V_{CC} - 0.5)$ V, $R_L > 1$ M Ω	$T = 25$ °C	85			dB
		-40 °C < $T < 125$ °C	83			
V_{OH}	High-level output voltage, $V_{OH} = V_{CC} - V_{out}$	$R_L = 10$ k Ω , $T = 25$ °C			70	mV
		$R_L = 10$ k Ω , -40 °C < $T < 125$ °C			100	
V_{OL}	Low-level output voltage	$R_L = 10$ k Ω , $T = 25$ °C			70	mV
		$R_L = 10$ k Ω , -40 °C < $T < 125$ °C			100	
I_{out}	I_{sink}	$V_{out} = V_{CC}$, $T = 25$ °C	11	14		mA
		$V_{out} = V_{CC}$, -40 °C < $T < 125$ °C	8			
	I_{source}	$V_{out} = 0$ V, $T = 25$ °C	9	12		
		$V_{out} = 0$ V, -40 °C < $T < 125$ °C	7			
I_{CC}	Supply current, per channel, $V_{out} = V_{CC}/2$, $R_L > 1$ M Ω	$T = 25$ °C		235	350	μA
		-40 °C < $T < 125$ °C			400	
AC performance						
GBP	Gain bandwidth product	$R_L = 10$ k Ω , $C_L = 100$ pF	700	850		kHz
F_u	Unity gain frequency			730		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ϕ_m	Phase margin	$R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$		55		Degrees
G_m	Gain margin			9		dB
SR	Slew rate	$R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}, V_{out} = 0.5\text{ V to } V_{CC} - 0.5\text{ V}$		1.1		V/ μ s
e_n	Equivalent input noise voltage density	$f = 1\text{ kHz}$		55		nV/ $\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		29		
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth, $f = 0.1\text{ to } 10\text{ Hz}$		15		μ Vpp
THD+N	Total harmonic distortion + noise	Follower configuration, $f_{in} = 1\text{ kHz}, R_L = 100\text{ k}\Omega, V_{icm} = (V_{CC} - 1.5\text{ V})/2, BW = 22\text{ kHz}, V_{out} = 2\text{ V}_{pp}$		0.002		%

1. Typical value is based on the V_{io} drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration.
2. Guaranteed by design

Table 5. Electrical characteristics at $V_{CC+} = 16\text{ V}$ with $V_{CC-} = 0\text{ V}, V_{icm} = V_{CC}/2, T_{amb} = 25\text{ °C}$, and $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	$T = 25\text{ °C}$			3	mV
		$-40\text{ °C} < T < 125\text{ °C}$			5	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	$-40\text{ °C} < T < 125\text{ °C}$		1		μ V/ $^{\circ}$ C
ΔV_{io}	Long-term input offset voltage drift	$T = 25\text{ °C}$ (1)		1.6		nV/ $\sqrt{\text{month}}$
I_{ib}	Input bias current, $V_{out} = V_{CC}/2$	$T = 25\text{ °C}$		1	100 (2)	pA
		$-40\text{ °C} < T < 125\text{ °C}$		1	200 (2)	
I_{io}	Input offset current, $V_{out} = V_{CC}/2$	$T = 25\text{ °C}$		1	100 (2)	pA
		$-40\text{ °C} < T < 125\text{ °C}$		1	200 (2)	
CMR1	Common mode rejection ratio, $CMR = 20\text{ log}(\Delta V_{ic}/\Delta V_{io}), V_{ic} = -0.1\text{ V to } V_{CC} - 1.5\text{ V}, V_{out} = V_{CC}/2, R_L > 1\text{ M}\Omega$	$T = 25\text{ °C}$	76	95		dB
		$-40\text{ °C} < T < 125\text{ °C}$	72			
CMR2	Common mode rejection ratio, $CMR = 20\text{ log}(\Delta V_{ic}/\Delta V_{io}), V_{ic} = -0.1\text{ V to } V_{CC} + 0.1\text{ V}, V_{out} = V_{CC}/2, R_L > 1\text{ M}\Omega$	$T = 25\text{ °C}$	60	78		dB
		$-40\text{ °C} < T < 125\text{ °C}$	56			
SVR	Common mode rejection ratio, $20\text{ log}(\Delta V_{CC}/\Delta V_{io}), V_{CC} = 3\text{ V to } 16\text{ V}, V_{out} = V_{icm} = V_{CC}/2$	$T = 25\text{ °C}$	76	90		dB
		$-40\text{ °C} < T < 125\text{ °C}$	72			
A_{vd}	Large signal voltage gain, $V_{out} = 0.5\text{ V to } (V_{CC} - 0.5\text{ V}), R_L > 1\text{ M}\Omega$	$T = 25\text{ °C}$	85			dB
		$-40\text{ °C} < T < 125\text{ °C}$	83			
V_{OH}	High-level output voltage, $V_{OH} = V_{CC} - V_{out}$	$R_L = 10\text{ k}\Omega, T = 25\text{ °C}$			70	mV
		$R_L = 10\text{ k}\Omega, -40\text{ °C} < T < 125\text{ °C}$			100	
V_{OL}	Low-level output voltage	$R_L = 10\text{ k}\Omega, T = 25\text{ °C}$			70	mV

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low-level output voltage	$R_L = 10\text{ k}\Omega$, $-40\text{ }^\circ\text{C} < T < 125\text{ }^\circ\text{C}$			100	mV
I_{out}	I_{sink}	$V_{out} = V_{CC}$, $T = 25\text{ }^\circ\text{C}$	40	92		mA
		$V_{out} = V_{CC}$, $-40\text{ }^\circ\text{C} < T < 125\text{ }^\circ\text{C}$	35			
	I_{source}	$V_{out} = 0\text{ V}$, $T = 25\text{ }^\circ\text{C}$	30	90		
		$V_{out} = 0\text{ V}$, $-40\text{ }^\circ\text{C} < T < 125\text{ }^\circ\text{C}$	25			
I_{CC}	Supply current, per channel, $V_{out} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$	$T = 25\text{ }^\circ\text{C}$		250	360	μA
		$-40\text{ }^\circ\text{C} < T < 125\text{ }^\circ\text{C}$			400	
AC performance						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	750	900		kHz
F_u	Unity gain frequency			750		
ϕ_m	Phase margin			55		Degrees
G_m	Gain margin			9		dB
SR	Slew rate	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $V_{out} = 0.5\text{ V}$ to $V_{CC} - 0.5\text{ V}$		1.1		V/ μs
e_n	Equivalent input noise voltage density	$f = 1\text{ kHz}$		48		nV/ $\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		27		
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth, $f = 0.1$ to 10 Hz		15		μV_{pp}
THD+N	Total harmonic distortion + noise	Follower configuration, $f_{in} = 1\text{ kHz}$, $R_L = 100\text{ k}\Omega$, $V_{icm} = (V_{CC} - 1.5\text{ V})/2$, $BW = 22\text{ kHz}$, $V_{out} = 5\text{ V}_{pp}$		0.0005		%

1. Typical value is based on the V_{io} drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration.
2. Guaranteed by design

4 Electrical characteristic curves

Figure 2. Supply current vs. supply voltage at $V_{icm} = V_{CC}/2$

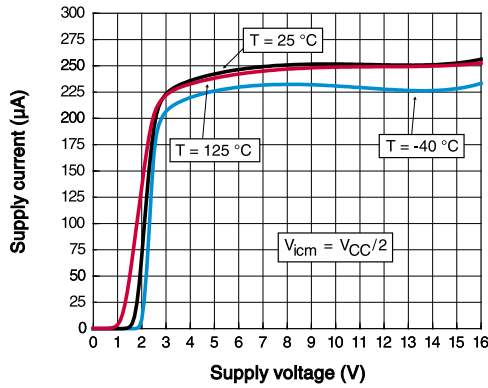


Figure 3. Output current vs. output voltage at $V_{CC} = 3.3$ V

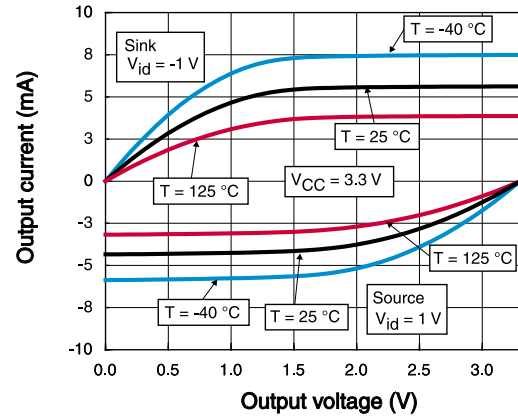


Figure 4. Output current vs. output voltage at $V_{CC} = 5$ V

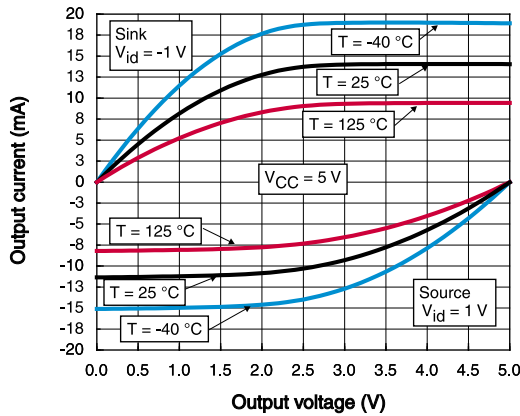


Figure 5. Output current vs. output voltage at $V_{CC} = 16$ V

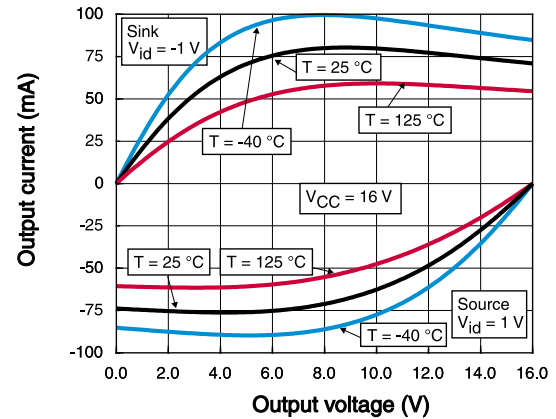


Figure 6. Bode diagram at $V_{CC} = 3.3$ V

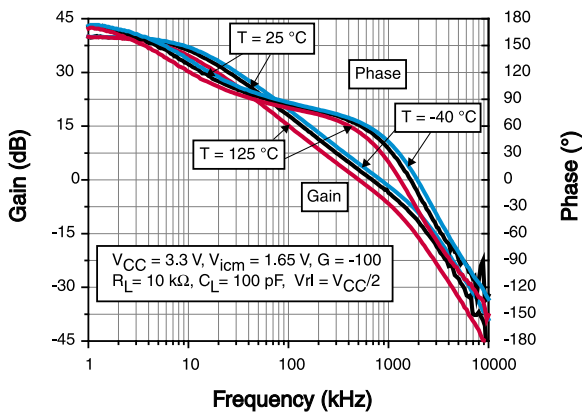


Figure 7. Bode diagram at $V_{CC} = 5$ V

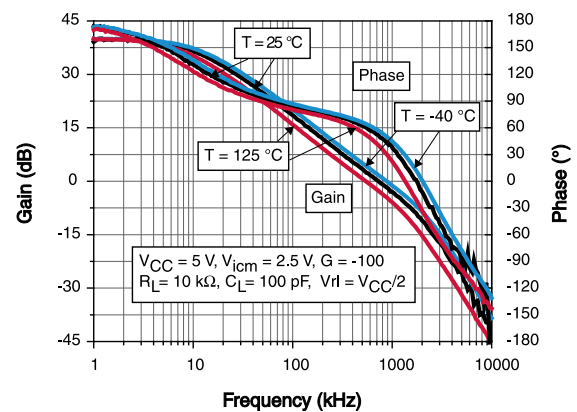


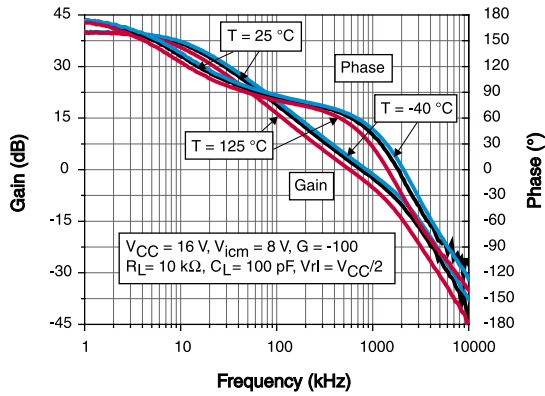
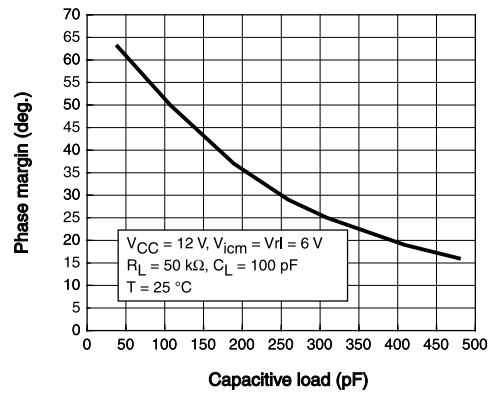
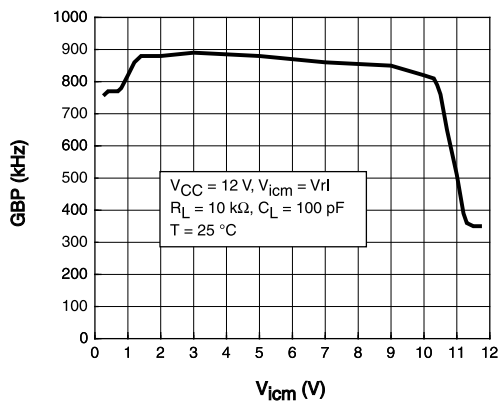
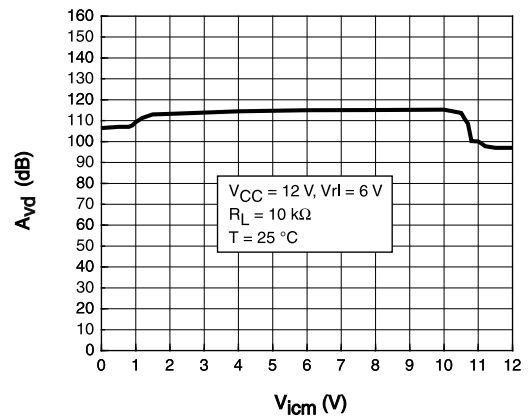
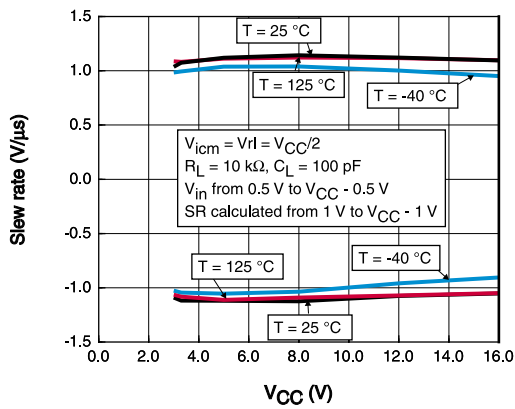
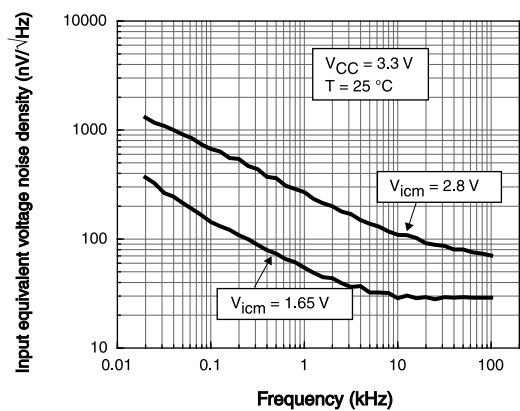
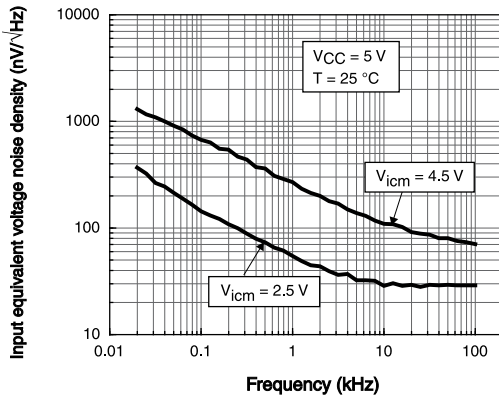
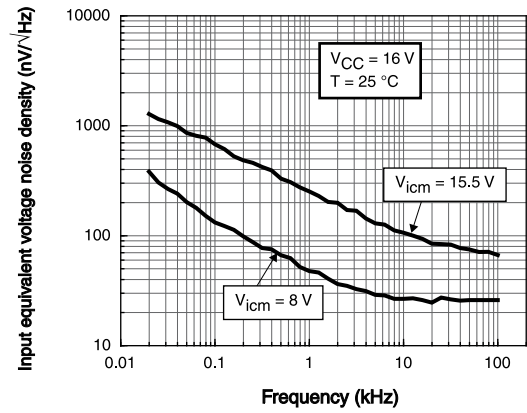
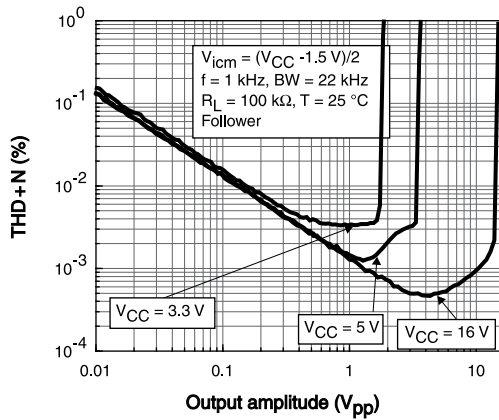
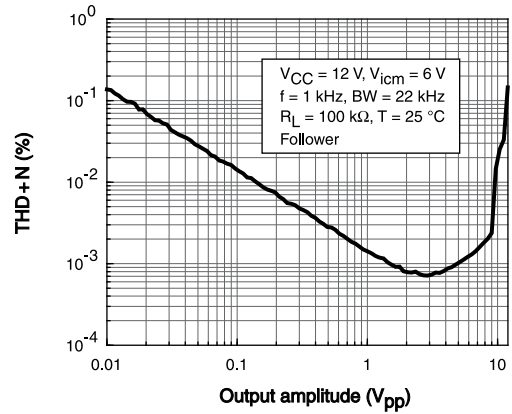
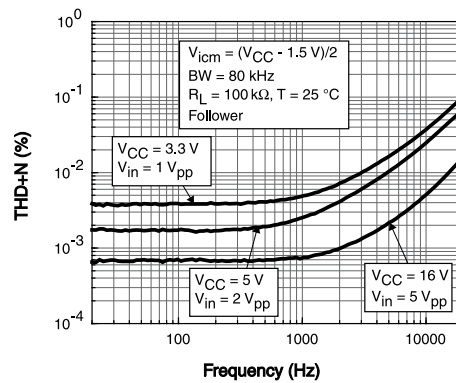
Figure 8. Bode diagram at $V_{CC} = 16\text{ V}$

Figure 9. Phase margin vs. capacitive load at $V_{CC} = 12\text{ V}$

Figure 10. GBP vs. input common-mode voltage at $V_{CC} = 12\text{ V}$

Figure 11. A_{vd} vs. input common-mode voltage at $V_{CC} = 12\text{ V}$

Figure 12. Slew rate vs. supply voltage

Figure 13. Noise vs. frequency at $V_{CC} = 3.3\text{ V}$


Figure 14. Noise vs. frequency at $V_{CC} = 5\text{ V}$

Figure 15. Noise vs. frequency at $V_{CC} = 16\text{ V}$

Figure 16. Distortion and noise vs. output voltage amplitude

Figure 17. Distortion and noise vs. amplitude at $V_{icsm} = V_{CC}/2$ and $V_{CC} = 12\text{ V}$

Figure 18. Distortion and noise vs. frequency


5 Application information

5.1 Operating voltages

The LMC7101 amplifier can operate from 3 V to 16 V. Its parameters are fully specified at 3.3 V, 5 V, and 16 V power supplies. However, the parameters are very stable in the full V_{CC} range. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 to 125 °C.

5.2 Rail-to-rail input

The LMC7101 device is built with two complementary PMOS and NMOS input differential pairs. The devices have a rail-to-rail input, and the input common mode range is extended from $(V_{CC-}) - 0.1$ V to $(V_{CC+}) + 0.1$ V.

However, the performance of this device is clearly optimized for the PMOS differential pairs (which means from $(V_{CC-}) - 0.1$ V to $(V_{CC+}) - 1.5$ V).

Beyond $(V_{CC+}) - 1.5$ V, the operational amplifiers are still functional but with degraded performance, as can be observed in the electrical characteristics section of this datasheet (mainly V_{io} and GBP). These performances are suitable for a number of applications that need to be rail-to-rail.

The devices are designed to prevent phase reversal.

5.3 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using [Equation 2](#).

Equation 2

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

Where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration constant in 1/V, constant technology parameter ($\beta = 1$)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in [Equation 3](#).

Equation 3

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S} \right)}$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate

k is the Boltzmann constant (8.6173×10^{-5} eV.K⁻¹)

T_U is the temperature of the die when V_U is used (K)

T_S is the temperature of the die under temperature stress (K)

The final acceleration factor, A_F , is the multiplication of the voltage acceleration factor and the temperature acceleration factor ([Equation 4](#)).

Equation 4

$$A_F = A_{FT} \times A_{FV}$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The A_F value can then be used in Equation 5 to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

Equation 5

$$\text{Months} = A_F \times 1000 \text{ h} \times 12 \text{ months} / (24 \text{ h} \times 365.25 \text{ days})$$

To evaluate the op amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The V_{io} drift (in μV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see Equation 6).

Equation 6

$$V_{CC} = \max V_{op} \text{ with } V_{icm} = V_{CC} / 2$$

The long term drift parameter (ΔV_{io}), estimating the reliability performance of the product, is obtained using the ratio of the V_{io} (input offset voltage value) drift over the square root of the calculated number of months (Equation 7).

Equation 7

$$\Delta V_{io} = \frac{V_{io} \text{ drift}}{\sqrt{(\text{months})}}$$

Where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

5.4 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

5.5 Macromodel

Accurate macromodels of the LMC7101 device are available on the STMicroelectronics' website at: www.st.com. These models are a trade-off between accuracy and complexity (that is, time simulation) of the LMC7101 operational amplifier. They emulate the nominal performance of a typical device within the specified operating conditions mentioned in the datasheet. They also help to validate a design approach and to select the right operational amplifier, *but they do not replace on-board measurements*.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SOT23-5 package information

Figure 19. SOT23-5 package outline

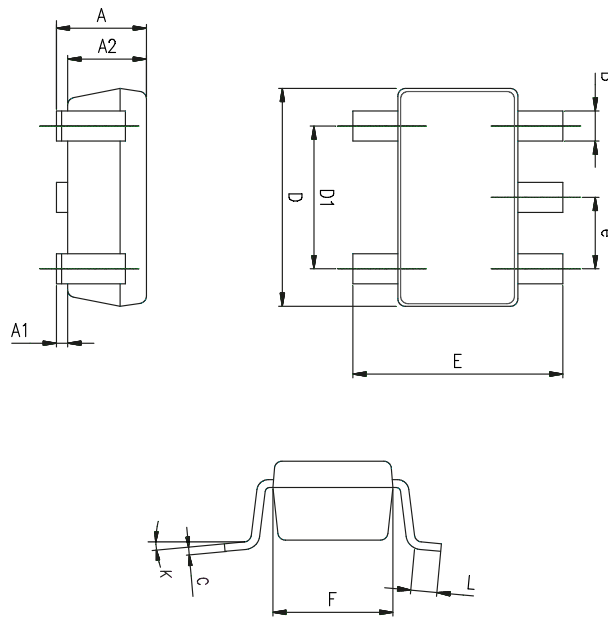


Table 6. SOT23-5 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0 degrees		10 degrees	0 degrees		10 degrees

7 Ordering information

Table 7. Order codes

Order code	Temperature range	Package	Packing	Marking
LMC7101ILT	-40 to 125 °C	SOT23-5	Tape and reel	K23

Revision history

Table 8. Document revision history

Date	Revision	Changes
09-Nov-2020	1	Initial release.

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