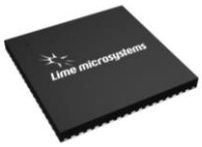
LMS7002M

FPRF MIMO Transceiver IC
With Integrated Microcontroller



SUMMARY FEATURES

- **Field Programmable Radio Frequency (FPRF) chip**
- **Dual transceiver ideal for MIMO**
- **User programmable on the fly**
- **Continuous coverage of the 100 kHz - 3.8 GHz RF frequency range**
- **Digital interface to baseband with on chip integrated 12 bit D/A and A/D converters**
- **Programmable RF modulation bandwidth up to 160 MHz using analog interface**
- **Programmable RF modulation bandwidth up to 96 MHz using digital interface**
- **Supports both TDD and full duplex FDD**
- **LimeLight™ digital IQ interface – JEDEC JESD207 TDD and FDD compliant**
- **Transceiver Signal Processor block employs advanced techniques for enhanced performance**
- **Single chip supports 2x2 MIMO. Multiple chips can be used to implement higher order MIMO**
- **On-chip RF calibration circuitry**
- **Fully differential baseband signals, analog IQ**
- **Few external components**
- **Low voltage operation, 1.25, 1.4 and 1.8V. Integrated LDOs to run on a single 1.8V supply voltage**
- **On chip integrated microcontroller for simplified calibration, tuning and control**
- **Integrated clock PLL for flexible clock generation and distribution**
- **User definable analog and digital filters for customised filtering**
- **RF and base band Received Signal Strength Indicator (RSSI)**
- **On chip integrated temperature sensor**
- **261 pin aQFN 11.5x11.5 mm package**
- **Power down option**
- **Serial port interface**
- **Low power consumption, typical 880mW in full 2x2 MIMO mode (550mW in SISO mode) using external LDOs**
- **Multiple bypass modes for greater flexibility**

APPLICATIONS

- **Broad band wireless communications**
- **GSM, CDMA2000, TD-SCDMA, WCDMA/HSPA, LTE**
- **IEEE® xxx.xxx radios**
- **WiFi operating in the Whitespace frequencies**
- **Software Defined Radio (SDR)**
- **Cognitive Radio**
- **Unmanned Aerial Vehicle (UAV)**
- **Other Whitespace applications**

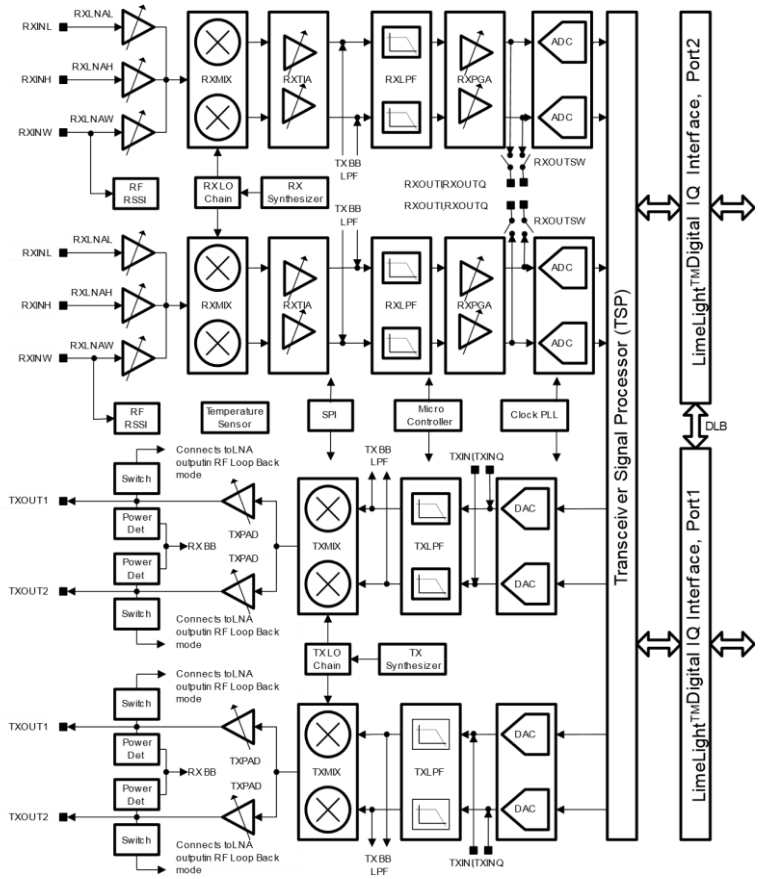


Figure 1: Functional block diagram

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GENERAL DESCRIPTION

LMS7002M is a fully integrated, multi-band, multi-standard RF transceiver that is highly programmable. It combines Low Noise Amplifiers (RXLNA), TX Power Amplifier Drivers (TXPAD) receiver/transmitter (RX/TX) mixers, RX/TX filters, synthesizers, RX gain control, TX power control, the analog-to-digital and digital-to-analog convertors (ADC/DACs) and has been designed to require very few external components.

The top level architecture of LMS7002M transceiver is shown in *Figure 1*. The chip contains two transmit and two receive chains for achieving a Multiple In Multiple Out (MIMO) platform. Both transmitters share one PLL and both receivers share another. Transmit and receive chains are all implemented as zero Intermediate Frequency (zero IF or ZIF) architectures providing up to 160MHz RF modulation bandwidths (equivalent to 80MHz baseband IQ bandwidth). For the purpose of simplifying this document, the explanation for the functionality and performance of the chip is based on one transmit and one receive circuitry, given that the other two work in exact the same manner.

On the transmit side, In-phase and Quadrature IQ DAC data samples, from the base band processor, are provided to the LMS7002M via the LimeLight™ digital IQ interface. LimeLight™ implements the JESD207 standard IQ interface protocol as well as de facto IQ multiplexed standard. JESD207 is Double Data Rate (DDR) by definition. In IQ multiplexed mode LimeLight™ also supports Single Data Rate (SDR). The IQ samples are then pre-processed by the digital Transceiver Signal Processor (TSP) for minimum analog / RF distortion and applied to the on chip transmit DACs. The DACs generate analog IQ signals which are provided for further processing to the analog/RF section. Transmit low pass filters (TXLPF) remove the images generated by zero hold effect of the DACs, as well as the DAC out-of-band noise. The analog IQ signals are then mixed with the transmit PLL (TXPLL) output to produce a modulated RF signal. This RF signal is then amplified by one of two separate / selectable power amplifier drivers and two open-drain differential outputs are provided as RF output for each MIMO path.

The LMS7002M provides an RF loop back option which enables the TX RF signal to be fed back into the baseband for calibration and test purposes. The RF loop back signal is amplified by the loopback amplifier in order to increase the dynamic range of the loop.

There are two additional loop back options implemented, one is an analog base band (BB) loop back and another is a digital loop back (DLB) as shown in *Figure* 1. The analog loop back is intended for testing while the DLB can be used to verify the LMS7002M connectivity to base band, FPGA, DSP or any other digital circuitry.

On the receive side, three separate inputs are provided each with a dedicated LNA optimised for narrow or wide band operation. Each port RF signal is first amplified by a programmable low noise amplifier (RXLNA). The RF signal is then mixed with the receive PLL (RXPLL) output to directly down convert to baseband. AGC steps can be implemented by a BB trans-impedance amplifier (RXTIA) prior to the programmable bandwidth low pass channel select / anti alias filters (RXLPF). The received IQ signal is further amplified by a programmable gain amplifier RXPGA. DC offset is applied at the input of RXTIA to prevent saturation and to preserve the receive ADC's dynamic range. The resulting analog receive IQ signals are converted into the digital domain with on-chip receive ADCs. Following the ADCs, the signal conditioning is performed by the digital Transceiver Signal Processor (TSP) and the resulting signals are then provided to the BB via the LimeLight™ digital IQ interface.

The analog receive signals can also be provided off chip at RXOUTI and RXOUTQ pins by closing the RXOUT switch. In this case it is possible to power down the on chip ADCs/TSP and use external parts which can be very useful for more resource demanding applications or where higher signal resolution is required. A similar option is also available on the TX side where the analog signal can be processed by external components. The on chip DACs/TSP can be powered down and analog inputs can be provided at TXINI and TXINQ pins.

There is on chip integrated temperature sensor which base band modem can read via the SPI and trigger re-calibration of the chip if significant chip/ambient temperature change is observed.

Parameter	Min.	Typ.	Max.	Unit	Condition/Comment
Operating Temperature Range	-40	25	85	°C	
Storage Temperature Range	-65	25	125	°C	
Operating Frequency Range	30 0.1		3800 3800	MHz	 Extended by TSP NCOs
RF Modulation Bandwidth			48 96 160	MHz	Through digital interface (MIMO) Through digital interface (SISO) Through analog interface
Frequency Resolution			24.8	Hz	Using 52 MHz PLL reference clock
Analog Supply Voltage, High (VDDAH)	1.71	1.8	1.89	V	Used for TXPAD
Analog Supply Voltage, Medium (VDDAM)	1.33	1.4	1.47	V	Generated using integrated low-dropout regulators (LDOs)
Analog Supply Voltage, Low (VDDAL)	1.2	1.25	1.3	V	Generated using integrated LDOs
Digital Core Supply Voltage	1.1	1.2	1.3	V	Generated using integrated LDOs
Digital Peripheral (IO) Supply Voltage	1.7	2.5	3.6	V	
TX Supply Current		350		mA	At -7 dBm output power, 2x2 MIMO, including the DACs and TSP
RX Supply Current		420		mA	For 2x2 MIMO, including the ADCs and TSP
Maximum RF Output Power		0		dBm	Continuous Wave
PLL Reference Clock	10		52	MHz	
Reference and Other Spurs Level		-100		dBm	Measured at TX RF output or RX RF input
IQ Imbalance Image		-70		dBc	After calibration
Interpolation/Decimation digital filters stop band suppression			108	dB	

Table 1: General specifications

Parameter	Min.	Typ.	Max.	Unit	Condition/Comment
RF channel frequency range	30 0.1		3800 3800	MHz	Extended by TSP NCOs
Transmit Analog Input Impedance		400		Ohms	Differential, programmable
Transmit Load Impedance at the Output Pins		40		Ohms	Differential, for maximum OIP3
Transmit Differential I and Q Input Current		625		uA	Differential Common mode
Transmit Gain Control Range		70		dB	TXTSP and TXPAD combined
Transmit Gain Control Step		1		dB	
TX Local Oscillator (LO) Leakage		-60		dBc	Calibrated
RXLNAL Frequency Range	0.1		2000	MHz	Narrow band tunable, set by external matching circuit
RXLNAH Frequency Range	30		3800	MHz	Narrow band tunable, set by external matching circuit
RXLNAW Frequency Range	30		3800	MHz	Broad band tunable, set by external matching circuit
Noise Figure		2.0 2.5 3.5		dB	at 0.95GHz at 2GHz at 3.8GHz
2nd Order Input Intercept Point		50		dBm	Total receiver gain ~50 dB or more, Noise Figure <3.5 dB in all bands. Two tone signals out of band.
3rd Order Input Intercept Point		4		dBm	Total receiver gain ~50 dB or more, Noise Figure <3.5 dB in all bands. Two tone signals out of band.
Receive Gain Control Range		89		dB	RXLNA, RXTIA, RXPGA and RXTSP combined
Receive Gain Control Step	0.5	1	1.5	dB	

Table 2: General RF specifications

Two transmitter outputs (TXOUT1, TXOUT2) and three receiver inputs (RXINL, RXINH, RXINW) are provided to facilitate multi-band multi-standard operation.

The functionality of the LMS7002M is fully controlled by a set of internal registers which can be accessed through a serial port and rapidly reprogrammed on the fly for advanced system architectures.

In order to enable full duplex operation, LMS7002M contains two separate synthesisers (TXPLL, RXPLL) both usually driven from the same reference clock source PLLCLK. Optionally, single PLL (TXPLL) can drive both RX and TX mixers for TDD/half duplex applications.

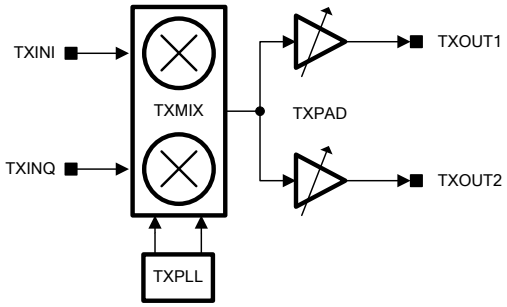


Figure 2: TX analog/RF gain control architecture

TX GAIN CONTROL

The LMS7002M transmitter has two programmable gain stages, where the TSP provides digital gain control and the TXPAD gives programmable gain of the RF signal.

Parameter	Min.	Typ.	Max.	Unit	Condition/Comment
Digital TSP Gain Control Range		15		dB	In steps of 1 LSB digital gain control
TXPAD Gain Control Range		55		dB	
TXPAD Gain Step Size		1		dB	for the higher 10 steps
TXPAD Gain Step Size		2		dB	for the lower 20 steps

Table 3: TX gain control

RX GAIN CONTROL

The LMS7002M receiver has three gain control elements, RXLNA, RXTIA, and RXPGA. If required, additional gain control can be implemented by RXTSP in digital domain.

RXLNA gain control consists of 30 dB with 1 dB steps at high gain settings and 3 dB steps at low gain settings for AGC when large adjacent channel blockers are present and a reduction in system noise figure (NF) is acceptable.

RXTIA offers 12 dB of control range. RXTIA is intended for AGC steps needed to reduce system gain prior to the channel filters when large in band blockers are present. This gain can be under the control of the baseband or fixed on calibration.

RXPGA provides gain control for the AGC if a constant RX signal level at the ADC input is required. It has a 32 dB gain range control in 1 dB steps.

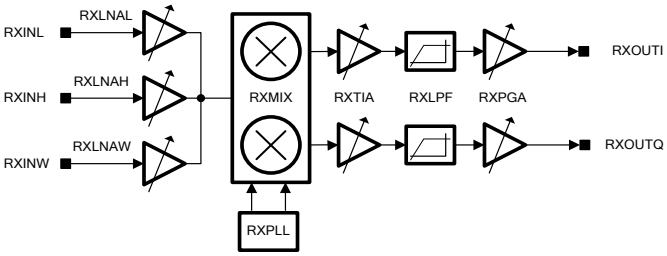


Figure 3: RX gain control architecture

Parameter	Min.	Typ.	Max.	Unit	Condition/Comment
Digital TSP Gain Control Range		15		dB	In steps of 1 LSB digital gain control
RXLNA Gain Control Range		30		dB	1 and 3 dB steps
RXTIA Gain Control Range		12		dB	
RXPGA Gain Control Range		32		dB	
RXPGA Gain Step Size		1		dB	

Table 4: RX gain control

SYNTHESISERS

The LMS7002M has two low phase noise synthesizers to enable full duplex operation and both are capable of output frequencies up to 3.8 GHz. Each synthesizer uses fractional-N PLL architecture as shown in *Figure 4*. The same reference frequency can be used for both synthesizers and is flexible between 10 to 52 MHz clock frequencies. The synthesizers produce complex outputs with suitable levels to drive IQ mixers in both the TX and the RX paths. The transmit PLL could also be routed via switches to the receive PLL so as to offer phase coherent operation in TDD mode.

The LMS7002M can accept clipped sine as well as CMOS level signals for the PLL reference clock. Both DC and AC coupling are supported as shown in *Figure 5*. Internal buffer self-biasing must be enabled for AC coupling mode. The PLL reference clock input can also be low voltage CMOS (<1.2V) which is implemented by lowering the clock buffer supply or bypassing the input buffer stage (CLKBUF).

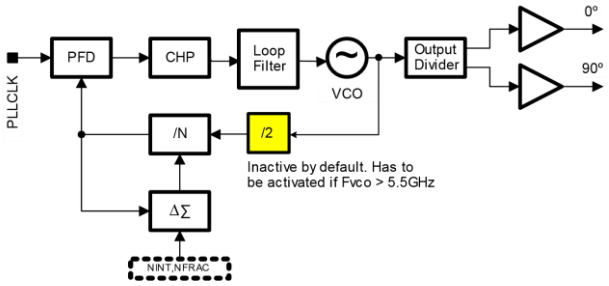


Figure 4: PLL architecture

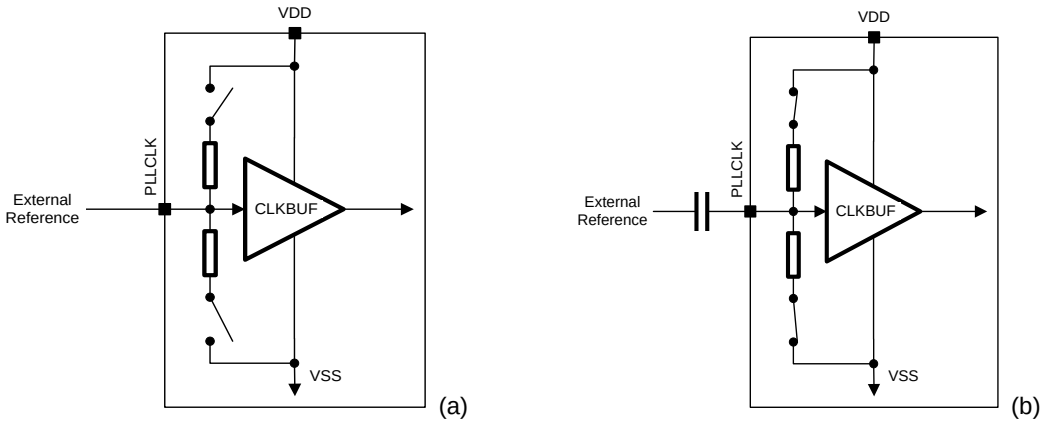


Figure 5: PLL reference clock input buffer, (a) DC coupled (b) AC coupled

Parameter	Min.	Typ.	Max.	Unit	Condition/Comment
Output Frequency Range	30		3800	MHz	
Reference Amplitude	0.2	0.8	2.5	Vpp	At PVDD>2.5V
Reference Frequency	10		52	MHz	For continuous LO frequency range
Frequency Resolution			24.8	Hz	Using 52 MHz PLL reference clock
881.5 MHz Phase Noise				dBc/Hz	E-UTRA Band 5
1 kHz offset	-101				
5 kHz offset	-105				
10 kHz offset	-106				
100 kHz offset	-109				
1 MHz offset	-132				
30 MHz offset	-158				
Integrated Phase Noise	0.16			deg	Integrated from 1kHz to 10MHz
2.14 GHz Phase Noise				dBc/Hz	E-UTRA Band 1
1 kHz offset	-92				
5 kHz offset	-98				
10 kHz offset	-99				
100 kHz offset	-104				
1 MHz offset	-132				
30 MHz offset	-158				
Integrated Phase Noise	0.27			deg	Integrated from 1kHz to 10MHz
2.655 GHz Phase Noise				dBc/Hz	E-UTRA Band 7
1 kHz offset	-93				
5 kHz offset	-96				
10 kHz offset	-98				
100 kHz offset	-100				
1 MHz offset	-129				
30 MHz offset	-158				
Integrated Phase Noise	0.39			deg	Integrated from 1kHz to 10MHz
3.55 GHz Phase Noise				dBc/Hz	E-UTRA Band 22
1 kHz offset	-91				
5 kHz offset	-93				
10 kHz offset	-95				
100 kHz offset	-98				
1 MHz offset	-121				
30 MHz offset	-152				
Integrated Phase Noise	0.57			deg	Integrated from 1kHz to 10MHz
PLL Settling Time		50	150	µs	Loop BW=70 kHz, from cold.

Table 5: Synthesizer specifications

RF PORTS

LMS7002M has two transmitter outputs and three receiver inputs for each of the dual transceivers.

The optimum transmitter output load is 40Ω differential at the output pads. The final stage amplifiers are open drain and require +1.8V voltage supply.

The receiver inputs are common-source with different inductive degeneration, optimized for different frequency bands. They need to be externally matched for optimized narrowband performance or broadband utilizing a wideband transformer.

TX and RX LOW PASS FILTERS

LMS7002M integrates selective low pass filters in both the TX and RX paths. Filters have programmable pass band in order to provide more flexibility on the DAC/ADC clock frequency and also to provide adjacent channel rejection in the receive chain. The complete filtering function is a combination of analog filtering and digital TSP filtering. RX analog filters are tunable from 0.7 MHz to 80 MHz. The digital filters provide a lower pass band of 0.7 MHz. Using such mixed mode filtering (digital and analog) provides 60 dB anti alias performance and 40 dB adjacent channel rejection as the worst case scenario. The TX filtering chain pass band is tunable from 2.5 MHz to 80 MHz. When combined with TX digital filters the chain offers enhanced performance in a similar way as the RX analog/digital filtering chain.

As shown in *Figure 6*, transmitter baseband has three independently controlled low pass filter stages:

1. 4th order ladder filter (TXLPFLAD),
2. 1st order real pole filter (TXLPFS5),
3. 2nd order high band filter (TXLPFH).

Low band filter (TXLPFL) path pass band is tunable from 2.5 MHz to 20 MHz and is comprised of two filter stages: 4th order low pass ladder filter (TXLPFLAD) and 1st order low pass real pole filter (TXLPFS5). The real pole stage filters the BB noise at the duplex frequency to meet the far-end noise specifications in some FDD systems. Real pole stage is by passable if not required. High band filter (TXLPFH) pass band is tunable from 20 MHz up to 80 MHz and is comprised of a single 2nd order low pass stage. Only one (TXLPFL or TXLPH) path can be active at the same time.

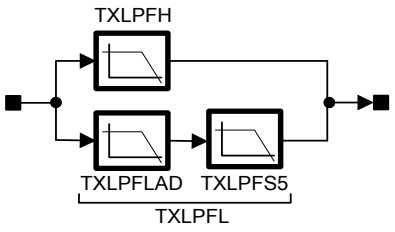


Figure 6: TX analog filtering chain

As shown in *Figure 7*, receiver baseband has three independently controlled low pass filter stages:

1. 1st order single pole filter (RXTIA),
2. 2nd order low band filter (RXLPFL),
3. 2nd order high band filter (RXLPFH).

The initial filtering is done by the trans-impedance amplifier (RXTIA) which acts as a single pole low pass filter. The RXTIA output is routed to one of two filter stages. Low band filter pass band is tunable from 0.7 MHz up to 18 MHz. High band filter pass band is tunable from 18 MHz up to 80 MHz. Both low band and high band stages are 2nd order low pass filters. Paired with the RXTIA, these stages produce a 3rd order low pass filter response. Only one (RXLPFL or RXLPH) path can be active at the same time.

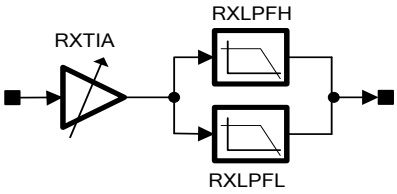


Figure 7: RX analog filtering chain

Figure 8 and Figure 9 illustrate selectivity and tunability of LMS7002M analog filters. Note that only few possible pass band configurations per filter are shown.

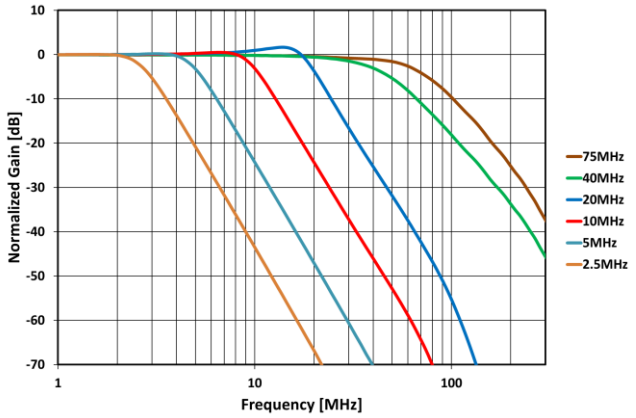


Figure 8: Analog TX LPF amplitude response (TXLPFS5 by passed)

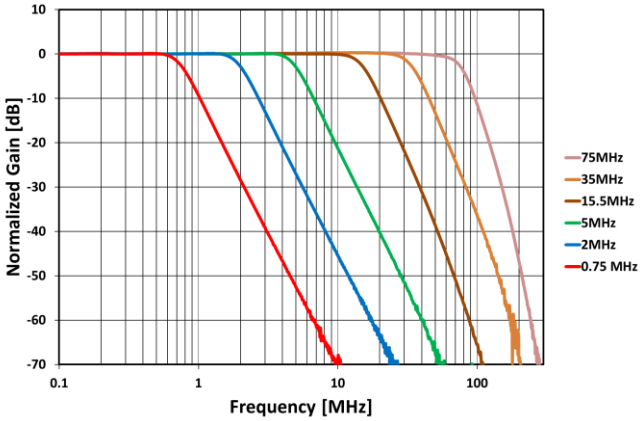


Figure 9: Analog RX LPF amplitude response

TRANSCEIVER SIGNAL PROCESSOR

LMS7002M includes a high digital gate count within the Transceiver Signal Processor (TSP) block. The function of the TSP is to employ advanced digital signal processing techniques to enhance the performance of the analog/RF parts. This results in an improved performance of the overall system and a saving on total current consumption.

The TSP is placed between the data converters and the LimeLight™ digital IQ interface as shown in *Figure 10*. Functionally, the RX and TX parts of the TSP are similar, as shown in *Figure 11* and *12,* respectively.

In both the TX and RX TSP blocks there are three general purpose finite impulse response (FIR) filters, G.P. FIR 1, G.P. FIR 2 and G.P. FIR 3. The filter coefficients are fully programmable and the implementation does not force their impulse response to be symmetrical.

On the TX side, one of these filters could be used as a phase equalizer, which is a requirement in some communication standards such as CDMA2000. Another can be used to flatten the amplitude response of the TXLPF while the third FIR could be used to further enhance the channel filtering function of the BB modem. If phase equalization is not required then one filter can be used to minimize group delay variation of the analog TXLPF.

Possible applications of the G.P. FIR filters on the RX side are similar. One could be used to minimize group delay variation of the analog RXLPF while another could help to improve RXLPF adjacent channel rejection performance.

The interpolation block within the TXTSP takes IQ data from the BB modem and increases the data sample rate. The advantages of having interpolation are as follows. For narrow band systems (GSM/EDGE) or even moderately broad band (WCDMA, CDMA2000) modulation standards, the BB modem does not need to interpolate IQ data to the target system (data converters) clock. The base band can provide output data at a much lower sample rate saving on power at the digital interface. Having a low data rate interface also simplifies the PCB design. However, the interpolator block generates data samples at the system clock rate, so the DACs run at a high sampling rate. As the DACs are running at a high frequency, it means that the quantization noise is spread over a wider frequency range which results in a better overall SNR. Also, the image generated by the DAC zero hold effect is further away from the wanted signal hence the specification for the TXLPF can be relaxed.

The reason for having decimation in the RXTSP is similar to that of interpolation in TXTSP. The ADCs can run at high frequency, and the specification of the RXLPF used as an anti-alias/channel select filter in this case is relaxed, the G.P. FIR improves adjacent channel rejection and the decimation circuit reduces the received data sample rate before sending the data to the BB modem.

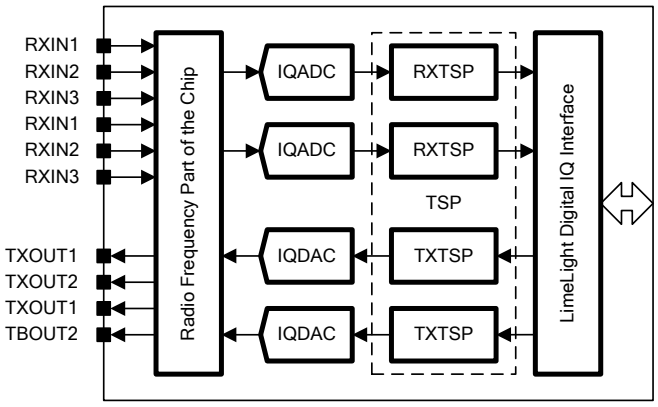


Figure 10: TSP part of the LMS7002M

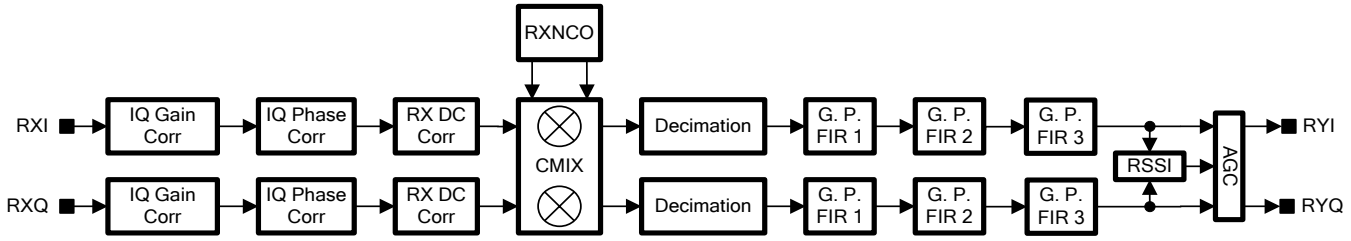


Figure 11: Structure of the RXTSP

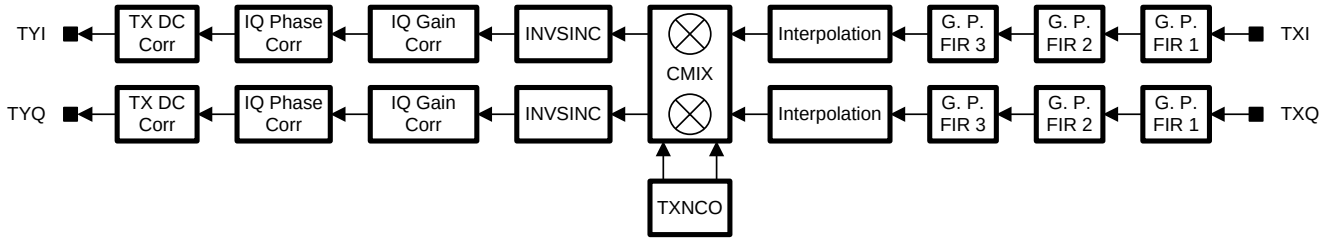


Figure 12: Structure of the TXTSP

The two Numerically Controlled Oscillators (NCO) and digital complex mixer (CMIX) in the TXTSP and RXTSP paths enable the LMS7002M to run in low digital IF.

Inverse sinc filters (INVSINC) within the TXTSP chain compensate for sinx/x amplitude roll off imposed by the DACs themselves.

The Tx DC Corr block is used to cancel residual DC offset of TXLPF. It is also used to cancel TX LO leakage feed-through as mentioned earlier.

There are three sources of the DC component at the RX output. These are the residual DC offset of the RXPGA and RXLPF, RX LO leakage feed-through and second order distortion (IP2). The Rx DC Corr blocks compensate for all of these sources of offset. The block is implemented as a real time tracking loop so any change of the RX DC due to either the signal level change, or due to RX gain change as well as any temperature effect will be tracked and cancelled automatically.

The IQ Gain Corr and IQ Phase Corr blocks correct IQ imbalance in both TXTSP and RXTSP in order to minimize the level of unwanted side band (image) component.

The last stage in the RXTSP path is a digital implementation of an Adaptive Gain Control (AGC) loop. Assuming that the BB modem does not require 12-bit full scale ADC outputs, the digital AGC block can provide a certain level of automatic gain control before the BB involves RF and IF gain stages.

More detailed descriptions of all the various TSP blocks are given in the following sections.

IQ Gain Correction

This block implements the following equation:

$$Iout = Iin * G\_I \quad .$$
$$Qout = Qin * G\_Q$$

Corresponding hardware is given in *Figure 13*. *G_I* and *G_Q* are programmable correction factors which are altered by the BB modem to minimize any unwanted side band component. The BB modem can combine IQ gain correction and digital gain control using the same module by calculating *G_I* and *G_Q* in the following way:

$$G\_I = G\_I\_corr * G\_digi \quad ,$$
$$G\_Q = G\_Q\_corr * G\_digi$$

where *G_I_corr* and *G_Q_corr* are IQ gain correction factors and *G_digi* is the desired digital gain.

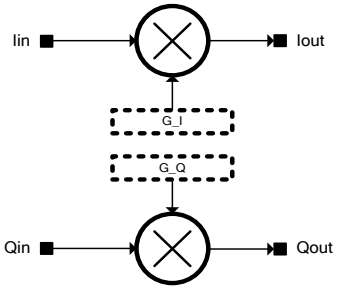


Figure 13: IQ gain correction implantation

IQ Phase Correction

IQ phase correction is in fact equivalent to vector rotation. If the quadrature phase error is α then the I and Q vectors are both rotated by $\alpha/2$ but in opposite directions hence IQ outputs of the corrector circuit are 90º phase shifted. IQ phase correction equations are given below while *Figure 14* shows the hardware implementation.

$$Iout = Iin + Qin * \tan\left(\frac{\alpha}{2}\right) \quad .$$

$$Qout = Qin + Iin * \tan\left(\frac{\alpha}{2}\right)$$

The value of tan*(α/2)* should be stored in the configuration register as a programmable correction parameter. The BB modem should adjust this value to minimize the unwanted side band component. The BB modem can also use the following approximation formula:

$$\tan\left(\frac{\alpha}{2}\right) \approx \frac{\alpha}{2}$$

when α is small, which is usually the case. The IQ phase corrector of the LMS7002M is designed to correct an IQ phase error up to +/- 20º.

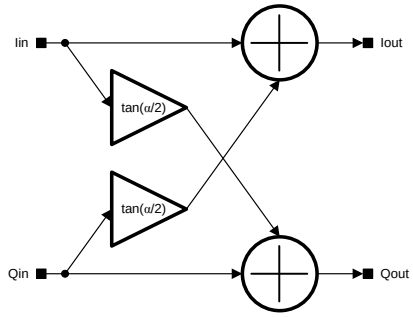


Figure 14: Implementation of IQ phase correction

TX DC Correction

DC offset correction in the TXTSP path is achieved by using the following equation:

$$Iout = Iin + DC\_I$$

$$Qout = Qin + DC\_Q$$

Here, *DC_I* and *DC_Q* are programmable DC offset correction parameters which the BB modem should adjust to minimize the TX DC and TX LO leakage feed-through. The hardware implementation is given below.

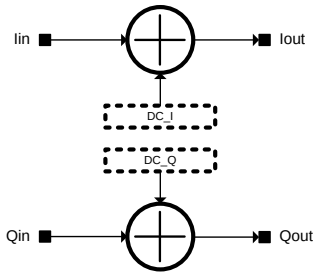


Figure 15: TX DC offset correction module

RX DC Correction

As mentioned previously, there are multiple reasons for DC to appear at the RX output. The most difficult to correct, in a static manner, is the second order distortion (IP2) component which changes with the RX input level as well as the RX gain set up. Hence, a compensation loop running in real time is required to track and correct the DC at the RX output. A simple digital implementation of such a loop is given in *Figure 16*.

The averaging (COMB) filter calculates the DC of the corrector input and subtracts it to cancel out the offset. The loop is running all the time so any change of the RX DC due to the signal level change, RX gain change or temperature will be tracked and cancelled automatically. The only programmable parameter in the loop is DCAVG which defines the averaging window size.

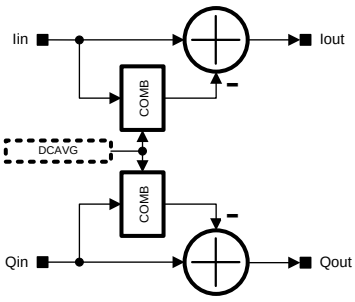


Figure 16: RX DC offset correction module

Inverse SINC Filter

The inverse sinc filter compensates for sinx/x amplitude roll off imposed by the DAC. The filter is designed to compensate from DC to $0.35f_s$ where f_s is the DAC sampling frequency. Impulse and amplitude responses are shown in *Figure 17* and *Figure 18*.a respectively. *Figure 18*.b plots the equivalent DAC amplitude response with the inverse sinc function compensation applied. The in band ($0 – 0.35f_s$) amplitude ripple is less than +/- 0.04 dB.

H(0) = 0.0101318 = h(4)
h(1) = -0.0616455 = h(3)
h(2) = 0.855469

Figure 17: INVSINC impulse response

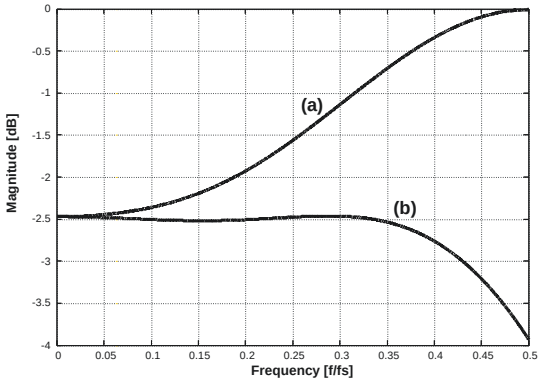


Figure 18: INVSINC (a) and equivalent DAC (b) amplitude response

Complex Mixer

The complex mixer used in the RXTSP and TXTSP is designed to implement the following set of equations:

$$I_{out} = I_{in}\cos\omega_c t \mp Q_{in}\sin\omega_c t ,$$

$$Q_{out} = \pm I_{in}\sin\omega_c t + Q_{in}\cos\omega_c t ,$$

where I_{in} and Q_{in} are provided from the IQ pre-processing stages while cosine and sine signals are generated by the NCO. An option to choose the sign in the mixing equations is implemented which in fact gives the ability to do up-mixing or down-mixing in both TX and RX chains.

The hardware implementation is shown in *Figure 19*.

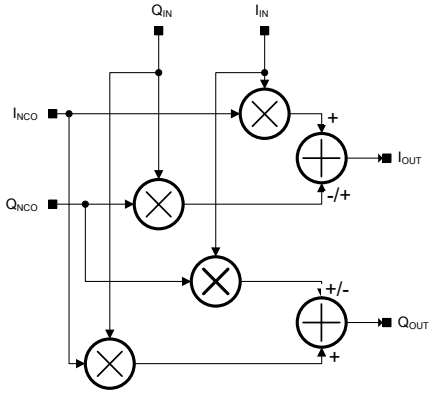


Figure 19: Complex mixer

Numerically Controlled Oscillator

The quadrature carrier signal, required to implement low digital IF, is generated by the local NCO. The internal NCO design is based on a DDFS (Direct Digital Frequency Synthesis) algorithm with a 32-bit

phase accumulator, 19-bit phase precision and provides 14 bit digital sine and cosine waveforms with the spurious performance better than –114 dBc.

The carrier frequency f_c generated by the NCO is defined using the following formula:

$$f_c = \frac{fcw}{2^{32}} f_{clk},$$

where *fcw* represents the decimal value of the 32-bit frequency control word and f_{clk} is the NCO clock frequency.

As shown in *Figure 20*, carrier phase offset can also be adjusted using the 16-bit configuration parameter *pho*. The carrier phase shift is calculated as follows:

$$\varphi = 2\pi \frac{pho}{2^{16}},$$

with *pho* being the decimal value stored in the carrier phase offset register.

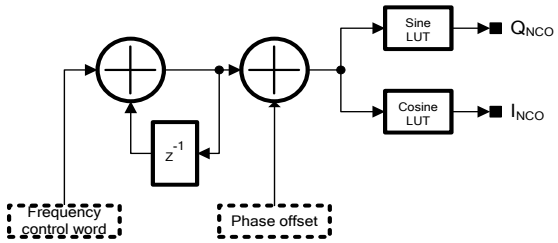


Figure 20: NCO architecture

Both frequency control and phase control words are easily accessible via SPI, therefore NCOs can be modulated by direct symbol insertion. Up to 16FSK or 16PSK modulations are supported in this way.

Interpolation

Interpolation within the TXTSP channel is implemented using the chain of five fixed coefficients half band FIR filters as shown in *Figure 21*. Each sub-filter in the chain interpolates by two. The interpolation ratio of the overall filter is set by selecting one of the sub-filter outputs and adjusting the clock rates accordingly. Hence, the interpolation ratio *K* can be programmed to be:

$$K = 1, 2, 4, 8, 16 \text{ or } 32.$$

Interpolation by 1 is achieved by bypassing all the interpolation filters. The filters are designed to provide a wide signal pass band from DC to f_p where:

$$f_p = x \cdot \frac{f_{clk}}{K},$$

with f_{clk} being TXTSP i.e. DACs clock frequency. Scaling factor *x* in the equation above, for *K=2, 4, 8, 16, 32*, should be set to one of the following values:

x <= 0.27 for >= 108dB interpolation image suppression,
x <= 0.30 for >= 75dB interpolation image suppression,
x <= 0.32 for >= 60dB interpolation image suppression.

Obviously, *x* can be used to trade off interpolation image suppression for the interpolation filter pass band.

For *K=1*, *x* should be set to x < 0.5 to limit the signal BW below Nyquist making the room for analog TX filters to operate. There is no interpolation image in this case hence more flexibility to set *x* for higher IF/RF bandwidth.

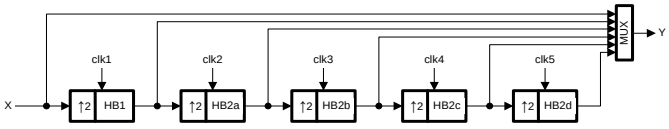


Figure 21: Programmable rate interpolation implemented by half band filters

```
h( 0) =  -4.673e-05 = h(30)
h( 1) =           0 = h(29)
h( 2) =  0.000392914 = h(28)
h( 3) =           0 = h(27)
h( 4) = -0.00181007 = h(26)
h( 5) =           0 = h(25)
h( 6) =   0.00600147 = h(24)
h( 7) =           0 = h(23)
h( 8) =  -0.0160789 = h(22)
h( 9) =           0 = h(21)
h(10) =   0.0378866 = h(20)
h(11) =           0 = h(19)
h(12) =  -0.0882454 = h(18)
h(13) =           0 = h(17)
h(14) =      0.3119 = h(16)
h(15) =         0.5
```

Figure 22: HB1 impulse response

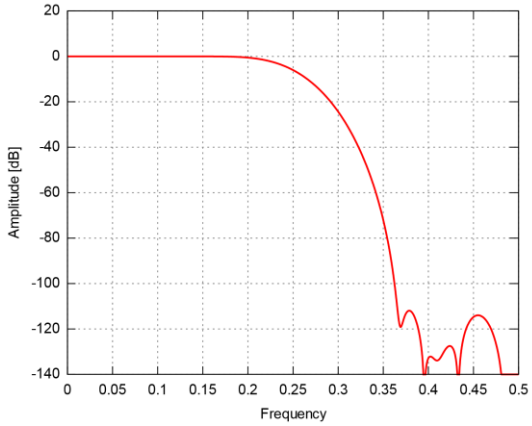


Figure 23: HB1 amplitude response

Only two different configurations are used within the filtering chain of *Figure 21*, HB1 and HB2. The impulse and amplitude response of HB1 are shown in *Figure 22* and *Figure 23*, respectively. The remaining three filters (HB2A, HB2B and HB2C) are all the same with their coefficients and amplitude response given in *Figure 24* and *Figure 25*, respectively. Frequency axis in *Figure 23* and *Figure 25* is scaled by the filters output sample rate which is twice the sample rate at the input. The overall interpolator can provide image suppression of better than –108 dB with negligible amplitude distortion (pass band ripple is less than10^{-5} dB).

```
h( 0) = -0.00164032 = h(14)
h( 1) =           0 = h(13)
h( 2) =   0.0138855 = h(12)
h( 3) =           0 = h(11)
h( 4) =  -0.0630875 = h(10)
h( 5) =           0 = h( 9)
h( 6) =    0.300842 = h( 8)
h( 7) =         0.5
```

Figure 24: HB2 impulse response

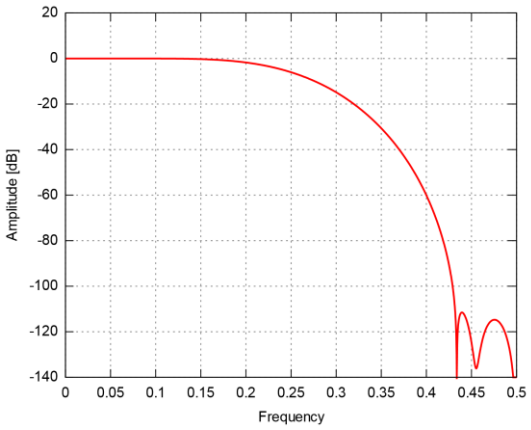


Figure 25: HB2 amplitude response

Decimation

The decimation function is implemented using the same filters as in the case for interpolation although the hardware is simplified slightly by taking advantage of only having to provide every second sample at the sub-filters output. The filter chain is shown in *Figure 26.*

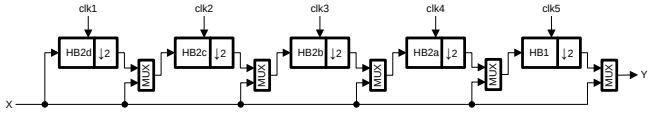


Figure 26: Programmable rate decimation implemented by half band filters

Decimation ratio *K* can be programmed to be:

$$K = 1, 2, 4, 8, 16 \text{ or } 32 .$$

Decimation by 1 is achieved by bypassing all the decimation filters. Decimator performance is the same as the performance of the interpolator i.e. pass band is:

$$f_p = x \cdot \frac{f_{clk}}{K} .$$

In this case f_{clk} is RXTSP i.e. ADCs clock frequency. As before, scaling factor *x* in the equation above, for *K=2, 4, 8, 16, 32*, should be set to one of the following values:

x <= 0.27 for >= 108dB decimation alias suppression,
x <= 0.30 for >= 75dB decimation alias suppression,
x <= 0.32 for >= 60dB decimation alias suppression.

Again, *x* can be used to trade off decimation alias suppression for the decimation filter pass band.

For *K=1*, *x* should be set to x < 0.5 to limit the signal BW below Nyquist making the room for additional filtering in BB, if required. There is no decimation alias in this case hence more flexibility to set *x* for higher IF/RF bandwidth.

In case of decimation, normalizing frequency in *Figure 23* and *Figure 25* is the filters input sample rate which is twice the sample rate at the output.

General Purpose FIR Filters

The LMS7002M features general purpose filters 1 and 2, which are based on a Multiply and Accumulate (MAC) FIR architecture. They can implement up to a 40-tap filtering function and the coefficients are fully programmable via SPI. The hardware implementation does not impose the constraint for the filter impulse response to be symmetrical hence the filter phase response can but does not need to be ideally linear. Therefore, it can be used in general filtering, as well as in phase nonlinear applications in which case the filter can implement phase equalization.

The filter coefficients are stored in five 8x16-bit internal memory banks as two's complement signed integers as shown in *Figure 27* where *L* is related to the filter length *N* as follows:

$$L = \left\lceil \frac{N}{5} \right\rceil .$$

Grey locations in *Figure 27* highlight the memory registers which are set to zero for 5*L* > *N*.

Evidently, the number of the filter taps *N* is limited by the size of the coefficients memory to:

$$N \le 5 * 8 = 40 .$$

The following relationship must be satisfied:

$$L \le K ,$$

K being the interpolation or decimation ratio, for the MAC hardware to be able to produce output samples on time.

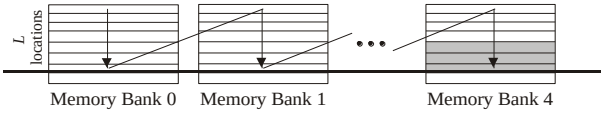


Figure 27: General purpose FIR filter coefficients memory organisation

General purpose FIR filter 3 hardware is composed of three filters (each equivalent to G.P. FIR 1 or 2) running in parallel in order to increase its processing power. For G.P. FIR 3 the equivalent equations are as below:

$$L = \left\lceil \frac{N}{3 * 5} \right\rceil ,$$
$$N \le 3 * 5 * 8 = 120 \text{ , and}$$
$$L \le K .$$

Coefficients memory is organised as in *Figure 27* with memory banks being tripled. This filter can be used as a channel select filter or for any other purpose which requires a larger number of filtering taps.

Received Signal Strength Indicators

A digital received signal strength indicator (RSSI) circuit calculates the level of the received complex signal (*I* + j*Q*) as follows:

$$RSSI = \frac{\sqrt{I^2 + Q^2}}{2} .$$

The following approximation of the square root is implemented in the chip:

$$\sqrt{a^2 + b^2} \approx \max\left(\left((M - 0.125M) + 0.5N\right), M\right),$$

where:

$$M = \max\left(|a|, |b|\right)$$
$$N = \min\left(|a|, |b|\right) .$$

The same RSSI block is used within the digital AGC loop. If digital AGC is not required then the RSSI output, after being averaged by the COMB filter, can be provided back to the BB modem via SPI as shown in *Figure 28*. In this way the BB can control RF and IF gain stages to implement analog AGC in which case the AGC loop is closed via the BB modem.

There is also an RF RSSI block implemented in the RF front end connected to the input of the wideband LNA, see *Figure 1.* This block

can be used to detect the presence of large interferers so the BB modem can adjust RX gain stages very quickly to counteract such scenarios. Reading the value of RF RSSI output is available through the SPI. Also, RF RSSI analog output can be provided off chip at the test pin and further processed by external circuits if required. The RSSI detects RF input from -70 dBm to -20 dBm.

Automatic Gain Control

The structure of the digital automatic gain control loop is shown in *Figure 28*. The AGC loop functions as follows:

- "Square root of two" (RSSI) block calculates the RMS of the AGC output.
- This signal is averaged by the COMB filter. The averaging window size AVG is programmable via SPI.
- An error signal is then calculated as the difference between the desired output signal level and the measured one. The desired amplitude level ADESIRED is programmable via SPI.
- After the loop gain stage, the error is integrated to construct the digital VGAs gain control signal. Loop gain K is programmable via SPI.
- VGAs gain cannot be negative and should not be zero either, hence max(1,x) module is provided in the feedback path.

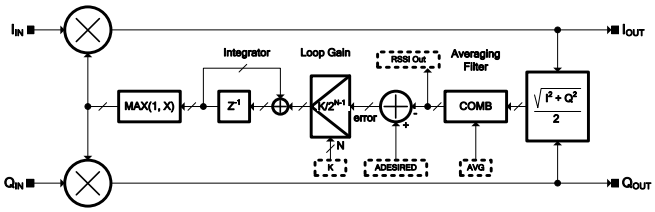


Figure 28: AGC architecture

Figure 29 illustrates two possible applications of the digital AGC. The first example (*Figure 29.a*) shows the case where the BB modem expects 4-bits instead of full 12-bit ADC output. In this case, ADESIRED loop parameter is set as shown in the figure, the gain of RF and IF stages are set for ADC not to produce full scale but ADESIRED level instead. The middle 4 bits are provided to BB. If the RF input signal level goes higher or lower, AGC will adapt the gain to keep its output at ADESIRED value so bits 7 to 4 will always contain 4 MSBs of the received signal. Since we have 4 bits on top and 4 bits below the middle 4 bits, the loop itself provides +/-24 dB automatic gain control range without using RF and IF gain stages.

The second example shown in *Figure 29.b* is a more general case. The BB modem will receive 10-bits while the loop provides +/- 6 dB gain control range without engaging RF and IF gain blocks.

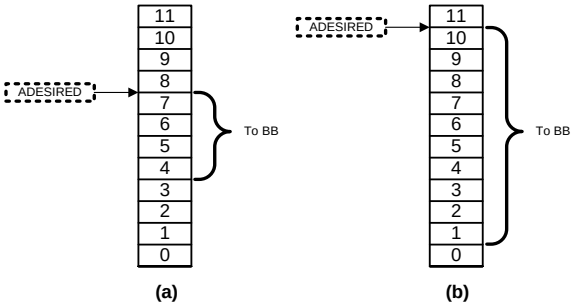


Figure 29: Truncation to (a) 4 bits and (b) 10 bits

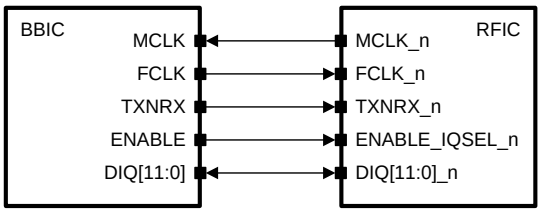
LIMELIGHT™ DIGITAL IQ DATA INTERFACE

Description

The LMS7002M implements LimeLight™ digital IQ interface to the BB modem. LimeLight™ can be configured to run in one of the following three modes:

1. JESD207 mode
2. TRXIQ double data rate (DDR) mode
3. TRXIQ single data rate (SDR) mode

All three modes are capable of supporting both TDD and FDD operation. The data throughput of JESD207 and TRX DDR is high enough to connect to up to 2x2 MIMO BB modems. TRXIQ SDR mode is backward compatible to the LMS6002D digital IQ interface.



Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

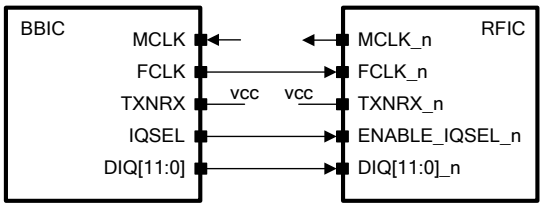
Figure 30: LimeLight™ port, JESD mode

Figure 30 shows typical connectivity between the LMS7002M and the BB modem with LimeLight™ running in JESD207 mode. LimeLight™ uses two such ports to support FDD. Signalling is defined by the JESD207 standard itself as specified by JEDEC.

Timing diagrams for the JESD207 mode can be seen in *Figure 33 – Figure 36*.

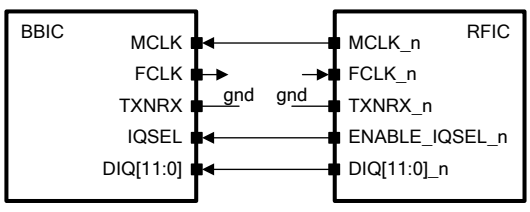
Connectivity in TRXIQ DDR and SDR modes is the same and is shown in *Figure 31* and *Figure 32*. The only difference is that in DDR mode the BB and RF chips sample at both edges of FCLK/MCLK. In TRXIQ-TX mode the BB modem provides IQSEL, DIO[11:0] and FCLK. The LMS7002M captures data using one or both edges of FCLK. In TRXIQ-RX mode, the LMS7002M provides IQSEL, DIO[11:0] and MCLK. The BB modem captures data using one or both edges of MCLK.

Timing diagrams for the TRXIQ DDR and SDR modes can be seen in *Figure 37 – Figure 40*.



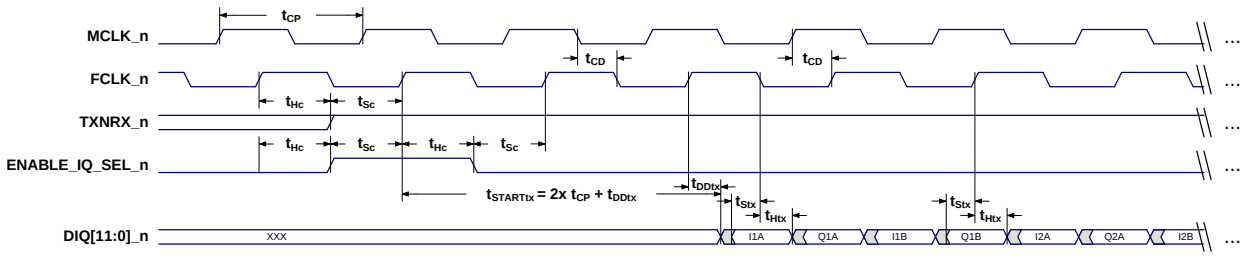
Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 31: LimeLight™ port, TRXIQ-TX mode



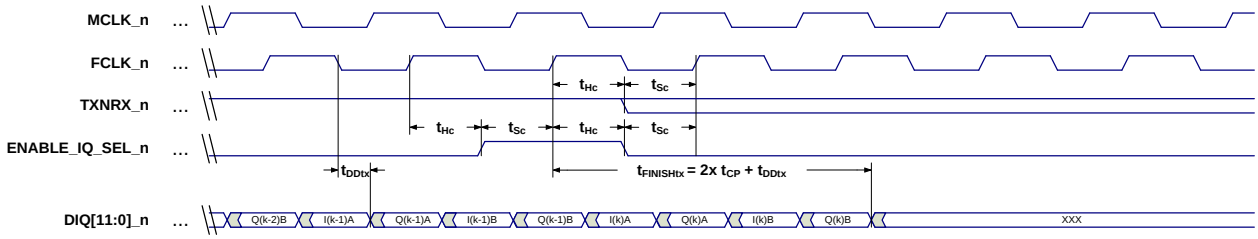
Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 32: LimeLight™ port, TRXIQ-RX mode



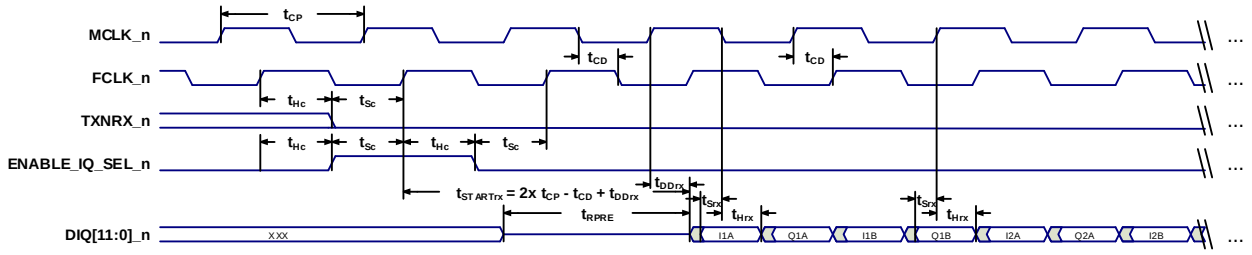
Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 33: Data path transmit burst start (JESD207 mode)



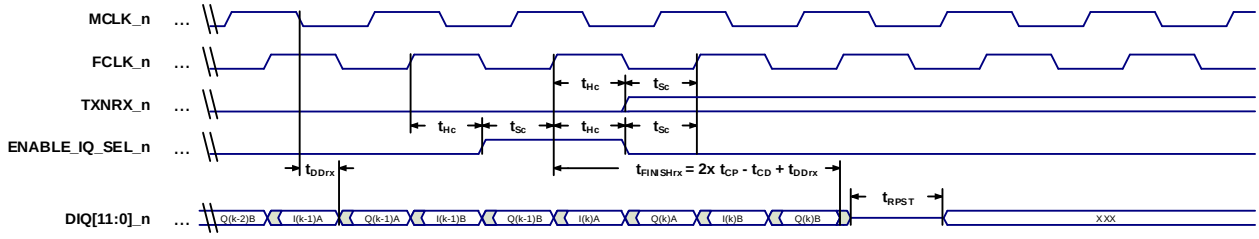
Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 34: Data path transmit burst finish (JESD207 mode)



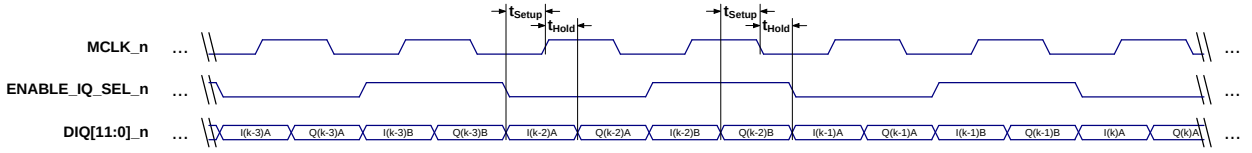
Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 35: Data path receive burst start (JESD207 mode)



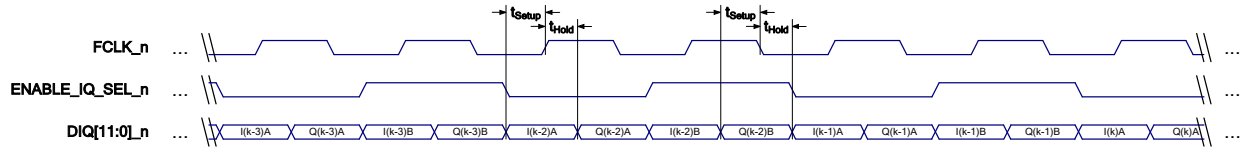
Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 36: Data path receive burst finish (JESD207 mode)



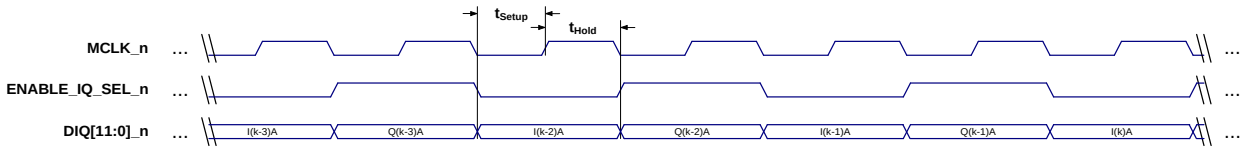
Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 37: Receive data path (TRXIQ double data rate (DDR) mode)



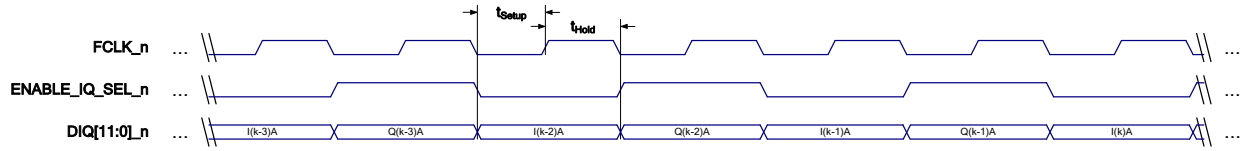
Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 38: Transmit data path (TRXIQ double data rate (DDR) mode)



Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 39: Receive data path (TRXIQ single data rate (SDR) mode)



Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 40: Transmit data path (TRXIQ single data rate (SDR) mode)

Implementing Low Voltage Digital IQ Interface

Digital IO buffers of LMS7002M are supplied using four pins (pin name – DIGPRVDD2, pin ID – W33, T32, H32, AH30). All these pins must be supplied by the same supply DVDD. There is one additional supply pin (pin name – DIGPRPOC, pin ID – W31) which performs Power On Control (POC) function for digital pads. To implement a low voltage digital interface, DVDD can be lowered to 1.8V. If DVDD=1.8V then all data lines in *Figure 41* must also be set to 1.8V CMOS IOs for correct interface operation.

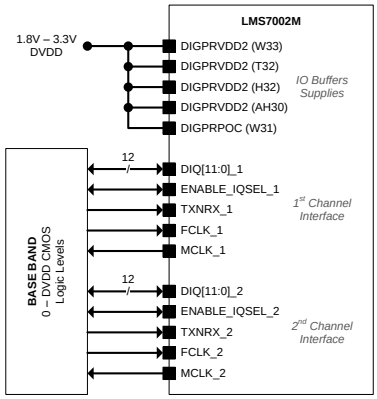


Figure 41: Digital IQ interface supplies

IQ Interface Timing Parameters

Parameter	Min.	Typ.	Max.	Unit
Data Setup Time (t_{SETUP})	1			ns
Data Hold Time (t_{HOLD})	0.2			ns
Data Output Delay (t_{OD}) at 15 pF load			6	ns

Table 6: Digital IQ interface timing parameters with 2.5V IO supply

Digital IQ Interface IO Buffers Specifications

Parameter	Min.	Typ.	Max.	Unit	Condition
Supply Voltage (PVDD)	1.7	2.5	3.6	V	Can go below 2.5V nominal to support LV CMOS signalling
Input High V_{IH}	PVDD-0.8			V	
Input Low V_{IL}			0.8	V	
Output High V_{OH}	PVDD-0.4			V	
Output Low V_{OL}			0.4	V	
Input Pad Capacitance C_{IN}			3.5	pF	
Output Drive Current	8		12	mA	Programmable

Table 7: Digital IO buffers specifications at 2.5V supply

DACs ELECTRICAL SPECIFICATIONS

Parameter	Min.	Typ.	Max.	Unit	Condition
Digital Core Supply	1.1	1.2	1.3	V	Generated using integrated LDOs
Analog Supply	1.1	1.2	1.3	V	Generated using integrated LDOs
Number of Bits		12		bits	Two's complement format
DAC Sampling Rate			640	MHz	
Full Scale Current		625		uA	Programmable
SFDR		63 62		dBc	Fin=10MHz,-1dBFS Fin=37MHz,-2dBFS
ENOB		9		bits	

Table 8: DACs electrical specifications

ADCs ELECTRICAL SPECIFICATIONS

Parameter	Min.	Typ.	Max.	Unit	Condition
Digital Core Supply	1.1	1.2	1.3	V	Generated using integrated LDOs
Analog Supply	1.1	1.2	1.3	V	Generated using integrated LDOs
Number of Bits		12		bits	Two's complement format
ADC Sampling Rate			160	MHz	
Input Amplitude		0.8		Vpp	Differential
Input Common Mode Voltage		0.55		V	
SFDR		63 62		dBc	Fin=10MHz,-1dBFS Fin=37MHz,-2dBFS
ENOB		9		bits	

Table 9: ADCs electrical specifications

SERIAL PORT INTERFACE

Description

The functionality of the LMS7002M transceiver is fully controlled by a set of internal registers which can be accessed through a serial port interface. Both write and read SPI operations are supported. The serial port can be configured to run in 3 or 4 wire mode with the following pins used:

- SEN serial port enable, active low
- SCLK serial clock, positive edge sensitive
- SDIO serial data in/out in 3 wire mode
  serial data input in 4 wire mode
- SDO serial data out in 4 wire mode
  don't care in 3 wire mode

Serial port key features:

- 32 SPI clock cycles are required to complete a write operation.
- 32 SPI clock cycles are required to complete a read operation.
- Multiple write/read operations are possible without toggling serial port enable signal.

All configuration registers are 16-bit wide. Write/read sequence consists of 16-bit instruction followed by 16-bit data to write or read. MSB of the instruction bit stream is used as SPI command where CMD = 1 for write and CMD = 0 for read. Next 4 bits are reserved (Reserved[3:0]) and must be zeroes. Next 5 bits represent module address (Maddress[4:0]) since the LMS7002M configuration registers are divided into logical blocks as shown in Table 11. The remaining 6 bits of the instruction are used to address particular registers (Reg[5:0]) within the block. Maddress and Reg compiles global 11-bit register address when concatenated ((Maddress << 6) | Reg).

The write/read cycle waveforms are shown in *Figure 42*, *Figure 43* and *Figure 44.* Note that the write operation is the same for both 3-wire and 4-wire modes. Although not shown in the figures, multiple write/read is possible by repeating the instruction/data sequence while keeping SEN low.

SPI Timing Parameters

Parameter	Min.	Typ.	Max.	Unit
Clock Frequency, 4-wire mode			50	MHz
3-wire mode			20	MHz
Enable Setup Time (t_{ES})	2			ns
Enable Hold Time (©)	0.2			ns
Data Setup Time (t_{DS})	1			ns
Data Hold Time (t_{DH})	0.2			ns
Data Output Delay (t_{OD}) at 12pF load			6	ns

Table 10: SPI timing parameters at 2.7V IO supply

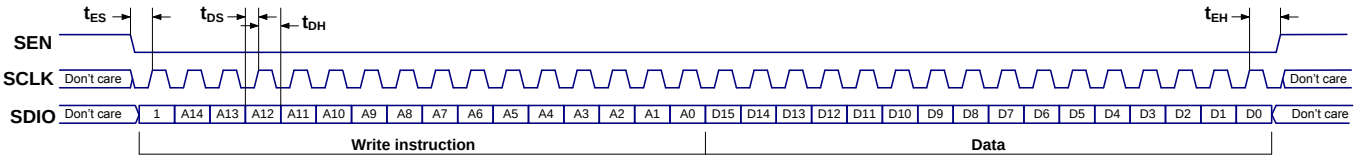


Figure 42: SPI write cycle, 3-wire and 4-wire modes

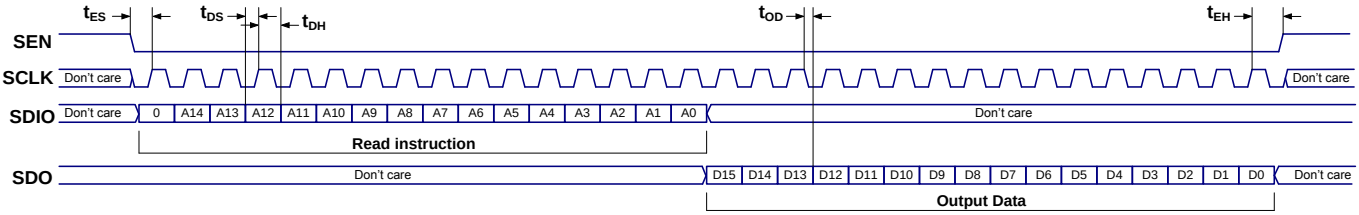


Figure 43: SPI read cycle, 4-wire mode (default)

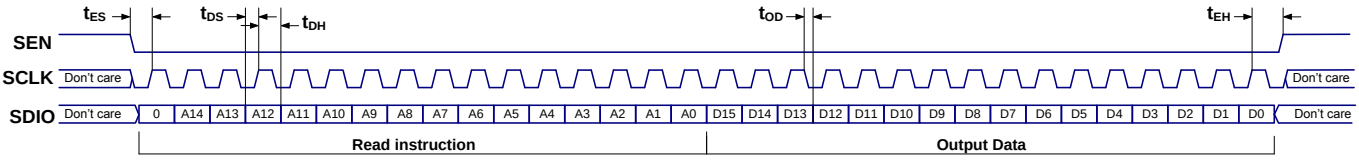


Figure 44: SPI read cycle, 3-wire mode

SPI Memory Map

The LMS7002M configuration registers are divided into a number of logical blocks as shown in Table 11.

Integer and fractional parts of the PLL feedback divider are stored in a number of configuration memory registers. To change their values, multiple SPI write cycles are required. Hence, the controlled PLL will continue to output at the previously selected frequency until all NINT and NFRAC registers are updated. Otherwise it would generate an unpredicted and wrong LO frequency while being configured. Such parameters are provided through shadow registers. Shadow registers are clocked by the PLL reference clock and output new values simultaneously at first positive clock edge after SEN goes high, i.e. after updating of shadowed parameters via SPI is finished.

Module Description	Module address [4:0]	Register address space [5:0]
Microcontroller (MCU)	00000	00xxxx
Lime Light port	00000	1xxxxx
Top Control (AFE, BIAS, XBUF, CGEN, LDO, BIST)	0001x	xxxxxx
TRX (TRF(A/B), TBB(A/B), RFE(A/B), RBB(A/B), SX(R/T)	0010x	xxxxxx
TxTSP(A/B)	01000	0xxxxx
TxNCO(A/B)	01001	xxxxxx
TxGFIR1(A/B)	01010	xxxxxx
TxGFIR2(A/B)	01011	xxxxxx
TxGFIR3a(A/B)	01100	xxxxxx
TxGFIR3b(A/B)	01101	xxxxxx
TxGFIR3c(A/B)	01110	xxxxxx
RxTSP(A/B)	10000	0xxxxx
RxNCO(A/B)	10001	xxxxxx
RxGFIR1(A/B)	10010	xxxxxx
RxGFIR2(A/B)	10011	xxxxxx
RxGFIR3a(A/B)	10100	xxxxxx
RxGFIR3b(A/B)	10101	xxxxxx
RxGFIR3c(A/B)	10110	xxxxxx

Table 11: LMS7002M SPI memory map

Implementing Low Voltage SPI

Digital IO buffers in the SPI region are all supplied from the same pins as the digital IQ interface (pin name – DIGPRVDD2, pin ID – W33, T32, H32, AH30). All these pins must be supplied by the same supply DVDD. There is one additional supply pin (pin name – DIGPRPOC, pin ID – W31) which controls the power on circuitry of the digital pads. To implement a low voltage SPI interface, DVDD can be lowered to 1.8V. If DVDD=1.8V then all data lines in *Figure 45* must also be set to 1.8V CMOS IOs for correct interface operation. The PLL reference clock input level is controlled independently of the DVDD voltage. By default it is 1.8V, but can be further lowered to 1.2V by chip controls if needed.

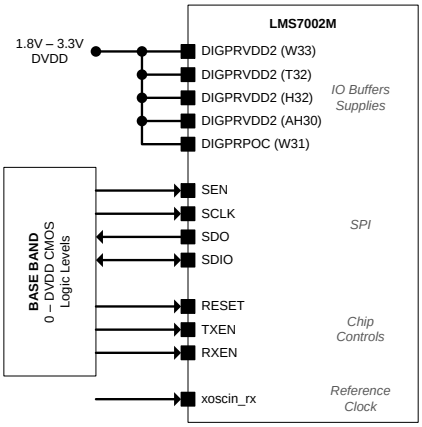


Figure 45: SPI supplies

ON CHIP MICROCONTROLLER

Description

The LMS7002M can be fully controlled by external BB/DSP/FPGA ICs using 4-wire or 3-wire serial port interface. The controlling processor needs to implement a set of calibration, tuning and control functions to get the best performance out of the transceiver. The on chip microcontroller unit (MCU) provides the option for independent control using code provided by Lime. This allows the LMS7002M to be independent of the BB/DSP/FPGA and off-loads these devices. Users can still implement full control in their preferred way by developing their own code and/or bypassing on chip microcontroller.

MCU integration within the LMS7002M chip is shown in *Figure 46*. Since the chip communication to the outside world is done through SPI, the MCU uses the same protocol hence the block mSPI (master SPI) is placed in front of it. The MCU communicates to the transceiver circuitry using the same SPI protocol as the BB processor itself. This is implemented via ucSPI lines shown in *Figure 46*. There is two way communication between the MCU and BB via mSPI. The baseband can trigger different calibration/tuning/control functions the MCU is programmed to perform. The MCU reports a success, failure or an error code back to the base band processor.

In this architecture, the base band processor acts as master since it controls the whole chip, (transceiver as well as MCU). The base band processor also controls the SPI switch (via SPISW_CTRL control bit/line of mSPI) i.e. taking control over the transceiver part or handing it over to the MCU. The MCU acts as a slave processor. It can control the transceiver only if the base band allows that via the SPI switch.

The base band has full control over the chip including calibration, tuning and control. It also can trigger the MCU for assistance. In this case, it works in the following way:

1. The base band sets the transceiver for the targets (TX LO frequency, RX LO frequency, TX gain, RX gain, …).
2. The base band hands over SPI control to the MCU by setting SPISW_CTRL.
3. The base band triggers the function for the MCU to execute.
4. The base band periodically checks to see if the MCU has finished and for the status (success, failure, error code).

MCU Boot Up and EEPROM Programming

Two options are supported, one using external (off chip) EEPROM and another without external EEPROM.

Option A: Using external EEPROM

1. The base band processor uploads 16 KB into the on chip program memory.
2. After receiving 16 KB, the MCU flushes program memory into EEPROM.
3. The base band resets the MCU.
4. The MCU reads EEPROM content back into the program memory and starts executing the code.

After initial EEPROM programming only steps 3 and 4 are required.

Option B: No external EEPROM

1. The base band processor uploads 16 KB into the on chip program memory.
2. After receiving 16 KB, the MCU starts executing the code.

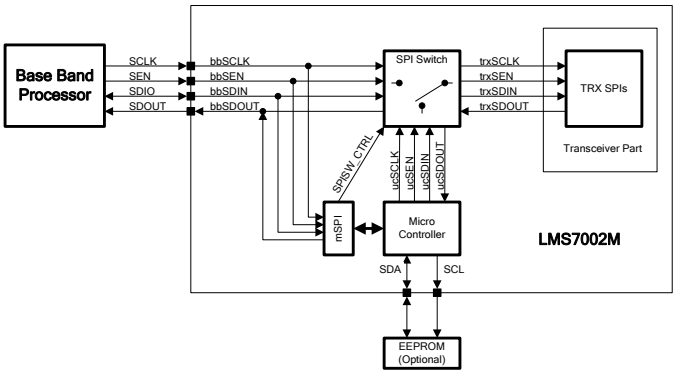


Figure 46: On chip microcontroller connection

Specifications

- 8-bit microcontroller.
- Industry standard 8051 instruction set compatible.
- Running up to 60 MHz.
- Memory
  - 16 KB SRAM program memory
  - 2 KB SRAM working memory
  - 256 B dual port RAM
  - All on chip, integrated.

DATA CONVERTERS CLOCK GENERATION

The clock generation circuit for the data converters is shown in *Figure 47*. It shares the same reference clock input REFCLK with the RF synthesizers as specified in *Table 1*. The clock PLL then generates a continuous frequency range centered around 2.5 GHz. The feed forward divider (FFDIV) is programmable and capable of implementing division values as below:

$$N = 2(n+1),\ n = 0, 1, \ldots, 255$$

There is a fixed divide by 4 within the ADC block hence clock division on the DAC side to provide more flexibility. There is a MUX to connect either Fpll, or Fpll/M to either ADC or DAC clocks. *M* is programmable and can be set to *M* = 1, 2, 4 or 8. The other CLKMUX output will be connected to the other data converter clock input.

TSP blocks receive the same clock as the corresponding data converter, hence there is no need for complex non-power of two or fractional interpolation/decimation. TSP blocks have programmable interpolation/decimation and generate MCLK clocks going back to the base band processor via the LimeLight™ port.

The circuit implements a continuous clock frequency range from 5 MHz to 640 MHz for the data converters.

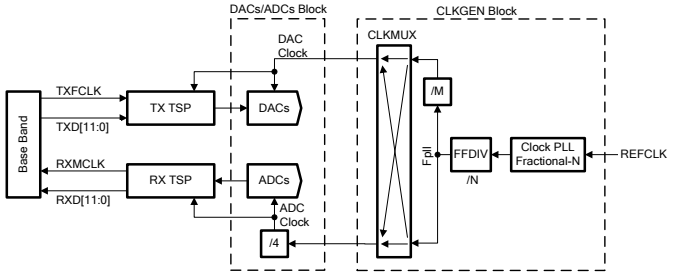


Figure 47: Clock generation and distribution

CALIBRATION AND INITIALIZATION

There are a number of calibrations which the LMS7002M can carry out internally when instructed via the SPI. These calibrations can be initiated on power up/reset to produce optimum settings. Initialization and calibration steps are summarized below.

Initialization

- Power up the chip. In case of using multiple off chip LDOs, power up sequence is not important.
- Apply RESET pulse (active low). This sets all the configuration registers to their default values.
- Overwrite some registers defaults if required.

Available calibration options and recommended order of execution

- On-chip resistor and capacitor calibration
- TX, RX and clock synthesizer VCO tuning
- TX and RX analog LPF pass band tuning
- RX DC offset and RX LO leakage cancellation
- TX DC offset and TX LO leakage cancellation
- TX IQ imbalance calibration
- RX IQ imbalance calibration

This section shows three key calibration algorithms. Others are either similar or very simple. Please see the "LMS7002M Programming and Calibration Guide" and other relevant application notes for more details.

VCO Tuning

In order to lock RF or clock synthesiser while having phase noise close to optimum, VCO capacitance has to be selected carefully. A flexible algorithm, based on monitoring on chip Vtune comparators state, is described below.

Assuming the synthesiser is configured for target LO/clock frequency (correct VCO powered up, integer and fractional part of the divider set, …), *Figure 48* shows typical measured Vtune variation with the VCOCAP codes for the two target LO frequencies, 1.95GHz and 2.14GHz. Obviously, Vtune is changing from 1.17V down to 0.05V. However, PLL lock is guaranteed only when Vtune is in the range between Vth Low and Vth High. Vth High is fixed to 0.92V while Vth Low can be programmed to be 0.18V or 0.1V. For the best phase noise performance, Vtune should be kept around the middle of the Vth Low and Vth High range.

There are two on chip Vtune comparators per synthesiser: CMPH and CMPL. Their threshold voltages are set to Vth High=0.92V and Vth Low=0.18V or 0.1V. The state of the comparators can be obtained by powering them up and reading the corresponding SPI register. True table is given below.

CMPH	CMPL	Status
1	0	OK, Vtune in range
0	0	Vtune is high (> 0.92V), PLL lock not guaranteed.
1	1	Vtune is low (< 0.18V or <0.1V), PLL lock not guaranteed.
0	1	Not possible.

These can be used to choose VCOCAP code. All we need to find is the code CMIN when comparators change the state from "00" to "10" and the code CMAX when the comparators change the state from "10" to "11". Optimum VCOCAP code is then the middle one between CMIN and CMAX. For LO=2.4GHz, this is illustrated in *Figure 48*. Once the synthesiser is set, Vtune comparators can also be used as lock (in range) indication.

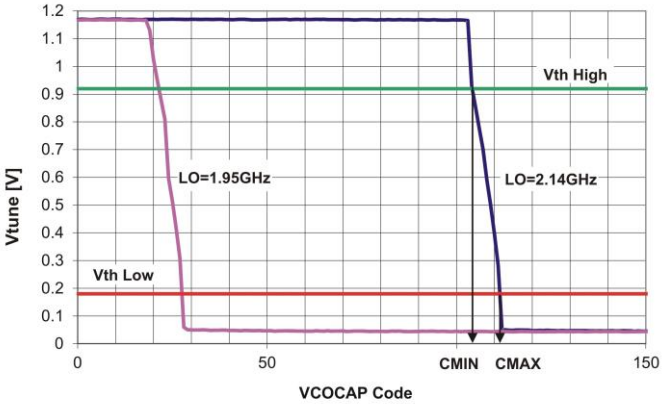


Figure 48: VCO capacitance selection

Analog Filters Pass Band Tuning

As shown in *Figure* 6 and *Figure* 7, LMS7002M has six analog low pass filtering stages. Pass band of each stage can independently be programmed and/or tuned. Tuning is very useful as it takes into account process, temperature, sample-to-sample and voltage supply variations.

The algorithm uses on chip options as follows:

- TXNCO generates digital test tones (CW).
- Digital test tones are converted into analog by the DACs.
- INVERSE sinc filter must be enabled to flatten DACs amplitude response.
- LMS7002M is set into either base-band or RF TX-to-RX loop back mode.
- Only LPF being tuned should be enabled. Other TX and RX filters should be bypassed or widely open.
- Loop back signal is converted back into digital domain by the ADCs.
- Digital RX RSSI block measures the amplitude of the loop back signal.

In this set up TXNCO test tone drives the filter input while filter output is measured by RSSI block which enables filter amplitude response to be determined.

All filtering stages are implemented as active RC blocks hence their pass band is controllable by changing resistors and/or capacitors. Only two parameters per stage are available to change via SPI: one for filter resistors control and another one for capacitors control. If resistors control parameter is changed then all resistors within the filter are scaled equally. If capacitors control code is changed then all capacitors within the filter are scaled equally. Therefore, component ratio is kept constant which preserves designed filter amplitude response (Chebyshev for example) disregarding the control codes.

There are two types of filter stages: trans-impedance (TXLPFLAD, TXLPFH, RXTIA) and voltage gain (TXLPFS5, RXLPFL, RXLPFH). Tuning is essentially the same for all stages with minor differences between trans-impedance and voltage gain types. The algorithm is two steps process described below and illustrated in *Figure 49*.

Step 1: Check point

TXNCO generates very low frequency (close to DC) test tone (200kHz in *Figure 49* example) which is by design guaranteed to be within filter pass band for all possible RC values.

Tune the gain of the measurement loop (use DACs current amplifiers and RXPGA) to get RSSI reading few dB backed off from its maximum. This maximizes the measurement dynamic range while still having some margin to measure filter gain which may be higher than the gain at low frequencies due to in band amplitude ripple.

Step 2: RC search
TXNCO generates test tone which is target 3dB cut-off frequency (4MHz in *Figure 49* example).

a. Alter C components of the filter to get RSSI reading 3dB below the reading obtained at the end of step 1.

b. If step 2.a fails to reach the target, change R components of the filter. If filter stage is trans-impedance go to step 1, otherwise go to step 2.a. Note that changing R in trans-impedance stage changes its gain hence the need to repeat step 1.

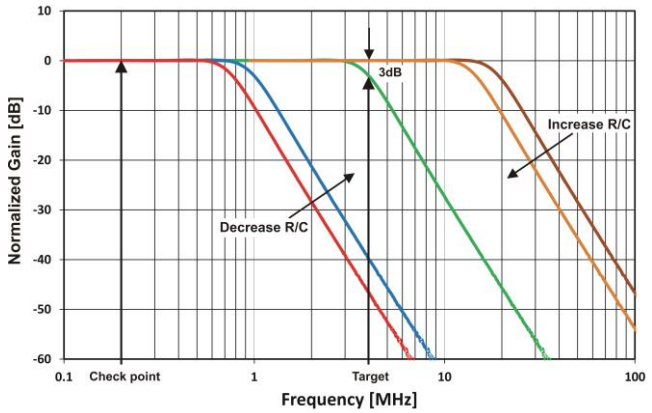


Figure 49: Pass band tuning algorithm

DC Offset and IQ Imbalance Calibration

In order to show the basis of this kind of calibrations, let us first analyse the scenario with LMS7002M configured as below.

- Drive TXTSP with digital 12-bit two's complement DC i.e.
  - TXI = 011111111111 = +max 12-bit word
  - TXQ = 10000000000 = -max 12-bit word

  This can be done through on chip test option, no need to engage LimeLight™ with assistance from BB.
- Bypass IQ Gain Correction, IQ Phase Correction and TX DC Correction TXTSP blocks. Keep INVERSE sinc filter running.
- Configure TXLPF pass band to be able to filter DAC images.
- Tune TX Synthesiser to f_{TXLO}. Tune RX Synthesiser to f_{RXLO} offset from f_{TXLO} by few MHz and keep $f_{TXLO} > f_{RXLO.}$
- Close RF Loopback switch.
- Set TXPAD, RXTIA and RXPGA gain not to overload ADCs.
- Open RXLPF pass band as much as possible to clearly see all tones generated in this setup.
- Bypass IQ Gain Correction, IQ Phase Correction and RX DC Correction RXTSP blocks. Bypass Decimation filter to see all tones generated by the whole setup.
- Set RXNCO frequency to 0. Set TXNCO to f_{TXNCO} where $f_{TXLO} – f_{RXLO} > f_{TXNCO.}$

The test setup described above uses minimum filtering to clearly show unwanted tones we need to cancel. The spectrum of *Figure 50* shows RX output while LMS7002M works in RF loopback mode. Tones and the reasons for their existence are as below.

(1) TX DC and TX LO leakage. It is down converted by f_{RXLO} hence it appears in BB frequencies at f_{TXLO}-f_{RXLO}
(2) This is wanted TX sideband. Offset from TX LO leakage by TXNCO frequency .f_{TXNCO}.
(3) Unwanted TX sideband caused by TX IQ imbalance.
(4) RX DC offset and RX LO leakage. Appears at DC.
(3a) RX unwanted side band caused by component (3)
(1a) RX unwanted side band caused by component (1)
(2a) RX unwanted side band caused by component (2)

Note that all tones at negative frequencies are the consequence of RX IQ imbalance.

Figure 50 shows that with single measurement we can capture all tones we need to cancel. There are two problems with this approach. We need to perform complex FFT which is computationally intensive i.e. takes long time. On chip MCU is not computationally powerful enough so FFT has to be done by BB processor which we want to avoid. Alternative would be to use digital RSSI for measurement instead of FFT. RSSI can accurately measure only single tone, not multi tone as in *Figure 50*. Fortunately, choosing the order of calibration steps carefully and with the help of on chip available options (digital and/or analogue filters, TX and RX NCOs) this is possible.

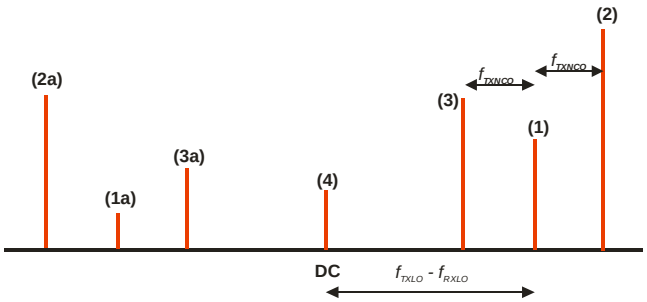


Figure 50: Spectral tones generated by the set up described above

TX IQ imbalance calibration step is shown here as an illustration. Other calibration steps are similar. Let us assume that RX DC/LO leakage as well as TX DC/LO leakage calibration steps are already performed, i.e. tones (1), (1a), and (4) are minimized. In this case we will have four remaining tones as shown in *Figure 51.a*. The goal of this calibration is to minimize tone (3) keeping wanted tone (2) untouched. Tone (2) will introduce huge error if present in RSSI measurement so some filtering will be required. Decimation filter is used for this purpose rather than general purpose FIR filters due to the fact that decimation filter is much simpler and faster to configure. Resulting spectrum after digital filtering is shown in *Figure 51.b*.

The same spectrum of *Figure 51.b* drives digital RSSI block. In fact RSSI measures the level of two tone signal (3) and (3a) where (3a) is due to RX IQ imbalance. However tones are correlated. In other words, minimizing (3), tone (3a) will go down for the same amount. RSSI output will be composite power level of those two tones and is valid measure. If we minimize RSSI output we are minimizing TX IQ imbalance disregarding the presence of two (correlated) tones.

Algorithm is then simple. First alter on chip analog IQ phase correction parameters if available to minimize RSSI output. After that alter TX Gain correction and TX Phase correction parameters of TXTSP digital block to further minimise RSSI output. Resulting spectrum is shown in *Figure 51.c*.

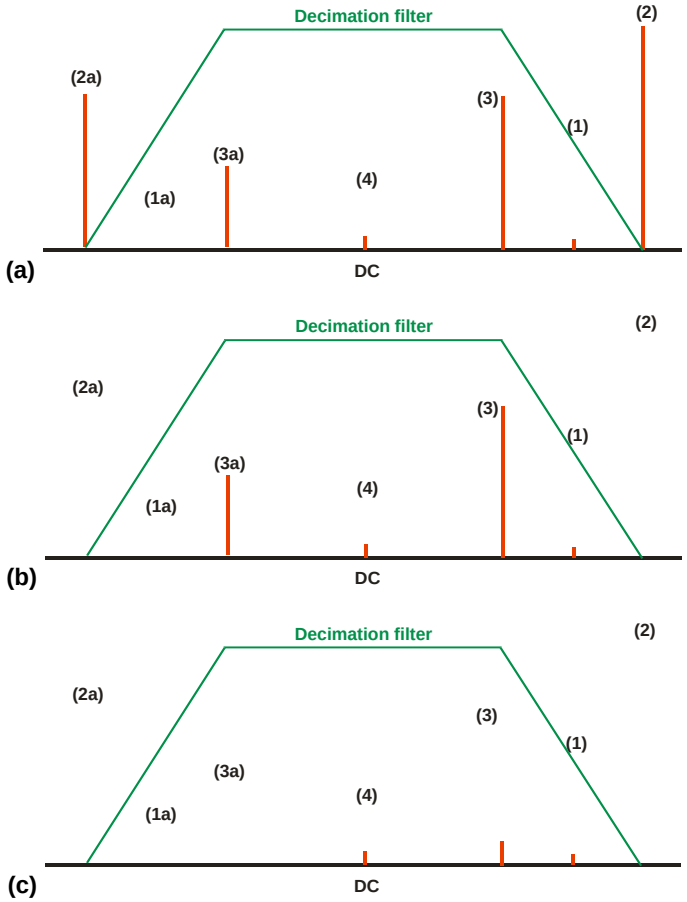


Figure 51: TX IQ imbalance calibration. Spectral tones:
(a) before digital filtering
(b) after digital filtering
(c) after calibration

TDD/FDD MODE ENHANCMENT OPTION

In both TDD and FDD mode the LMS7002M is capable of running from a single PLL, allowing one on chip PLL to be powered down. In TDD mode, a single PLL output drives both TX and RX mixers. In FDD mode, a single PLL drives both mixers as well, while UL/DL frequency separation is implemented in the digital domain using the NCO and complex mixer parts of the TSP block. The maximum frequency shift range which can be achieved in the digital domain is as below:

$$f_{TXLO} = f_{PLL} \pm 0.6 * f_{DAC} / 2$$
$$f_{RXLO} = f_{PLL} \pm 0.6 * f_{ADC} / 2 \text{ ,}$$

where f_{TXLO} and f_{RXLO} are effective TX and RX LO frequencies, f_{PLL} is the shared PLL output frequency while f_{DAC} and f_{ADC} are data converter sampling rates. Note that the Nyquist frequency of the NCOs is scaled by a factor of 0.6 to make space for TXLPF and RXLPF to operate.

Running the LMS7002M in single PLL mode has the following advantages:

- Current consumption is significantly reduced since one PLL is powered down.
- Fast TX<->RX switching time in TDD mode is achievable since the PLL does not need to relock.
- There is no TXVCO<->RXVCO polling issue since a single PLL is used.
- Using the digital domain for LO frequency shifts enables implementation of very fast frequency hopping systems.

IMPROVING FRACTIONAL-N CLOSE TO INTEGER RF SYNTHESISER SPURS PERFORMANCE

Due to PFD/CHP ‘dead zone’ i.e. nonlinearity around zero, fractional-N synthesisers are prone to generate unwanted spurs when set close to integer frequency. These spurs are unfortunately in the loop pass band and cannot be filtered. One of the solutions is to set constant charge pump current offset to shift PFD/CHP away from zero i.e. operating them into more linear region. However, this CHP offset value depends on how far PLL output frequency is away from the nearest integer frequency and has to be tuned accordingly.

Digital blocks can help this case. Set charge pump offset current to some middle value and keep it constant disregarding how far close to integer frequency is away from integer frequency. Offset PLL wanted frequency away enough from integer frequency in order not to have close to integer spurs issue. This introduces PLL output frequency error which can be corrected by corresponding NCO available in the digital TSP block.

PACKAGE OUTLINE AND PIN DESCRIPTION

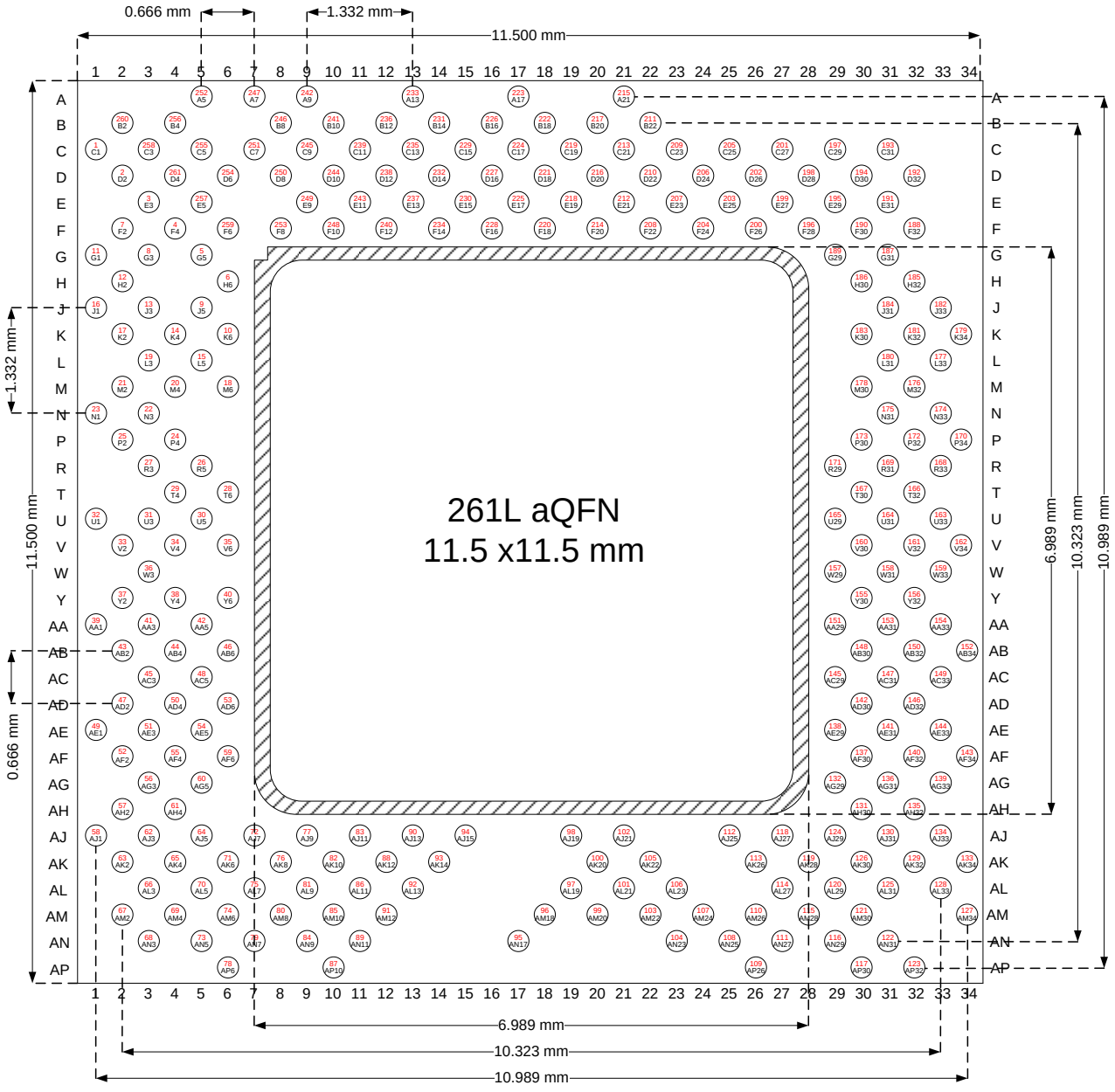


Figure 52: 261L aQFN package (top view)

Pin No	Pin ID	Pin Name	Type	Description	Notes
1	C1	UNUSED	-	-	
2	D2	UNUSED	-	-	
3	E3	UNUSED	-	-	
4	F4	UNUSED	-	-	
5	G5	VDD12_TXBUF	analog supply	1.25V supply – TX XOSC buffer	
6	H6	VDD18_TXBUF	analog supply	1.8V supply – TX XOSC buffer	
7	F2	UNUSED	-	-	
8	G3	VDD18_VCO_SXT	analog supply	1.8V supply – TX SX VCO	
9	J5	VDD12O_VCO_SXT	analog supply	1.25V supply – TX SX VCO	
10	K6	VDD12_VCO_SXT	analog supply	1.25V supply – TX SX VCO	
11	G1	UNUSED	-	-	
12	H2	GND_VCO_SXT	analog gnd	GND – TX SX VCO	
13	J3	VDD_CP_SXT	analog supply	1.25V supply – TX SX Charge pump	
14	K4	GND_CP_SXT	analog gnd	GND – TX SX Charge pump	
15	L5	VDD_DIV_SXT	analog supply	1.25V supply – TX SX frequency divider	
16	J1	UNUSED	-	-	
17	K2	VDDO_DIV_SXT	analog supply	1.25V supply – TX SX frequency divider	
18	M6	UNUSED	-	-	
19	L3	GND_DIV_SXT	analog gnd	GND – TX SX frequency divider	
20	M4	DVDD_SXT	digital supply	1.25V supply – digital supply for TX SX	
21	M2	UNUSED	-	-	
22	N3	DGND_SXT	digital gnd	GND – digital supply for TX SX	
23	N1	VDD18_LDO_TX	analog supply	1.8V supply – TX LDO	
24	P4	VDD_TBB	analog supply	1.25V supply – TX baseband	
25	P2	tbbqn_pad_1	in	TX change input pad to externally drive the TX BB Channel 1	
26	R5	tbbin_pad_1	in	TX change input pad to externally drive the TX BB Channel 1	
27	R3	tbbqp_pad_1	in	TX change input pad to externally drive the TX BB Channel 1	
28	T6	tbbin_pad_2	in	TX change input pad to externally drive the TX BB Channel 2	
29	T4	tbbip_pad_1	in	TX change input pad to externally drive the TX BB Channel 1	
30	U5	adcin_in_1	in	ADC input pads – To use external filtering Channel 1	
31	U3	tbbqp_pad_2	in	TX change input pad to externally drive the TX BB Channel 2	
32	U1	tbbqn_pad_2	in	TX change input pad to externally drive the TX BB Channel 2	
33	V2	tbbip_pad_2	in	TX change input pad to externally drive the TX BB Channel 2	
34	V4	adcin_ip_1	in	ADC input pads – To use external filtering Channel 1	
35	V6	adcin_in_2	in	ADC input pads – To use external filtering Channel 2	
36	W3	adcin_qn_1	in	ADC 21nput pads – To use external filtering Channel 1	
37	Y2	adcin_qp_1	in	ADC input pads – To use external filtering Channel 1	
38	Y4	adcin_qn_2	in	ADC input pads – To use external filtering Channel 2	
39	AA1	adcin_ip_2	in	ADC input pads – To use external filtering Channel 2	
40	Y6	rbbip_pad_1	out	RX BB output – To use external filtering Channel 1	
41	AA3	adcin_qp_2	in	ADC input pads – To use external filtering Channel 2	
42	AA5	rbbqn_pad_1	out	RX BB output – To use external filtering Channel 1	
43	AB2	rbbin_pad_1	out	RX BB output – To use external filtering Channel 1	
44	AB4	rbbqp_pad_1	out	RX BB output – To use external filtering Channel 1	
45	AC3	rbbin_pad_2	out	RX BB output – To use external filtering Channel 2	
46	AB6	rbbqn_pad_2	out	RX BB output – To use external filtering Channel 2	
47	AD2	rbbip_pad_2	out	RX BB output – To use external filtering Channel 2	
48	AC5	rbbqp_pad_2	out	RX BB output – To use external filtering Channel 2	
49	AE1	UNUSED	-	-	
50	AD4	VDD14_RBB	analog supply	1.4V supply- RX baseband	
51	AE3	VDD18_TIA_RFE	analog supply	1.8V supply- RXFE TIA	
52	AF2	VDD14_TIA_RFE	analog supply	1.4V supply- RXFE TIA	
53	AD6	VDD12_TIA_RFE	analog supply	1.25V supply- RXFE TIA	
54	AE5	UNUSED	-	-	
55	AF4	VDD18_LDO_RX	analog supply	1.8V supply- RX LDO	
56	AG3	UNUSED	-	-	
57	AH2	UNUSED	-	-	
58	AJ1	UNUSED	-	-	
59	AF6	VDD14_LNA_RFE	analog supply	1.4V supply- RXFE LNA	
60	AG5	VDD12_LNA_RFE	analog supply	1.25V supply- RXFE LNA	
61	AH4	UNUSED	-	-	
62	AJ3	UNUSED	-	-	
63	AK2	UNUSED	-	-	
64	AJ5	UNUSED	-	-	
65	AK4	UNUSED	-	-	
66	AL3	UNUSED	-	-	
67	AM2	UNUSED	-	-	
68	AN3	rfgp_w_RFE_2	in	LNA input gate Wideband LNA – Gate : Channel 2	
69	AM4	rfgn_w_RFE_2	in	LNA input gate Wideband LNA – Gate : Channel 2	

Table 12 Pin descriptions

Pin No	Pin ID	Pin Name	Type	Description	Notes
70	AL5	UNUSED	-	-	
71	AK6	UNUSED	-	-	
72	AJ7	rfsn_l_RFE_2	in/out	LNA Lowband LNA – Source: Channel 2	
73	AN5	rfgp_l_RFE_2	in	LNA input gate Lowband LNA – Gate : Channel 2	
74	AM6	UNUSED	-	-	
75	AL7	UNUSED	-	-	
76	AK8	UNUSED	-	-	
77	AJ9	rfsp_l_RFE_2	in/out	LNA Lowband LNA – Source : Channel 2	
78	AP6	rfgn_l_RFE_2	in	LNA input gate Lowband LNA – Gate : Channel 2	
79	AN7	rfgp_h_RFE_2	in	LNA input gate Highband LNA – Gate : Channel 2	
80	AM8	rfgn_h_RFE_2	in	LNA input gate Highband LNA – Gate : Channel 2	
81	AL9	UNUSED	-	-	
82	AK10	UNUSED	-	-	
83	AJ11	UNUSED	-	-	
84	AN9	rfgp_w_RFE_1	in	LNA input gate Wideband LNA – Gate : Channel 1	
85	AM10	UNUSED	-	-	
86	AL11	UNUSED	-	-	
87	AP10	rfgn_w_RFE_1	in	LNA input gate Wideband LNA – Gate : Channel 1	
88	AK12	rfsn_l_RFE_1	in/out	LNA Lowband LNA – Source : Channel 1	
89	AN11	rfgp_l_RFE_1	in	LNA input gate Lowband LNA – Gate : Channel 1	
90	AJ13	UNUSED	-	-	
91	AM12	rfgn_l_RFE_1	in	LNA input gate Lowband LNA – Gate : Channel 1	
92	AL13	rfsp_l_RFE_1	in/out	LNA Lowband LNA – Source : Channel 1	
93	AK14	rfgp_h_RFE_1	in	LNA input gate Highband LNA – Gate : Channel 1	
94	AJ15	rfgn_h_RFE_1	in	LNA input gate Highband LNA – Gate : Channel 1	
95	AN17	VDD_MXLOBUF_RFE	analog supply	1.25V supply: RX LO buffers	
96	AM18	VDD18_SXR	analog supply	1.8V supply: RX SX	
97	AL19	VDD_CP_SXR	analog supply	1.25V supply: RX SX Charge pump	
98	AJ19	GND_CP_SXR	analog gnd	GND: RX SX Charge pump	
99	AM20	VDD_DIV_SXR	analog supply	1.25V supply: RX SX frequency divider	
100	AK20	GND_DIV_SXR	analog gnd	GND: RX SX frequency divider	
101	AL21	DVDD_SXR	digital supply	1.25V digital supply: RX SX f	
102	AJ21	UNUSED	-	-	
103	AM22	DGND_SXR	digital gnd	GND: RX SX	
104	AN23	VDD12_VCO_SXR	analog supply	1.25V supply: RX SX	
105	AK22	VDD18_VCO_SXR	analog supply	1.8V supply: RX SX	
106	AL23	GND_VCO_SXR	analog gnd	GND: RX SX VCO	
107	AM24	xoscin_rx	in		
108	AN25	GND_RXBUF	analog gnd	GND – RX XOSC buffer	
109	AP26	VDD12_RXBUF	analog supply	1.25V supply – RX XOSC buffer	
110	AM26	VDD18_RXBUF	analog supply	1.8V supply – RX XOSC buffer	
111	AN27	UNUSED	-	-	
112	AJ25	VDD_AFE	analog supply	1.25V supply – ADC/DAC	
113	AK26	UNUSED	-	-	
114	AL27	UNUSED	-	-	
115	AM28	UNUSED	-	-	
116	AN29	UNUSED	-	-	
117	AP30	UNUSED	-	-	
118	AJ27	UNUSED	-	-	
119	AK28	UNUSED	-	-	
120	AL29	UNUSED	-	-	
121	AM30	UNUSED	-	-	
122	AN31	UNUSED	-	-	
123	AP32	UNUSED	-	-	
124	AJ29	UNUSED	-	-	
125	AL31	UNUSED	-	-	
126	AK30	UNUSED	-	-	
127	AM34	UNUSED	-	-	
128	AL33	UNUSED	-	-	
129	AK32	UNUSED	-	-	
130	AJ31	UNUSED	-	-	
131	AH30	DIGPRVDD2	DVDD	Digital Pad Ring power supply for post-driver	
132	AG29	DIGPRGND1	pad gnd	Digital Pad Ring ground for pre-driver	
133	AK34	UNUSED	-	-	
134	AJ33	UNUSED	-	-	
135	AH32	UNUSED	-	-	
136	AG31	DIQ1_D0	IO_cmos1225	DIQ bus, bit 0. LML Port 1	
137	AF30	DIQ1_D1	IO_cmos1225	DIQ bus, bit 1. LML Port 1	
138	AE29	DIGPRVDD1	DVDD	Digital Pad Ring power supply for pre-driver	

Table 13: Pin descriptions (continued)

Pin No	Pin ID	Pin Name	Type	Description	Notes
139	AG33	UNUSED	-	-	
140	AF32	DIGPRGND2	pad gnd	Digital Pad Ring ground for post-driver	
141	AE31	DIQ1_D3	IO_cmos1225	DIQ bus, bit 3. LML Port 1	
142	AD30	DIQ1_D4	IO_cmos1225	DIQ bus, bit 4. LML Port 1	
143	AF34	DIQ1_D2	IO_cmos1225	DIQ bus, bit 2. LML Port 1	
144	AE33	DIQ1_D6	IO_cmos1225	DIQ bus, bit 6. LML Port 1	
145	AC29	DIQ1_D5	IO_cmos1225	DIQ bus, bit 5. LML Port 1	
146	AD32	DIQ1_D7	IO_cmos1225	DIQ bus, bit 7. LML Port 1	
147	AC31	DIQ1_D8	IO_cmos1225	DIQ bus, bit 8. LML Port 1	
148	AB30	DIQ1_D10	IO_cmos1225	DIQ bus, bit 10. LML Port 1	
149	AC33	DIQ1_D9	IO_cmos1225	DIQ bus, bit 9. LML Port 1	
150	AB32	DIQ1_D11	IO_cmos1225	DIQ bus, bit 11. LML Port 1	
151	AA29	DIGPRVDD1	DVDD	Digital Pad Ring power supply for pre-driver	
152	AB34	MCLK1	out_cmos1225	Clock from RFIC to BBIC in JESD207 mode. LML Port 1	
153	AA31	DIGPRGND1	DGND	Digital Pad Ring ground for pre-driver	
154	AA33	FCLK1	in_cmos1225	Clock from BBIC to RFIC in JESD207 mode. LML Port 1	
155	Y30	DIGPRGND2	pad gnd	Digital Pad Ring ground for post-driver	
156	Y32	ENABLE_IQSEL1	IO_cmos1225	IQ flag in RXTXIQ mode; enable flag in JESD207 mode. LML Port 1	
157	W29	DIGPRGND1	pad gnd	Digital Pad Ring ground for pre-driver	
158	W31	DIGPRPOC	POC	POC circuit	
159	W33	DIGPRVDD2	DVDD	Digital Pad Ring power supply for post-driver	
160	V30	LOGIC_RESET	analog supply/gnd	Not used	
161	V32	TXNRX1	in_cmos1225	IQ data protocol control in JESD207 mode. LML Port 1	
162	V34	RXEN	in_cmos1225	RX hard power off	
163	U33	CORE_LDO_EN	analog supply/gnd	External enable control signal for the internal LDO's.	Should be fixed to analog supply if internal LDO's are used. Should be fixed to analog gnd if internal LDO's are NOT used.
164	U31	TXNRX2	in_cmos1225	IQ data protocol control in JESD207 mode. LML Port 2	
165	U29	TXEN	in_cmos1225	TX hard power off	
166	T32	DIGPRVDD2, DIGPRPOC	DVDD	Digital Pad Ring power supply for post-driver and POC	
167	T30	DIGPRGND1, DIGPRGND2	pad gnd	Digital Pad Ring ground for pre-driver and post-driver	
168	R33	ENABLE_ IQSEL2	IO_cmos1225	IQ flag in RXTXIQ mode; enable flag in JESD207 mode. LML Port 2	
169	R31	DIGPRVDD1	DVDD	Digital Pad Ring power supply for pre-driver	
170	P34	MCLK2	out_cmos1225	Clock from RFIC to BBIC in JESD207 mode. LML Port 2	
171	R29	FCLK2	in_cmos1225	Clock from BBIC to RFIC in JESD207 mode. LML Port 2	
172	P32	DIQ2_D11	IO_cmos1225	DIQ bus, bit 11. LML Port 2	
173	P30	DIQ2_D10	IO_cmos1225	DIQ bus, bit 10. LML Port 2	
174	N33	DIQ2_D9	IO_cmos1225	DIQ bus, bit 9. LML Port 2	
175	N31	DIQ2_D8	IO_cmos1225	DIQ bus, bit 8. LML Port 2	
176	M32	DIQ2_D7	IO_cmos1225	DIQ bus, bit 7. LML Port 2	
177	L33	DIGPRVDD1	DVDD	Digital Pad Ring power supply for pre-driver	
178	M30	DIQ2_D6	IO_cmos1225	DIQ bus, bit 6. LML Port 2	
179	K34	DIQ2_D5	IO_cmos1225	DIQ bus, bit 5. LML Port 2	
180	L31	DIQ2_D4	IO_cmos1225	DIQ bus, bit 4. LML Port 2	
181	K32	DIQ2_D3	IO_cmos1225	DIQ bus, bit 3. LML Port 2	
182	J33	DIGPRGND1	DGND	Digital Pad Ring ground for pre-driver	
183	K30	DIQ2_D2	IO_cmos1225	DIQ bus, bit 2. LML Port 2	
184	J31	DIQ2_D1	IO_cmos1225	DIQ bus, bit 1. LML Port 2	
185	H32	DIGPRVDD2	DVDD	Digital Pad Ring supply for post-driver	
186	H30	DIQ2_D0	IO_cmos1225	DIQ bus, bit 0. LML Port 2	
187	G31	DIGPRGND2	pad gnd	Digital Pad Ring ground for post-driver	
188	F32	UNUSED	-	-	
189	G29	UNUSED	-	-	
190	F30	SDIO	IO_cmos1225	Serial port data input-output in 3 wire mode, Serial port data input in 4 wire mode, CMOS	
191	E31	UNUSED	-	-	
192	D32	UNUSED	-	-	
193	C31	UNUSED	-	-	
194	D30	UNUSED	-	-	
195	E29	UNUSED	-	-	
196	F28	SDO	out_cmos1225	Serial port data output, CMOS	
197	C29	SCLK	in_cmos1225	Serial port clock, positive edge sensitive, CMOS	
198	D28	SEN	in_cmos1225	Serial port enable, active low, CMOS	
199	E27	RESET	in_cmos1225	Hardware reset, active low, CMOS level	
200	F26	UNUSED	-	-	
201	C27	SCL	IO_cmos1225	uControler	
202	D26	SDA	IO_cmos1225	uControler	
203	E25	GND_SPI_BUF	digital gnd	GND – SPI buffer	
204	F24	VDD_SPI_BUF	digital supply	1.25V supply – SPI buffer	

Table 14: Pin descriptions (continued)

Pin No	Pin ID	Pin Name	Type	Description	Notes
205	C25	VDD12_DIG	digital supply	output 1.2V supply for digital LDO	
206	D24	VDD18_DIG	digital supply	1.8V supply for digital LDO	
207	E23	UNUSED	-	-	
208	F22	tstdo<1>	out_cmos1225	digital output test pin	
209	C23	GND_DIG	digital gnd	GND for the digital LDO	
210	D22	tstdo<0>	out_cmos1225	digital output test pin	
211	B22	tstao	out_cmos1225	analog test pin	
212	E21	VDD18_VCO_CGEN	analog supply	1.8V supply – VCO CLKGEN	
213	C21	VDD14_VCO_CGEN	analog supply	1.4V supply – VCO CLKGEN	
214	F20	VDD_CP_CGEN	analog supply	1.25V supply – Charge Pump – CLKGEN	
215	A21	UNUSED	-	-	
216	D20	GND_DIV_CGEN	analog gnd	GND –frequency divider – CLKGEN	
217	B20	GND_CP_CGEN	analog gnd	GND –Charge Pump – CLKGEN	
218	E19	VDD_DIV_CGEN	analog supply	1.25V supply – frequency divider – CLKGEN	
219	C19	UNUSED	-	-	
220	F18	vr_rext	in	external 10 kOhm accurate reference resistor	
221	D18	UNUSED	-	-	
222	B18	DGND_CGEN	digital gnd	GND – CLKGEN	
223	A17	DVDD_CGEN	digital supply	1.25V supply- Digital supply for CLK GEN	
224	C17	UNUSED	-	-	
225	E17	VDD18_BIAS	analog supply	1.8V supply – Bias	
226	B16	VDD_TPAD_TRF	analog supply	1.25V supply – TX PAD	
227	D16	VDD18_TRF	analog supply	1.8V supply – TX RF	
228	F16	UNUSED	-	-	
229	C15	UNUSED	-	-	
230	E15	UNUSED	-	-	
231	B14	pa2on_2	out	PA driver output RF pad PAD2, Channel 2	
232	D14	UNUSED	-	-	
233	A13	pa2op_2	out	PA driver output RF pad PAD2, Channel 2	
234	F14	UNUSED	-	-	
235	C13	UNUSED	-	-	
236	B12	pa1op_2	out	PA driver output RF pad PAD1, Channel 2	
237	E13	UNUSED	-	-	
238	D12	UNUSED	-	-	
239	C11	pa1on_2	out	PA driver output RF pad PAD1, Channel 2	
240	F12	UNUSED	-	-	
241	B10	pa2on_1	out	PA driver output RF pad PAD2, Channel 1	
242	A9	pa2op_1	out	PA driver output RF pad PAD2, Channel 1	
243	E11	UNUSED	-	-	
244	D10	UNUSED	-	-	
245	C9	UNUSED	-	-	
246	B8	pa1op_1	out	PA driver output RF pad PAD1, Channel 1	
247	A7	pa1on_1	out	PA driver output RF pad PAD1, Channel 1	
248	F10	UNUSED	-	-	
249	E9	UNUSED	-	-	
250	D8	UNUSED	-	-	
251	C7	GND_TLOBUF_TRF	analog gnd	Ground for TX LO buffers	
252	A5	UNUSED	-	-	
253	F8	VDD_TLOBUF_TRF	analog supply	1.25V supply – TX LO BUFFER	
254	D6	VDDO_TLOBUF_TRF	analog supply		
255	C5	UNUSED	-	-	
256	B4	UNUSED	-	-	
257	E5	xoscin_tx	in	TX XOSC buffer input	
258	C3	UNUSED	-	-	
259	F6	GND_TXBUF	analog gnd	GND supply – TX XOSC buffer	
260	B2	UNUSED	-	-	
261	D4	UNUSED	-	-	

Table 15: Pin descriptions (continued)

TYPICAL APPLICATION

RF Section Example

A typical application circuit of the LMS7002M is given in *Figure 53*. Note that only the RF part of a single MIMO TRX chain is shown. More details can be found in the LMS7002M evaluation board schematics.

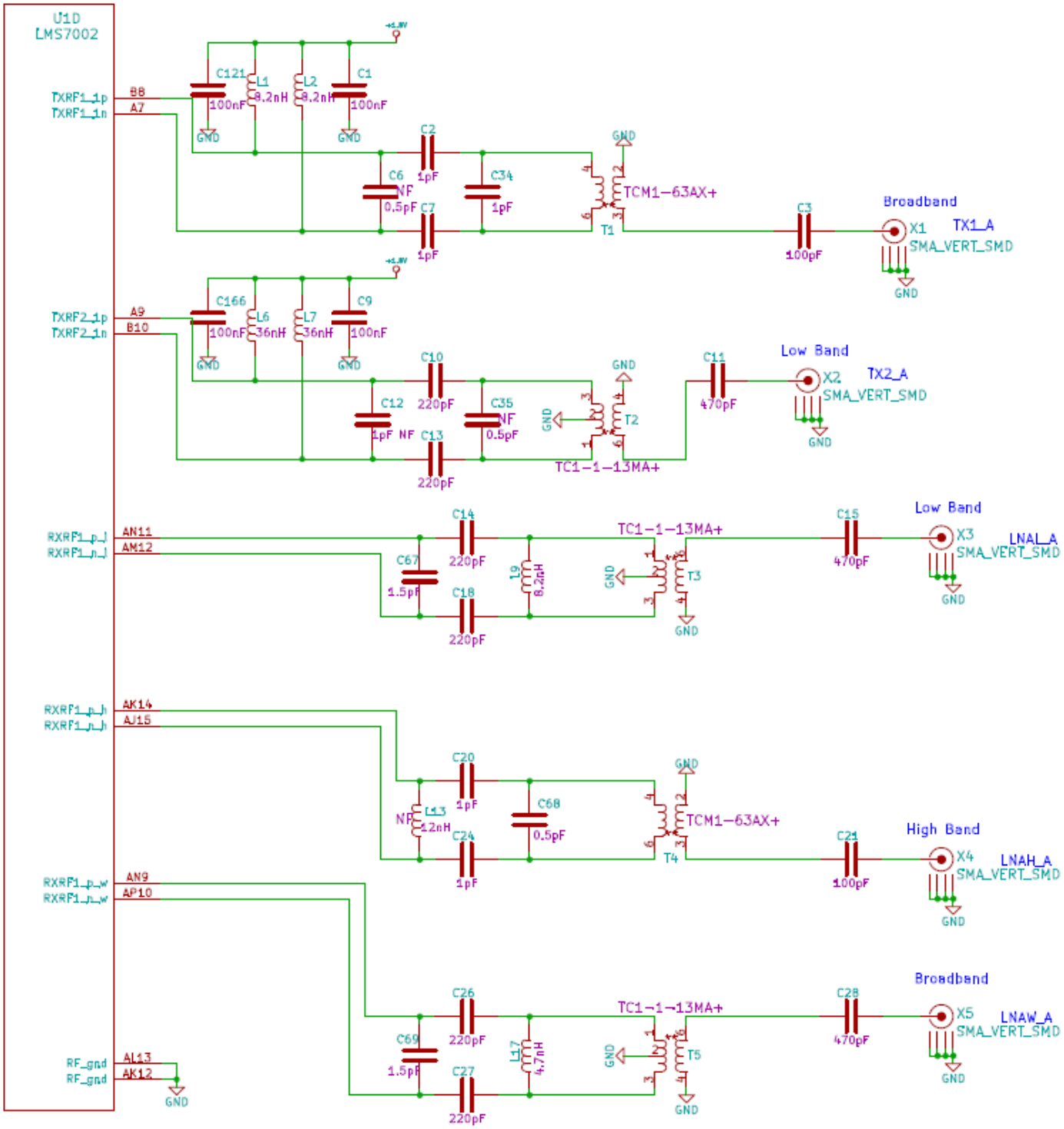


Figure 53: Typical RF application circuit

Digital Interface Configuration Example

Figure 54 shows one useful example of clock generation and distribution as well as interfacing LMS7002M to digital BB modem. Note that interface control signals such as ENABLE, TXNRX, IQSEL are not shown for clarity. As can be seen, CLKPLL block generates 491.52MHz (integer multiple of 61.44MHz) clock. CLKPLL output is divided by programmable divider (division set to 4 in this example) to construct 122.88MHz clock driving DACs, TXTSP and TX part of LimeLight™. Similarly, CLKPLL output is divided by fixed division of 4 to construct 122.88MHz clock driving ADCs, RXTSP and RX part of LimeLight™. Interpolation and decimation are both set to 2. Hence, the configuration provides 245.76MS/s double data rate (DDR) interface to BB modem. This translates into the overall system performance as below:

- TX/RX IF bandwidth: 20MHz
- TX/RX RF bandwidth: 40MHz
- Digital interpolation image suppression: 60dB
- DACs analog image suppression: 72dB
- ADCs analog alias suppression: 43dB assuming no off chip filtering
- Digital decimation alias suppression: 60dB

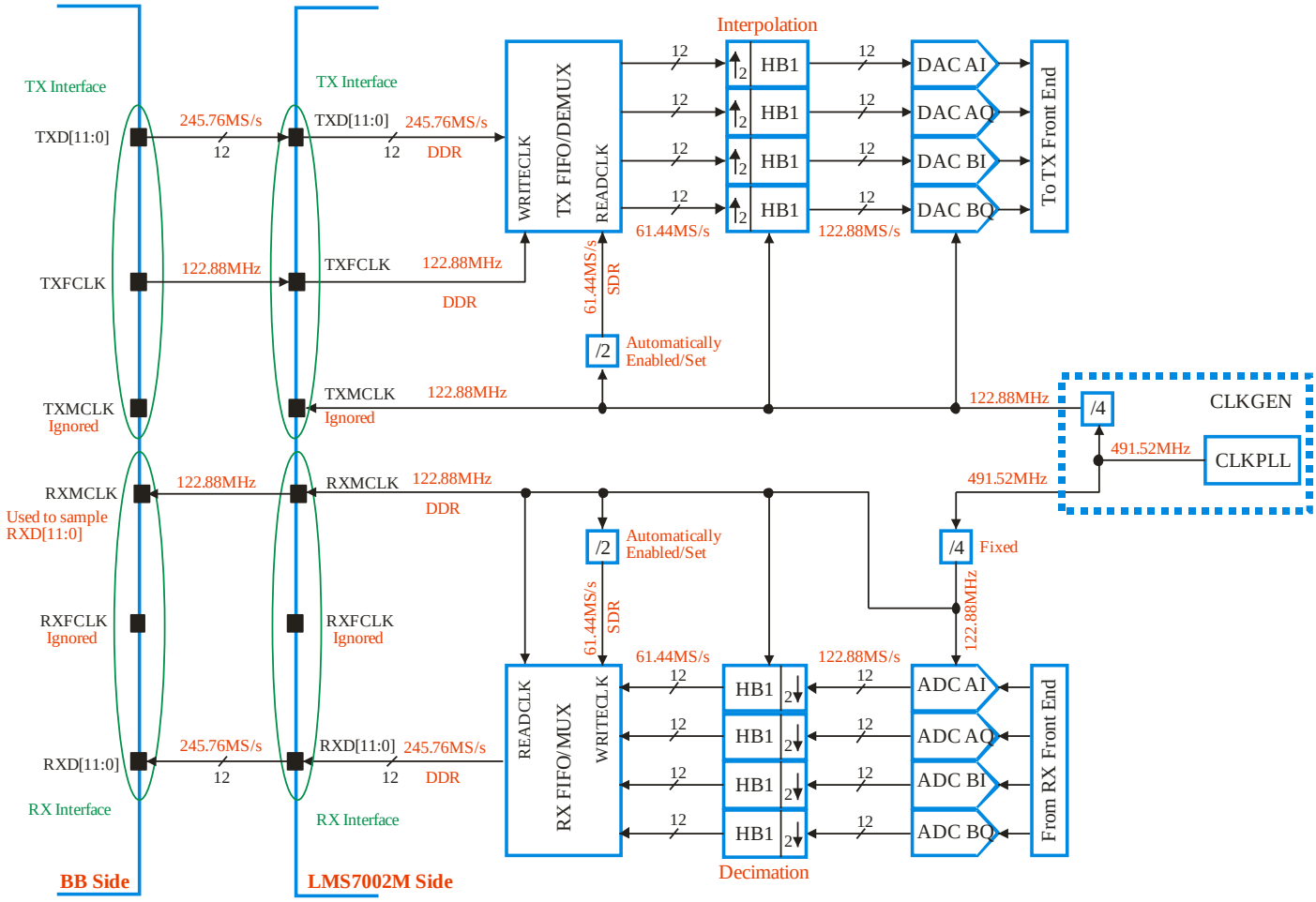


Figure 54: Digital interface setup