

# LSF0108-Q100

8-bit bidirectional multi-voltage level translator; open-drain;  
push-pull

Rev. 2 — 30 July 2020

Product data sheet

## 1. General description

The LSF0108-Q100 is an 8 Channel bidirectional multi-voltage level translator for open-drain and push-pull applications. It supports up to 100 MHz up translation and  $\geq 100$  MHz down translation at  $\leq 30$  pF capacitive load. There is no need for a direction pin which minimizes system effort.

The LSF0108-Q100 supports 5 V tolerant I/O pins for compatibility with TTL levels in a variety of applications. The ability to set up different voltage translation levels on each channel makes the device very flexible and suitable for a lot of different applications.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from  $-40$  °C to  $+125$  °C
- Bidirectional voltage translation with no direction pin
- Up translation
  - $\leq 100$  MHz;  $C_L = 30$  pF
  - $\leq 40$  MHz;  $C_L = 50$  pF
- Down translation
  - $\geq 100$  MHz;  $C_L = 30$  pF
  - $\leq 40$  MHz;  $C_L = 50$  pF
- Hot insertion
- Bidirectional voltage level translation between:
  - 0.95 V and 1.8 V, 2.5 V, 3.3 V and 5.0 V
  - 1.2 V and 1.8 V, 2.5 V, 3.3 V and 5.0 V
  - 1.8 V and 2.5 V, 3.3 V and 5.0 V
  - 2.5 V and 3.3 V and 5.0 V
  - 3.3 V and 5.0 V
- Low standby current
- 5 V tolerant I/O pins to support TTL
- Low  $R_{ON}$  provides less signal distortion
- High-impedance I/O pins for  $EN = Low$ .
- Flow-through pinout for easy PCB trace routing.
- Latch-up performance exceeds 100 mA per JESD78 class II level A
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 exceeds 2000 V
  - CDM ANSI/ESDA/JEDEC JS-002 exceeds 1000 V
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

### 3. Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I<sup>2</sup>C, and other interfaces in Telecom infrastructure
- Industrial
- Personal computing
- Automotive

### 4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
LSF0108PW-Q100	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
LSF0108BQ-Q100	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

### 5. Functional diagram

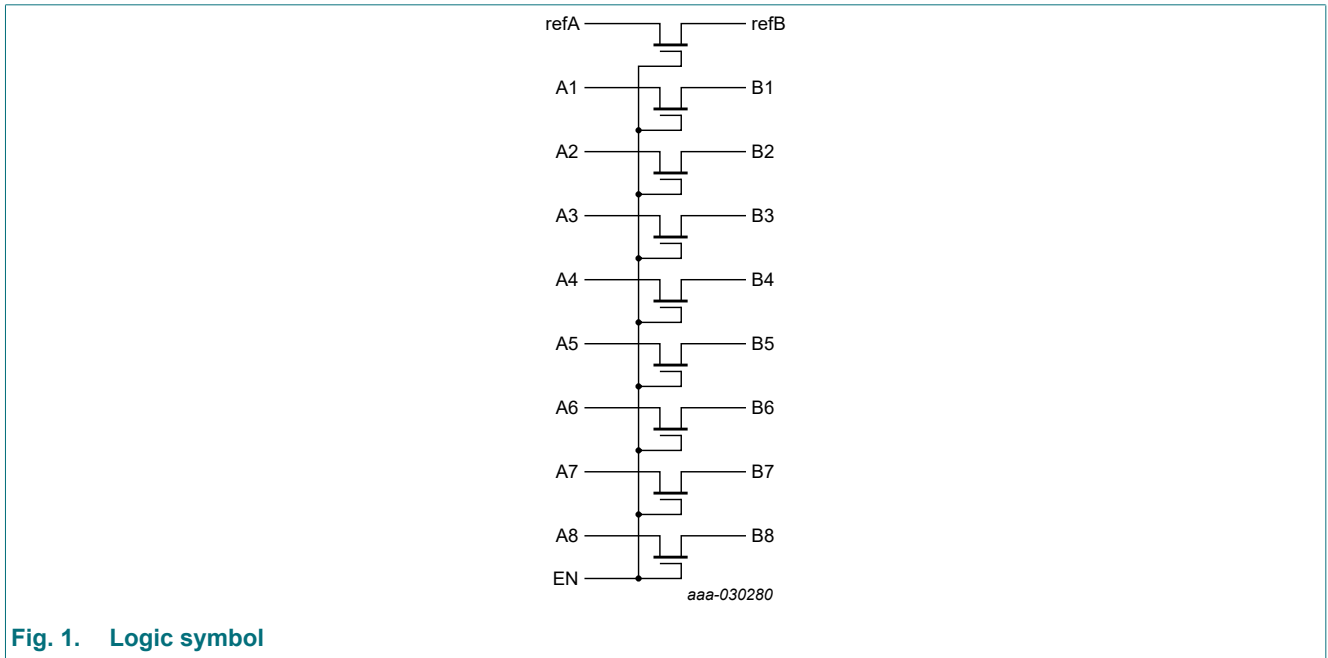
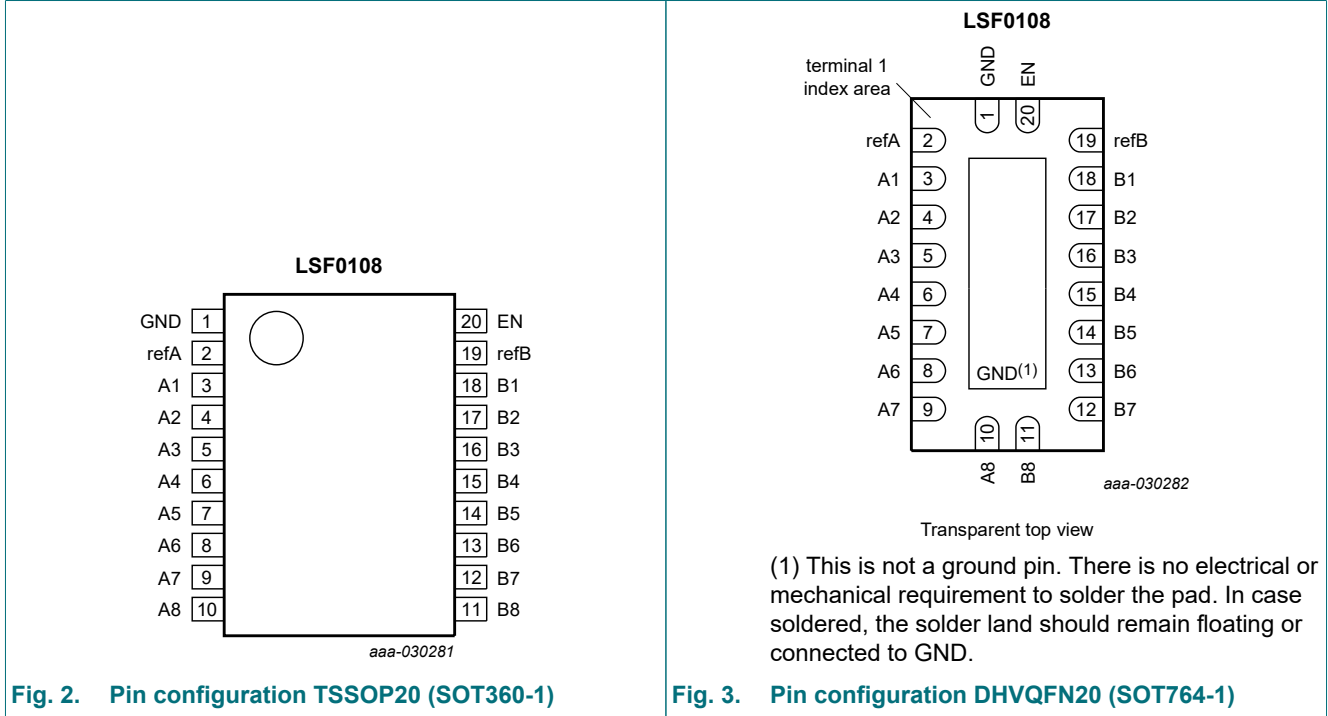


Fig. 1. Logic symbol

## 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
GND	1	ground (0 V)
refA	2	reference voltage A
A1, A2, A3, A4, A5, A6, A7, A8	3, 4, 5, 6, 7, 8, 9, 10	data input/output A
B1, B2, B3, B4, B5, B6, B7, B8	18, 17, 16, 15, 14, 13, 12, 11	data input/output B
refB	19	reference voltage B
EN	20	enable input (active HIGH)

## 7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	input/output
EN	An, Bn channel
H	An = Bn
L	Z

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_I$	input voltage	pins refA, refB, An, Bn and EN [1]	-0.5	+7.0	V
$I_{I/O}$	input/output current	pins refA, refB, An and Bn; continuous channel current	-	+128	mA
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	[2]	-	500	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] For SOT360-1 (TSSOP20) package:  $P_{tot}$  derates linearly with 10.0 mW/K above 100 °C.  
For SOT764-1 (DHVQFN20) package:  $P_{tot}$  derates linearly with 12.9 mW/K above 111 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_I$	input voltage	pins refA, refB, An, Bn and EN	0.0	5.0	V
$I_{I/O}$	input/output current	pins refA, refB, An and Bn; continuous channel current	-	+64	mA
$T_{amb}$	ambient temperature		-40	+125	°C

## 10. Static characteristics

**Table 6. Static characteristics**

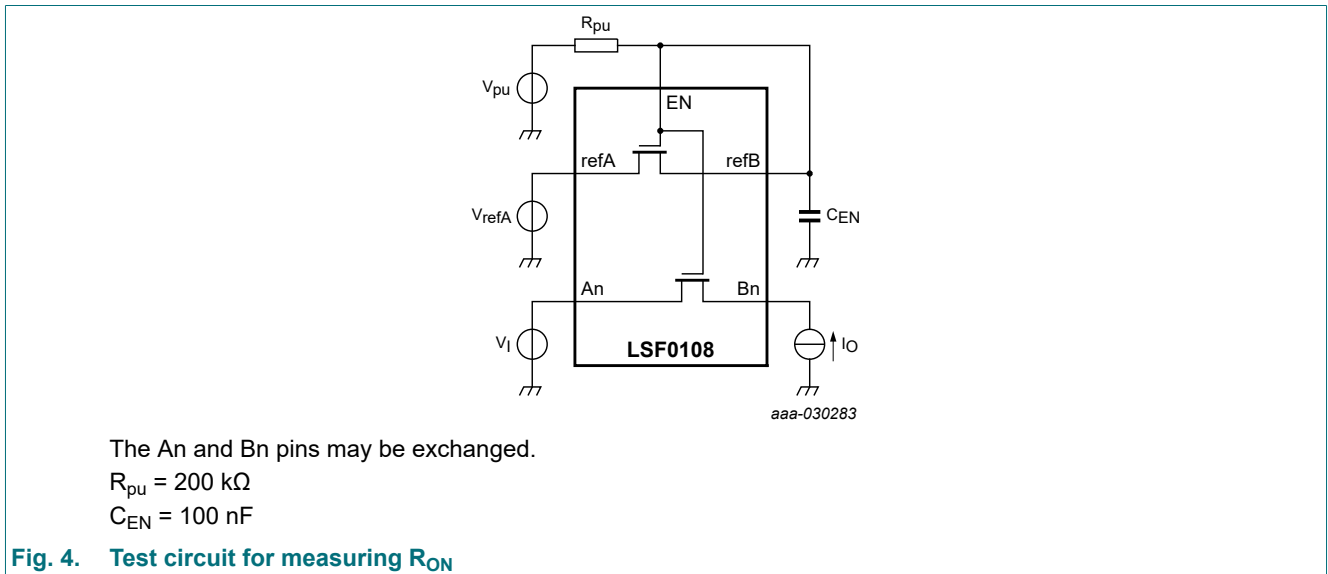
At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = -40$ °C to $+125$ °C			Unit
			Min	Typ[1]	Max	
$V_{IK}$	input clamping voltage	$V_{EN} = 0$ V; $I_I = -18$ mA	-1.2	-	-	V
$I_I$	leakage current	pins An, Bn, refA, refB and EN; $V_I =$ GND to 5.0 V	-	1	5	μA
$C_I$	input capacitance	pins refA, refB and EN; $V_I = 0$ V or 3 V	-	11	-	pF
$C_{io(off)}$	OFF-state input/output capacitance	pins An, Bn; $V_O = 0$ V or 3 V; $V_{EN} = 0.0$ V	-	2.6	6.0	pF
$C_{io(on)}$	ON-state input/output capacitance	pins An, Bn; $V_O = 0$ V or 3 V; $V_{EN} = 3.0$ V	-	5.3	12.5	pF

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Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
R <sub>ON</sub>	ON resistance	see Fig. 4 [2]				
		V <sub>I</sub> = 0 V; V <sub>pu</sub> = 5.0 V; I <sub>O</sub> = 64 mA				
		V <sub>refA</sub> = 3.3 V	-	3	-	Ω
		V <sub>refA</sub> = 1.8 V	-	4	-	Ω
		V <sub>refA</sub> = 1.0 V	-	7	-	Ω
		V <sub>I</sub> = 0 V; V <sub>pu</sub> = 5.0 V; I <sub>O</sub> = 32mA				
		V <sub>refA</sub> = 1.8 V	-	4	-	Ω
		V <sub>refA</sub> = 2.5 V	-	3	-	Ω
		V <sub>I</sub> = 1.8 V; V <sub>pu</sub> = 5.0 V; I <sub>O</sub> = 15 mA				
		V <sub>refA</sub> = 3.3 V	-	4	-	Ω
		V <sub>I</sub> = 1.0 V; V <sub>pu</sub> = 3.3 V; I <sub>O</sub> = 10 mA				
		V <sub>refA</sub> = 1.8 V	-	7	-	Ω
		V <sub>I</sub> = 0 V; V <sub>pu</sub> = 3.3 V; I <sub>O</sub> = 10 mA				
		V <sub>refA</sub> = 1.0 V	-	5	-	Ω
V <sub>I</sub> = 0 V; V <sub>pu</sub> = 1.8 V; I <sub>O</sub> = 10 mA						
V <sub>refA</sub> = 1.0 V	-	6	-	Ω		

- [1] All typical values are measured at T<sub>amb</sub> = 25 °C.
- [2] Measured by the voltage drop between the An and Bn pins at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (An or Bn) pins.



## 11. Dynamic characteristics

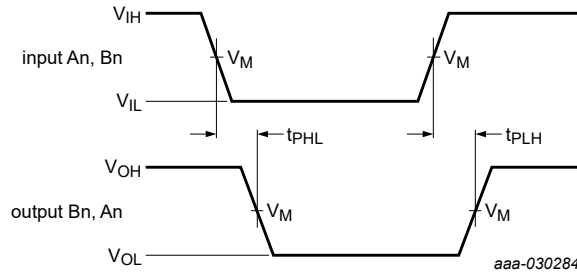
**Table 7. Switching characteristics**

$GND = 0\text{ V}$ ; for waveform see Fig. 5; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+125\text{ °C}$			Unit
			Min	Typ [1]	Max	
<b>Translating down</b>						
$t_{PLH}$	LOW to HIGH propagation delay	An to Bn or Bn to An; $V_{IH} = V_{pu} = V_{refA} + 1\text{ V}$				
		$V_{refA} = 1.5\text{ V}$ ; $C_L = 15\text{ pF}$	-	0.8	-	ns
		$V_{refA} = 1.5\text{ V}$ ; $C_L = 30\text{ pF}$	-	1.45	-	ns
		$V_{refA} = 1.5\text{ V}$ ; $C_L = 50\text{ pF}$	-	2.0	-	ns
		$V_{refA} = 2.3\text{ V}$ ; $C_L = 15\text{ pF}$	-	0.75	-	ns
		$V_{refA} = 2.3\text{ V}$ ; $C_L = 30\text{ pF}$	-	1.4	-	ns
		$V_{refA} = 2.3\text{ V}$ ; $C_L = 50\text{ pF}$	-	1.9	-	ns
$t_{PHL}$	HIGH to LOW propagation delay	An to Bn or Bn to An; $V_{IH} = V_{pu} = V_{refA} + 1\text{ V}$				
		$V_{refA} = 1.5\text{ V}$ ; $C_L = 15\text{ pF}$	-	0.9	-	ns
		$V_{refA} = 1.5\text{ V}$ ; $C_L = 30\text{ pF}$	-	1.55	-	ns
		$V_{refA} = 1.5\text{ V}$ ; $C_L = 50\text{ pF}$	-	2.1	-	ns
		$V_{refA} = 2.3\text{ V}$ ; $C_L = 15\text{ pF}$	-	0.85	-	ns
		$V_{refA} = 2.3\text{ V}$ ; $C_L = 30\text{ pF}$	-	1.5	-	ns
		$V_{refA} = 2.3\text{ V}$ ; $C_L = 50\text{ pF}$	-	2.0	-	ns
<b>Translating up</b>						
$t_{PLH}$	LOW to HIGH propagation delay	An to Bn or Bn to An; $V_{IH} = V_{refA}$ ; $V_{EXT} = V_{pu} = V_{refA} + 1\text{ V}$				
		$V_{refA} = 1.5\text{ V}$ ; $C_L = 15\text{ pF}$	-	0.8	-	ns
		$V_{refA} = 1.5\text{ V}$ ; $C_L = 30\text{ pF}$	-	1.35	-	ns
		$V_{refA} = 1.5\text{ V}$ ; $C_L = 50\text{ pF}$	-	1.8	-	ns
		$V_{refA} = 2.3\text{ V}$ ; $C_L = 15\text{ pF}$	-	0.9	-	ns
		$V_{refA} = 2.3\text{ V}$ ; $C_L = 30\text{ pF}$	-	1.55	-	ns
		$V_{refA} = 2.3\text{ V}$ ; $C_L = 50\text{ pF}$	-	2.1	-	ns
$t_{PHL}$	HIGH to LOW propagation delay	An to Bn or Bn to An; $V_{IH} = V_{refA}$ ; $V_{EXT} = V_{pu} = V_{refA} + 1\text{ V}$				
		$V_{refA} = 1.5\text{ V}$ ; $C_L = 15\text{ pF}$	-	0.9	-	ns
		$V_{refA} = 1.5\text{ V}$ ; $C_L = 30\text{ pF}$	-	1.45	-	ns
		$V_{refA} = 1.5\text{ V}$ ; $C_L = 50\text{ pF}$	-	1.9	-	ns
		$V_{refA} = 2.3\text{ V}$ ; $C_L = 15\text{ pF}$	-	1.0	-	ns
		$V_{refA} = 2.3\text{ V}$ ; $C_L = 30\text{ pF}$	-	1.65	-	ns
		$V_{refA} = 2.3\text{ V}$ ; $C_L = 50\text{ pF}$	-	2.1	-	ns

[1] All typical values are measured at  $T_{amb} = 25\text{ °C}$ .

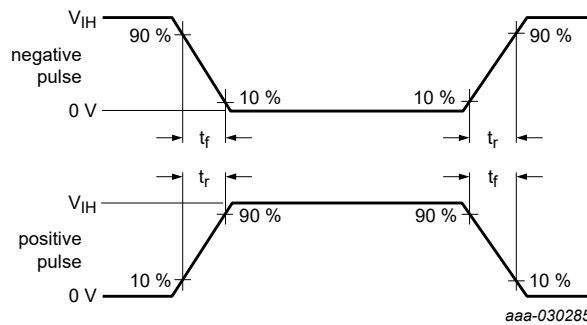
11.1. Waveforms and test circuit



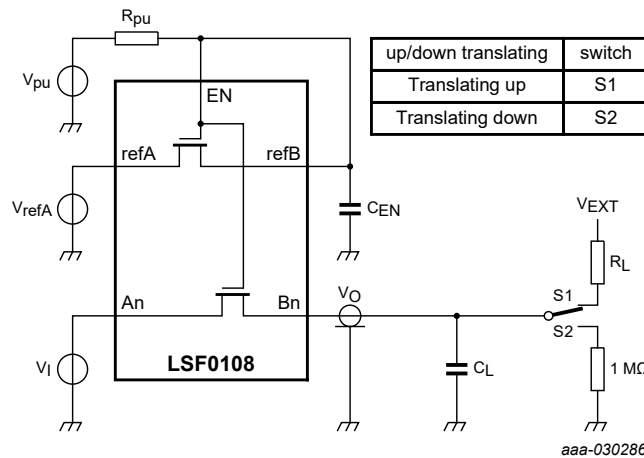
Measurement points are given in [Table 8](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 5. The data input (An, Bn) to output (Bn, An) propagation delay times



a.  $V_I$  source waveform



b. Test circuit

Test data is given in [Table 8](#). The An and Bn pins may be exchanged.

All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz;  $Z_O = 50 \Omega$ .

Definitions test circuit:

$C_L$  = Load capacitance including jig and probe capacitance;  $C_{EN}$  = Decoupling capacitance;

$R_{pu}$  = Pull-up resistance;  $R_L$  = Load resistance; S1/S2 = Test selection switch.

Fig. 6. Test circuit for measuring switching times

Table 8. Test data

Input		Output	Load			
$t_r, t_f$	$V_M$	$V_M$	$C_L$	$C_{EN}$	$R_L$	$R_{pu}$
$\leq 2 \text{ ns}$	$0.5V_{refA}$	$0.5V_{refA}$	15 pF, 30 pF, 50 pF	100 nF	300 $\Omega$	200 k $\Omega$

## 12. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

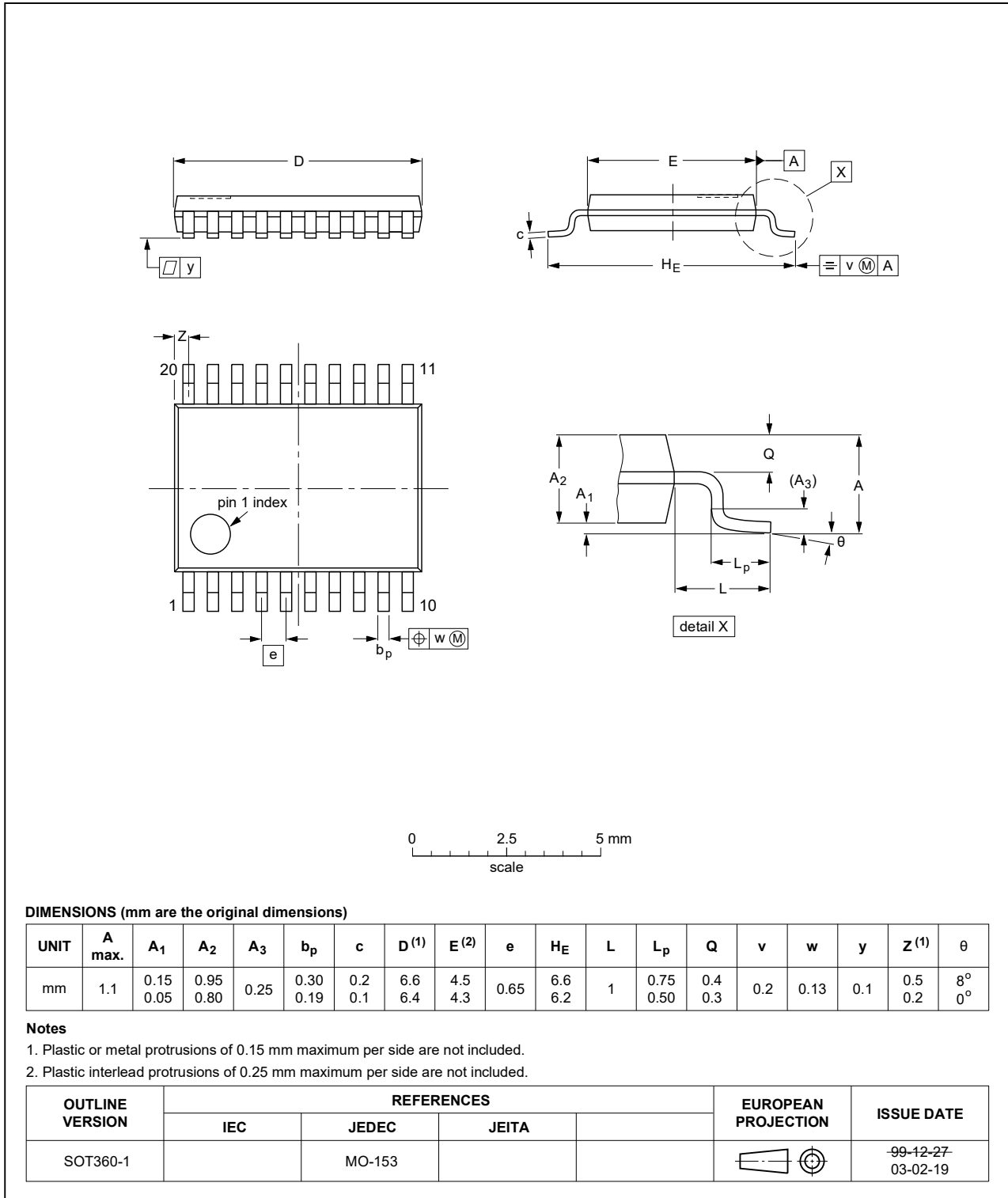


Fig. 7. Package outline SOT360-1 (TSSOP20)



8-bit bidirectional multi-voltage level translator; open-drain; push-pull

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

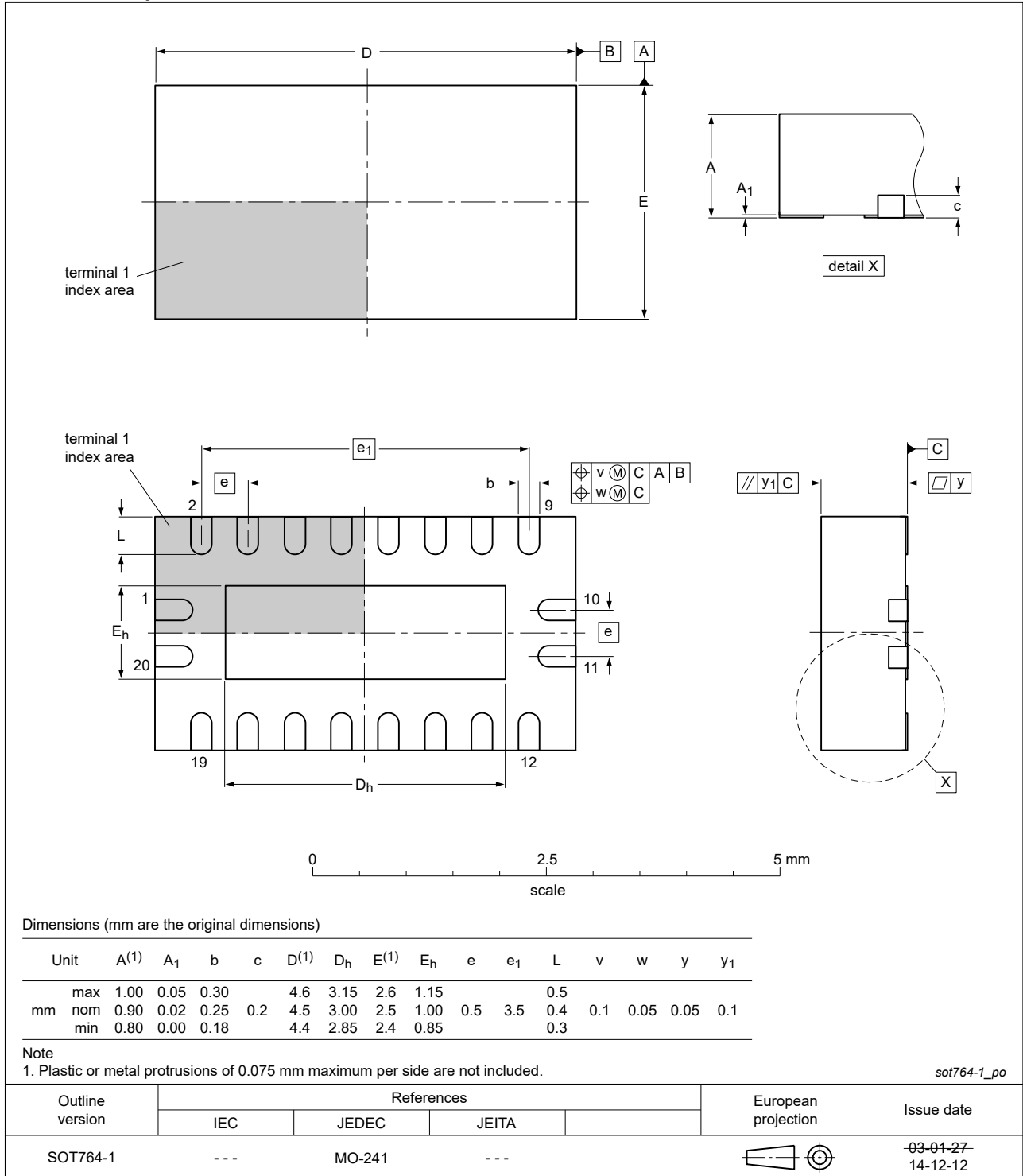


Fig. 8. Package outline SOT764-1 (DHVQFN20)

## 13. Abbreviations

**Table 9. Abbreviations**

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

## 14. Revision history

**Table 10. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
LSF0108_Q100 v.2	20200730	Product data sheet	-	LSF0108_Q100 v.1
Modifications:	• <a href="#">Section 2</a> updated.			
LSF0108_Q100 v.1	20190918	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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