LINEAR SYSTEMS

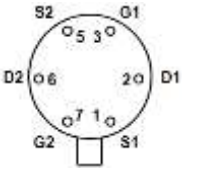
Over 30 Years of Quality Through Innovation

LSK489A/B

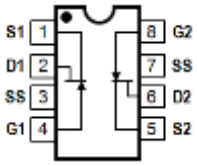
Low Noise, Monolithic Dual N-Channel JFET Amplifier

INDUSTRY'S LOWEST INPUT CAPACITANCE MONOLITHIC DUAL N-CHANNEL JFET

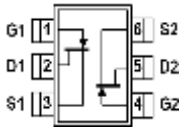
Absolute Maximum Ratings @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation, TA = 25°C	
Continuous Power Dissipation, per side [4]	300mW
Power Dissipation, total [5]	500mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = 60V
Gate to Drain	V_{GDS} = 60V
Features	
Low Noise (f = 1kHz, NBW = 1Hz)	e_n = 1.8nV/√Hz
Low Input Capacitance	Ciss = 4pF



TO-71
Top View



SOIC-A
Top View



SOT-23
Top View

* For equivalent single version, see LSK189

Features

- Low Noise: e_n = 1.8nV/√Hz (typ), *f* = 1kHz, NBW = 1Hz
- Very Low Common Source Input Capacitance of C_{ISS} = 4pF – typ
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage I_{GSS} and I_G
- High CMRR 102 dB

Benefits

- Tight Differential Voltage Match vs. Current
- Improved Op Amp Speed Settling Time Accuracy
- Minimum Input Error Trimming Error Voltage
- Lower Intermodulation Distortion Due to Low Input Capacitance

Applications

- Wideband Differential Amplifiers
- High Speed Temperature Compensated Single Ended Input Amplifier
- High Speed Comparators
- Impedance Converters
- Sonobouys and Hydrophones
- Acoustic Sensors

Description

The LSK489 is the industry's lowest input capacitance and low-noise monolithic dual N-Channel JFET. Low input capacitance substantially reduces intermodulation distortion. In addition, these dual JFETs feature tight offset voltage and low drift over temperature range, and are targeted for use in a wide range of precision instrumentation and sensor applications. The LSK489 is available in surface mount plastic SOIC 8L and SOT-23 6L, as well as thru-hole metal TO-71 6L packages. For an equivalent single N-Channel version refer to the LSK189 datasheet. LSK489 TO-71 6L and SOIC 8L are fit, form and pin compatible to the same LSK389 product.

The LSK489 provides a dramatic increase in capabilities for a wide range of low-noise applications. The most significant aspect of the LSK489 is how it combines a noise level nearly as low as the LSK389 while having much lower gate-to-drain capacitance, 4pF versus the 25pF. The slightly higher noise of the LSK489, versus the LSK389, is not significant in most instances, while the much lower capacitance enables designers to produce simpler, more elegant circuit designs with fewer devices that cost less in production. Also notice that the LSK489 and LSK389 TO-71 and SOIC packages are the same and pin compatible, therefore, they can be used interchangeably.

Like the Linear Systems LSK389, the LSK489 features a unique design construction of interleaving both JFETs on the same piece of silicon to provide excellent matching and thermal tracking, as well a low-noise profile having nearly zero popcorn noise. I_{DSS} range is divided into two segments providing designers improved resolution, which are A grade (ΔI_{DSS} = 6mA) and B grade (ΔI_{DSS} = 7mA). Contact Linear Systems for improved En, I_{DSS}, V_{GS}(off), ΔV_{GS} or any other limits. Based on new limits, LS will assign a new SELXXXX code to be used in shipments.

Matching Characteristics @ 25°C (unless otherwise stated)

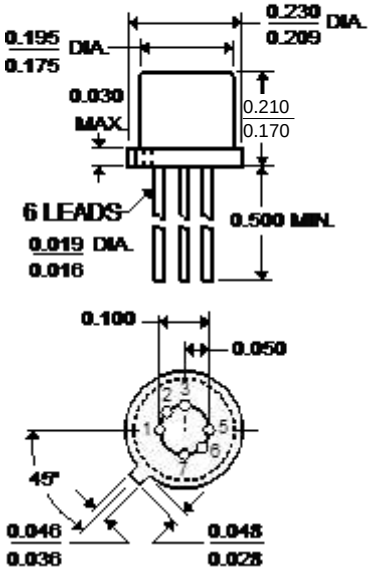
Symbol	Characteristic	Min.	Typ.	Max	Units	Conditions
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate to Source Cutoff Voltage	-	8	20	mV	V_{DS} = 10V, I_D = 1mA
$\frac{I_{DSS1}}{I_{DSS2}}$	Gate to Source Saturation Current Ratio	0.9	-	1.0	-	V_{DS} = 10V, V_{GS} = 0V
CMRR	**Common Mode Rejection Ratio** -20 log $\lvert \Delta V_{GS1-2}/\Delta V_{DS} \rvert$	95	102	-	dB	V_{DS} = 10V to 20V, I_D = 200µA
e_n	Noise Voltage	-	1.8	-	nV/√Hz	V_{DS} = 15V, I_D = 2.0mA, *f* = 1kHz, NBW = 1Hz
e_n	Noise Voltage	-	3.5	-	nV/√Hz	V_{DS} = 15V, I_D = 2.0mA, *f* = 10Hz, NBW = 1Hz
C_{ISS}	Common Source Input Capacitance	-	4	-	pF	V_{DS} = 15V, I_D = 500µA, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Capacitance	-	2	-	pF	

Electrical Characteristics @ 25°C (unless otherwise stated)

Symbol	Characteristic		Min.	Typ.	Max	Units	Conditions
BV_{GSS}	Gate to Source Breakdown Voltage		-60	-	-	V	V_{DS} = 0, I_D = -1nA
$V_{(BR)G1 - G2}$	Gate to Gate Breakdown Voltage		±30	±45	-	V	I_G= ±1µA, I_D=I_S=0 A (Open Circuit)
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage		-1.5	-	-3.5	V	V_{DS} = 15V, I_D = 1nA
V_{GS}	Gate to Source Operating Voltage		-0.5	-	-3.5	V	V_{DS} = 15V, I_D = 500µA
I_{DSS}	Drain to Source Saturation Current	LSK489A	2.5	5.5	8.5	mA	V_{DG} = 15V, V_{GS} = 0
		LSK489B	8.0	11.5	15.0		
I_G	Gate Operating Current		-	-2	-25	pA	V_{DG} = 15V, I_D = 200µA
			-	-0.8	-10	nA	T_A = 125°C
I_{GSS}	Gate to Source Leakage Current		-	-	-100	pA	V_{DG} = -15V, V_{DS} = 0
G_{fs}	Full Conductance Transconductance		1500	-	-	µS	V_{DG} = 15V, V_{GS} = 0, *f* = 1kHz
G_{fs}	Transconductance		1000	1500	-	µS	V_{DG} = 15V, I_D = 500µA
G_{OS}	Full Output Conductance		-	-	40	µS	V_{DG} = 15V, V_{GS} = 0
G_{OS}	Output Conductance		-	1.8	2.7	µS	V_{DG} = 15V, I_D = 200µA

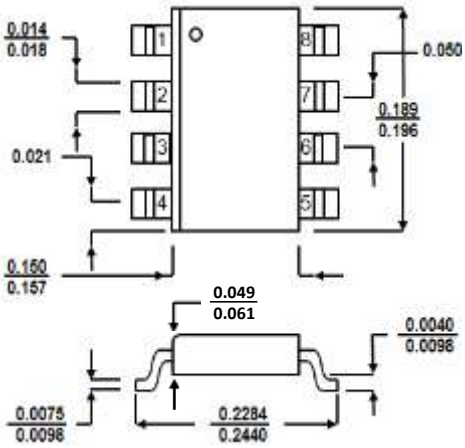
Package Dimensions

TO-71
Six Lead



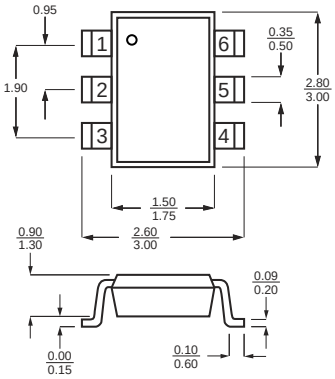
DIMENSIONS IN INCHES

SOIC-A
8 Lead



DIMENSIONS IN INCHES

SOT-23
Six Lead

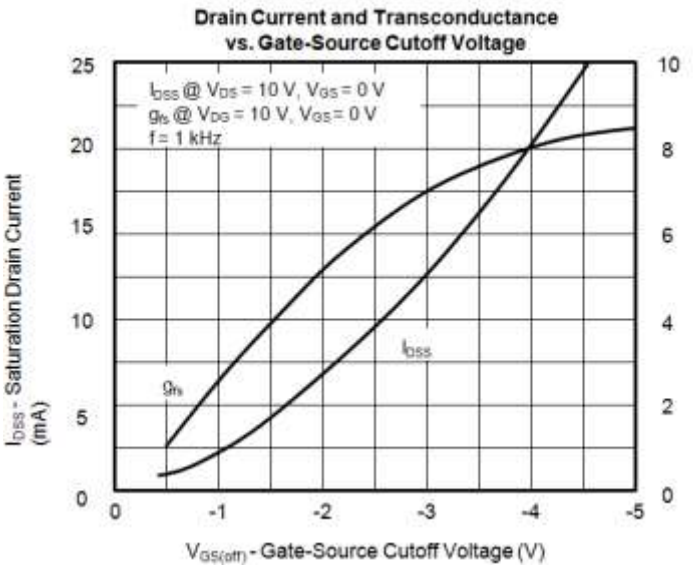


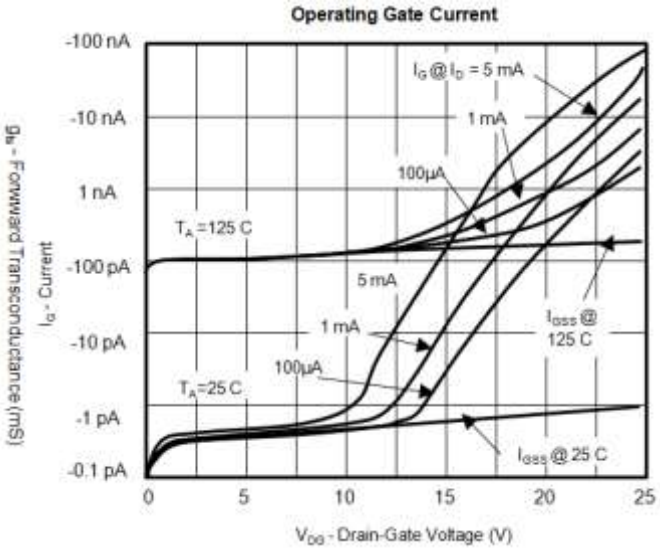
DIMENSIONS IN MILLIMETERS

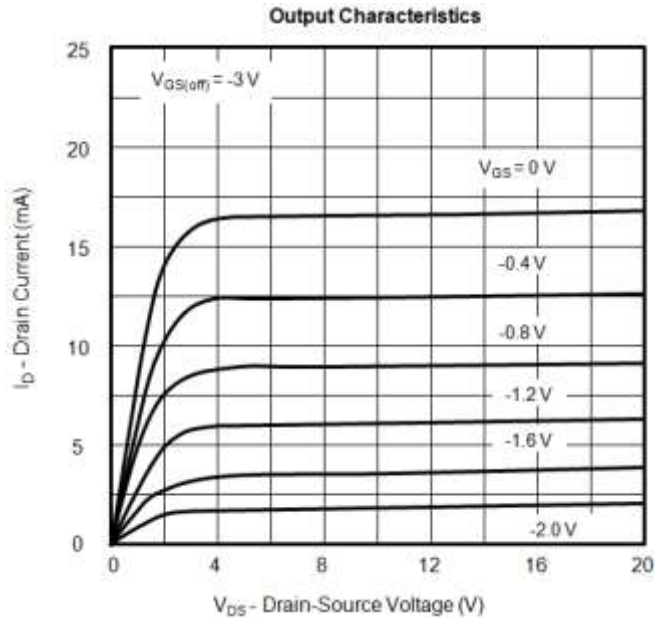
Notes

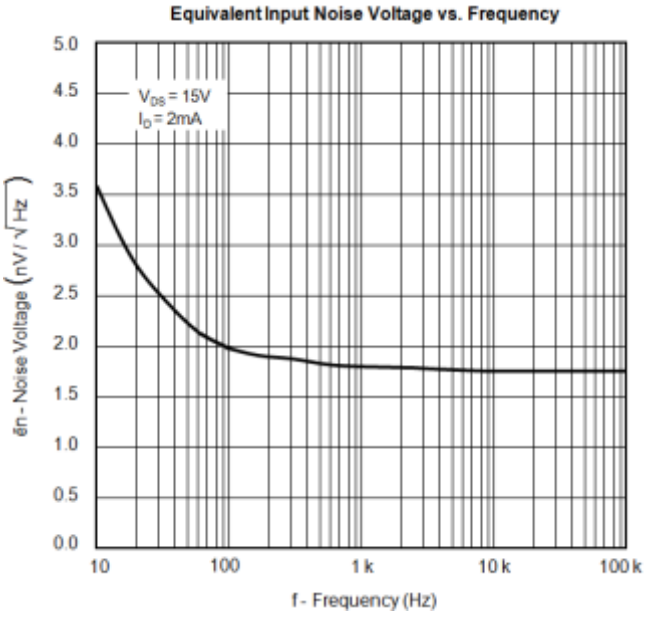
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse width ≤2$_{ms}$.
3. All MIN/TYP/MAX Limits are absolute values. Negative signs indicate electrical polarity only.
4. Derate 2.4 mW/°C above 25°C.
5. Derate 4 mW/°C above 25°C.

Typical Characteristics



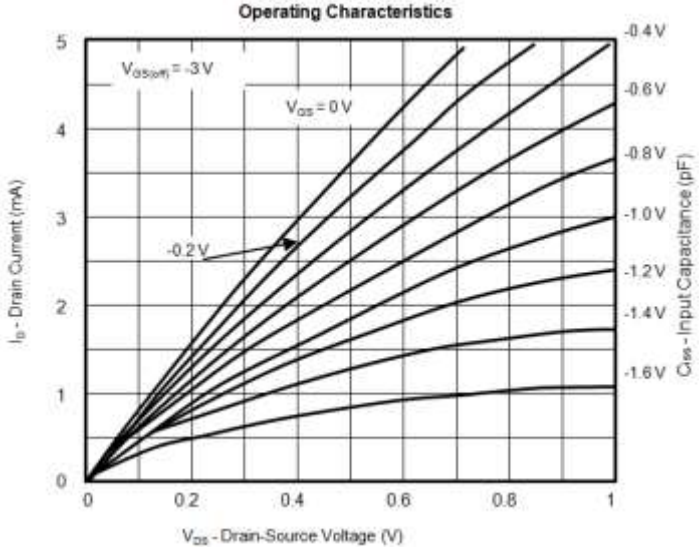




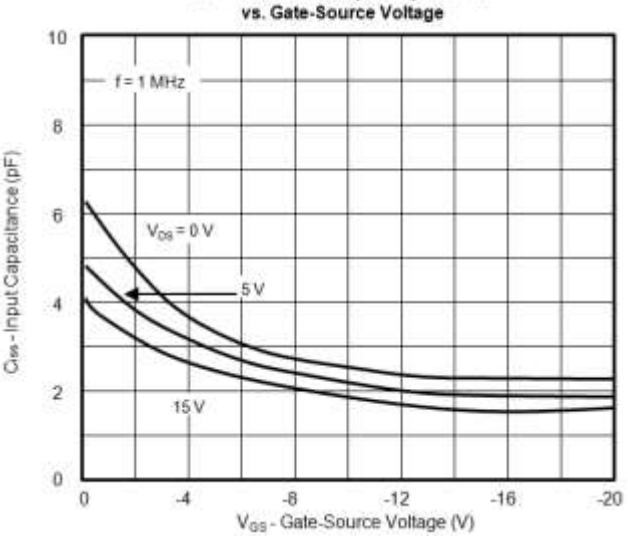


Typical Characteristics (Cont'd)

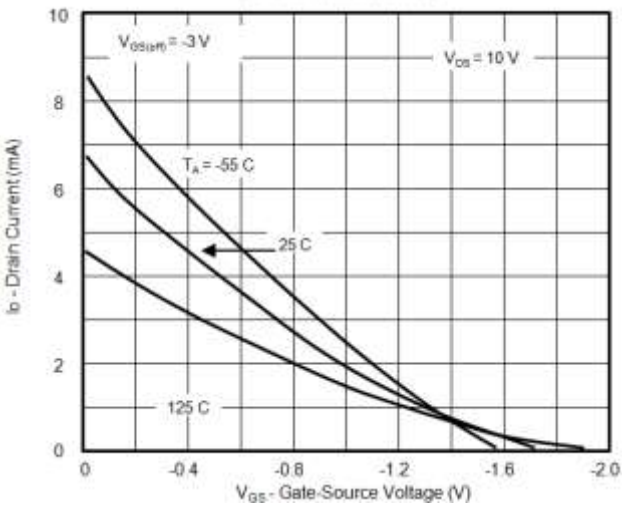
Operating Characteristics



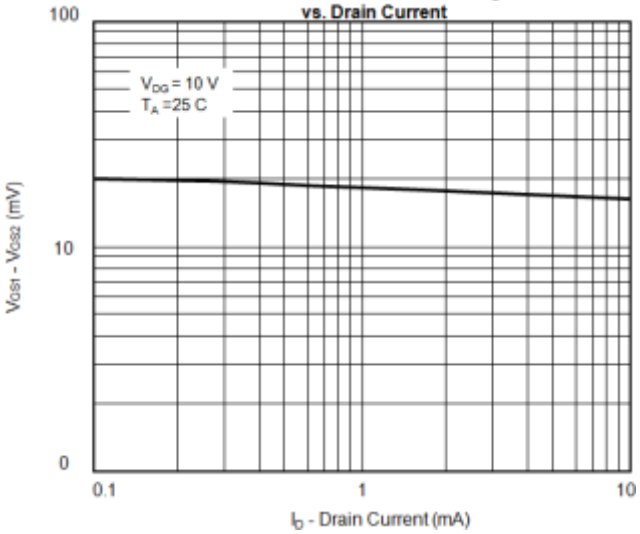
Common-Source Input Capacitance vs. Gate-Source Voltage



Transfer Characteristics

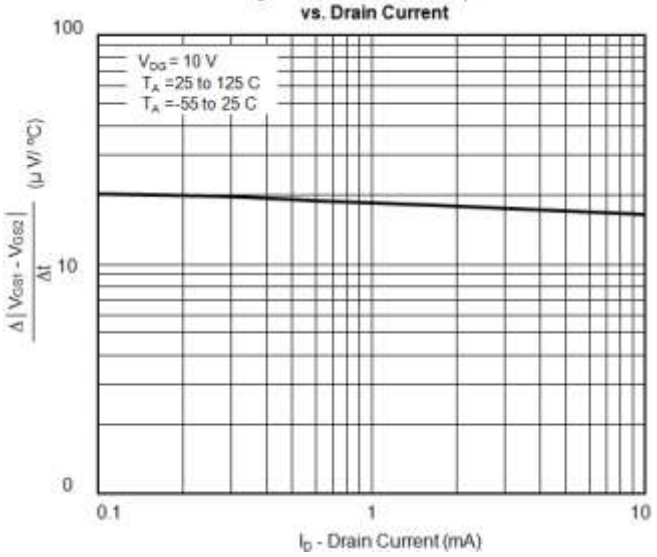


Gate-Source Differential Voltage vs. Drain Current

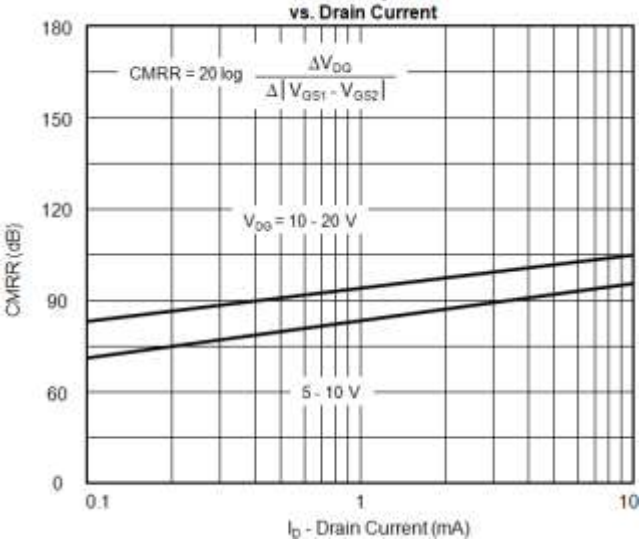


Typical Characteristics (Cont'd)

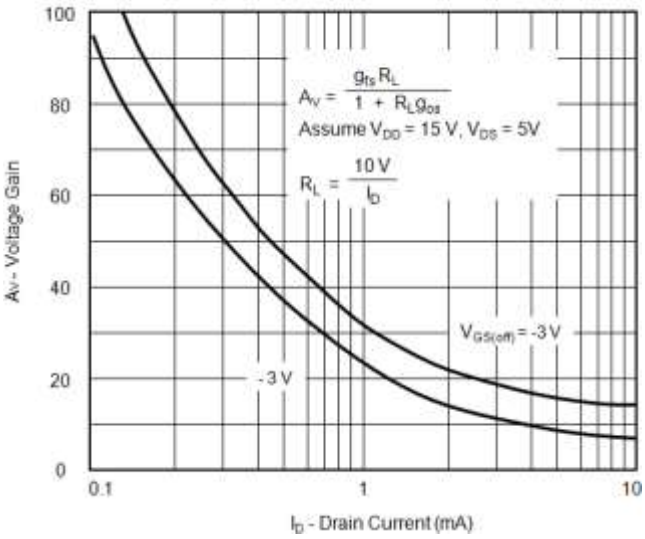
Voltage Differential with Temperature vs. Drain Current



Common Mode Rejection Ration vs. Drain Current



Circuit Voltage Gain vs. Drain Current



On-Resistance vs. Drain Current