

## FEATURES

- **Tight Initial Output Voltage:** <math><0.05\%</math>
- **Ultralow Drift:** 3ppm/°C Typical
- **Series or Shunt Operation**
- Curvature Corrected
- Ultrahigh Line Rejection:  $\approx 0.5\text{ppm/V}$
- Low Output Impedance:  $\approx 0.02\Omega$
- Plug-In Replacement for Present References
- Available at 2.5V, 4.5V, 5V, and 10V
- 100% Noise Tested
- Temperature Output
- Industrial Temperature Range in SO-8
- Available in 8-Lead N8 and S8 Packages

## APPLICATIONS

- Negative Shunt References
- A/D and D/A Converters
- Precision Regulators
- Constant Current Sources
- V/F Converters
- Bridge Excitation

## DESCRIPTION

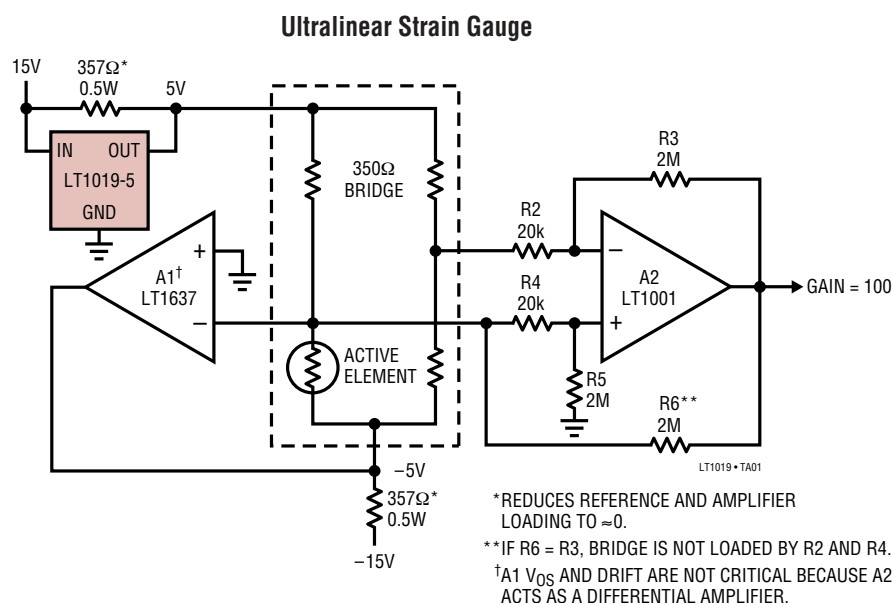
The LT<sup>®</sup>1019 is a third generation bandgap voltage reference utilizing thin film technology and a greatly improved curvature correction technique. Wafer level trimming of both reference and output voltage combines to produce very low TC and tight initial output voltage tolerance.

The LT1019 can both sink and source up to 10mA and can be used in either the series or shunt mode, allowing the reference to operate with positive or negative output voltages without external components. Minimum input/output voltage is less than 1V in the series mode, providing improved tolerance of low line conditions and excellent line regulation.

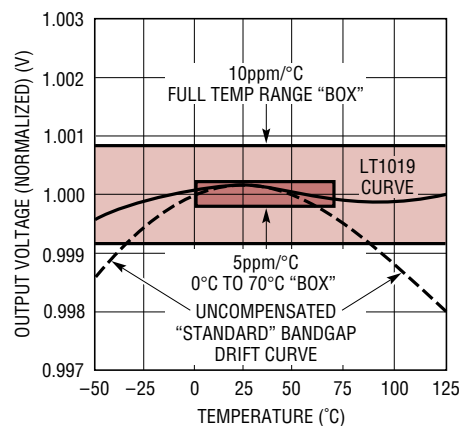
The LT1019 is available in four voltages: 2.5V, 4.5V, 5V and 10V. It is a direct replacement for most bandgap references presently available including AD580, AD581, REF-01, REF-02, MC1400, MC1404 and LM168.

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## TYPICAL APPLICATION



## Output Voltage Drift



**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Input Voltage .....	40V	Specified Temperature Range	
Output Voltage (Note 2)		Commercial .....	0°C to 70°C
LT1019-5, LT1019-10 .....	16V	Industrial .....	-40°C to 85°C
LT1019-2.5, LT1019-4.5 .....	7V	Military .....	-55°C to 125°C
Output Short-Circuit Duration (Note 2)		Trim Pin Voltage .....	±30V
$V_{IN} < 20V$ .....	Indefinite	Temp Pin Voltage .....	5V
$20V \leq V_{IN} \leq 35V$ .....	10 sec	Storage Temperature Range (Note 11)	-65°C to 150°C
		Lead Temperature (Soldering, 10 sec) .....	300°C

**PACKAGE/ORDER INFORMATION**

<p>TOP VIEW</p> <p>DNC* 8</p> <p>DNC* 1 7 DNC*</p> <p>INPUT 2 6 OUTPUT</p> <p>TEMP 3 5 TRIM</p> <p>GND (CASE) 4</p> <p>H PACKAGE 8-LEAD TO-5 METAL CAN</p> <p>*INTERNALLY CONNECTED. DO NOT CONNECT EXTERNALLY</p> <p><math>T_{JMAX} = 150^{\circ}C, \theta_{JA} = 150^{\circ}C/W, \theta_{JC} = 45^{\circ}C/W</math></p>	<p>TOP VIEW</p> <p>DNC* 1 8 DNC*</p> <p>INPUT 2 7 DNC*</p> <p>TEMP 3 6 OUTPUT</p> <p>GND 4 5 TRIM</p> <p>N8 PACKAGE 8-LEAD PDIP</p> <p>*INTERNALLY CONNECTED. DO NOT CONNECT EXTERNALLY.</p> <p><math>T_{JMAX} = 100^{\circ}C, \theta_{JA} = 130^{\circ}C/W</math></p>	<p>TOP VIEW</p> <p>DNC* 1 8 DNC*</p> <p>INPUT 2 7 DNC*</p> <p>TEMP 3 6 OUTPUT</p> <p>GND 4 5 TRIM</p> <p>S8 PACKAGE 8-LEAD PLASTIC SO</p> <p>*INTERNALLY CONNECTED. DO NOT CONNECT EXTERNALLY.</p> <p><math>T_{JMAX} = 100^{\circ}C, \theta_{JA} = 130^{\circ}C/W</math></p>	
<p>ORDER PART NUMBER</p>	<p>ORDER PART NUMBER</p>	<p>ORDER PART NUMBER</p>	<p>S8 PART MARKING</p>
<p>LT1019ACH-2.5    LT1019CH-2.5</p> <p>LT1019ACH-4.5    LT1019CH-4.5</p> <p>LT1019ACH-5        LT1019CH-5</p> <p>LT1019ACH-10      LT1019CH-10</p> <p>LT1019AMH-2.5    LT1019MH-2.5</p> <p>LT1019AMH-4.5    LT1019MH-4.5</p> <p>LT1019AMH-5        LT1019MH-5</p> <p>LT1019AMH-10     LT1019MH-10</p> <p><b>OBSOLETE</b></p> <p>CONSIDER THE N8 OR S8 FOR ALTERNATE SOURCES.</p>	<p>LT1019ACN8-2.5    LT1019CN8-5</p> <p>LT1019ACN8-4.5    LT1019CN8-10</p> <p>LT1019ACN8-5      LT1019IN8-2.5</p> <p>LT1019ACN8-10     LT1019IN8-4.5</p> <p>LT1019CN8-2.5     LT1019IN8-5</p> <p>LT1019CN8-4.5     LT1019IN8-10</p>	<p>LT1019ACS8-2.5</p> <p>LT1019ACS8-5</p> <p>LT1019AIS8-2.5</p> <p>LT1019AIS8-5</p> <p>LT1019CS8-2.5</p> <p>LT1019CS8-4.5</p> <p>LT1019CS8-5</p> <p>LT1019CS8-10</p> <p>LT1019IS8-2.5</p> <p>LT1019IS8-5</p>	<p>019A25</p> <p>1019A5</p> <p>19AI25</p> <p>019AI5</p> <p>1925</p> <p>1945</p> <p>1905</p> <p>1910</p> <p>19I25</p> <p>19I05</p>

## AVAILABLE OPTIONS

OUTPUT VOLTAGE (V)	TEMPERATURE (°C)	ACCURACY (%)	TEMPERATURE COEFFICIENT (ppm/°C)	PACKAGE TYPE		
				TO-5 H8	SO-8 S8	PDIP-8 N8
2.5	0 to 70	0.05 0.2	5 20	LT1019ACH-2.5 LT1019CH-2.5	LT1019ACS8-2.5 LT1019CS8-2.5	LT1019ACN8-2.5 LT1019CN8-2.5
	-40 to 85	0.05 0.2	10 20		LT1019AIS8-2.5 LT1019IS8-2.5	LT1019IN8-2.5
	-55 to 125	0.05 0.2	10 25	LT1019AMH-2.5 LT1019MH-2.5		
4.5	0 to 70	0.05 0.2	5 20	LT1019ACH-4.5 LT1019CH-4.5	LT1019CS8-4.5	LT1019ACN8-4.5 LT1019CN8-4.5
	-40 to 85	0.2	20			LT1019IN8-4.5
	-55 to 125	0.05 0.2	10 25	LT1019AMH-4.5 LT1019MH-4.5		
5	0 to 70	0.05 0.2	5 20	LT1019ACH-5 LT1019CH-5	LT1019ACS8-5 LT1019CS8-5	LT1019ACN8-5 LT1019CN8-5
	-40 to 85	0.05 0.2	10 20		LT1019AIS8-5 LT1019IS8-5	LT1019IN8-5
	-55 to 125	0.05 0.2	10 25	LT1019AMH-5 LT1019MH-5		
10	0 to 70	0.05 0.2	5 20	LT1019ACH-10 LT1019CH-10	LT1019CS8-10	LT1019ACN8-10 LT1019CN8-10
	-40 to 85	0.2	20			LT1019IN8-10
	-55 to 125	0.05 0.2	10 25	LT1019AMH-10 LT1019MH-10		

## ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 15\text{V}$ ,  $I_{OUT} = 0$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1019A			LT1019			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
	Output Voltage Tolerance				0.02	0.05		0.02	0.2	%
TC	Output Voltage Temperature Coefficient (Note 3)	LT1019C (0°C to 70°C) LT1019I (-40°C to 85°C) LT1019M (-55°C to 125°C)	●		3	5		5	20	ppm/°C
			●		3	10		5	20	ppm/°C
			●		5	10		8	25	ppm/°C
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation (Note 4)	$(V_{OUT} + 1.5\text{V}) \leq V_{IN} \leq 40\text{V}$			0.5	3		0.5	3	ppm/V
			●		1.0	5		1.0	5	ppm/V
RR	Ripple Rejection	$50\text{Hz} \leq f \leq 400\text{Hz}$		90	110		90	110		dB
			●	84			84			dB

## ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 15\text{V}$ ,  $I_{OUT} = 0$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1019A			LTC1019			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation Series Mode (Notes 4, 5)	$0 \leq I_{OUT} \leq 10\text{mA}$ (Note 5)	●	0.02	0.05	0.08	0.02	0.05	0.08	mV/mA ( $\Omega$ )
	Load Regulation, Shunt Mode	$1\text{mA} \leq I_{SHUNT} \leq 10\text{mA}$ (Notes 5, 6) 2.5V, 4.5V, 5V 10V	● ●	0.1	0.4	0.8	0.1	0.4	0.8	mV/mA ( $\Omega$ ) mV/mA ( $\Omega$ )
	Thermal Regulation (Note 7)	$\Delta P = 200\text{mW}$ , $t = 50\text{ms}$		0.1	0.5		0.1	0.5		ppm/mW
$I_Q$	Quiescent Current Series Mode		●	0.65	1.0	1.3	0.65	1.2	1.5	mA mA
	Minimum Shunt Current	(Note 8)	●	0.5	0.8		0.5	0.8		mA
	Minimum Input/Output Voltage Differential	$I_{OUT} \leq 1\text{mA}$ $I_{OUT} = 10\text{mA}$	● ●	0.9	1.1	1.3	0.9	1.1	1.3	V V
	Trim Range	LT1019-2.5 LT1019-5 LT1019-10		$\pm 3.5$ $\pm 3.5$ $\pm 3.5$	$\pm 6$ 5, -13 5, -27		$\pm 3.5$ $\pm 3.5$ $\pm 3.5$	$\pm 6$ 5, -13 5, -27		% % %
$I_{SC}$	Short-Circuit Current Output Connected to GND	$2\text{V} \leq V_{IN} \leq 35\text{V}$	●	15	25	50	15	25	50	mA
				10			10			mA
$e_n$	Output Voltage Noise (Note 10)	$10\text{Hz} \leq f \leq 1\text{kHz}$		2.5	4		2.5	4		ppm (RMS)
		$0.1\text{Hz} \leq f \leq 10\text{Hz}$		2.5			2.5			ppm (P-P)

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** These are high power conditions and are therefore guaranteed only at temperatures equal to or below  $70^\circ\text{C}$ . Input is either floating, tied to output or held higher than output.

**Note 3:** Output voltage drift is measured using the box method. Output voltage is recorded at  $T_{MIN}$ ,  $25^\circ\text{C}$  and  $T_{MAX}$ . The lowest of these three readings is subtracted from the highest and the resultant difference is divided by  $(T_{MAX} - T_{MIN})$ .

**Note 4:** Line regulation and load regulation are measured on a pulse basis with low duty cycle. Effects due to die heating must be taken into account separately. See thermal regulation and application section.

**Note 5:** Load regulation is measured at a point  $1/8"$  below the base of the package with Kelvin contacts.

**Note 6:** Shunt regulation is measured with the input floating. This parameter is also guaranteed with the input connected ( $V_{IN} - V_{OUT} > 1\text{V}$ ,  $0\text{mA} \leq I_{SINK} \leq 10\text{mA}$ . Shunt and sink current flow into the output.

**Note 7:** Thermal regulation is caused by die temperature gradients created by load current or input voltage changes. This effect must be added to normal line or load regulation.

**Note 8:** Minimum shunt current is measured with shunt voltage held 20mV below the value measured at 1mA shunt current.

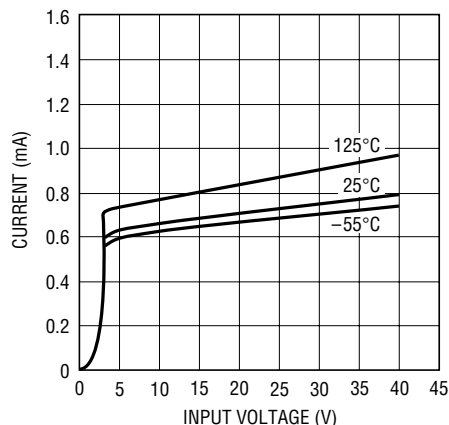
**Note 9:** Minimum input/output voltage is measured by holding input voltage 0.5V above the nominal output voltage, while measuring  $V_{IN} - V_{OUT}$ .

**Note 10:** RMS noise is measured with a single pole highpass filter at 10Hz and a 2-pole lowpass filter at 1kHz. The resulting output is full-wave rectified and then integrated for a fixed period, making the final reading an average as opposed to RMS. A correction factor of 1.1 is used to convert from average to RMS, and a second correction of 0.88 is used to correct the nonideal bandpass of the filters.

**Note 11:** If the part is stored outside of the specified temperature range, the output may shift due to hysteresis.

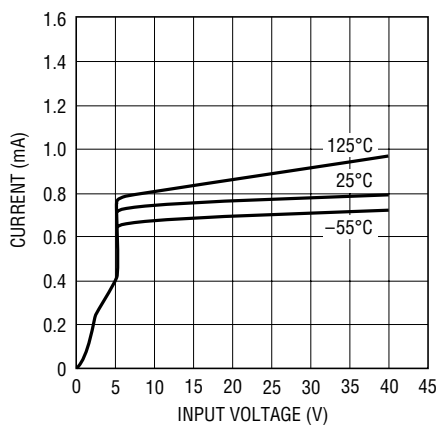
# TYPICAL PERFORMANCE CHARACTERISTICS

**Quiescent Current (LT1019-2.5)**



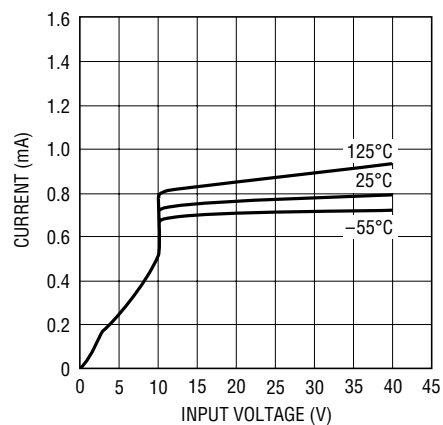
LT1019 • TPC01

**Quiescent Current (LT1019-4.5/LT1019-5)**



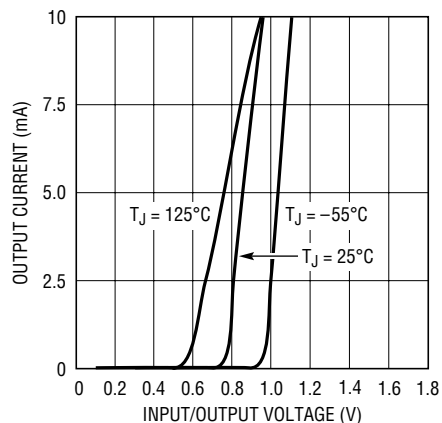
LT1019 • TPC02

**Quiescent Current (LT1019-10)**



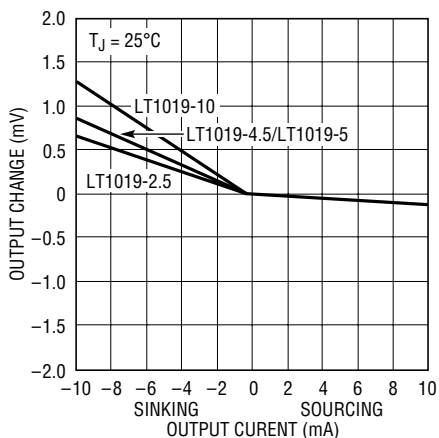
LT1019 • TPC03

**Minimum Input/Output Voltage Differential**



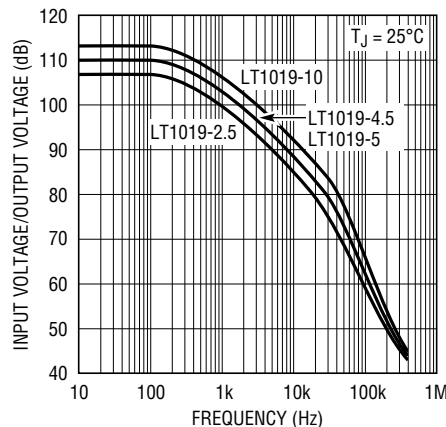
LT1019 • TPC04

**Load Regulation**



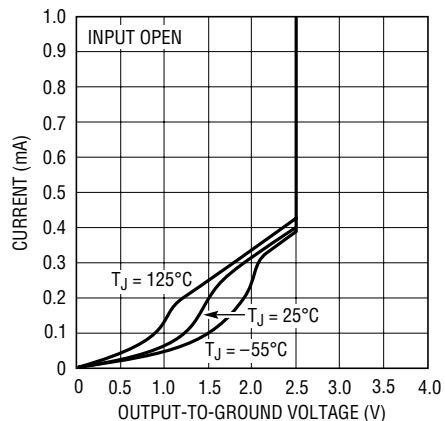
LT1019 • TPC05

**Ripple Rejection**



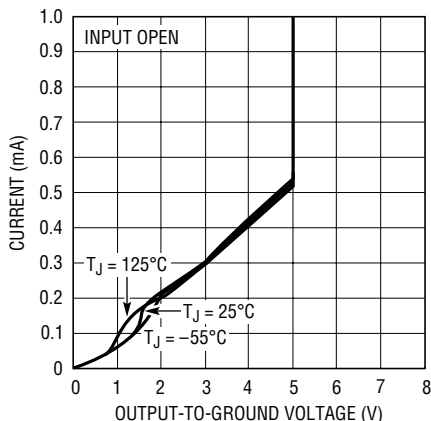
LT1019 • TPC06

**Shunt Mode Characteristics (LT1019-2.5)**



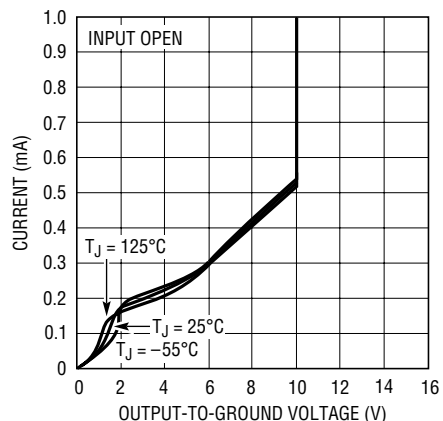
LT1019 • TPC07

**Shunt Mode Characteristics (LT1019-5)**



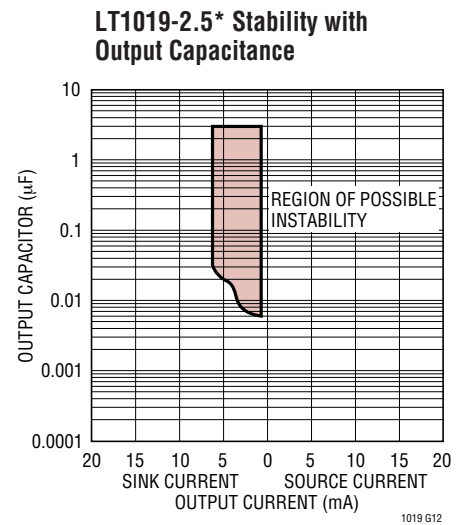
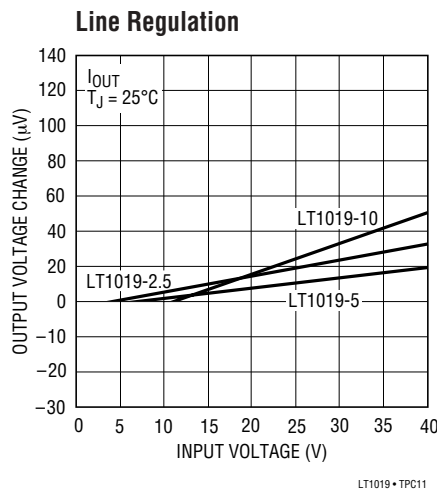
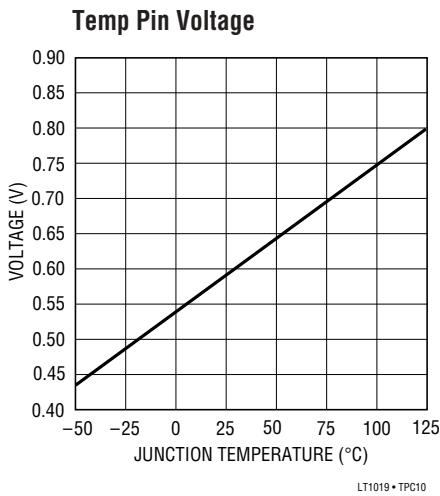
LT1019 • TPC08

**Shunt Mode Characteristics (LT1019-10)**



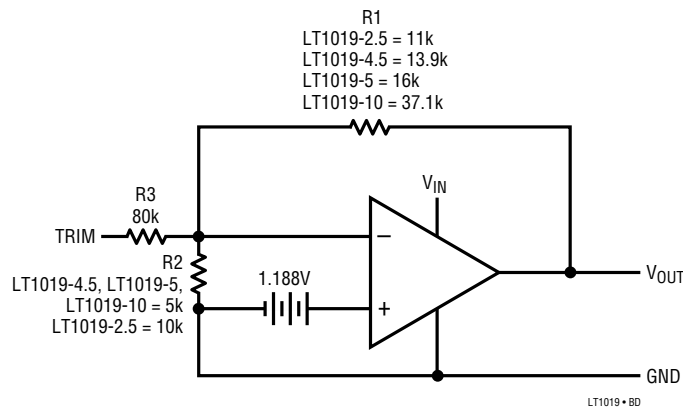
LT1019 • TPC09

## TYPICAL PERFORMANCE CHARACTERISTICS



\* LT1019-4.5/LT1019-5/LT1019-10 ARE STABLE WITH ALL LOAD CAPACITANCE.

## BLOCK DIAGRAM



## APPLICATIONS INFORMATION

### Line and Load Regulation

Line regulation on the LT1019 is nearly perfect. A 10V change in input voltage causes a typical output shift of less than 5ppm. Load regulation (sourcing current) is nearly as good. A 5mA change in load current shifts output voltage by only 100µV. These are *electrical* effects, measured with low duty cycle pulses to eliminate heating effects. In real world applications, the *thermal* effects of load and line changes must be considered.

Two separate thermal effects are evident in monolithic circuits. One is a gradient effect, where power dissipation on the die creates temperature gradients. These gradients can cause output voltage shifts *even if the overall temperature coefficient of the reference is zero*. The LT1019, unlike previous references, specifies thermal regulation caused by die temperature gradients. The specification is 0.5ppm/mW. To calculate the effect on output voltage, simply multiply the *change* in device power dissipation by

## APPLICATIONS INFORMATION

the thermal regulation specification. Example: a 10V device with a nominal input voltage of 15V and load current of 5mA. Find the effect of an input voltage change of 1V and a load current change of 2mA.

$$\begin{aligned}\Delta P \text{ (line change)} &= (\Delta V_{IN})(I_{LOAD}) = (1V)(5mA) = 5mW \\ \Delta V_{OUT} &= (0.5\text{ppm/mW})(5mW) = 2.5\text{ppm}\end{aligned}$$

$$\begin{aligned}\Delta P \text{ (load change)} &= (\Delta I_{LOAD})(V_{IN} - V_{OUT}) \\ &= (2mA)(5V) = 10mW\end{aligned}$$

$$\Delta V_{OUT} = (0.5\text{ppm/mW})(10mW) = 5\text{ppm}$$

Even though these effects are small, they should be taken into account in critical applications, especially where input voltage or load current is high.

The second thermal effect is overall die temperature change. The magnitude of this change is the product of change in power dissipation times the thermal resistance ( $\theta_{JA}$ ) of the IC package  $\approx (100^\circ\text{C/W to } 150^\circ\text{C/W})$ . The effect on the reference output is calculated by multiplying die temperature change by the temperature drift specification of the reference. Example: same conditions as above with  $\theta_{JA} = 150^\circ\text{C/W}$  and an LT1019 with 20ppm/ $^\circ\text{C}$  drift specification.

$$\begin{aligned}\Delta P \text{ (line change)} &= 5mW \\ \Delta V_{OUT} &= (5mW)(150^\circ\text{C/W})(20\text{ppm}/^\circ\text{C}) \\ &= 15\text{ppm}\end{aligned}$$

$$\begin{aligned}\Delta P \text{ (load change)} &= 10mW \\ \Delta V_{OUT} &= (10mW)(150^\circ\text{C/W})(20\text{ppm}/^\circ\text{C}) \\ &= 30\text{ppm}\end{aligned}$$

These calculations show that thermally induced output voltage variations can easily exceed the electrical effects. In critical applications where shifts in power dissipation are expected, a small clip-on heat sink can significantly improve these effects by reducing overall die temperature change. Alternately, an LT1019A can be used with four times lower TC. If warm-up drift is of concern, these measures will also help. With warm-up drift, *total* device power dissipation must be considered. In the example given, warm-up drift (worst case) is equal to:

$$\begin{aligned}\text{Warm-up drift} &= [(V_{IN})(I_Q) + (V_{IN} - V_{OUT})(I_{LOAD})] \\ & \quad [(\theta_{JA})(TC)]\end{aligned}$$

with  $I_Q$  (quiescent current) = 0.6mA,

$$\begin{aligned}\text{Warm-up drift} &= [(15V)(0.6mA) + (5V)(5mA)] \\ & \quad [(150^\circ\text{C/W})(25\text{ppm}/^\circ\text{C})] \\ &= 127.5\text{ppm}\end{aligned}$$

Note that 74% of the warm-up drift is due to load current times input/output differential. This emphasizes the importance of keeping both these numbers low in critical applications.

Note that line regulation is now affected by reference output impedance. R1 should have a wattage rating high enough to withstand full input voltage if output shorts must be tolerated. Even with load currents below 10mA, R1 can be used to reduce power dissipation in the LT1019 for lower warm-up drift, etc.

### Output Trimming

Output voltage trimming on the LT1019 is nominally accomplished with a potentiometer connected from output to ground with the wiper tied to the trim pin. The LT1019 was made compatible with existing references, so the trim range is large: +6%, -6% for the LT1019-2.5, +5%, -13% for the LT1019-5, and +5%, -27% for the LT1019-10. This large trim range makes precision trimming rather difficult. One solution is to insert resistors in series with both ends of the potentiometer. This has the disadvantage of potentially poor tracking between the fixed resistors and the potentiometer. A second method of reducing trim range is to insert a resistor in series with the wiper of the potentiometer. This works well only for very small trim range because of the mismatch in TCs between the series resistor and the internal thin film resistors. These film resistors can have a TC as high as 500ppm/ $^\circ\text{C}$ . That same TC is then transferred to the change in output voltage: a 1% shift in output voltage causes a  $(500\text{ppm})(1\%) = 5\text{ppm}/^\circ\text{C}$  change in output voltage drift.

## APPLICATIONS INFORMATION

The worst-case error in initial output voltage for the LT1019 is 0.2%, so a series resistor is satisfactory if the output is simply trimmed to nominal value. The maximum TC shift expected would be 1ppm/°C.

### Using the Temp Pin

The LT1019 has a TEMP pin like several other bandgap references. The voltage on this pin is directly proportional to absolute temperature (PTAT) with a slope of approximately 2.1mV/°C. Room temperature voltage is therefore approximately  $(295^{\circ}\text{K})(2.1\text{mV}/^{\circ}\text{C}) = 620\text{mV}$ . This voltage varies with process parameters and should not be used to measure absolute temperature, but rather relative temperature changes. Previous bandgap references have been very sensitive to any loading on the TEMP pin because it is an integral part of the reference “core” itself. The LT1019 “taps” the core at a special point which has much less effect on the reference. The relationship between TEMP pin loading and a change in reference output voltage is less than 0.05%/μA, about ten times improvement over previous references.

### Output Bypassing

The LT1019 is designed to be stable with a wide range of load currents and output capacitors. The 4.5V, 5V, and 10V devices do not oscillate under any combination of

capacitance and load. The 2.5V device can oscillate when sinking currents between 1mA and 6mA for load capacitance between 400pF and 2μF (see Figure 1).

If output bypassing is desired to reduce high frequency output impedance, keep in mind that loop phase margin is significantly reduced for output capacitors between 500pF and 1μF if the capacitor has low ESR (Effective Series Resistance). This can make the output “ring” with tran-

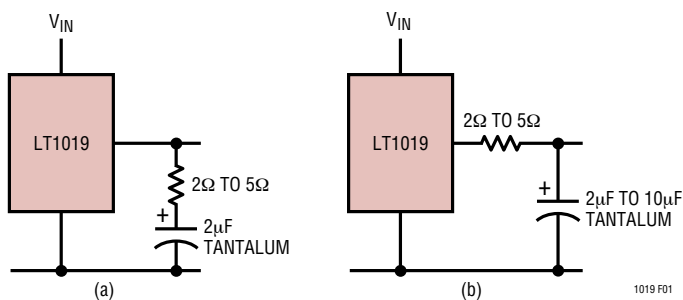
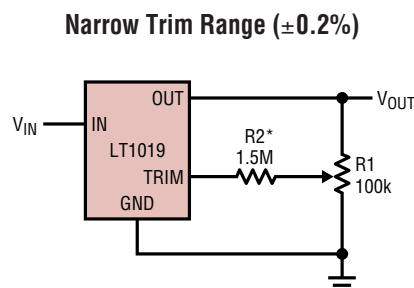
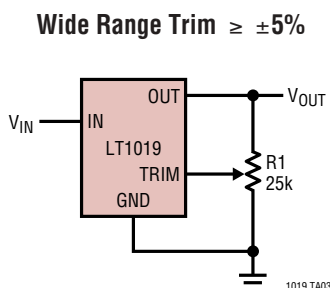


Figure 1. Output Bypassing

sient loads. The best transient load response is obtained by deliberately adding a resistor to increase ESR as shown in Figure 1.

Use configuration (a) if DC voltage error cannot be compromised as load current changes. Use (b) if absolute minimum peak perturbation at the load is needed. For best transient response, the output can be loaded with  $\geq 1\text{mA}$  DC current.

## TYPICAL APPLICATIONS

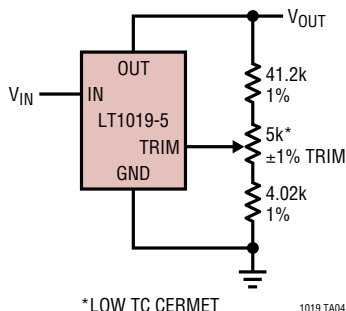


\*INCREASE TO 4.7M FOR LT1019A ( $\pm 0.05\%$ )

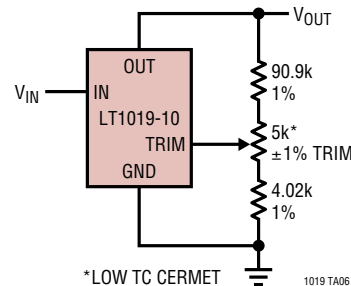


# TYPICAL APPLICATIONS

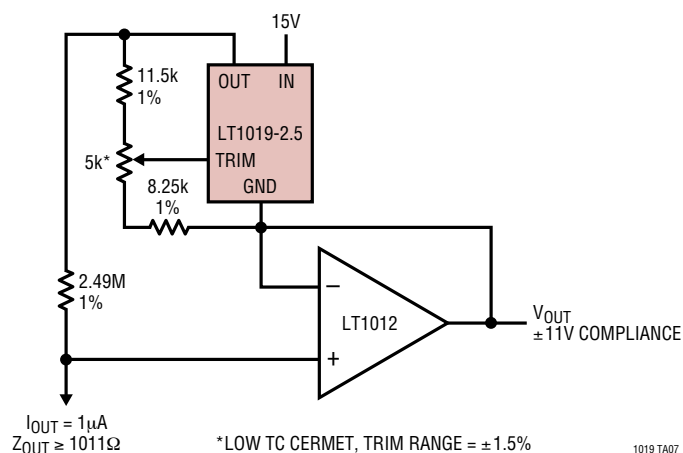
Trimming LT1019-5 Output to 5.120V



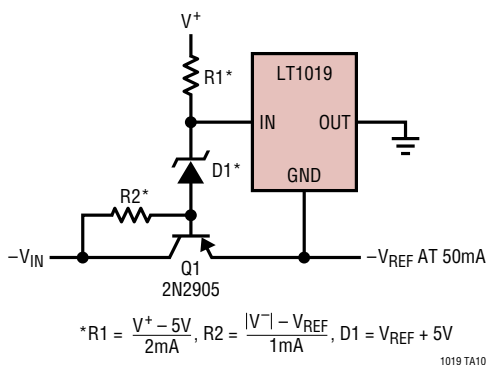
Trimming LT1019-10 Output to 10.240V



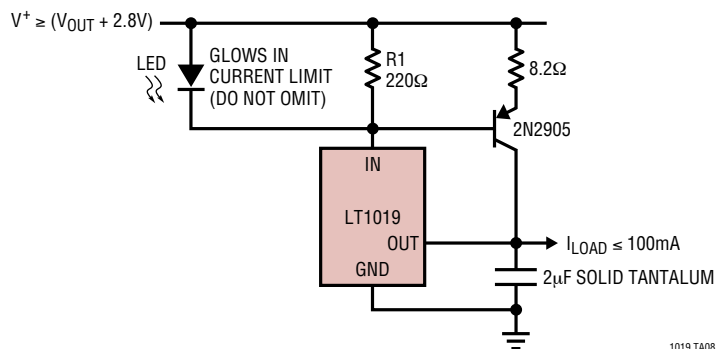
Precision 1μA Current Source



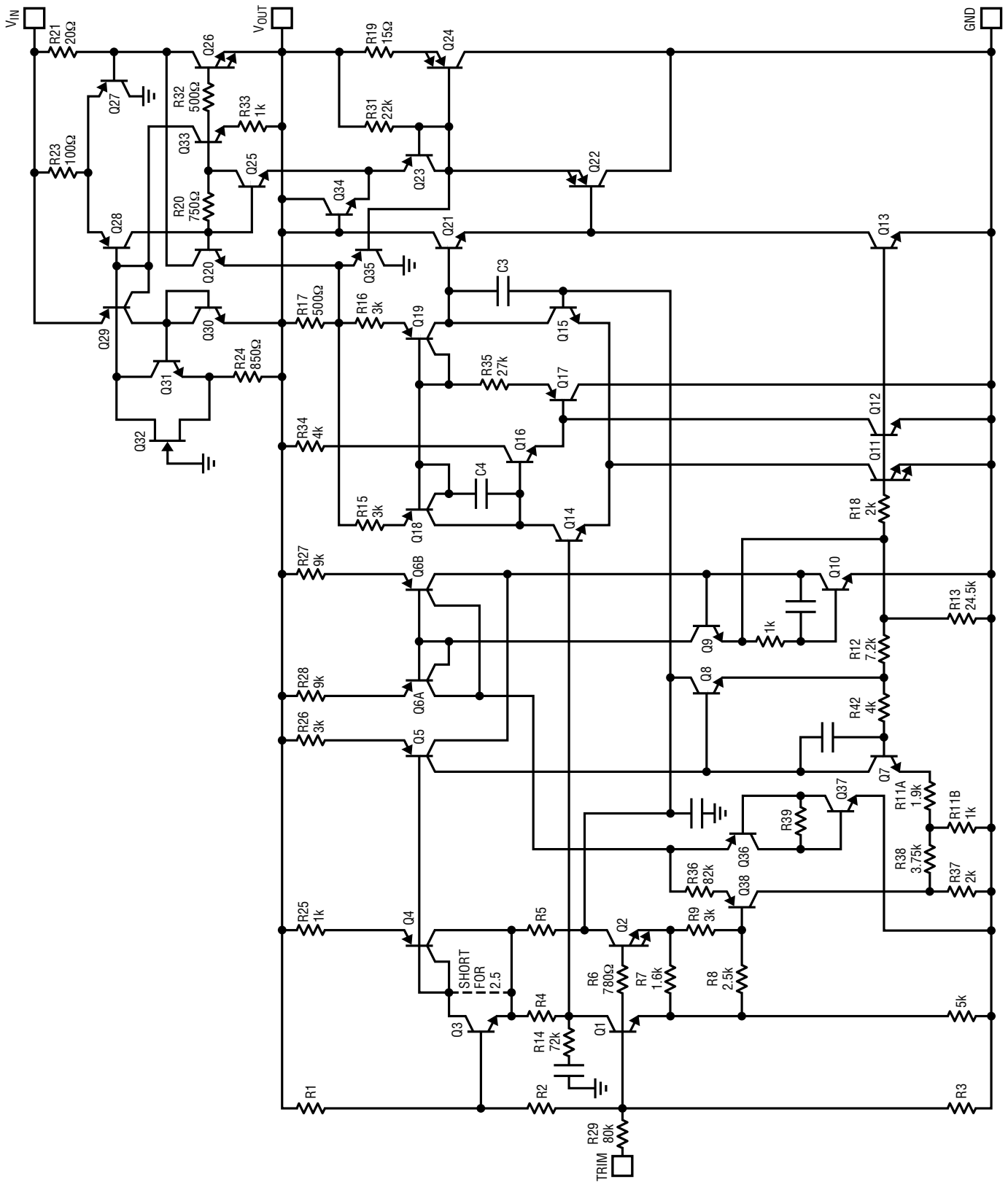
Negative Series Reference



Output Current Boost with Current Limit

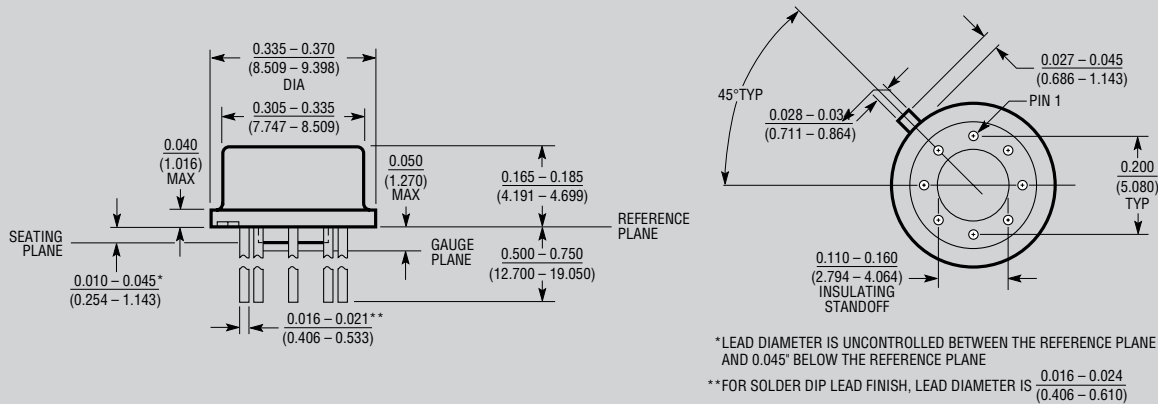


# SCHEMATIC DIAGRAM



# PACKAGE DESCRIPTION

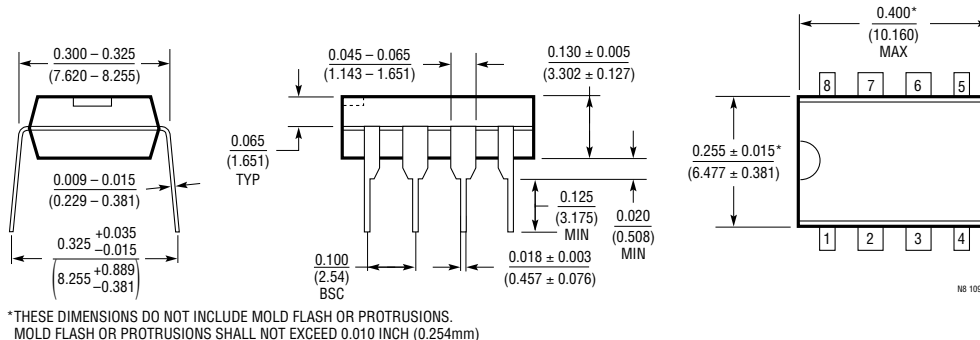
## H Package 8-Lead TO-5 Metal Can (0.200 PCD) (LTC DWG # 05-08-1320)



**OBSOLETE**

HR(TO-5) 0.200 PCD 1197

## N8 Package 8-Lead PDIP (Narrow 0.300) (LTC DWG # 05-08-1510)



## S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)

