Precision, Low Noise, High Stability Hermetic Voltage Reference

FEATURES

- Hermetic 5mm × 5mm LCC Leadless Chip Carrier Package:
  - Insensitive to Humidity
  - Thermal Hysteresis: 8ppm (0°C to 70°C)
  - Thermal Hysteresis: 12ppm (–40°C to 85°C)
- Low Drift: 5ppm/°C Max
- High Accuracy: ±0.10% Max
- Low Noise: <1ppm Peak-to-Peak (0.1Hz to 10Hz)
- Low Long Term Drift
  - 12ppm at 1000Hr
  - 18ppm at 3000Hr
- Sinks 10mA, Sources 15mA
- Wide Supply Range to 40V
- 8-Pin (5mm × 5mm) LS8 Package

APPLICATIONS

- Instrumentation and Test Equipment
- High Resolution Data Acquisition Systems
- A/D and D/A Converters
- Precision Regulators
- Precision Scales
- Digital Voltmeters

DESCRIPTION

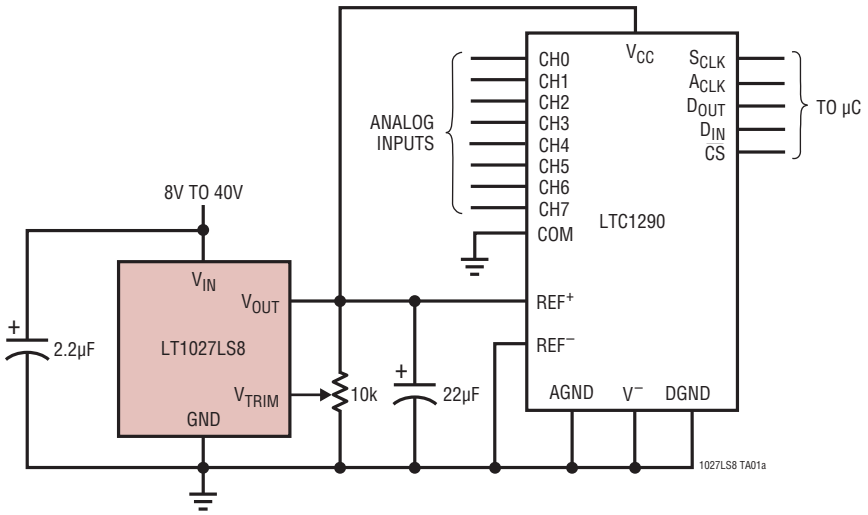
The LT®1027LS8 is a precision reference that combines low drift and noise with excellent long-term stability and high output accuracy. The reference output will source up to 15mA and sink up to 10mA, and remain constant with input voltage variations.

The hermetic package provides outstanding humidity and thermal hysteresis performance. The LT1027LS8 is only 5mm × 5mm × 1.5mm, offering an alternative to large through-hole metal can voltage references, such as the industry standard LT1021. The LT1027LS8 offers similar performance to the LT1027, with additional stability from the hermetic package.

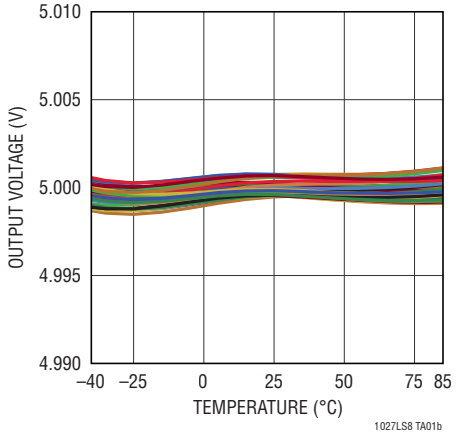
LT1027LS8 is based on a buried Zener diode structure, which enables temperature and time stability, and extremely low noise performance of < 1ppm peak-to-peak. The LT1027LS8 operates on a supply voltage from 8V up to 40V. The subsurface Zener exhibits better time stability than even the best bandgap reference, and the hermetic package maintains that stability over a wide range of environmental conditions.

TYPICAL APPLICATION

Supplying V_{REF} and V_{CC} to the LTC1290 12-Bit ADC



Output Voltage Temperature Drift

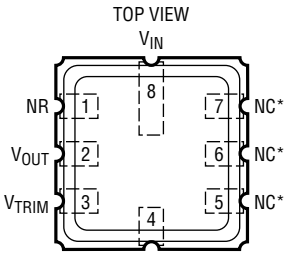


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Voltage.....40V
Input/Output Voltage Differential 35V
Output to Ground Voltage 7V
V_{TRIM} to Ground Voltage
  Positive.....5V
  Negative.....–0.3V
Output Short-Circuit Duration
  V_{IN} > 20V.....10 sec
  V_{IN} ≤ 20V..... Indefinite
Operating Temperature Range
  LT1027C..... 0°C to 70°C
  LT1027I.....–40°C to 85°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



LS8 PACKAGE
8-PIN LEADLESS CHIP CARRIER (5mm × 5mm)

*CONNECTED INTERNALLY.
DO NOT CONNECT EXTERNAL
CIRCUITRY TO THESE PINS

**SEE APPLICATIONS
INFORMATION SECTION

T_{JMAX} = 125°C, θ_{JA} = 120°C/W
PACKAGE LID IS GND

ORDER INFORMATION

(http://www.linear.com/product/LT1027LS8#orderinfo)

LEAD FREE FINISH	PART MARKING	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1027DCLS8-5#PBF	10275	8-Lead Ceramic LCC 5mm × 5mm	0°C to 70°C
LT1027DILS8-5#PBF	10275	8-Lead Ceramic LCC 5mm × 5mm	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 10V, I_{LOAD} = 0A unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage (Note 2)			4.995	5.000	5.005	V
TCV_{OUT}	Output Voltage Temperature Coefficient (Note 3)		●		2	5	ppm/°C
	Line Regulation (Note 4)	8V ≤ V_{IN} ≤ 10V	 ●		6	12 25	ppm/V ppm/V
		10V ≤ V_{IN} ≤ 40V	 ●		3	6 8	ppm/V ppm/V
	Load Regulation (Notes 4, 6)	Sourcing Current 0 ≤ I_{OUT} ≤ 15mA, 0°C to 85°C 0 ≤ I_{OUT} ≤ 5mA, –40°C	 ● 	 –8 –10 –10	 8 	 12 15 15	 ppm/mA ppm/mA ppm/mA
		Sinking Current 0 ≤ I_{OUT} ≤ 10mA 0°C to 85°C –40°C	 ● 		 30 	 120 160	 ppm/mA ppm/mA
	Supply Current		 ●		2.2	3.1 3.5	mA mA
	V_{TRIM} Adjust Range		●	±30	±50		mV
e_n	Output Noise (Note 5)	0.1Hz ≤ f ≤ 10Hz			3		μV_{P-P}
		10Hz ≤ f ≤ 1kHz			2.0	6.0	μV_{RMS}
	Long-Term Stability of Output Voltage (Note 7)	Δt = First 1000Hrs Δt = First 3000Hrs			12 18		ppm ppm
	Temperature Hysteresis of Output (Note 8)	ΔT = ±25°C ΔT = 0°C to 70°C ΔT = –40°C to 85°C			6 8 12		ppm ppm ppm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Output voltage is measured immediately after turn-on. Changes due to chip warm-up are typically less than 0.005%.

Note 3: Temperature coefficient is measured by dividing the change in output voltage over the temperature range by the change in temperature.

Note 4: Line and load regulation are measured on a pulse basis. Output changes due to die temperature change must be taken into account separately.

Note 5: RMS noise is measured with an 8-pole bandpass filter with a center frequency of 30Hz and a Q of 1.5. The filter output is then rectified and integrated for a fixed time period, resulting in an average, as opposed to RMS voltage. A correction factor is used to convert average to RMS. This value is then used to obtain RMS noise voltage in the 10Hz to 1000Hz frequency band. This test also screens for low frequency "popcorn" noise within the bandwidth of the filter.

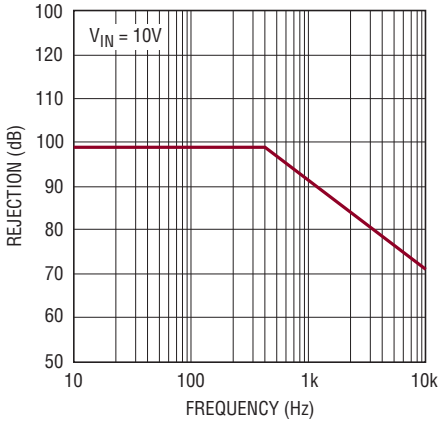
Note 6: Devices typically exhibit a slight negative DC output impedance of –0.015Ω. This compensates for PC trace resistance, improving regulation at the load.

Note 7: Long-term stability typically has a logarithmic characteristic and therefore, changes after 1000 hours tend to be much smaller than before that time. Total drift in the second thousand hours is normally less than one third that of the first thousand hours, with a continuing trend toward reduced drift with time. Significant improvement in long-term drift can be realized by preconditioning the IC with a 100-200 hour, 125°C burn in. Long term stability will also be affected by differential stresses between the IC and the board material created during board assembly. Temperature cycling and baking of completed boards is often used to reduce these stresses in critical applications.

Note 8: Hysteresis in output voltage is created by package stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to high or low temperature before successive measurements. Hysteresis is roughly proportional to the square of temperature change. Hysteresis is not normally a problem for operational temperature excursions, but can be significant in critical narrow temperature range applications where the instrument might be stored at high or low temperatures. Hysteresis measurements are preconditioned by one temperature cycle.

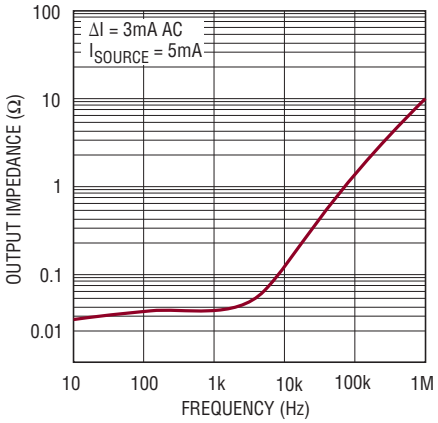
TYPICAL PERFORMANCE CHARACTERISTICS

Ripple Rejection



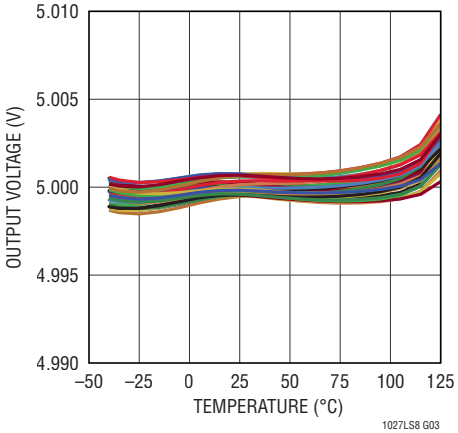
1027LS8 G01

Output Impedance vs Frequency



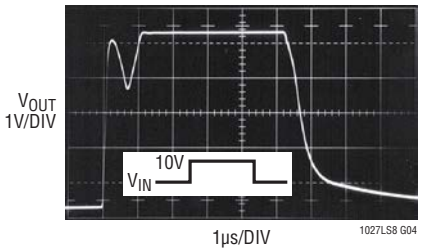
1027LS8 G02

Output Voltage Temperature Drift



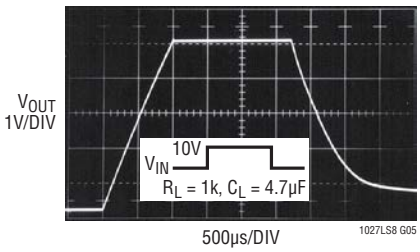
1027LS8 G03

Start-Up and Turn-Off (No Load)



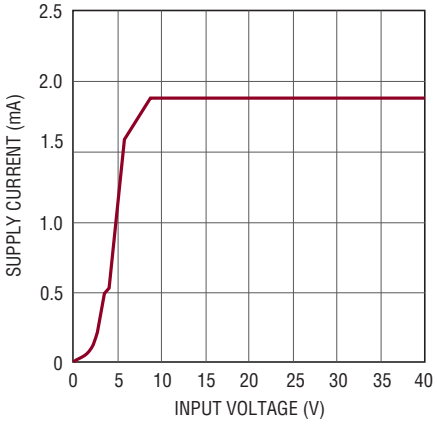
1027LS8 G04

Start-Up and Turn-Off



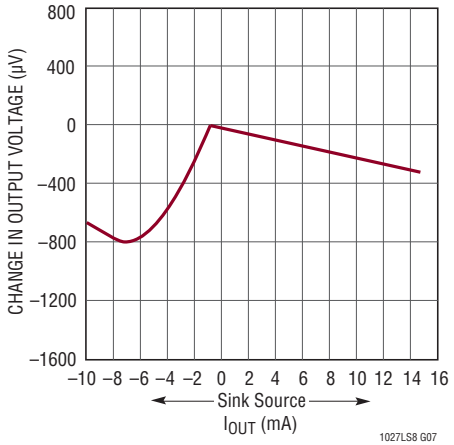
1027LS8 G05

Quiescent Current



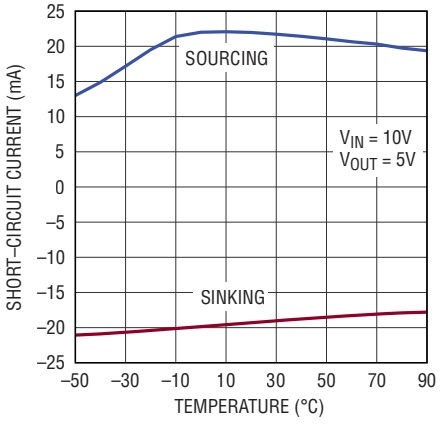
1027LS8 G06

Load Regulation



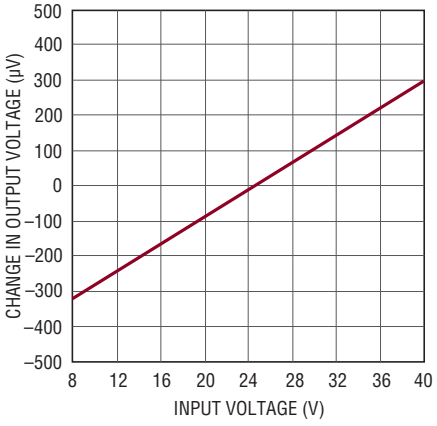
1027LS8 G07

Output Short-Circuit Current vs Temperature



1027LS8 G08

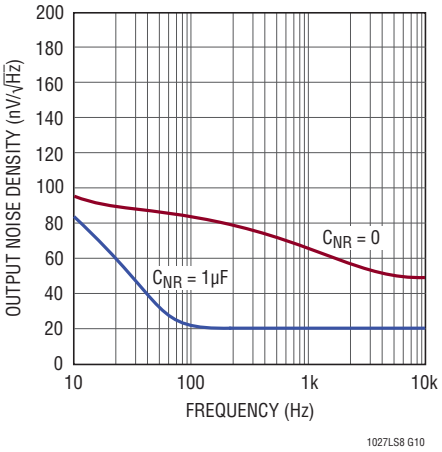
Line Regulation



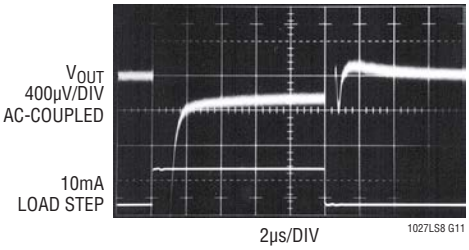
1027LS8 G09

TYPICAL PERFORMANCE CHARACTERISTICS

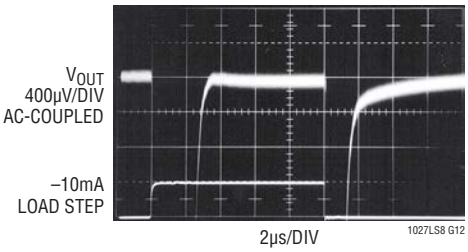
Output Noise Voltage Density



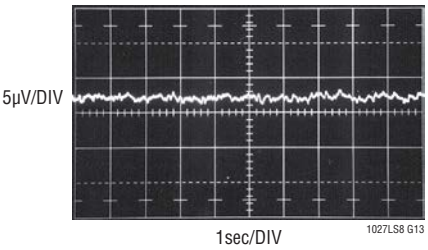
Output Settling Time (Sourcing)



Output Settling Time (Sinking)



0.1Hz to 10Hz Output Noise
Filtering = 1 Zero at 0.1Hz
2 Poles at 10Hz



PIN FUNCTIONS

NR (Pin 1): Noise Reduction Pin. Add a capacitor to reduce wideband noise. See the Applications Information section for details.

V_{OUT} (Pin 2): Output Voltage. See the Applications Information section for details regarding DC and capacitive loading and stability.

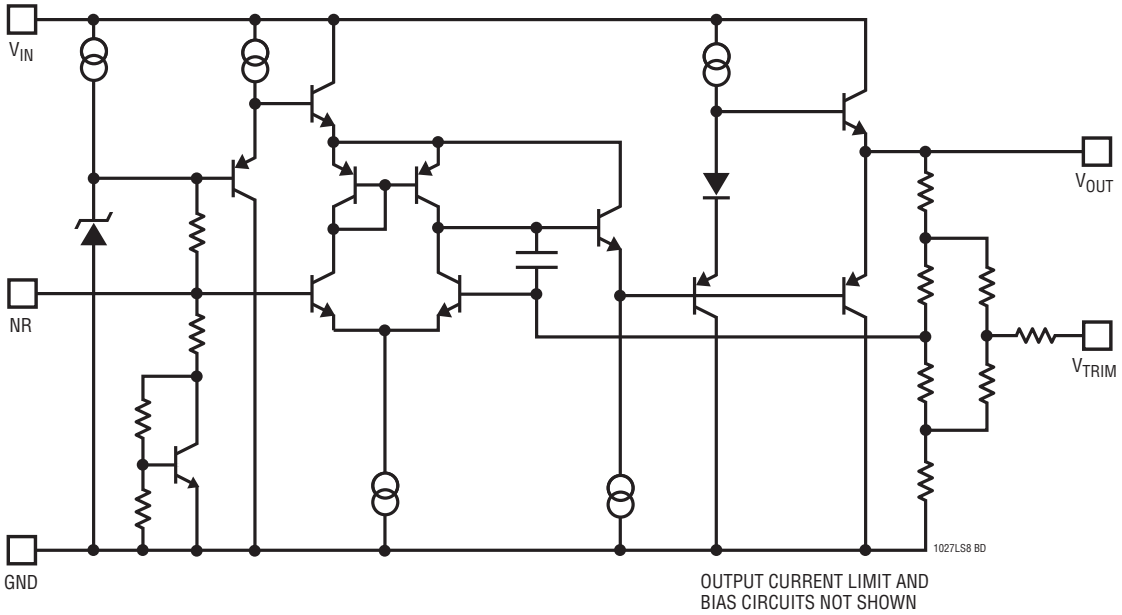
V_{TRIM} (Pin 3): Allows adjustment of output voltage. See the Applications Information section for details.

GND (Pin 4): Device Ground. See the Applications Information section for recommended connection methods.

NC (Pins 5, 6, 7): Connected internally, do not connect.

V_{IN} (Pin 8): Power Supply. Bypass with 0.1µF (or larger) capacitor to ground.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Effect of Reference Drift on System Accuracy

A large portion of the temperature drift error budget in many systems is the system reference voltage. Figure 1 indicates the maximum temperature coefficient allowable if the reference is to contribute no more than 0.5LSB error to the overall system performance. The example shown is a 12-bit system designed to operate over a temperature range from 25°C to 65°C. Assuming the system calibration is performed at 25°C, the temperature span is 40°C. It can be seen from the graph that the temperature coefficient of the reference must be no worse than 6ppm/°C if it is to contribute less than 1LSB error. For this reason, the LT1027LS8 has been optimized for low drift.

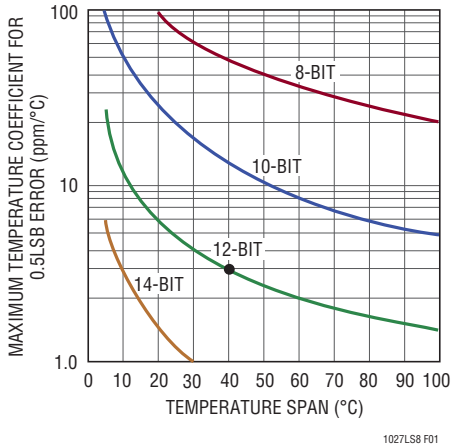


Figure 1. Maximum Allowable Reference Drift

Trimming Output Voltage

The LT1027LS8 has an adjustment pin for trimming output voltage. The impedance of the V_{TRIM} pin is approximately 20kΩ with an open-circuit voltage of 2.5V. A ±30mV guaranteed trim range is achievable by tying the V_{TRIM} pin to the wiper of a 10k potentiometer connecting between the output and ground. Trimming output voltage does not affect the TC of the device.

Noise Reduction

The positive input of the internal scaling amplifier is brought out as the Noise Reduction (NR) pin. Connecting a 1µF Mylar capacitor between this pin and ground will reduce the wideband noise of the LT1027LS8 from 2.0µV_{RMS} to approximately 1.2µV_{RMS} in a 10Hz to 1kHz bandwidth. Transient response is not affected by this capacitor. Start-up settling time will increase to several milliseconds due to the 7kΩ impedance looking into the NR pin. The capacitor *must* be a low leakage type. Electrolytics are *not* suitable for this application. Just 100nA leakage current will result in a 150ppm error in output voltage. This pin is the most sensitive pin on the device. For maximum protection a guard ring is recommended. The ring should be driven from a resistive divider from V_{OUT} set to 4.4V (the open-circuit voltage on the NR pin).

Transient Response

The LT1027LS8 has been optimized for transient response. Settling time is under 2µs when an AC-coupled 10mA load transient is applied to the output. The LT1027LS8 achieves fast settling by using a class B NPN/PNP output stage. When sinking current, the device may oscillate with capacitive loads greater than 100pF. The LT1027LS8 is stable with all capacitive loads when at no DC load or when sourcing current, although for best settling time either no output bypass capactor or a 4.7µF tantalum unit is recommended. An 0.1µF ceramic output capacitor will *maximize output ringing* and is *not* recommended.

Kelvin Connections

Although the LT1027LS8 does not have true force-sense capability, proper hook-up can improve line loss and ground loop problems significantly. Since the ground pin of the LT1027LS8 carries only 2mA, it can be used as a low-side sense line, greatly reducing ground loop problems on the low side of the reference. The V_{OUT} pin should be close to the load or connected via a heavy trace as the resistance of this trace directly affects load regulation. It is important to remember that a 1.22mV drop due to trace resistance is equivalent to a 1LSB error in a $5V_{FS}$, 12-bit system.

APPLICATIONS INFORMATION

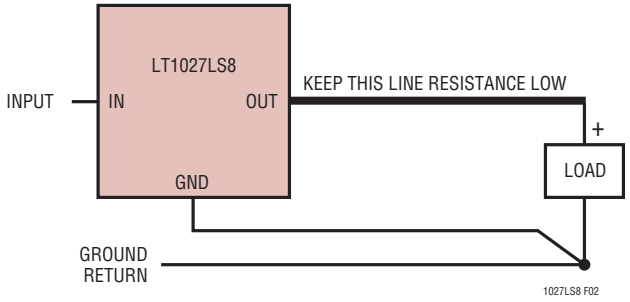
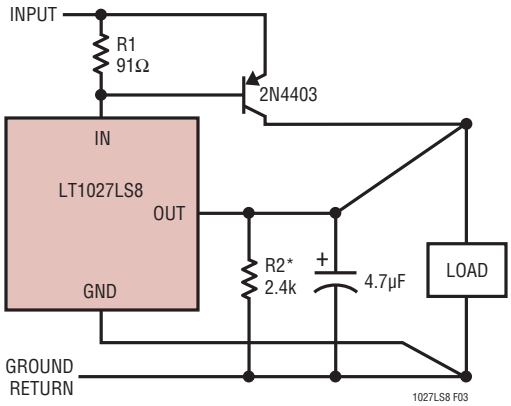


Figure 2. Standard Connection



*OPTIONAL–REDUCES CURRENT IN OUTPUT SENSE LEAD

Figure 3. Driving Higher Load Currents

The circuits in Figure 2 and Figure 3 illustrate proper connections to minimize errors due to ground loops and line losses. Losses in the output lead can be further reduced by adding a PNP boost transistor if load current is 5mA or higher. R2 can be added to further reduce current in the output sense load.

Long-Term Drift

Long-term drift cannot be extrapolated from accelerated high temperature testing. This erroneous technique gives drift numbers that are wildly optimistic. The only way long-term drift can be determined is to measure it over the time interval of interest.

The LT1027LS8 long-term drift data was collected on 80 parts that were soldered into printed circuit boards similar to a *real world* application. The boards were then placed into a constant temperature oven with a T_A = 35°C, their outputs were scanned regularly and measured with an 8.5 digit DVM. Typical long-term drift is illustrated in Figure 4.

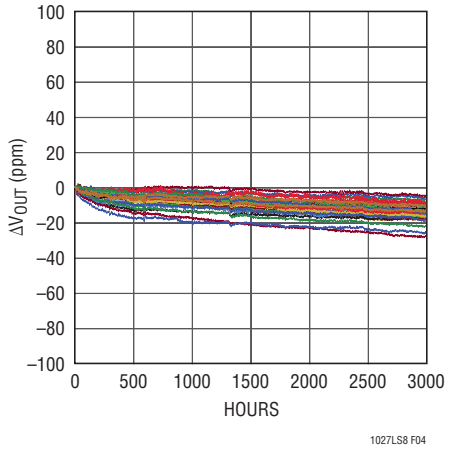


Figure 4. Long-Term Drift

APPLICATIONS INFORMATION

Hysteresis

Thermal hysteresis is a measure of change of output voltage as a result of temperature cycling. Figure 5, Figure 6 and Figure 7 illustrate the typical hysteresis based on data taken from the LT1027LS8. A proprietary design technique minimizes thermal hysteresis.

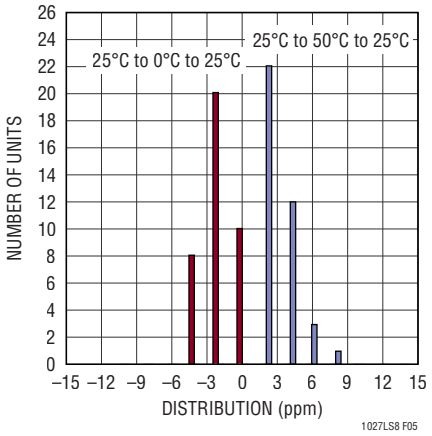


Figure 5. Thermal Hysteresis Plot, 0°C to 50°C

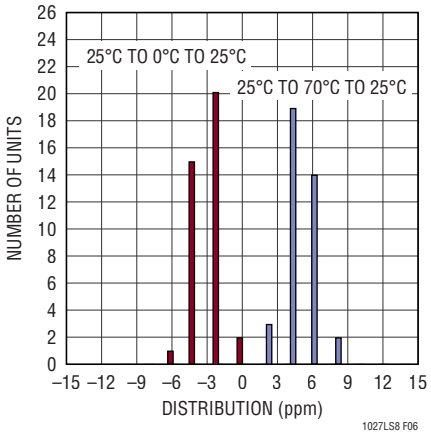


Figure 6. Thermal Hysteresis Plot, 0°C to 70°C

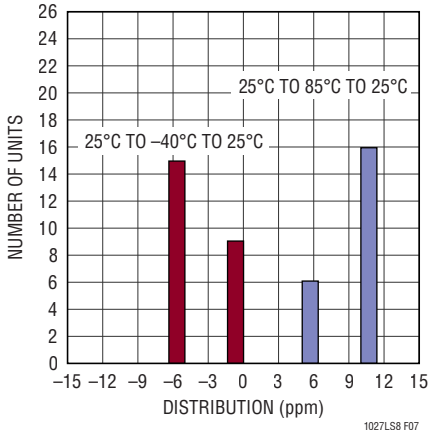


Figure 7. Thermal Hysteresis Plot, –40°C to 85°C

TYPICAL APPLICATIONS

Humidity Sensitivity

Plastic mold compounds absorb water. With changes in relative humidity, plastic packaging materials change the amount of pressure they apply to the die inside. These pressure changes can cause slight changes in the output of a voltage reference, usually on the order of 100ppm. The LS8 package is hermetic, so it is not affected by humidity, and is therefore more stable in environments where humidity may be a concern. However, PC board material may absorb water and apply mechanical stress to the LT1027LS8. Proper board materials and layout are essential.

For best stability, the PC board layout is critical. Change in temperature and position of the PC board, as well as aging, can alter the mechanical stress applied to components soldered to the board. FR4 and similar materials also absorb water, causing the board to swell. Even conformal coating or potting of the board does not always eliminate this effect, though it may delay the symptoms by reducing the rate of absorption.

Power and ground planes should be omitted under the voltage reference IC for best stability. Figure 8a shows a tab cut through the PC board on three sides of an LT1027LS8, which significantly reduces stress on the IC, as described in Application Note 82. For even better performance, Figure 8b shows slots cut through the PC board on all four sides. The slots should be as long as possible, and the corners just large enough to accommodate routing of traces. It has been shown that for PC boards designed in this way, humidity sensitivity can be reduced to less than 35ppm for a change in relative humidity of approximately 60%. Mounting the reference near the center of the board, with slots on four sides, can further reduce the sensitivity to less than 10ppm.

An additional advantage of slotting the PC board is that the LT1027LS8 is thermally isolated from surrounding circuitry. This separation can help reduce thermocouple effects and improve accuracy.

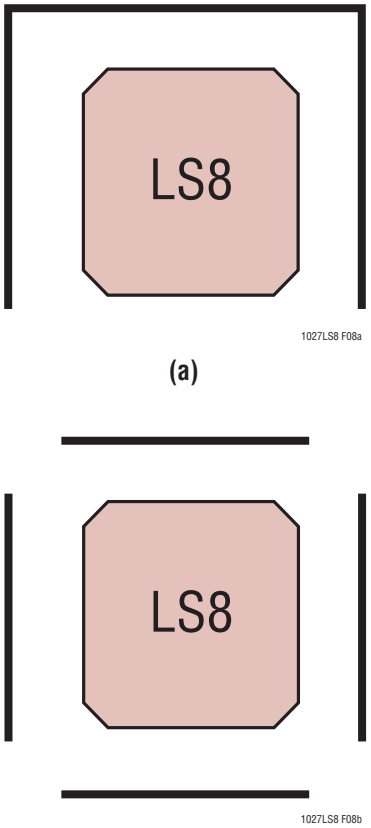


Figure 8. (a) 3-Sided PCB Tab Cutout, (b) 4-Sided PCB Cutout. Lines Represent Cuts All the Way Through the PCB

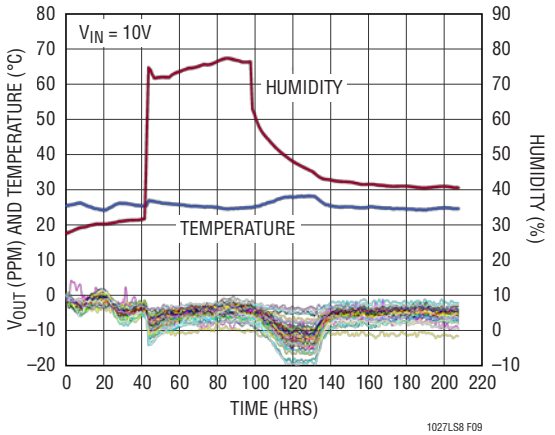
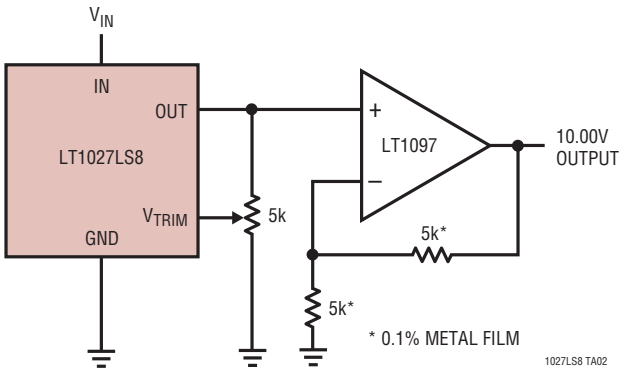


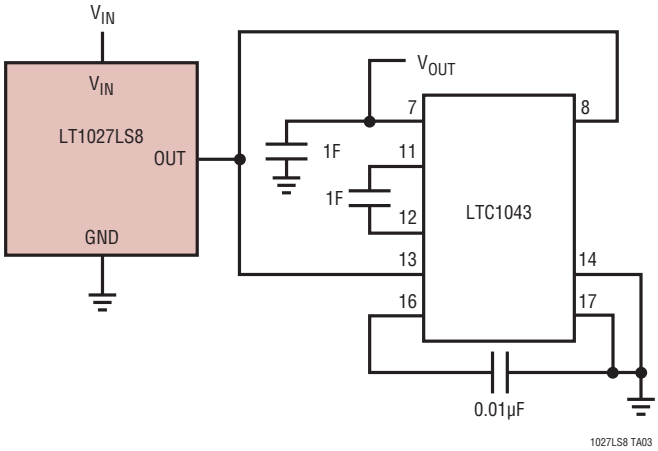
Figure 9. Illustrates Drift of LT1027LS8 with Large Changes in Humidity. Using Proper PCB Layout Techniques Limits This Drift to a Few ppm

TYPICAL APPLICATIONS

10V Reference

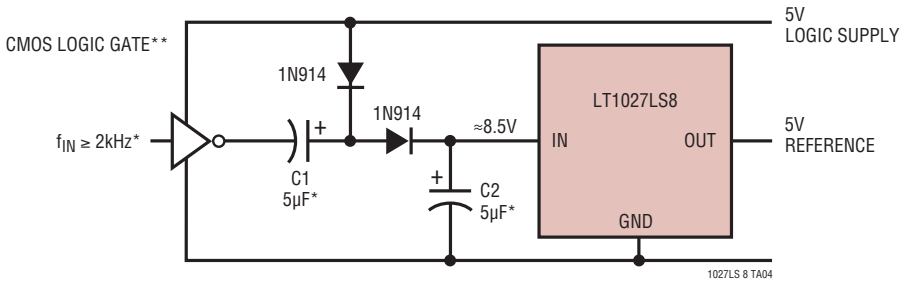


10V Reference



TYPICAL APPLICATIONS

Operating 5V Reference from 5V Supply

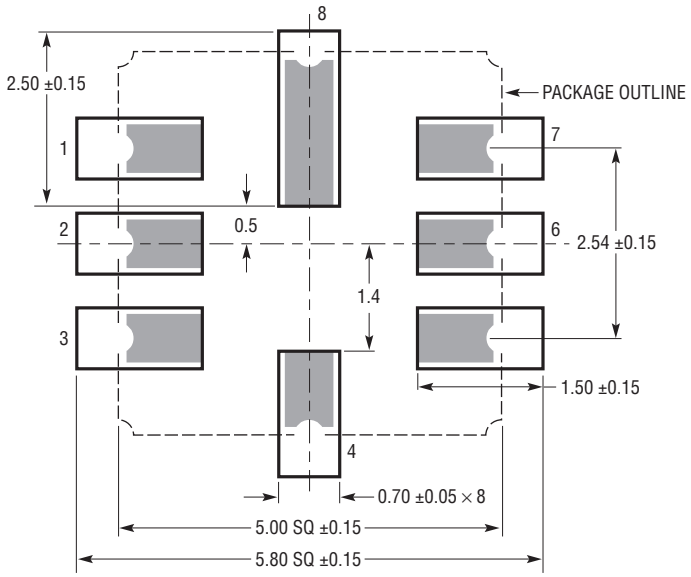


*FOR HIGHER FREQUENCIES C1 AND C2 MAY BE DECREASED
**PARALLEL GATES FOR HIGHER REFERENCE CURRENT LOADING

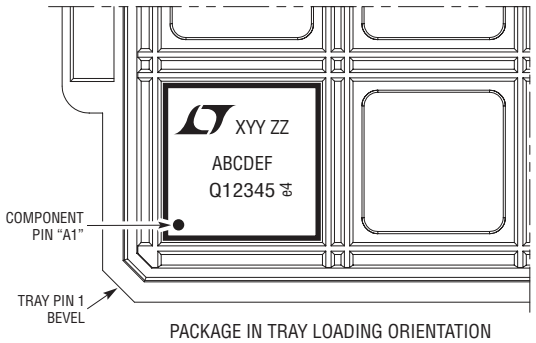
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT1027LS8#packaging/ for the most recent package drawings.

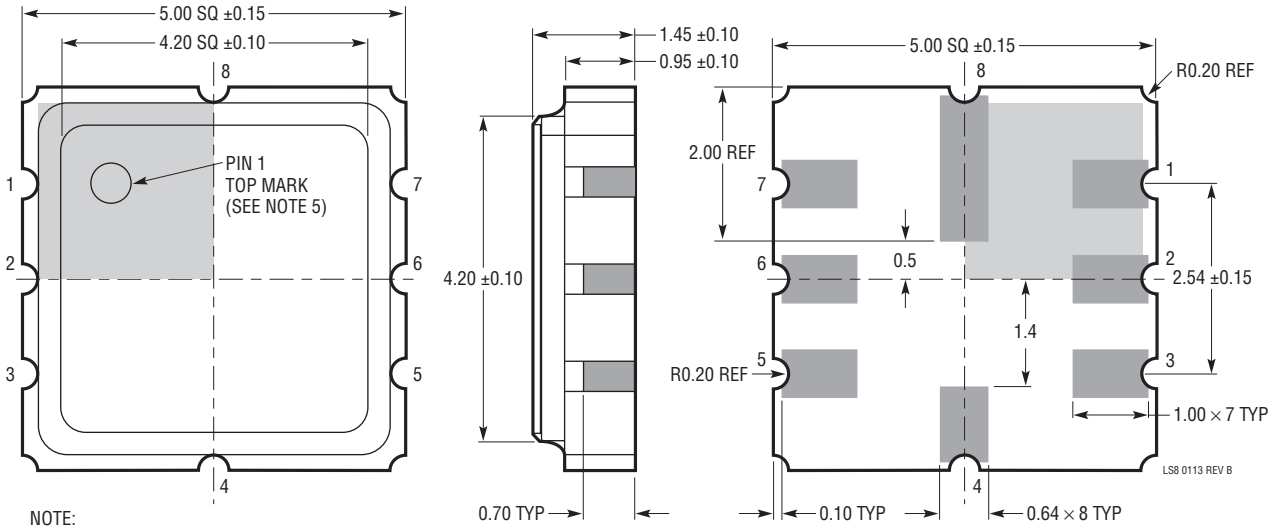
LS8 Package
8-Pin Leadless Chip Carrier (5mm × 5mm)
(Reference LTC DWG # 05-08-1852 Rev B)



APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



PACKAGE IN TRAY LOADING ORIENTATION



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS PACKAGE DO NOT INCLUDE PLATING BURRS
   PLATING BURRS, IF PRESENT, SHALL NOT EXCEED 0.30mm ON ANY SIDE
4. PLATING—ELECTO NICKEL MIN 1.25UM, ELECTRO GOLD MIN 0.30UM
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE