# Ultralow Noise Precision High Speed Op Amps

## FEATURES

- Voltage Noise
  - 1.1nV/√Hz Max at 1kHz
  - 0.85nV/√Hz Typ at 1kHz
  - 1.0nV/√Hz Typ at 10Hz
  - $35nV_{P-P}$ Typ, 0.1Hz to 10Hz
- Voltage and Current Noise 100% Tested
- Gain-Bandwidth Product
  - LT1028: 50MHz Min
  - LT1128: 13MHz Min
- Slew Rate
  - LT1028: 11V/μs Min
  - LT1128: 5V/μs Min
- Offset Voltage: 40μV Max
- Drift with Temperature: 0.8μV/°C Max
- Voltage Gain: 7 Million Min
- Available in 8-Lead SO Package

## APPLICATIONS

- Low Noise Frequency Synthesizers
- High Quality Audio
- Infrared Detectors
- Accelerometer and Gyro Amplifiers
- 350Ω Bridge Signal Conditioning
- Magnetic Search Coil Amplifiers
- Hydrophone Amplifiers

## DESCRIPTION

The LT®1028(gain of –1 stable)/LT1128(gain of +1 stable) achieve a new standard of excellence in noise performance with 0.85nV/√Hz 1kHz noise, 1.0nV/√Hz 10Hz noise. This ultralow noise is combined with excellent high speed specifications (gain-bandwidth product is 75MHz for LT1028, 20MHz for LT1128), distortion-free output, and true precision parameters (0.1μV/°C drift, 10μV offset voltage, 30 million voltage gain). Although the LT1028/LT1128 input stage operates at nearly 1mA of collector current to achieve low voltage noise, input bias current is only 25nA.

The LT1028/LT1128's voltage noise is less than the noise of a 50Ω resistor. Therefore, even in very low source impedance transducer or audio amplifier applications, the LT1028/LT1128's contribution to total system noise will be negligible.

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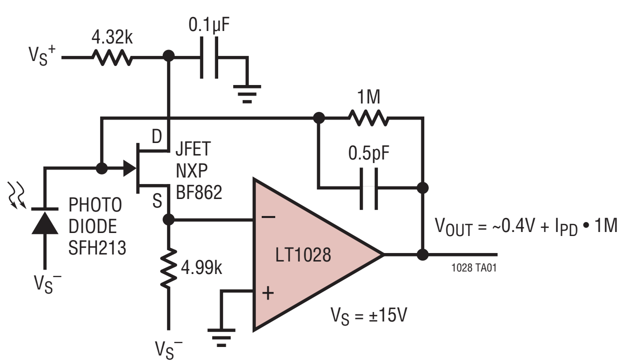
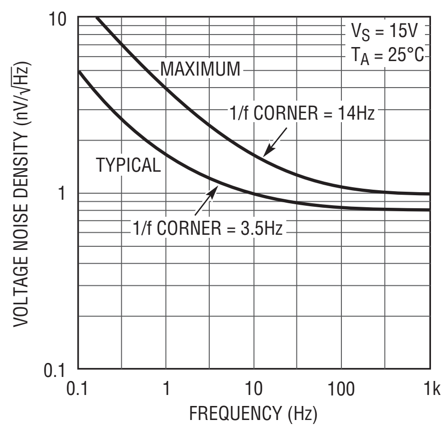
## TYPICAL APPLICATION

**Ultralow Noise 1M TIA Photodiode Amplifier**




**Voltage Noise vs Frequency**



## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Supply Voltage
- –55°C to 105°C ................................................ ±22V
- 105°C to 125°C ................................................ ±16V

Differential Input Current (Note 9) ......................±25mA
Input Voltage............................Equal to Supply Voltage
Output Short-Circuit Duration .......................... Indefinite

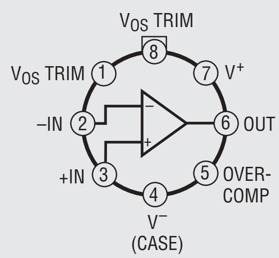
Operating Temperature Range
- LT1028/LT1128AM, M **(OBSOLETE)**... –55°C to 125°C
- LT1028/LT1128AC, C (Note 11) ............–40°C to 85°C

Storage Temperature Range
- All Devices ........................................–65°C to 150°C

Lead Temperature (Soldering, 10 sec.)..................300°C

## PIN CONFIGURATION

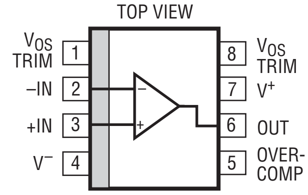
TOP VIEW




H PACKAGE
8-LEAD TO-5 METAL CAN
$T_{JMAX}$ = 175°C, $\theta_{JA}$ = 140°C/W, $\theta_{JC}$ = 40°C/W

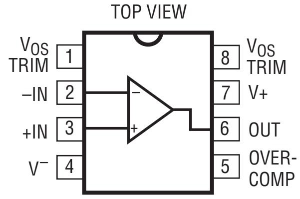
**OBSOLETE PACKAGE**

TOP VIEW




S8 PACKAGE
8-LEAD PLASTIC SOIC
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 140°C/W

TOP VIEW

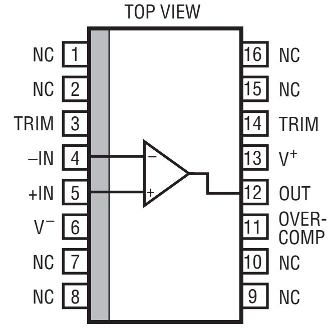



N8 PACKAGE
8-LEAD PLASTIC DIP
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 150°C/W

J8 PACKAGE
8-LEAD CERAMIC DIP
$T_{JMAX}$ = 175°C, $\theta_{JA}$ = 140°C/W, $\theta_{JC}$ = 40°C/W

**OBSOLETE PACKAGE**

TOP VIEW




SW PACKAGE
16-LEAD PLASTIC SOL
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 130°C/W
NOTE: THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGNS

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE |
|---|---|---|---|---|
| LT1028ACN8#PBF | N/A | LT1028ACN8 | 8-Lead PDIP | 0°C to 70°C |
| LT1028CN8#PBF | N/A | LT1028CN8 | 8-Lead PDIP | 0°C to 70°C |
| LT1128ACN8#PBF | N/A | LT1128ACN8 | 8-Lead PDIP | 0°C to 70°C |
| LT1128CN8#PBF | N/A | LT1128CN8 | 8-Lead PDIP | 0°C to 70°C |
| LT1028CS8#PBF | LT1028CS8#TRPBF | 1028 | 8-Lead Plastic Small Outline | 0°C to 70°C |
| LT1128CS8#PBF | LT1128CS8#TRPBF | 1128 | 8-Lead Plastic Small Outline | 0°C to 70°C |
| LT1028CSW#PBF | LT1028CSW#TRPBF | LT1028CSW | 16-Lead Plastic SOIC (Wide) | 0°C to 70°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$ unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | | LT1028AM/AC LT1128AM/AC MIN | TYP | MAX | LT1028M/C LT1128M/C MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | (Note 2) | | | 10 | 40 | | 20 | 80 | µV |
| $\frac{\Delta V_{OS}}{\Delta Time}$ | Long Term Input Offset Voltage Stability | (Note 3) | | | 0.3 | | | 0.3 | | µV/Mo |
| $I_{OS}$ | Input Offset Current | $V_{CM} = 0V$ | | | 12 | 50 | | 18 | 100 | nA |
| $I_B$ | Input Bias Current | $V_{CM} = 0V$ | | | ±25 | ±90 | | ±30 | ±180 | nA |
| $e_n$ | Input Noise Voltage | 0.1Hz to 10Hz (Note 4) | | | 35 | 75 | | 35 | 90 | $nV_{P-P}$ |
| | Input Noise Voltage Density | $f_O = 10Hz$ (Note 5)<br>$f_O = 1000Hz$, 100% Tested | | | 1.00<br>0.85 | 1.7<br>1.1 | | 1.0<br>0.9 | 1.9<br>1.2 | $nV/\sqrt{Hz}$<br>$nV/\sqrt{Hz}$ |
| $I_n$ | Input Noise Current Density | $f_O = 10Hz$ (Notes 4 and 6)<br>$f_O = 1000Hz$, 100% Tested | | | 4.7<br>1.0 | 10.0<br>1.6 | | 4.7<br>1.0 | 12.0<br>1.8 | $pA/\sqrt{Hz}$<br>$pA/\sqrt{Hz}$ |
| | Input Resistance<br>Common Mode<br>Differential Mode | | | | <br>300<br>20 | | | <br>300<br>20 | | <br>MΩ<br>kΩ |
| | Input Capacitance | | | | 5 | | | 5 | | pF |
| | Input Voltage Range | | | ±11.0 | ±12.2 | | ±11.0 | ±12.2 | | V |
| CMRR | Common Mode Rejection Ratio | $V_{CM} = \pm11V$ | | 114 | 126 | | 110 | 126 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_S = \pm4V$ to $\pm18V$ | | 117 | 133 | | 110 | 132 | | dB |
| $A_{VOL}$ | Large-Signal Voltage Gain | $R_L \geq 2k$, $V_O = \pm12V$<br>$R_L \geq 1k$, $V_O = \pm10V$<br>$R_L \geq 600\Omega$, $V_O = \pm10V$ | | 7.0<br>5.0<br>3.0 | 30.0<br>20.0<br>15.0 | | 5.0<br>3.5<br>2.0 | 30.0<br>20.0<br>15.0 | | V/µV<br>V/µV<br>V/µV |
| $V_{OUT}$ | Maximum Output Voltage Swing | $R_L \geq 2k$<br>$R_L \geq 600\Omega$ | | ±12.3<br>±11.0 | ±13.0<br>±12.2 | | ±12.0<br>±10.5 | ±13.0<br>±12.2 | | V<br>V |
| SR | Slew Rate | $A_{VCL} = -1$<br>$A_{VCL} = -1$ | LT1028<br>LT1128 | 11.0<br>5.0 | 15.0<br>6.0 | | 11.0<br>4.5 | 15.0<br>6.0 | | V/µs<br>V/µs |
| GBW | Gain-Bandwidth Product | $f_O = 20kHz$ (Note 7)<br>$f_O = 200kHz$ (Note 7) | LT1028<br>LT1128 | 50<br>13 | 75<br>20 | | 50<br>11 | 75<br>20 | | MHz<br>MHz |
| $Z_O$ | Open-Loop Output Impedance | $V_O = 0$, $I_O = 0$ | | | 80 | | | 80 | | Ω |
| $I_S$ | Supply Current | | | | 7.4 | 9.5 | | 7.6 | 10.5 | mA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the operating temperature range –55°C ≤ $T_A$ ≤ 125°C. $V_S$ = ±15V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | LT1028AM LT1128AM MIN | TYP | MAX | LT1028M LT1128M MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | (Note 2) | ● | | 30 | 120 | | 45 | 180 | µV |
| $\frac{\Delta V_{OS}}{\Delta Temp}$ | Average Input Offset Drift | (Note 8) | ● | | 0.2 | 0.8 | | 0.25 | 1.0 | µV/°C |
| $I_{OS}$ | Input Offset Current | $V_{CM}$ = 0V | ● | | 25 | 90 | | 30 | 180 | nA |
| $I_B$ | Input Bias Current | $V_{CM}$ = 0V | ● | | ±40 | ±150 | | ±50 | ±300 | nA |
| | Input Voltage Range | | ● | ±10.3 | ±11.7 | | ±10.3 | ±11.7 | | V |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ = ±10.3V | ● | 106 | 122 | | 100 | 120 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_S$ = ±4.5V to ±16V | ● | 110 | 130 | | 104 | 130 | | dB |
| $A_{VOL}$ | Large-Signal Voltage Gain | $R_L$ ≥ 2k, $V_O$ = ±10V<br>$R_L$ ≥ 1k, $V_O$ = ±10V | ● | 3.0<br>2.0 | 14.0<br>10.0 | | 2.0<br>1.5 | 14.0<br>10.0 | | V/µV<br>V/µV |
| $V_{OUT}$ | Maximum Output Voltage Swing | $R_L$ ≥ 2k | ● | ±10.3 | ±11.6 | | ±10.3 | ±11.6 | | V |
| $I_S$ | Supply Current | | ● | | 8.7 | 11.5 | | 9.0 | 13.0 | mA |

**The ● denotes the specifications which apply over the operating temperature range 0°C ≤ $T_A$ ≤ 70°C. $V_S$ = ±15V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | LT1028AC LT1128AC MIN | TYP | MAX | LT1028C LT1128C MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | (Note 2) | ● | | 15 | 80 | | 30 | 125 | µV |
| $\frac{\Delta V_{OS}}{\Delta Temp}$ | Average Input Offset Drift | (Note 8) | ● | | 0.1 | 0.8 | | 0.2 | 1.0 | µV/°C |
| $I_{OS}$ | Input Offset Current | $V_{CM}$ = 0V | ● | | 15 | 65 | | 22 | 130 | nA |
| $I_B$ | Input Bias Current | $V_{CM}$ = 0V | ● | | ±30 | ±120 | | ±40 | ±240 | nA |
| | Input Voltage Range | | ● | ±10.5 | ±12.0 | | ±10.5 | ±12.0 | | V |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$= ±10.5V | ● | 110 | 124 | | 106 | 124 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_S$ = ±4.5V to ±18V | ● | 114 | 132 | | 107 | 132 | | dB |
| $A_{VOL}$ | Large-Signal Voltage Gain | $R_L$ ≥ 2k, $V_O$ = ±10V<br>$R_L$ ≥ 1k, $V_O$ = ±10V | ● | 5.0<br>4.0 | 25.0<br>18.0 | | 3.0<br>2.5 | 25.0<br>18.0 | | V/µV<br>V/µV |
| $V_{OUT}$ | Maximum Output Voltage Swing | $R_L$ ≥ 2k<br>$R_L$ ≥ 600Ω (Note 10) | ● | ±11.5<br>±9.5 | ±12.7<br>±11.0 | | ±11.5<br>±9.0 | ±12.7<br>±10.5 | | V<br>V |
| $I_S$ | Supply Current | | ● | | 8.0 | 10.5 | | 8.2 | 11.5 | mA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the operating temperature range –40°C ≤ $T_A$ ≤ 85°C. $V_S$ = ±15V, unless otherwise noted. (Note 11)**

| SYMBOL | PARAMETER | CONDITIONS | | LT1028AC LT1128AC MIN | TYP | MAX | LT1028C LT1128C MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | | ● | | 20 | 95 | | 35 | 150 | µV |
| $\frac{\Delta V_{OS}}{\Delta Temp}$ | Average Input Offset Drift | (Note 8) | ● | | 0.2 | 0.8 | | 0.25 | 1.0 | µV/°C |
| $I_{OS}$ | Input Offset Current | $V_{CM}$ = 0V | ● | | 20 | 80 | | 28 | 160 | nA |
| $I_B$ | Input Bias Current | $V_{CM}$ = 0V | ● | | ±35 | ±140 | | ±45 | ±280 | nA |
| | Input Voltage Range | | ● | ±10.4 | ±11.8 | | ±10.4 | ±11.8 | | V |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ = ±10.5V | ● | 108 | 123 | | 102 | 123 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_S$ = ±4.5V to ±18V | ● | 112 | 131 | | 106 | 131 | | dB |
| $A_{VOL}$ | Large-Signal Voltage Gain | $R_L$ ≥ 2k, $V_O$ = ±10V<br>$R_L$ ≥ 1k, $V_O$ = ±10V | ● | 4.0<br>3.0 | 20.0<br>14.0 | | 2.5<br>2.0 | 20.0<br>14.0 | | V/µV<br>V/µV |
| $V_{OUT}$ | Maximum Output Voltage Swing | $R_L$ ≥ 2k | ● | ±11.0 | ±12.5 | | ±11.0 | ±12.5 | | V |
| $I_S$ | Supply Current | | ● | | 8.5 | 11.0 | | 8.7 | 12.5 | mA |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 sec. after application of power. In addition, at $T_A$ = 25°C, offset voltage is measured with the chip heated to approximately 55°C to account for the chip temperature rise when the device is fully warmed up.

**Note 3:** Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in $V_{OS}$ during the first 30 days are typically 2.5µV.

**Note 4:** This parameter is tested on a sample basis only.

**Note 5:** 10Hz noise voltage density is sample tested on every lot with the exception of the S8 and S16 packages. Devices 100% tested at 10Hz are available on request.

**Note 6:** Current noise is defined and measured with balanced source resistors. The resultant voltage noise (after subtracting the resistor noise on an RMS basis) is divided by the sum of the two source resistors to obtain current noise. Maximum 10Hz current noise can be inferred from 100% testing at 1kHz.

**Note 7:** Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

**Note 8:** This parameter is not 100% tested.

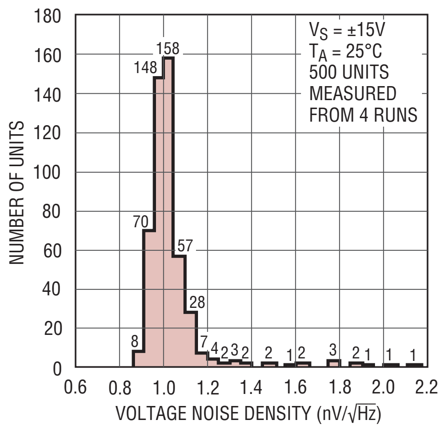
Note 9: The inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±1.8V, the input current should be limited to 25mA.

**Note 10:** This parameter guaranteed by design, fully warmed up at $T_A$ = 70°C. It includes chip temperature increase due to supply and load currents.

**Note 11:** The LT1028/LT1128 are designed, characterized and expected to meet these extended temperature limits, but are not tested at –40°C and 85°C. Guaranteed I-grade parts are available. Consult factory.

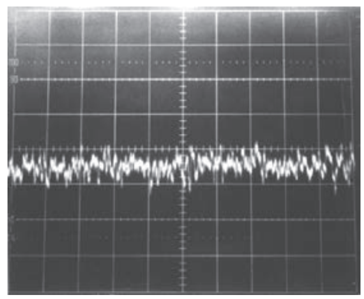
# TYPICAL PERFORMANCE CHARACTERISTICS

### 10Hz Voltage Noise Distribution




1028 G01

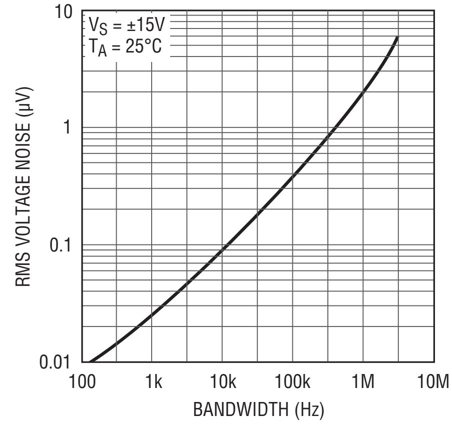
### Wideband Noise, DC to 20kHz



VERTICAL SCALE = 0.5μV/DIV
HORIZONTAL SCALE = 0.5ms/DIV

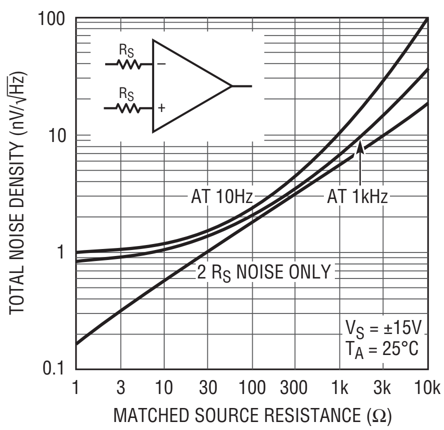
1028 G02

### Wideband Voltage Noise (0.1Hz to Frequency Indicated)



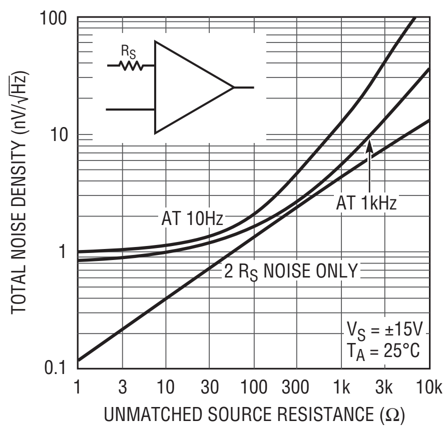

1028 G03

### Total Noise vs Matched Source Resistance



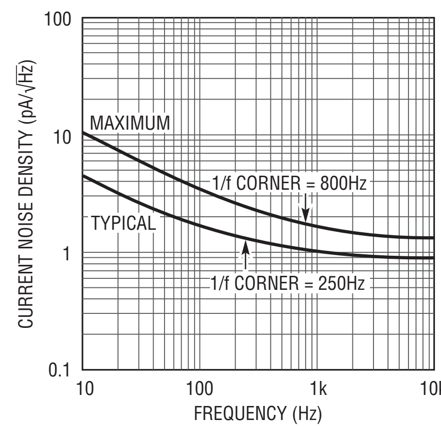

1028 G04

### Total Noise vs Unmatched Source Resistance



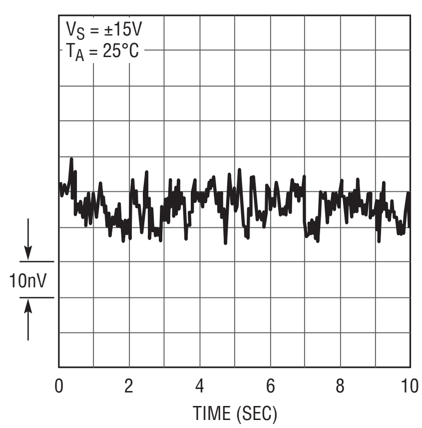

1028 G05

### Current Noise Spectrum



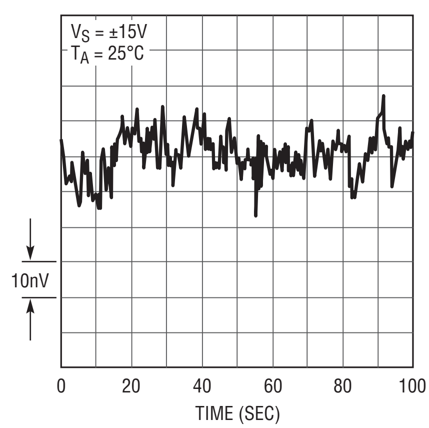

1028 G06

### 0.1Hz to 10Hz Voltage Noise



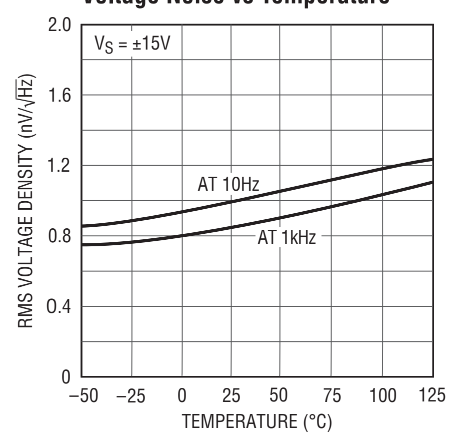

1028 G07

### 0.01Hz to 1Hz Voltage Noise




1028 G08

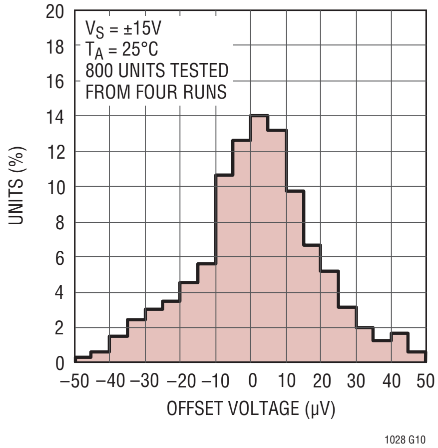
### Voltage Noise vs Temperature



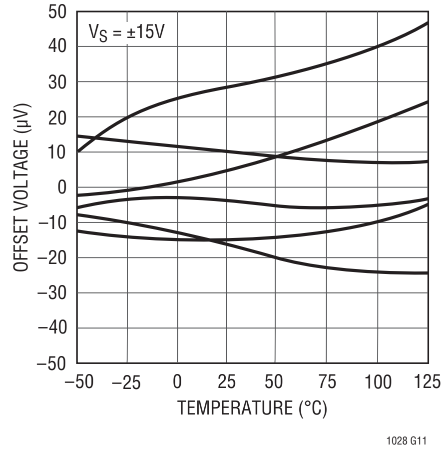

1028 G09

# TYPICAL PERFORMANCE CHARACTERISTICS

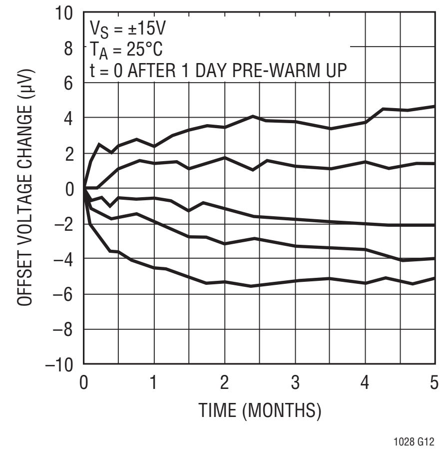
### Distribution of Input Offset Voltage



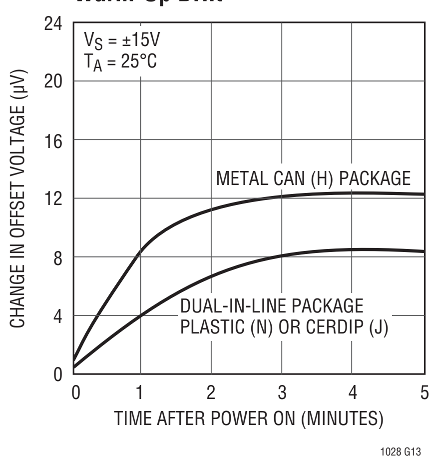

### Offset Voltage Drift with Temperature of Representative Units



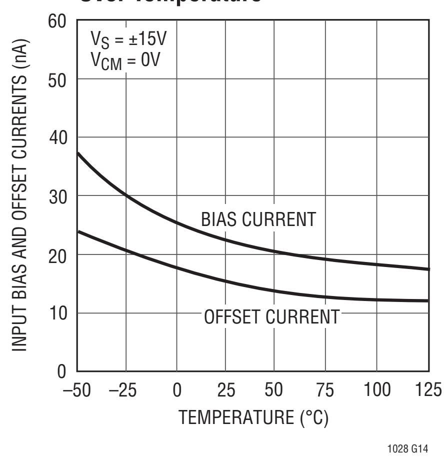

### Long-Term Stability of Five Representative Units



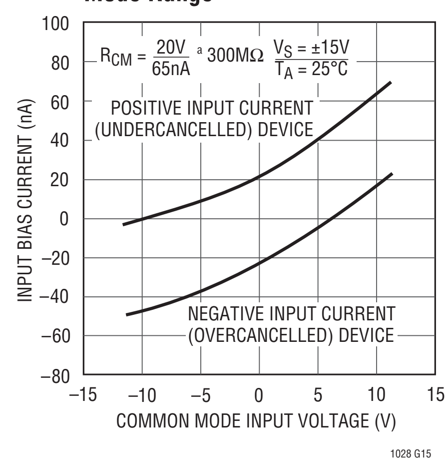

### Warm-Up Drift



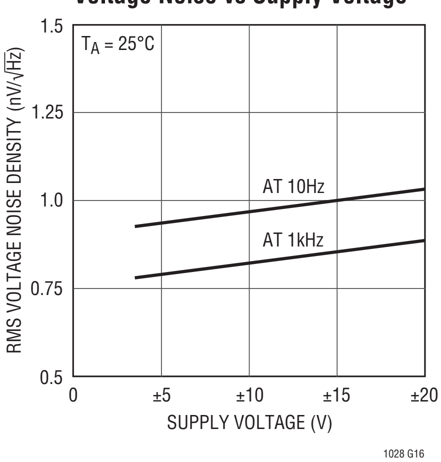

### Input Bias and Offset Currents Over Temperature



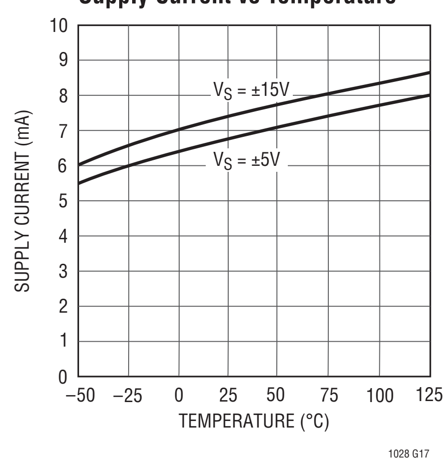

### Bias Current Over the Common Mode Range



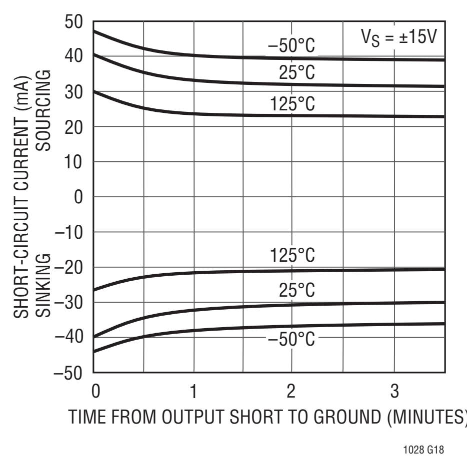

### Voltage Noise vs Supply Voltage




### Supply Current vs Temperature

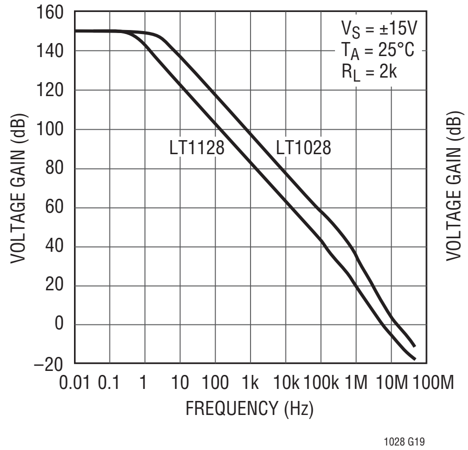



### Output Short-Circuit Current vs Time

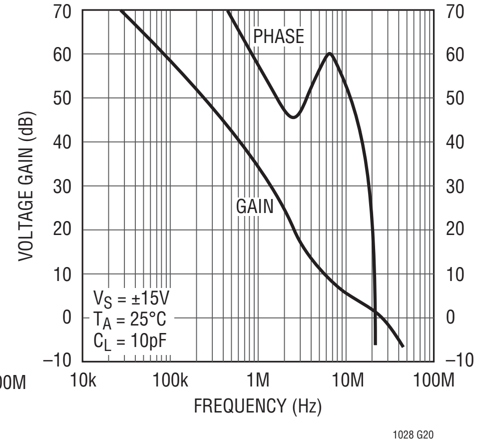


## TYPICAL PERFORMANCE CHARACTERISTICS

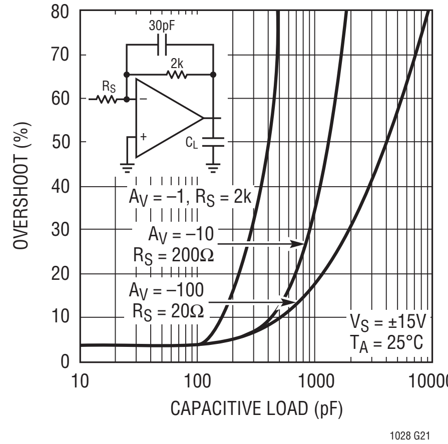
### Voltage Gain vs Frequency



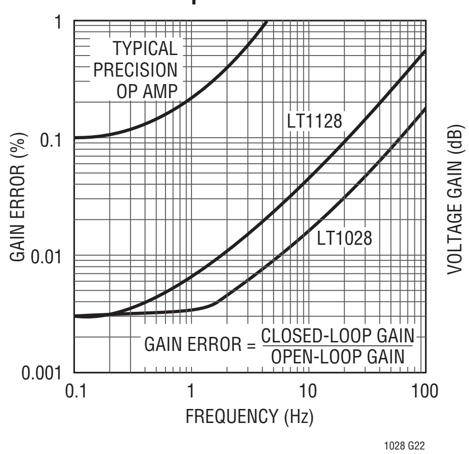

### LT1028
### Gain, Phase vs Frequency



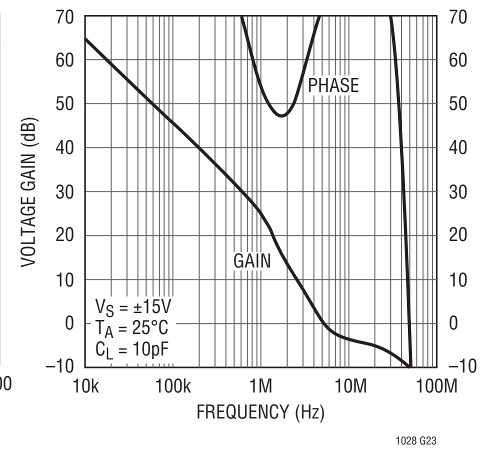

### LT1028
### Capacitance Load Handling



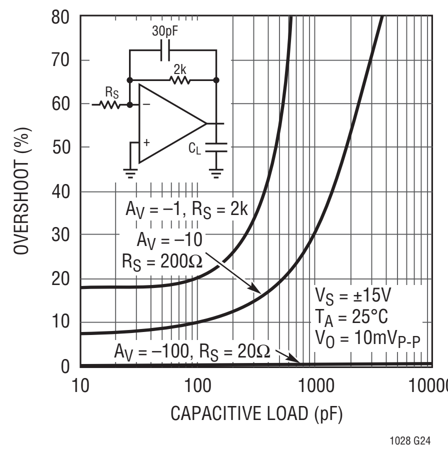

### Gain Error vs Frequency
### Closed-Loop Gain = 1000



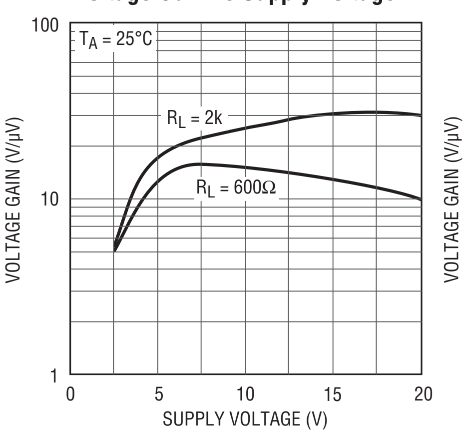

### LT1128
### Gain Phase vs Frequency



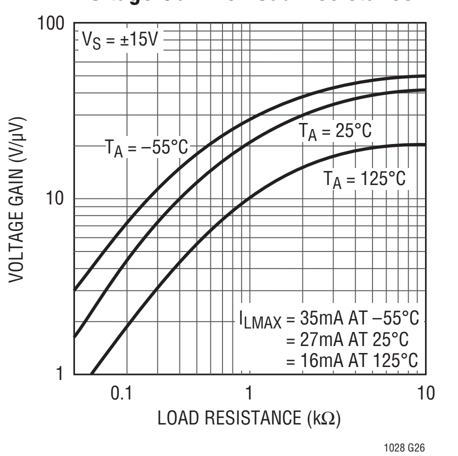

### LT1128
### Capacitance Load Handling



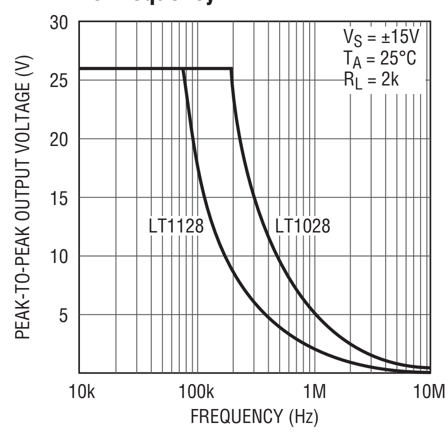

### Voltage Gain vs Supply Voltage




### Voltage Gain vs Load Resistance

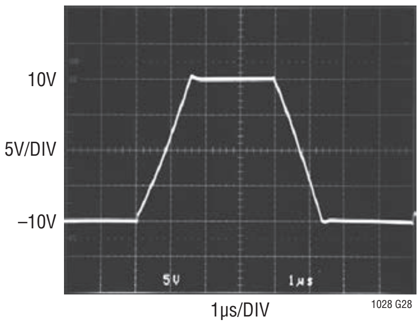



### Maximum Undistorted Output vs Frequency



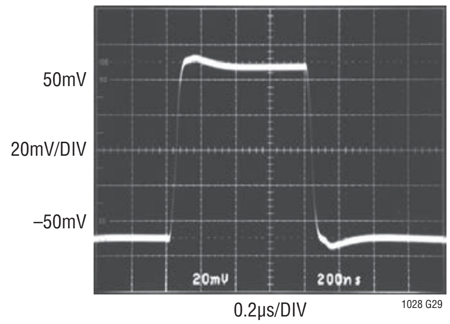
## TYPICAL PERFORMANCE CHARACTERISTICS

**LT1028**
**Large-Signal Transient Response**



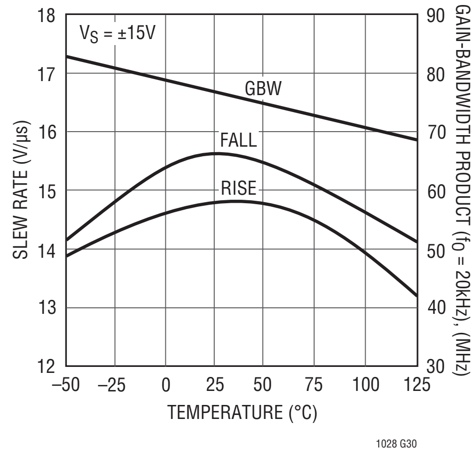

$A_V = –1, R_S = R_F = 2k, C_F = 15pF$

**LT1028**
**Small-Signal Transient Response**

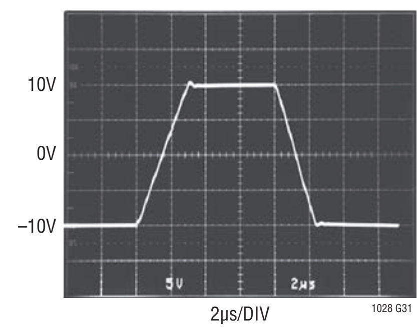



$A_V = –1, R_S = R_F = 2k,$
$C_F = 15pF, C_L = 80pF$

**LT1028**
**Slew Rate, Gain-Bandwidth Product Over Temperature**

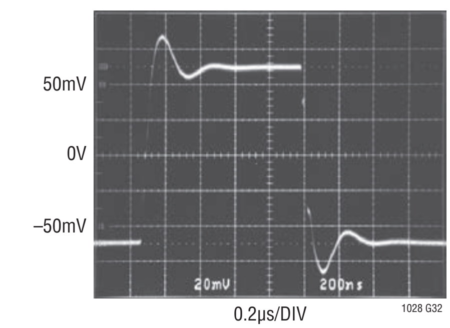



**LT1128**
**Large-Signal Transient Response**



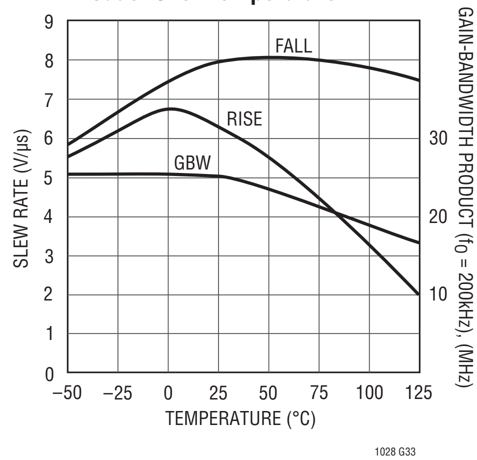

$A_V = –1, R_S = R_F = 2k, C_F = 30pF$

**LT1128**
**Small-Signal Transient Response**

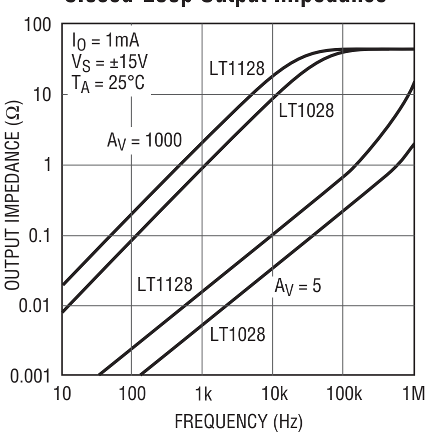



$A_V = –1, C_L = 10pF$

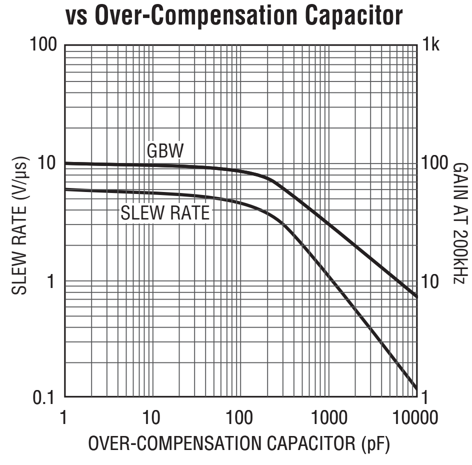
**LT1128**
**Slew Rate, Gain-Bandwidth Product Over Temperature**



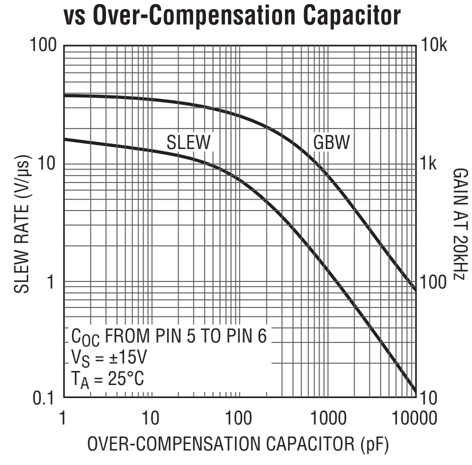

**Closed-Loop Output Impedance**




**LT1128**
**Slew Rate, Gain-Bandwidth Product vs Over-Compensation Capacitor**

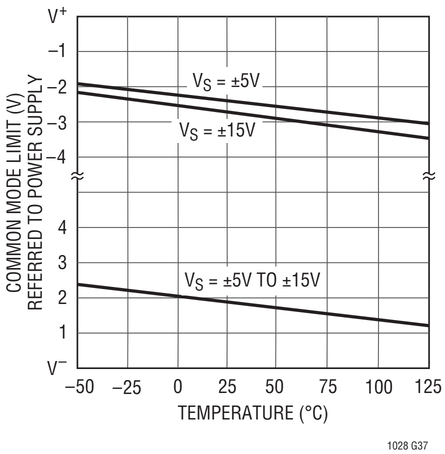



**LT1028**
**Slew Rate, Gain-Bandwidth Product vs Over-Compensation Capacitor**

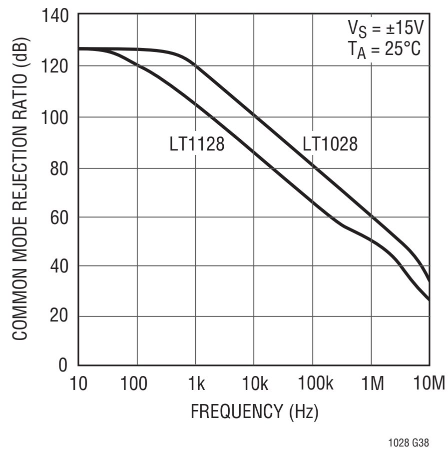


# TYPICAL PERFORMANCE CHARACTERISTICS

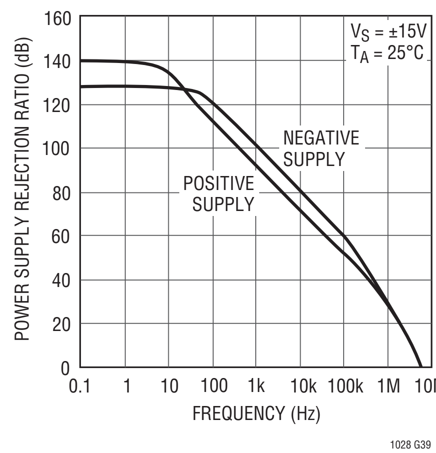
### Common Mode Limit Over Temperature



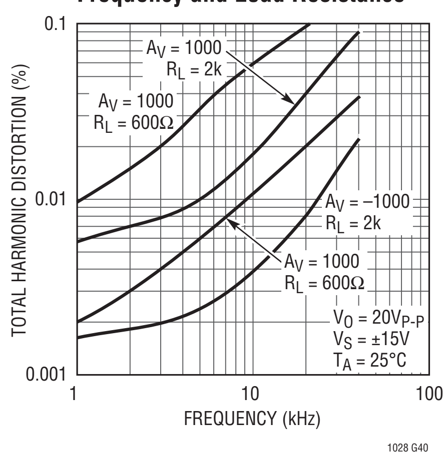

### Common Mode Rejection Ratio vs Frequency



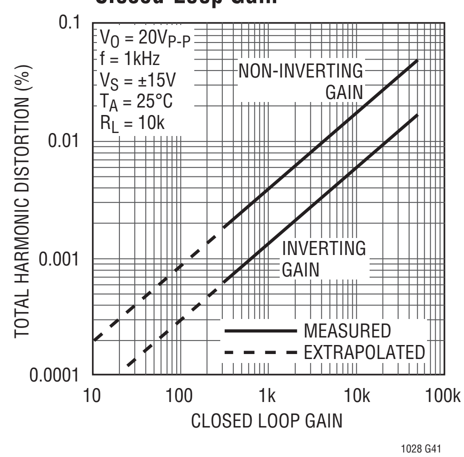

### Power Supply Rejection Ratio vs Frequency



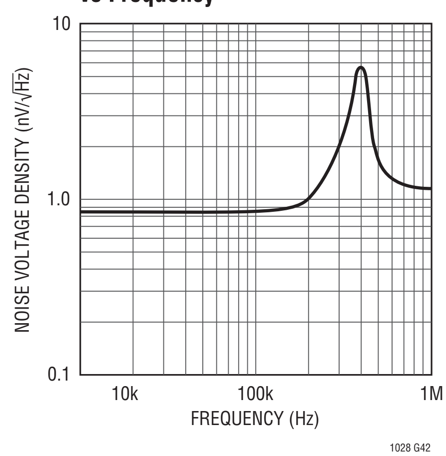

### LT1028 Total Harmonic Distortion vs Frequency and Load Resistance



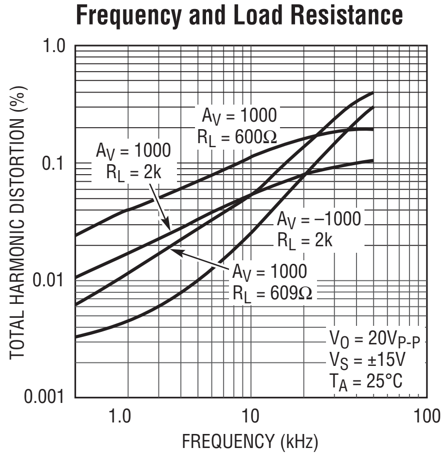

### LT1028 Total Harmonic Distortion vs Closed-Loop Gain



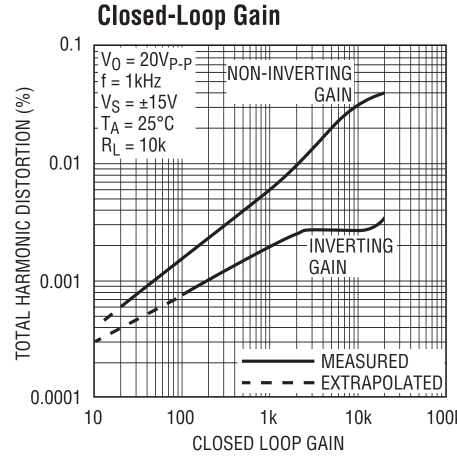

### High Frequency Voltage Noise vs Frequency




### LT1128 Total Harmonic Distortion vs Frequency and Load Resistance




### LT1128 Total Harmonic Distortion vs Closed-Loop Gain



# APPLICATIONS INFORMATION – NOISE

### Voltage Noise vs Current Noise

The LT1028/LT1128's less than $1nV/\sqrt{Hz}$ voltage noise is three times better than the lowest voltage noise heretofore available (on the LT1007/1037). A necessary condition for such low voltage noise is operating the input transistors at nearly 1mA of collector currents, because voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. Consequently, the LT1028/LT1128's current noise is significantly higher than on most monolithic op amps.

Therefore, to realize truly low noise performance it is important to understand the interaction between voltage noise ($e_n$), current noise ($I_n$) and resistor noise ($r_n$).

### Total Noise vs Source Resistance

The total input referred noise of an op amp is given by:

$$e_t = [e_n^2 + r_n^2 + (I_nR_{eq})^2]^{1/2}$$

where $R_{eq}$ is the total equivalent source resistance at the two inputs, and

$$r_n = \sqrt{4kTR_{eq}} = 0.13\sqrt{Req} \text{ in } nV/\sqrt{Hz} \text{ at } 25°C$$

As a numerical example, consider the total noise at 1kHz of the gain 1000 amplifier shown in Figure 1.

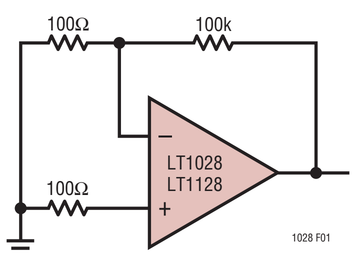



Figure 1

$$R_{eq} = 100\Omega + 100\Omega \,||\, 100k \approx 200\Omega$$
$$r_n = 0.13\sqrt{200} = 1.84nV\sqrt{Hz}$$
$$e_n = 0.85nV\sqrt{Hz}$$
$$I_n = 1.0pA/\sqrt{Hz}$$

$$e_t = [0.85^2 + 1.84^2 + (1.0 \times 0.2)^2]^{1/2} = 2.04nV/\sqrt{Hz}$$

$$\text{Output noise} = 1000\ e_t = 2.04\mu V/\sqrt{Hz}$$

At very low source resistance ($R_{eq} < 40\Omega$) voltage noise dominates. As $R_{eq}$ is increased resistor noise becomes the largest term, as in the example above, and the LT1028/LT1128's voltage noise becomes negligible. As $R_{eq}$ is further increased, current noise becomes important. At 1kHz, when $R_{eq}$ is in excess of 20k, the current noise component is larger than the resistor noise. The total noise versus matched source resistance plot illustrates the above calculations.

The plot also shows that current noise is more dominant at low frequencies, such as 10Hz. This is because resistor noise is flat with frequency, while the 1/f corner of current noise is typically at 250Hz. At 10Hz when $R_{eq}$ > 1k, the current noise term will exceed the resistor noise.

When the source resistance is unmatched, the total noise versus unmatched source resistance plot should be consulted. Note that total noise is lower at source resistances below 1k because the resistor noise contribution is less. When $R_S$ > 1k total noise is not improved, however. This is because bias current cancellation is used to reduce input bias current. The cancellation circuitry injects two correlated current noise components into the two inputs. With matched source resistors the injected current noise creates a common-mode voltage noise and gets rejected by the amplifier. With source resistance in one input only, the cancellation noise is added to the amplifier's inherent noise.

In summary, the LT1028/LT1128 are the optimum amplifiers for noise performance, provided that the source resistance is kept low. The following table depicts which op amp manufactured by Linear Technology should be used to minimize noise, as the source resistance is increased beyond the LT1028/LT1128's level of usefulness.

**Table 1. Best Op Amp for Lowest Total Noise vs Source Resistance**

| SOURCE RESISTANCE (Ω) (Note 1) | BEST OP AMP | |
|---|---|---|
| | AT LOW FREQ (10Hz) | WIDEBAND (1kHz) |
| 0 to 400 | LT1028/LT1128 | LT1028/LT1128 |
| 400 to 4k | LT1007/1037 | LT1028/LT1128 |
| 4k to 40k | LT1001 | LT1007/LT1037 |
| 40k to 500k | LT1012 | LT1001 |
| 500k to 5M | LT1012 or LT1055 | LT1012 |
| >5M | LT1055 | LT1055 |

Note 1: Source resistance is defined as matched or unmatched, e.g., $R_S$ = 1k means: 1k at each input, or 1k at one input and zero at the other.

# APPLICATIONS INFORMATION – NOISE

### Noise Testing – Voltage Noise

The LT1028/LT1128's RMS voltage noise density can be accurately measured using the Quan Tech Noise Analyzer, Model 5173 or an equivalent noise tester. Care should be taken, however, to subtract the noise of the source resistor used. Prefabricated test cards for the Model 5173 set the device under test in a closed-loop gain of 31 with a 60Ω source resistor and a 1.8k feedback resistor. The noise of this resistor combination is $0.13\sqrt{58} = 1.0nV/\sqrt{Hz}$. An LT1028/LT1128 with $0.85nV/\sqrt{Hz}$ noise will read $(0.85^2 + 1.0^2)^{1/2} = 1.31nV/\sqrt{Hz}$. For better resolution, the resistors should be replaced with a 10Ω source and 300Ω feedback resistor. Even a 10Ω resistor will show an apparent noise which is 8% to 10% too high.

The 0.1Hz to 10Hz peak-to-peak noise of the LT1028/LT1128 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 35nV peak-to-peak noise performance of the LT1028/LT1128 requires special test precautions:

(a) The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 10µV due to its chip temperature increasing 30°C to 40°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

(b) For similar reasons, the device must be well shielded from air current to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.

(c) Sudden motion in the vicinity of the device can also feedthrough to increase the observed noise.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

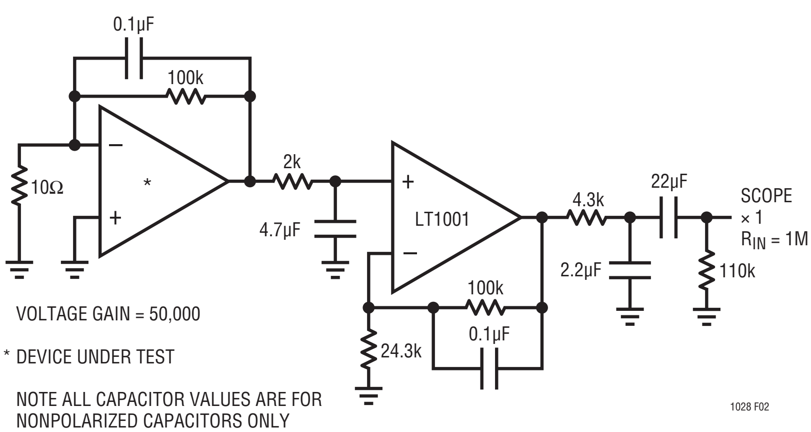



**Figure 2. 0.1Hz to 10Hz Noise Test Circuit**

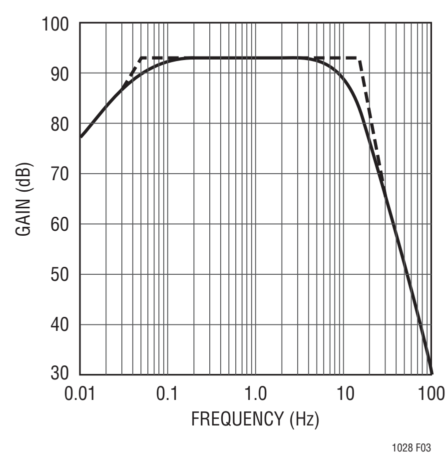



**Figure 3. 0.1Hz to 10Hz Peak-to-Peak Noise Tester Frequency Response**

# APPLICATIONS INFORMATION – NOISE

### Noise Testing – Current Noise

Current noise density ($I_n$) is defined by the following formula, and can be measured in the circuit shown in Figure 4.

$$I_n = \frac{\left[e_{no}^2 - \left(31 \bullet 18.4\text{nV}/\sqrt{\text{Hz}}\right)^2\right]^{1/2}}{20k \bullet 31}$$

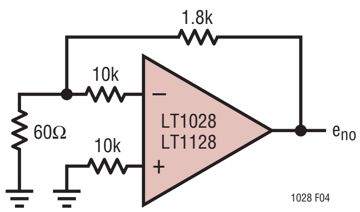



**Figure 4**

If the Quan Tech Model 5173 is used, the noise reading is input-referred, therefore the result should not be divided by 31; the resistor noise should not be multiplied by 31.

### 100% Noise Testing

The 1kHz voltage and current noise is 100% tested on the LT1028/LT1128 as part of automated testing; the approximate frequency response of the filters is shown. The limits on the automated testing are established by extensive correlation tests on units measured with the Quan Tech Model 5173.

10Hz voltage noise density is sample tested on every lot. Devices 100% tested at 10Hz are available on request for an additional charge.

10Hz current noise is not tested on every lot but it can be inferred from 100% testing at 1kHz. A look at the current noise spectrum plot will substantiate this statement. The only way 10Hz current noise can exceed the guaranteed limits is if its 1/f corner is higher than 800Hz and/or its white noise is high. If that is the case then the 1kHz test will fail.

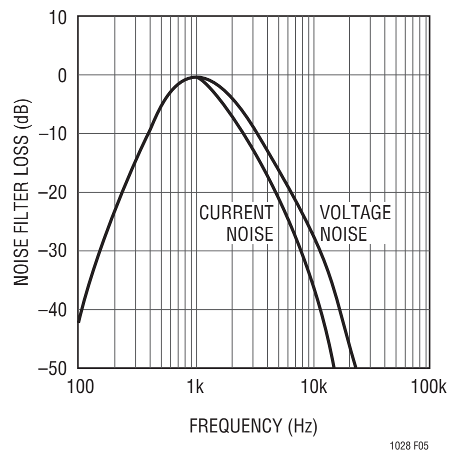



**Figure 5. Automated Tester Noise Filter**

## APPLICATIONS INFORMATION

### General

The LT1028/LT1128 series devices may be inserted directly into OP-07, OP-27, OP-37, LT1007 and LT1037 sockets with or without removal of external nulling components. In addition, the LT1028/LT1128 may be fitted to 5534 sockets with the removal of external compensation components.

### Offset Voltage Adjustment

The input offset voltage of the LT1028/LT1128 and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of $V_{OS}$ is necessary, the use of a 1k nulling potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of ($V_{OS}$/300)μV/°C, e.g., if $V_{OS}$ is adjusted to 300μV, the change in drift will be 1μV/°C.

The adjustment range with a 1k pot is approximately ±1.1mV.

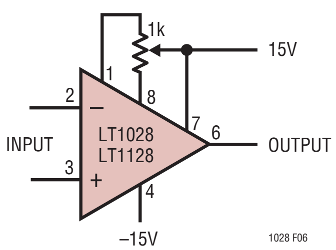



Figure 6

### Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

The circuit shown in Figure 7 to measure offset voltage is also used as the burn-in configuration for the LT1028/LT1128.

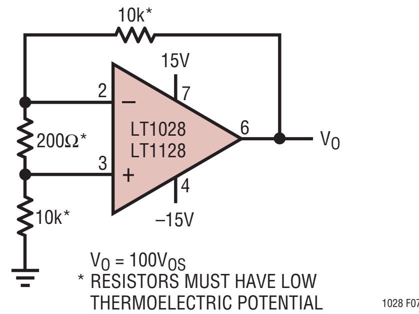



**Figure 7. Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature**

### Unity-Gain Buffer Applications (LT1128 Only)

When $R_F \leq 100\Omega$ and the input is driven with a fast, large-signal pulse (>1V), the output waveform will look as shown in the pulsed operation diagram (Figure 8).

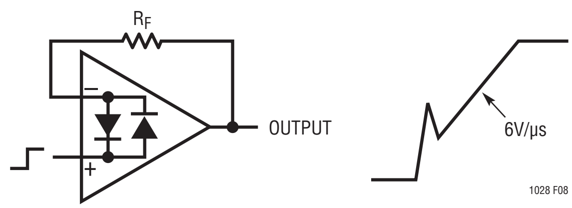



Figure 8

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_F \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V) and the amplifier stays in its active mode and a smooth transition will occur.

As with all operational amplifiers when $R_F > 2k$, a pole will be created with RF and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20pF to 50pF) in parallel with $R_F$ will eliminate this problem.

# APPLICATIONS INFORMATION

## Frequency Response

The LT1028's Gain, Phase vs Frequency plot indicates that the device is stable in closed-loop gains greater than +2 or –1 because phase margin is about 50° at an open-loop gain of 6dB. In the voltage follower configuration phase margin seems inadequate. This is indeed true when the output is shorted to the inverting input and the noninverting input is driven from a 50Ω source impedance. However, when feedback is through a parallel R-C network (provided $C_F$ < 68pF), the LT1028 will be stable because of interaction between the input resistance and capacitance and the feedback network. Larger source resistance at the non-inverting input has a similar effect. The following voltage follower configurations are stable:

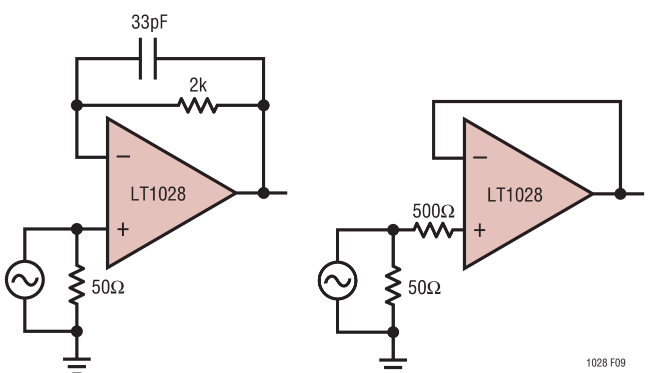



**Figure 9**

Another configuration which requires unity-gain stability is shown below. When $C_F$ is large enough to effectively short the output to the input at 15MHz, oscillations can occur. The insertion of $R_{S2} \geq 500\Omega$ will prevent the LT1028 from oscillating. When $R_{S1} \geq 500\Omega$, the additional noise contribution due to the presence of $R_{S2}$ will be minimal. When $R_{S1} \leq 100\Omega$, $R_{S2}$ is not necessary, because $R_{S1}$ represents a heavy load on the output through the $C_F$ short. When $100\Omega < R_{S1} < 500\Omega$, $R_{S2}$ should match $R_{S1}$. For example, $R_{S1} = R_{S2} = 300\Omega$ will be stable. The noise increase due to $R_{S2}$ is 40%.

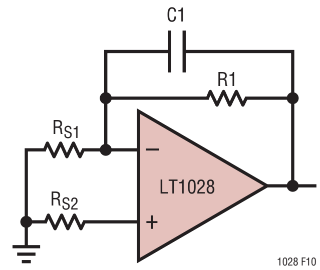



**Figure 10**

If $C_F$ is only used to cut noise bandwidth, a similar effect can be achieved using the over-compensation terminal.

The Gain, Phase plot also shows that phase margin is about 45° at gain of 10 (20dB). The following configuration has a high (≈70%) overshoot without the 10pF capacitor because of additional phase shift caused by the feedback resistor – input capacitance pole. The presence of the 10pF capacitor cancels this pole and reduces overshoot to 5%.

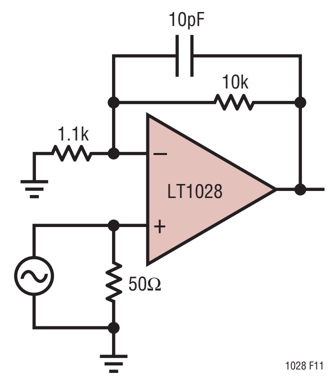


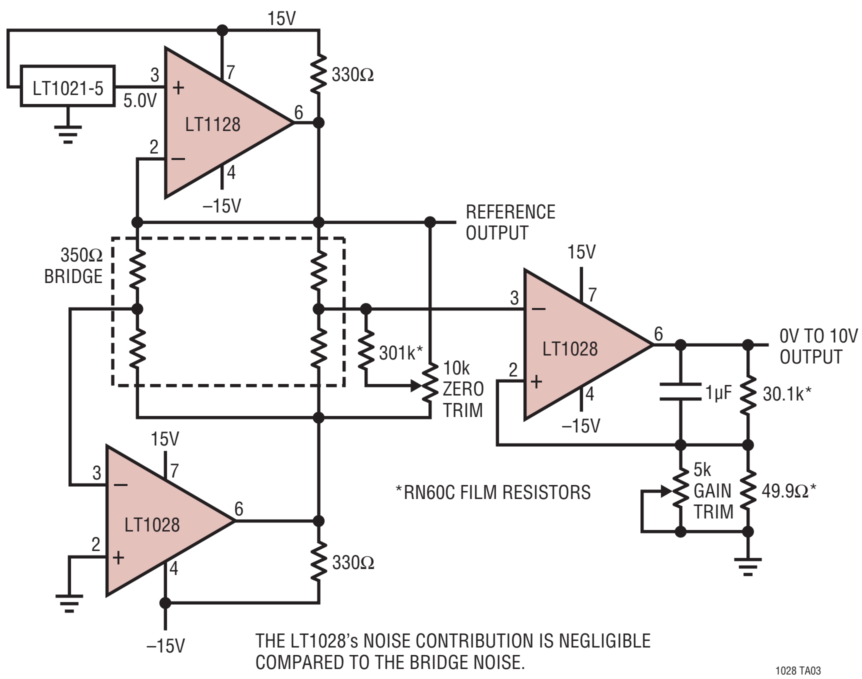

**Figure 11**

## Over-Compensation

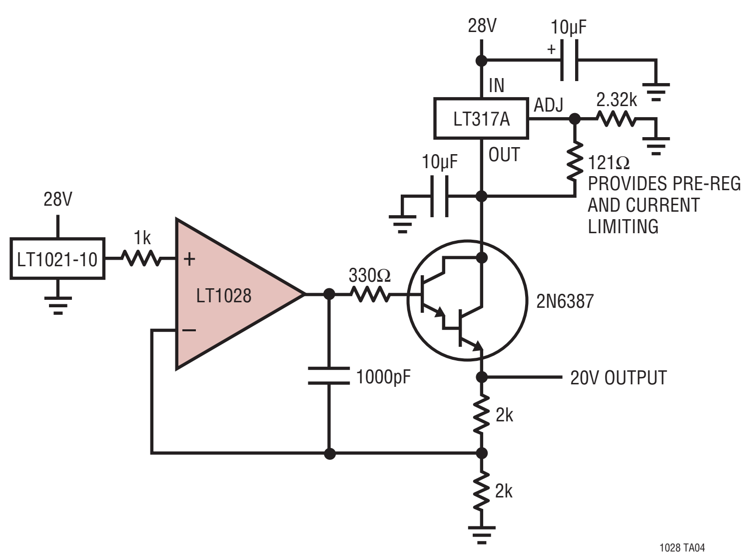
The LT1028/LT1128 are equipped with a frequency over-compensation terminal (Pin 5). A capacitor connected between Pin 5 and the output will reduce noise bandwidth. Details are shown on the Slew Rate, Gain-Bandwidth Product vs Over-Compensation Capacitor plot. An additional benefit is increased capacitive load handling capability.

## TYPICAL APPLICATIONS

**Strain Gauge Signal Conditioner with Bridge Excitation**

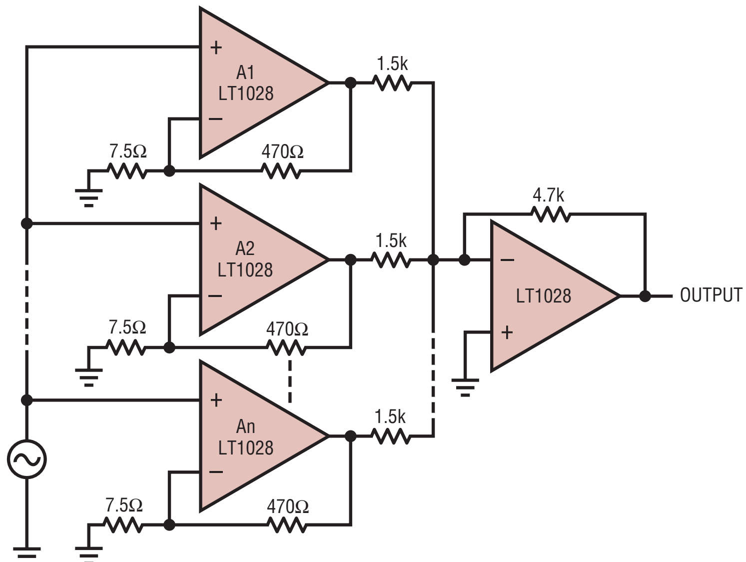



**Low Noise Voltage Regulator**



# TYPICAL APPLICATIONS

**Paralleling Amplifiers to Reduce Voltage Noise**

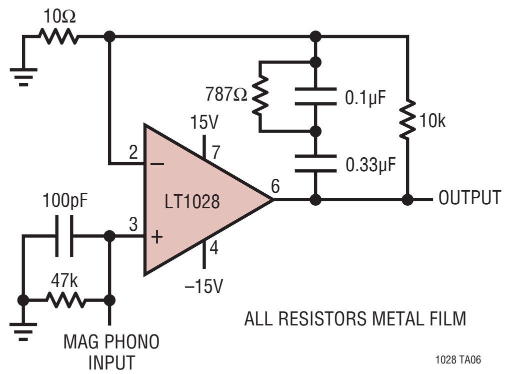



1. ASSUME VOLTAGE NOISE OF LT1028 AND 7.5Ω SOURCE RESISTOR = $0.9nV/\sqrt{Hz}$.
2. GAIN WITH n LT1028s IN PARALLEL = n • 200.
3. OUTPUT NOISE = $\sqrt{n}$ • 200 • $0.9nV/\sqrt{Hz}$.
4. INPUT REFERRED NOISE = $\frac{\text{OUTPUT NOISE}}{n \cdot 200} = \frac{0.9}{\sqrt{n}}$ $nV/\sqrt{Hz}$.
5. NOISE CURRENT AT INPUT INCREASES $\sqrt{n}$ TIMES.
6. IF n = 5, GAIN = 1000, BANDWIDTH = 1MHz, RMS NOISE, DC TO 1MHz = $\frac{2\mu V}{\sqrt{5}}$ = 0.9μV.

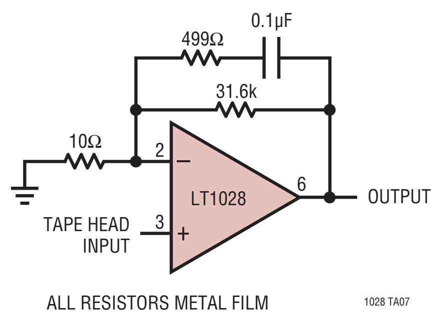
1028 TA05

## TYPICAL APPLICATIONS

**Phono Preamplifier**

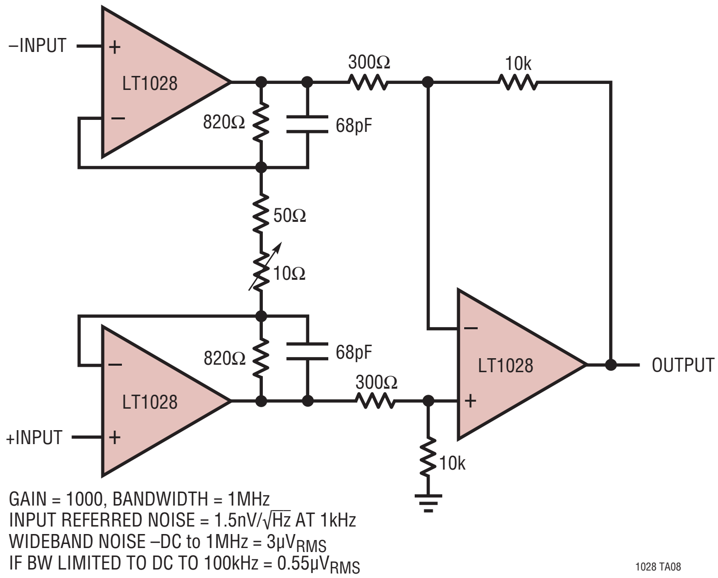



**Tape Head Amplifier**

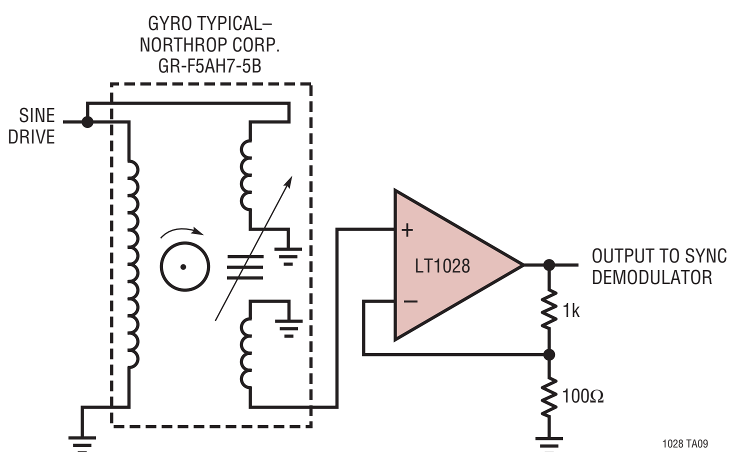


## TYPICAL APPLICATIONS

**Low Noise, Wide Bandwidth Instrumentation Amplifier**

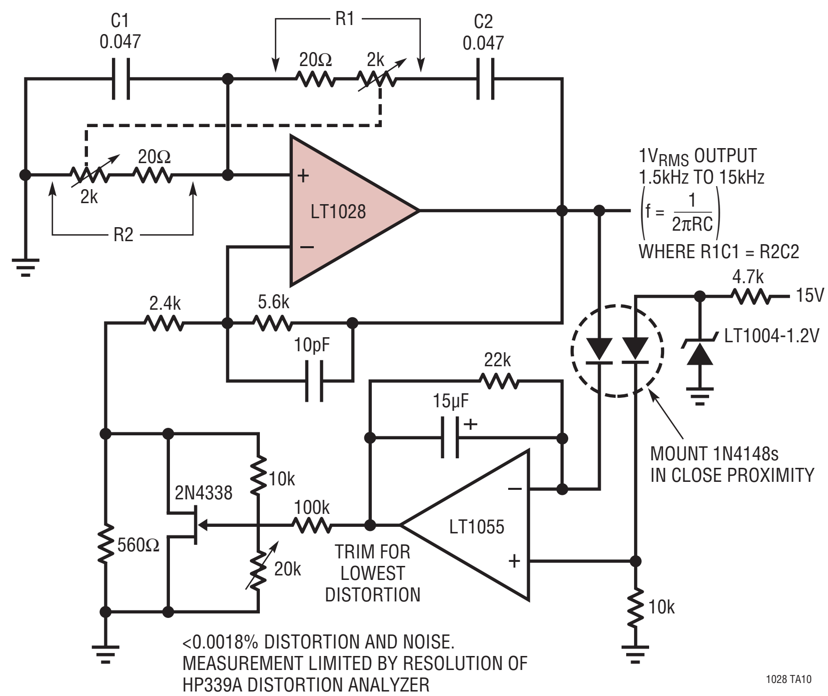



**Gyro Pick-Off Amplifier**

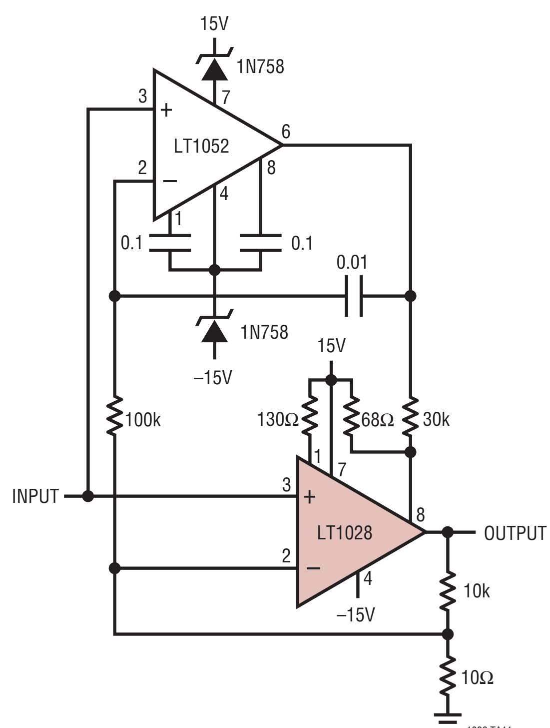


# TYPICAL APPLICATIONS

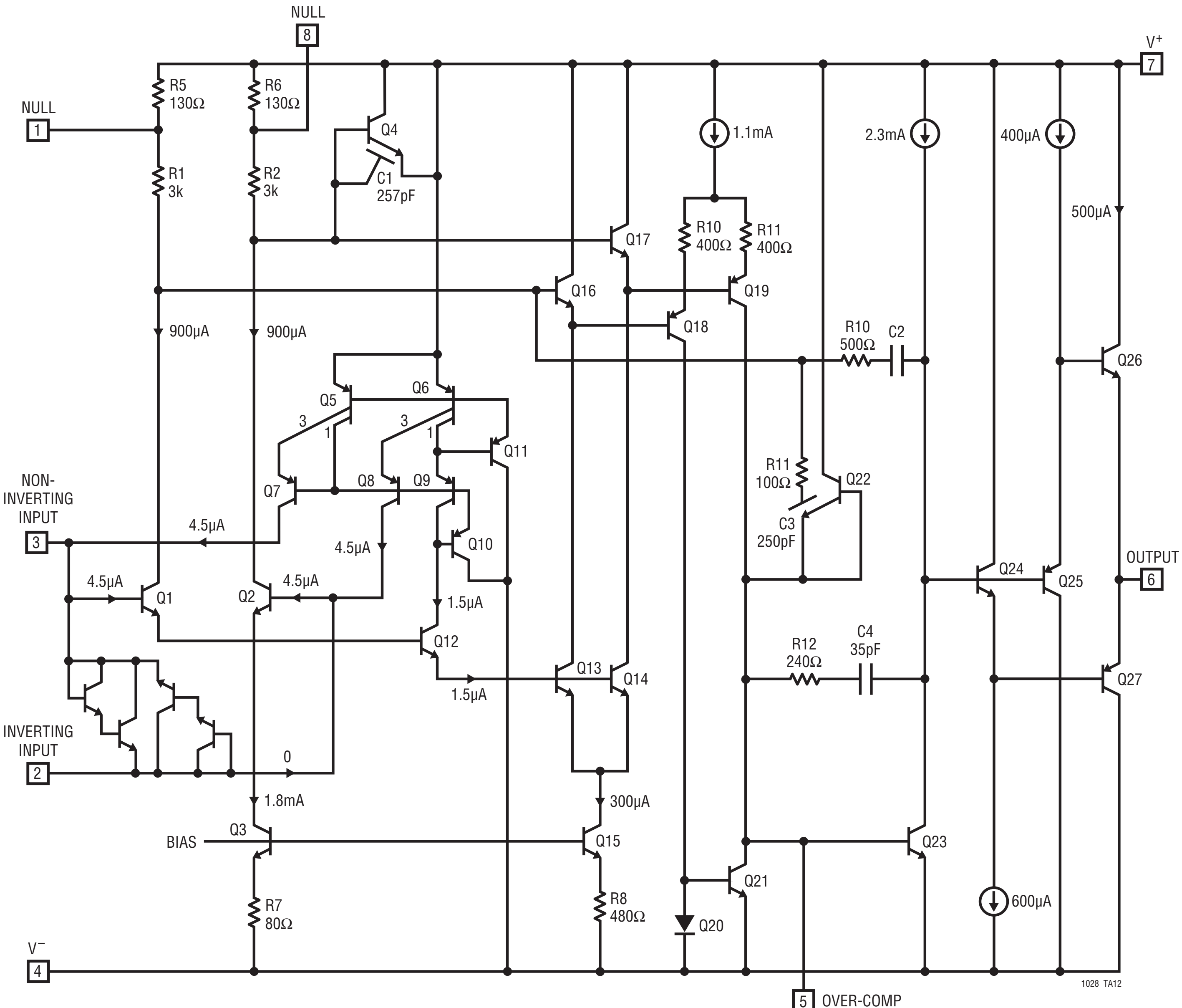
**Super Low Distortion Variable Sine Wave Oscillator**




**Chopper-Stabilized Amplifier**



## SCHEMATIC DIAGRAM

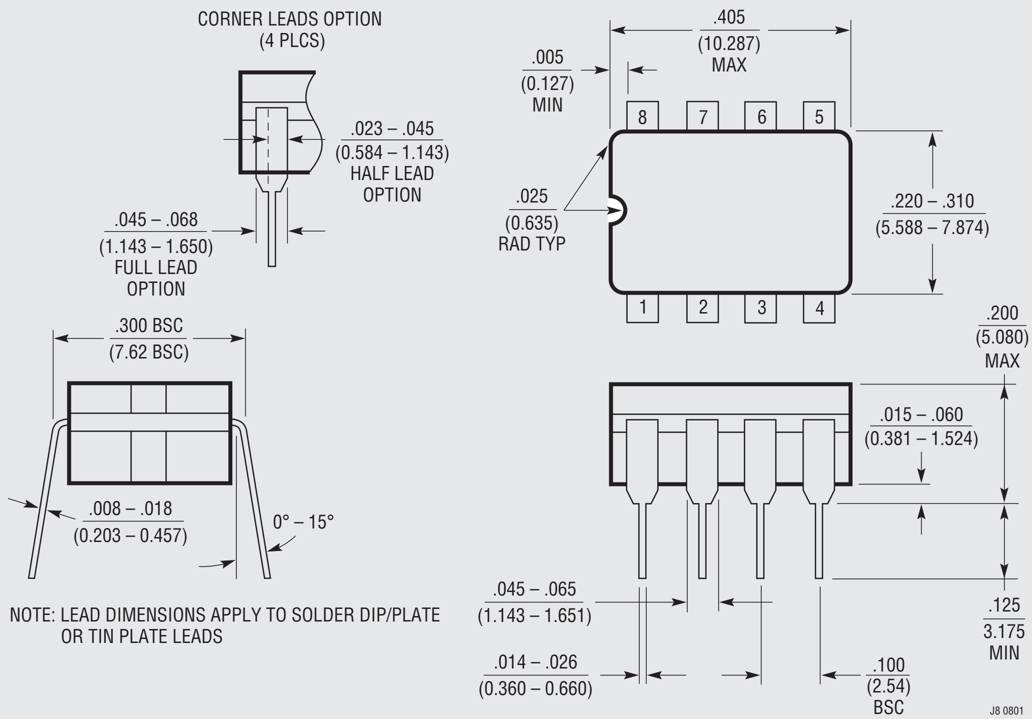



C2 = 50pF for LT1028
C2 = 275pF for LT1128

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/product/LT1028#packaging for the most recent package drawings.**

**J8 Package**
**3-Lead CERDIP (Narrow .300 Inch, Hermetic)**
(Reference LTC DWG # 05-08-1110)

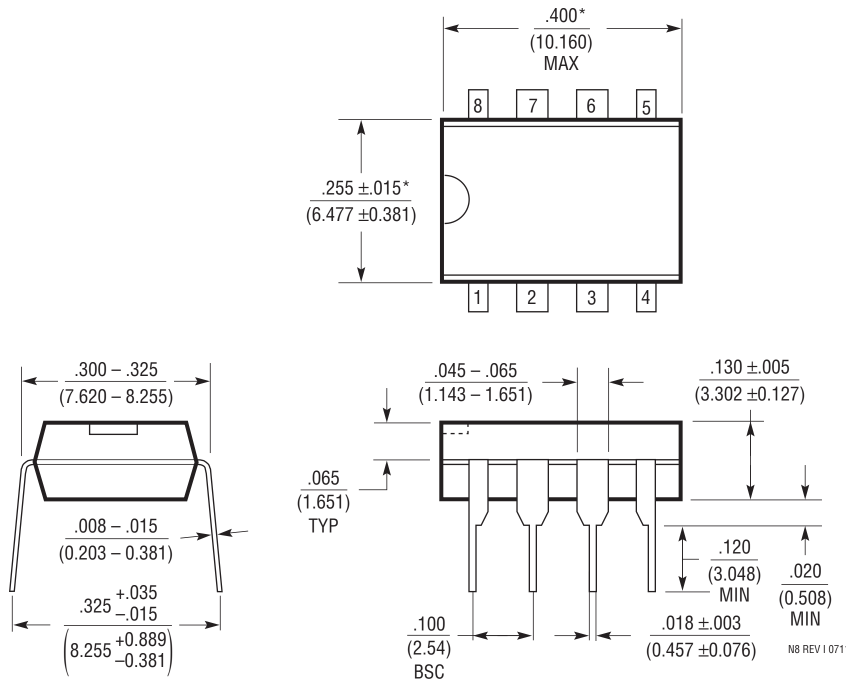



**OBSOLETE PACKAGE**

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/product/LT1028#packaging for the most recent package drawings.**

**N Package**
**8-Lead PDIP (Narrow .300 Inch)**
(Reference LTC DWG # 05-08-1510 Rev I)

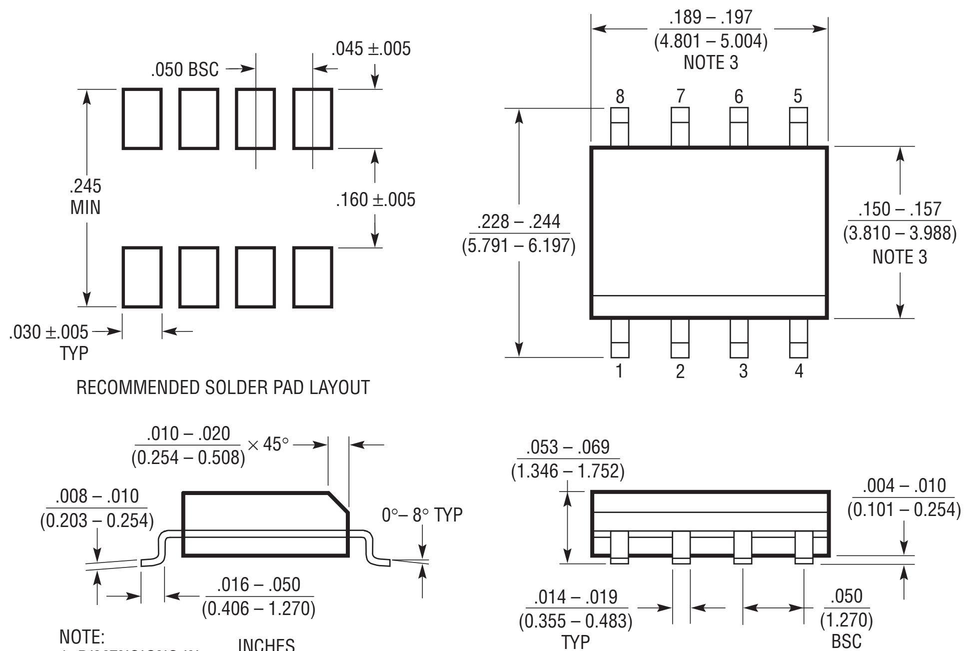



NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/product/LT1028#packaging for the most recent package drawings.**

**S8 Package**
**8-Lead Plastic Small Outline (Narrow .150 Inch)**
(Reference LTC DWG # 05-08-1610 Rev G)



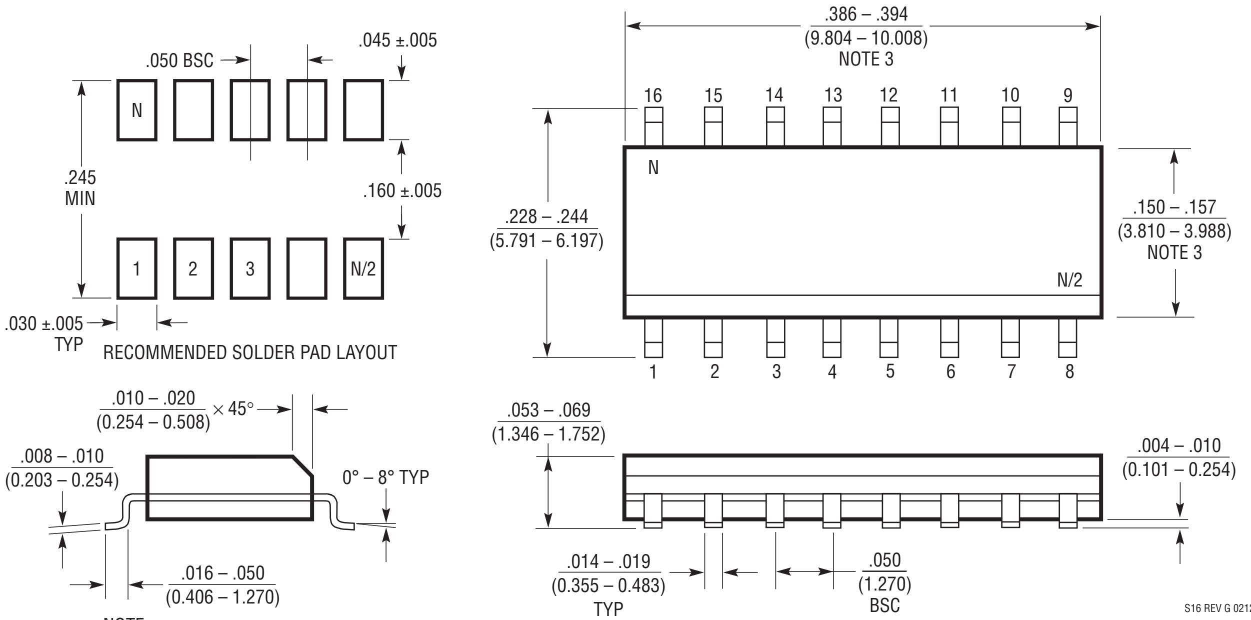

NOTE:
1. DIMENSIONS IN INCHES / (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

SO8 REV G 0212

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/product/LT1028#packaging for the most recent package drawings.**

**S Package**
**16-Lead Plastic Small Outline (Narrow .150 Inch)**
(Reference LTC DWG # 05-08-1610 Rev G)

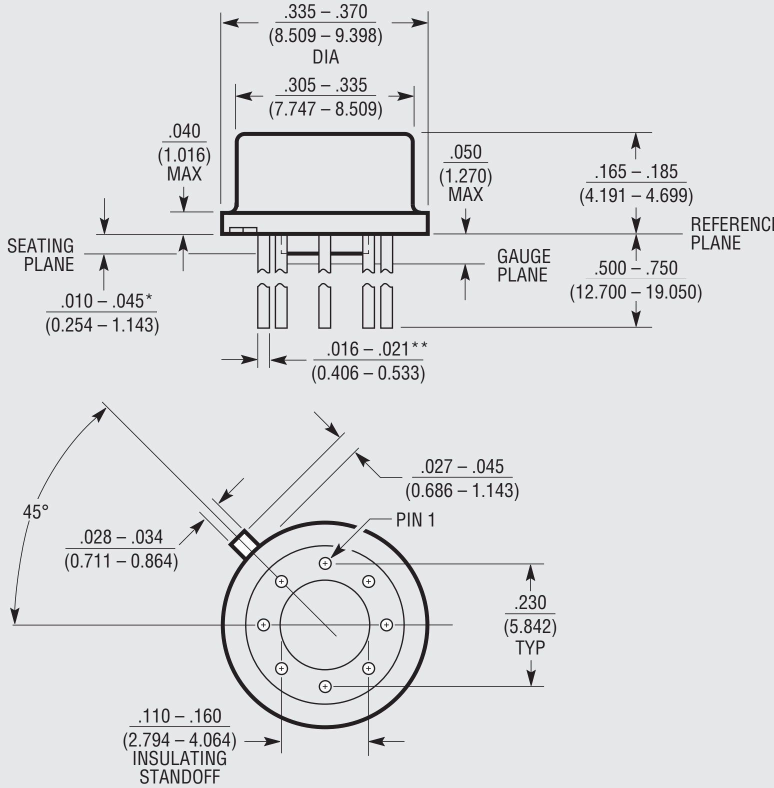



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

## PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/product/LT1028#packaging for the most recent package drawings.**

**H Package**
**8-Lead TO-5 Metal Can (.230 Inch PCD)**
(Reference LTC DWG # 05-08-1321)




*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND THE SEATING PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{.016 – .024}{(0.406 – 0.610)}$ H8 (TO-5) 0.230 PCD 0204

**OBSOLETE PACKAGE**

## REVISION HISTORY (Revision history begins at Rev B)

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| B | 10/12 | Replaced the Typical Application. | 1 |
| C | 10/14 | Corrected diagram to show N8 package is not obsolete. | 2 |
| | | Changed $T_{JMAX}$ to 150°C for S8 and SW packages. | 2 |
| | | Corrected right-hand Electrical Characteristics column to reflect non-A-grade specs. | 3 |
| | | Corrected LM301A and LT1012 input polarity. | 28 |
| D | 10/15 | Corrected component values in Low Noise Voltage Regulator circuit. | 16 |



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