

# Decompensated Low Noise, High Speed Precision Op Amps

## FEATURES

- 100% Tested Low Voltage Noise:  $2.7\text{nV}/\sqrt{\text{Hz}}$  Typ,  $4.2\text{nV}/\sqrt{\text{Hz}}$  Max
- Slew Rate:  $11\text{V}/\mu\text{s}$  Typ
- Gain-Bandwidth Product:  $65\text{MHz}$  Typ
- Offset Voltage, Prime Grade:  $70\mu\text{V}$  Max  
Low Grade:  $100\mu\text{V}$  Max
- High Voltage Gain: 5 Million Min
- Supply Current Per Amplifier:  $3.1\text{mA}$  Max
- Common Mode Rejection:  $112\text{dB}$  Min
- Power Supply Rejection:  $116\text{dB}$  Min
- Available in 8-Lead SOIC, 8-Lead DIP, 16-Lead SO and 14-Lead DIP Packages

## APPLICATIONS

- Two and Three Op Amp Instrumentation Amplifiers
- Low Noise Signal Processing
- Active Filters
- Microvolt Accuracy Threshold Detection
- Strain Gauge Amplifiers
- Direct Coupled Audio Gain Stages
- Tape Head Preamplifiers
- Microphone Preamplifiers
- Accelerometer Amplifiers
- Infrared Detectors

## DESCRIPTION

The LT<sup>®</sup>1126 dual and LT1127 quad are high performance, decompensated op amps that offer higher slew rate and bandwidth than the LT1124 dual and the LT1125 quad operational amplifiers. The enhanced AC performance is available without degrading DC specs of the LT1124/LT1125. Both LT1126/LT1127 are stable in a gain of 10 or more.

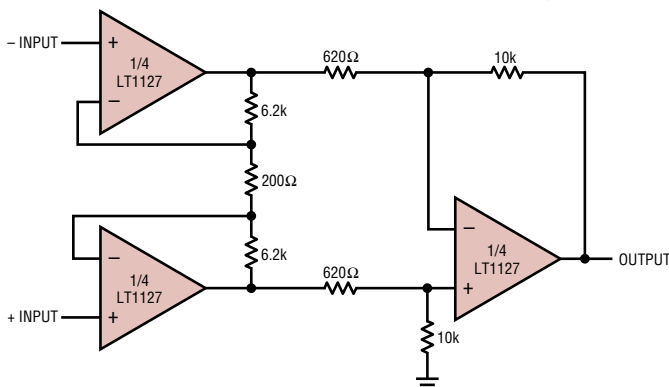
In the design, processing and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Slew rate, gain-bandwidth and 1kHz noise are 100% tested for each individual amplifier. Consequently, the specifications of even the lowest cost grades (the LT1126C and the LT1127C) have been enhanced.

Power consumption of the dual LT1126 is less than one half of two OP-37s. Low power and high performance in an 8-pin SO package makes the LT1126 a first choice for surface mounted systems and where board space is restricted.

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## TYPICAL APPLICATION

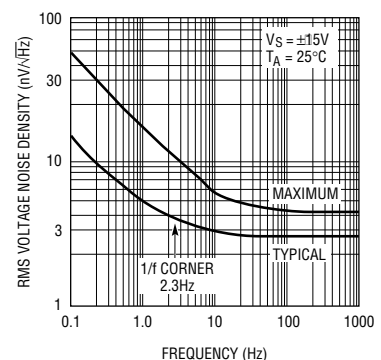
Low Noise, Wide Bandwidth Instrumentation Amplifier



GAIN = 1000, BANDWIDTH =  $480\text{kHz}$   
 INPUT REFERRED NOISE =  $4.5\text{nV}/\sqrt{\text{Hz}}$  AT  $1\text{kHz}$ ,  $6\mu\text{V}_{\text{RMS}}$  OVER BANDWIDTH

1126-7 TA01

Voltage Noise vs Frequency



1126-7 TA01b

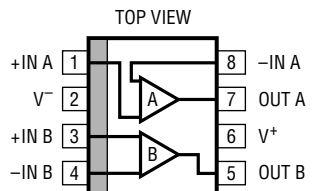
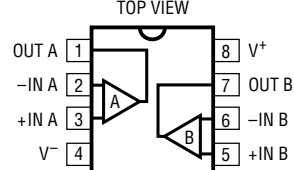
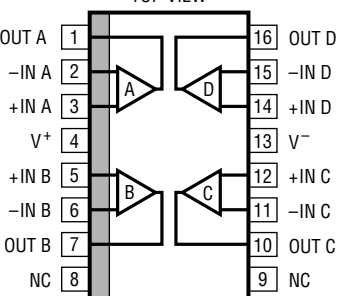
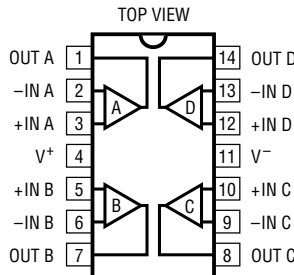
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**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Supply Voltage ..... ±22V  
 Input Voltage ..... Equal to Supply Voltage  
 Output Short Circuit Duration ..... Indefinite  
 Differential Input Current (Note 5) ..... ±25mA  
 Lead Temperature (Soldering, 10 sec.) ..... 300°C

Operating Temperature Range  
 LT1126AM/LT1126M  
 LT1127AM/LT1127M (**OBSELETE**) .. -55°C to 125°C  
 LT1126AC/LT1126C  
 LT1127AC/LT1127C ..... -40°C to 85°C  
 Storage Temperature Range  
 All Grades ..... -65°C to 150°C

**PACKAGE/ORDER INFORMATION**

 <p>TOP VIEW</p> <p>1 +IN A 8 -IN A                  2 V<sup>-</sup> 7 OUT A                  3 +IN B 6 V<sup>+</sup>                  4 -IN B 5 OUT B</p> <p>S8 PACKAGE                  8-LEAD PLASTIC SO  <math>T_{JMAX} = 140^{\circ}C, \theta_{JA} = 190^{\circ}C/W</math></p> <p>NOTE: THIS PIN CONFIGURATION DIFFERS FROM THE 8-PIN PDIP CONFIGURATION. INSTEAD, IT FOLLOWS THE INDUSTRY STANDARD LT1013DS8 SO PACKAGE PIN LOCATIONS</p>	<p>ORDER PART NUMBER</p> <p>LT1126CS8</p> <p>S8 PART MARKING</p> <p>1126</p>	 <p>TOP VIEW</p> <p>1 OUT A 8 V<sup>+</sup>                  2 -IN A 7 OUT B                  3 +IN A 6 -IN B                  4 V<sup>-</sup> 5 +IN B</p> <p>N8 PACKAGE                  8-LEAD PDIP  <math>T_{JMAX} = 140^{\circ}C, \theta_{JA} = 130^{\circ}C</math></p> <p>J8 PACKAGE                  8-LEAD CERAMIC DIP  <math>T_{JMAX} = 160^{\circ}C, \theta_{JA} = 100^{\circ}C/W</math>  <b>OBSELETE PACKAGE</b>                  Consider the N8 for Alternate Source</p>	<p>ORDER PART NUMBER</p> <p>LT1126ACN8                  LT1126CN8</p> <p>LT1126AMJ8                  LT1126MJ8                  LT1126CJ8</p>
 <p>TOP VIEW</p> <p>1 OUT A 16 OUT D                  2 -IN A 15 -IN D                  3 +IN A 14 +IN D                  4 V<sup>+</sup> 13 V<sup>-</sup>                  5 +IN B 12 +IN C                  6 -IN B 11 -IN C                  7 OUT B 10 OUT C                  8 NC 9 NC</p> <p>SW PACKAGE                  16-LEAD PLASTIC SO WIDE  <math>T_{JMAX} = 140^{\circ}C, \theta_{JA} = 130^{\circ}C/W</math></p>	<p>LT1127CSW</p>	 <p>TOP VIEW</p> <p>1 OUT A 14 OUT D                  2 -IN A 13 -IN D                  3 +IN A 12 +IN D                  4 V<sup>+</sup> 11 V<sup>-</sup>                  5 +IN B 10 +IN C                  6 -IN B 9 -IN C                  7 OUT B 8 OUT C</p> <p>N PACKAGE                  14-LEAD PDIP  <math>T_{JMAX} = 140^{\circ}C, \theta_{JA} = 110^{\circ}C (N)</math></p> <p>J PACKAGE                  14-LEAD CERAMIC DIP  <math>T_{JMAX} = 160^{\circ}C, \theta_{JA} = 80^{\circ}C/W</math>  <b>OBSELETE PACKAGE</b>                  Consider the N for Alternate Source</p>	<p>LT1127ACN                  LT1127CN</p> <p>LT1127AMJ                  LT1127MJ                  LT1127CJ</p>
<p><b>Order Options</b> Tape and Reel: Add #TR                  Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF                  Lead Free Part Marking: <a href="http://www.linear.com/leadfree/">http://www.linear.com/leadfree/</a></p>			

Consult LTC Marketing for parts specified with wider operating temperature ranges.

**ELECTRICAL CHARACTERISTICS**  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)	LT1126AM/AC LT1127AM/AC			LT1126M/C LT1127M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	LT1126		20	70		25	100	$\mu V$
		LT1127		25	90		30	140	$\mu V$
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			0.3			0.3		$\mu V/Mo$
$I_{OS}$	Input Offset Current	LT1126		5	15		6	20	nA
		LT1127		6	20		7	30	nA
$I_B$	Input Bias Current			$\pm 7$	$\pm 20$		$\pm 8$	$\pm 30$	nA
$e_n$	Input Noise Voltage	0.1Hz to 10Hz (Notes 8, 9)		70	200		70		nVp-p
	Input Noise Voltage Density	$f_0 = 10Hz$ (Note 5)		3.0	5.5		3.0	5.5	$nV/\sqrt{Hz}$
		$f_0 = 1000Hz$ (Note 3)		2.7	4.2		2.7	4.2	$nV/\sqrt{Hz}$
$i_n$	Input Noise Current Density	$f_0 = 10Hz$		1.3			1.3		$pA/\sqrt{Hz}$
		$f_0 = 1000Hz$		0.3			0.3		$pA/\sqrt{Hz}$
$V_{CM}$	Input Voltage Range		$\pm 12.0$	$\pm 12.8$		$\pm 12.0$	$\pm 12.8$		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12V$		112	126		106	124	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$		116	126		110	124	dB
$A_{VOL}$	Large Signal Voltage Gain	$R_L \geq 10k\Omega$ , $V_0 = \pm 10V$		5.0	17.0		3.0	15.0	$V/\mu V$
		$R_L \geq 2k\Omega$ , $V_0 = \pm 10V$		2.0	4.0		1.5	3.0	$V/\mu V$
$V_{OUT}$	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$		$\pm 13.0$	$\pm 13.8$		$\pm 12.5$	$\pm 13.8$	V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Notes 3, 7)		8.0	11		8.0	11	$V/\mu s$
GBW	Gain-Bandwidth Product	$f_0 = 10kHz$ (Note 3)		45	65		45	65	MHz
$Z_0$	Open Loop Output Resistance	$V_0 = 0$ , $I_0 = 0$		75			75		$\Omega$
$I_S$	Supply Current Per Amplifier			2.6	3.1		2.6	3.1	mA
	Channel Separation	$f \leq 10Hz$ (Note 9) $V_0 = \pm 10V$ , $R_L = 2k\Omega$		134	150		130	150	dB

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $V_S = \pm 15V$ ,  $-55^\circ C \leq T_A \leq 125^\circ C$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1126AM LT1127AM			LT1126M LT1127M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	LT1126	●	50	170		60	250	$\mu V$
		LT1127	●	55	190		70	290	$\mu V$
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 5)	●	0.3	1.0		0.4	1.5	$\mu V/^\circ C$
$I_{OS}$	Input Offset Current	LT1126	●	18	45		20	60	nA
		LT1127	●	18	55		20	70	nA
$I_B$	Input Bias Current		●	$\pm 18$	$\pm 55$		$\pm 20$	$\pm 70$	nA
$V_{CM}$	Input Voltage Range		●	$\pm 11.3$	$\pm 12$		$\pm 11.3$	$\pm 12$	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11.3V$	●	106	122		100	120	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	●	110	122		104	120	dB
$A_{VOL}$	Large Signal Voltage Gain	$R_L \geq 10k\Omega$ , $V_0 = \pm 10V$	●	3.0	10.0		2.0	10.0	$V/\mu V$
		$R_L \geq 2k\Omega$ , $V_0 = \pm 10V$	●	1.0	3.0		0.7	2.0	$V/\mu V$
$V_{OUT}$	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	$\pm 12.5$	$\pm 13.6$		$\pm 12.0$	$\pm 13.6$	V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Notes 3, 7)	●	7.2	10		7.0	10	$V/\mu s$
$I_S$	Supply Current Per Amplifier		●	2.8	3.5		2.8	3.5	mA

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $V_S = \pm 15V$ ,  $0^\circ C \leq T_A \leq 70^\circ C$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)	LT1126AC LT1127AC			LT1126C LT1127C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	LT1126 LT1127	●	35 40	120 140	●	45 50	170 210	$\mu V$ $\mu V$
$\Delta V_{OS}/\Delta T$	Average Input Offset Voltage Drift	(Note 5)	●	0.3	1.0	●	0.4	1.5	$\mu V/^\circ C$
$I_{OS}$	Input Offset Current	LT1126 LT1127	●	6 7	25 35	●	7 8	35 45	nA nA
$I_B$	Input Bias Current		●	$\pm 8$	$\pm 35$	●	$\pm 9$	$\pm 45$	nA
$V_{CM}$	Input Voltage Range		●	$\pm 11.5$	$\pm 12.4$	●	$\pm 11.5$	$\pm 12.4$	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11.5V$	●	109	125	●	102	122	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	●	112	125	●	107	122	dB
$A_{VOL}$	Large Signal Voltage Gain	$R_L \geq 10k\Omega, V_O = \pm 10V$ $R_L \geq 2k\Omega, V_O = \pm 10V$	●	4.0 1.5	15.0 3.5	●	2.5 1.0	14.0 2.5	$V/\mu V$ $V/\mu V$
$V_{OUT}$	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	$\pm 12.5$	$\pm 13.7$	●	$\pm 12.0$	$\pm 13.7$	V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Notes 3, 7)	●	7.5	10.5	●	7.3	10.5	$V/\mu s$
$I_S$	Supply Current Per Amplifier		●	2.7	3.3	●	2.7	3.3	mA

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $V_S = \pm 15V$ ,  $-40^\circ C \leq T_A \leq 85^\circ C$ , unless otherwise noted. (Note 10)

SYMBOL	PARAMETER	CONDITIONS (Note 2)	LT1126AC LT1127AC			LT1126C LT1127C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	LT1126 LT1127	●	40 45	140 160	●	50 55	200 240	$\mu V$ $\mu V$
$\Delta V_{OS}/\Delta T$	Average Input Offset Voltage Drift	(Note 5)	●	0.3	1.0	●	0.4	1.5	$\mu V/^\circ C$
$I_{OS}$	Input Offset Current	LT1126 LT1127	●	15 15	40 50	●	17 17	55 65	nA nA
$I_B$	Input Bias Current		●	$\pm 15$	$\pm 50$	●	$\pm 17$	$\pm 65$	nA
$V_{CM}$	Input Voltage Range		●	$\pm 11.4$	$\pm 12.2$	●	$\pm 11.4$	$\pm 12.2$	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11.4V$	●	107	124	●	101	121	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	●	111	124	●	106	121	dB
$A_{VOL}$	Large Signal Voltage Gain	$R_L \geq 10k\Omega, V_O = \pm 10V$ $R_L \geq 2k\Omega, V_O = \pm 10V$	●	3.5 1.2	12.0 3.2	●	2.2 0.8	12.0 2.3	$V/\mu V$ $V/\mu V$
$V_{OUT}$	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	$\pm 12.5$	$\pm 13.6$	●	$\pm 12.0$	$\pm 13.6$	V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 7)	●	7.3	10.2	●	7.1	10.2	$V/\mu s$
$I_S$	Supply Current Per Amplifier		●	2.8	3.4	●	2.8	3.4	mA

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1127s (or 100 LT1126s) typically 240 op amps (or 120) will be better than the indicated specification.

**Note 3:** This parameter is 100% tested for each individual amplifier.

**Note 4:** This parameter is sample tested only.

**Note 5:** This parameter is not 100% tested.

**Note 6:** The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds  $\pm 1.4V$ , the input current should be limited to 25mA.

**Note 7:** Slew rate is measured in  $A_V = -10$ ; input signal is  $\pm 1V$ , output measured at  $\pm 5V$ .

**Note 8:** 0.1Hz to 10Hz noise can be inferred from the 10Hz noise voltage density test. See the test circuit and frequency response curve for 0.1Hz to 10Hz tester in the Applications Information section of the LT1007 or LT1028 datasheets.

**Note 9:** This parameter is guaranteed but not tested.

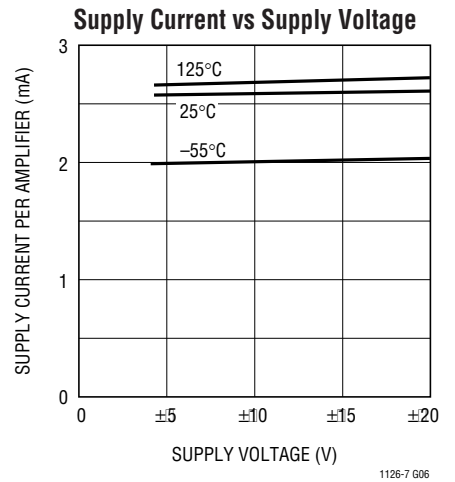
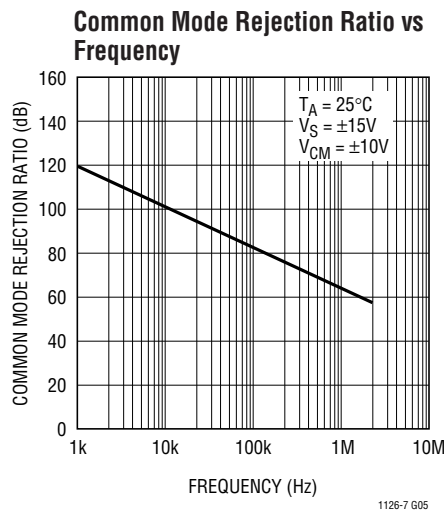
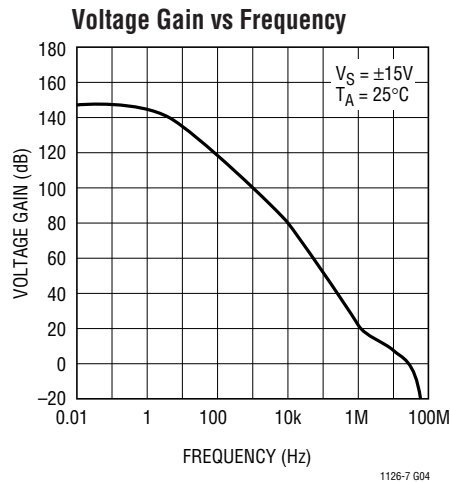
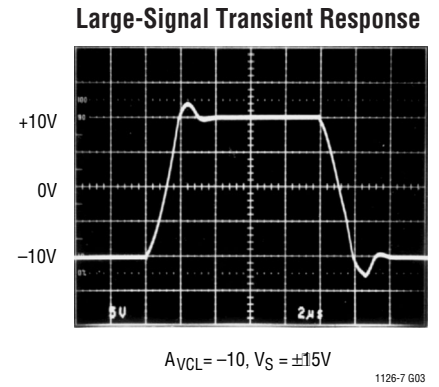
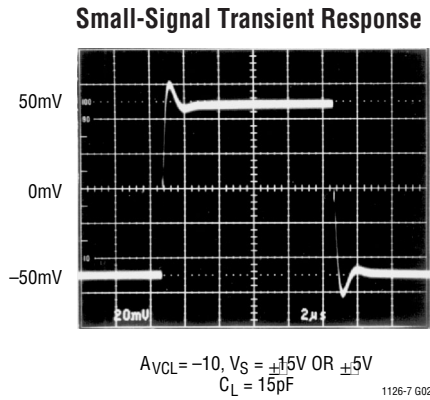
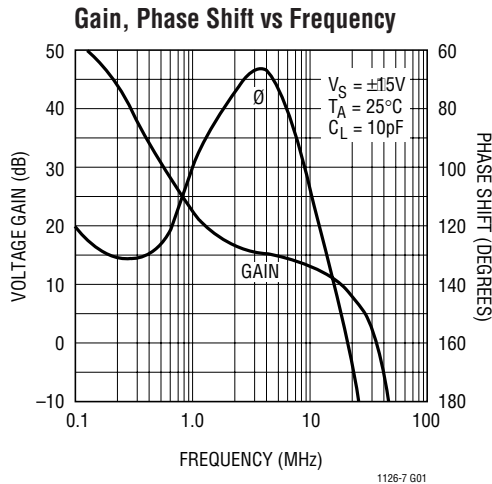
**Note 10:** The LT1126/LT1127 are designed, characterized and expected to meet these extended temperature limits, but are not tested at  $-40^\circ C$  and at  $85^\circ C$ . Guaranteed I grade parts are available. Consult factory.

## TYPICAL PERFORMANCE CHARACTERISTICS

The typical behavior of many LT1126/LT1127 parameters is identical to the LT1124/LT1125. Please refer to the LT1124/LT1125 data sheet for the following performance characteristics:

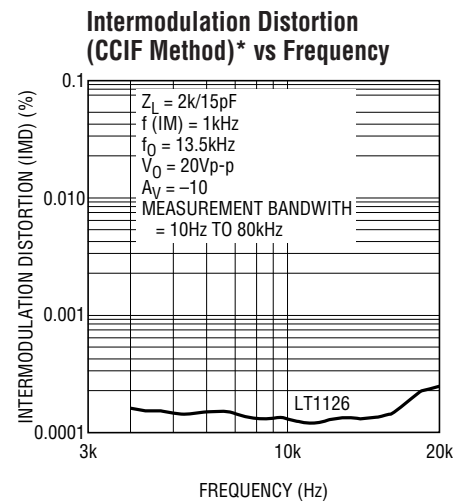
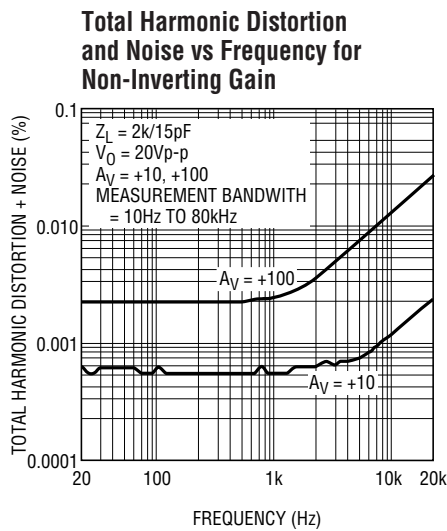
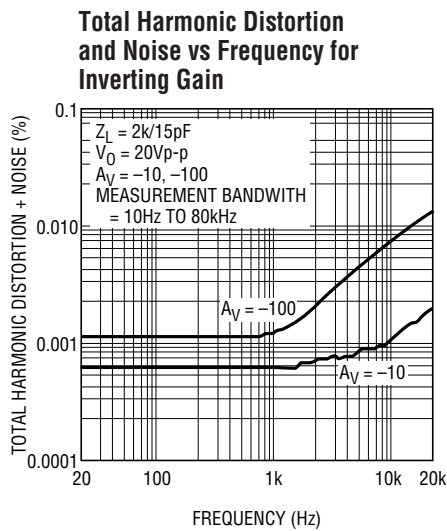
- 0.1Hz to 10Hz Voltage Noise
- 0.01Hz to 1Hz Voltage Noise
- Current Noise vs Frequency
- Input Bias or Offset Current vs Temperature
- Output Short Circuit Current vs Time

- Input Bias Current Over the Common Mode Range
- Voltage Gain vs Temperature
- Input Offset Voltage Drift Distribution
- Offset Voltage Drift with Temperature of Representative Units
- Output Voltage Swing vs Load Current
- Common Mode Limit vs Temperature
- Channel Separation vs Frequency
- Warm-Up Drift
- Power Supply Rejection Ratio vs Frequency



\*See LT1115 data sheet for definition of CCIF testing

## TYPICAL PERFORMANCE CHARACTERISTICS



\*See LT1115 data sheet for definition of CCIF testing

## APPLICATIONS INFORMATION

### Matching Specifications

In many applications the performance of a system depends on the matching between two op amps, rather than the individual characteristics of the two devices. The three op amp instrumentation amplifier configuration shown in this data sheet is an example. Matching characteristics are not 100% tested on the LT1126/LT1127.

Some specifications are guaranteed by definition. For example,  $70\mu V$  maximum offset voltage implies that mismatch cannot be more than  $140\mu V$ .  $112dB$  ( $= 2.5\mu V/V$ ) CMRR means that worst case CMRR match is  $106dB$  ( $5\mu V/V$ ). However, the following table can be used to estimate the expected matching performance between the two sides of the LT1126, and between amplifiers A and D, and between amplifiers B and C of the LT1127.

### Expected Match

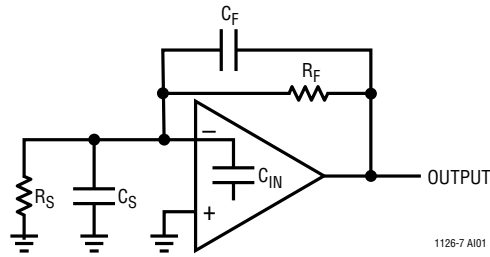
PARAMETER		LT1126A/M/C LT1127A/M/C		LT1126M/C LT1127M/C		UNITS
		50% YIELD	98% YIELD	50% YIELD	98% YIELD	
$V_{OS}$ Match, $\Delta V_{OS}$	LT1126	20	110	30	130	$\mu V$
	LT1127	30	150	50	180	$\mu V$
Temperature Coefficient Match		0.35	1.0	0.5	1.5	$\mu V/^\circ C$
Average Non-Inverting $I_B$		6	18	7	25	nA
Match of Non-Inverting $I_B$		7	22	8	30	nA
CMRR Match		126	115	123	112	dB
PSRR Match		127	118	127	114	dB

## APPLICATIONS INFORMATION

### High Speed Operation

When the feedback around the op amp is resistive ( $R_F$ ), a pole will be created with  $R_F$ , the source resistance and capacitance ( $R_S, C_S$ ), and the amplifier input capacitance ( $C_{IN} \approx 2\text{pF}$ ). In low closed loop gain configurations and

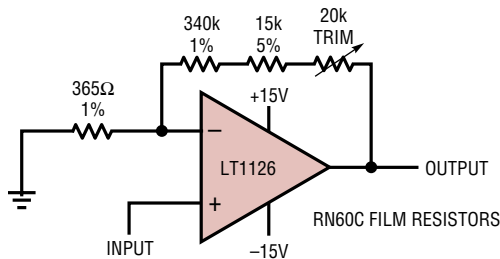
with  $R_S$  and  $R_F$  in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor ( $C_F$ ) in parallel with  $R_F$  eliminates this problem. With  $R_S (C_S + C_{IN}) = R_F C_F$ , the effect of the feedback pole is completely removed.



1126-7 AI01

## TYPICAL APPLICATIONS

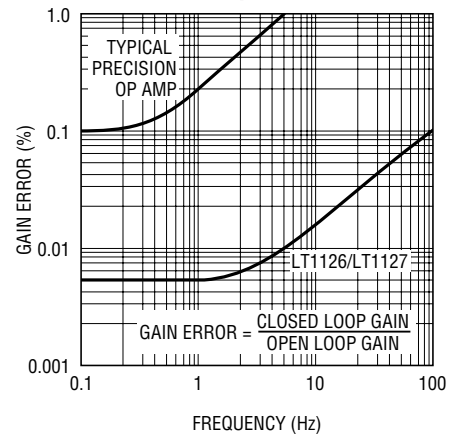
Gain 1000 Amplifier with 0.01% Accuracy, DC to 5Hz



THE HIGH GAIN AND WIDE BANDWIDTH OF THE LT1126/LT1127 IS USEFUL IN LOW FREQUENCY HIGH CLOSED LOOP GAIN AMPLIFIER APPLICATIONS. A TYPICAL PRECISION OP AMP MAY HAVE AN OPEN LOOP GAIN OF ONE MILLION WITH 500kHz BANDWIDTH. AS THE GAIN ERROR PLOT SHOWS, THIS DEVICE IS CAPABLE OF 0.1% AMPLIFYING ACCURACY UP TO 0.3Hz ONLY. EVEN INSTRUMENTATION RANGE SIGNALS CAN VARY AT A FASTER RATE. THE LT1126/LT1127 "GAIN PRECISION — BANDWIDTH PRODUCT" IS 330 TIMES HIGHER, AS SHOWN.

1126-7 TA02

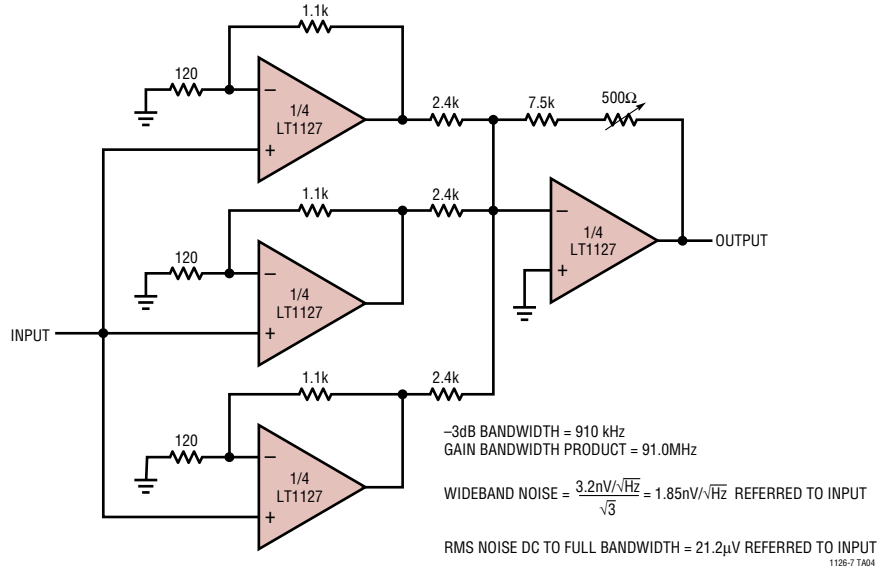
Gain Error vs Frequency  
Closed Loop Gain = 1000



1126-7 TA03

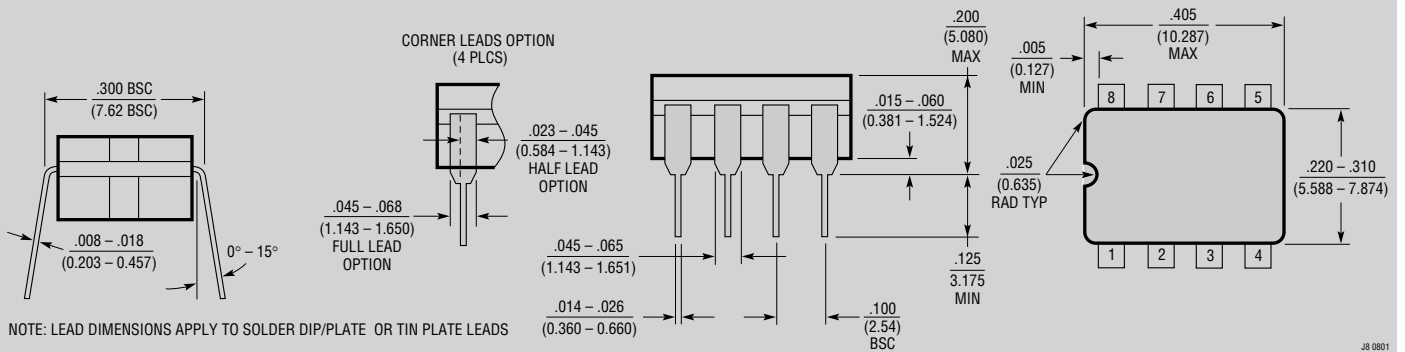
# TYPICAL APPLICATIONS

## Low Noise, Wideband, Gain = 100 Amplifier with High Input Impedance



# PACKAGE DESCRIPTION

## J8 Package 8-Lead CERDIP (Narrow .300 Inch, Hermetic) (Reference LTC DWG # 05-08-1110)

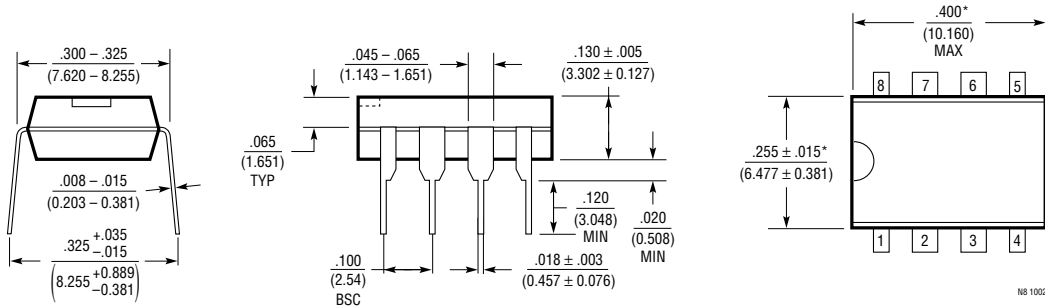


# OBSELETE PACKAGE



# PACKAGE DESCRIPTION

## N8 Package 8-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)



NOTE:  
1. DIMENSIONS ARE  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$   
\*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

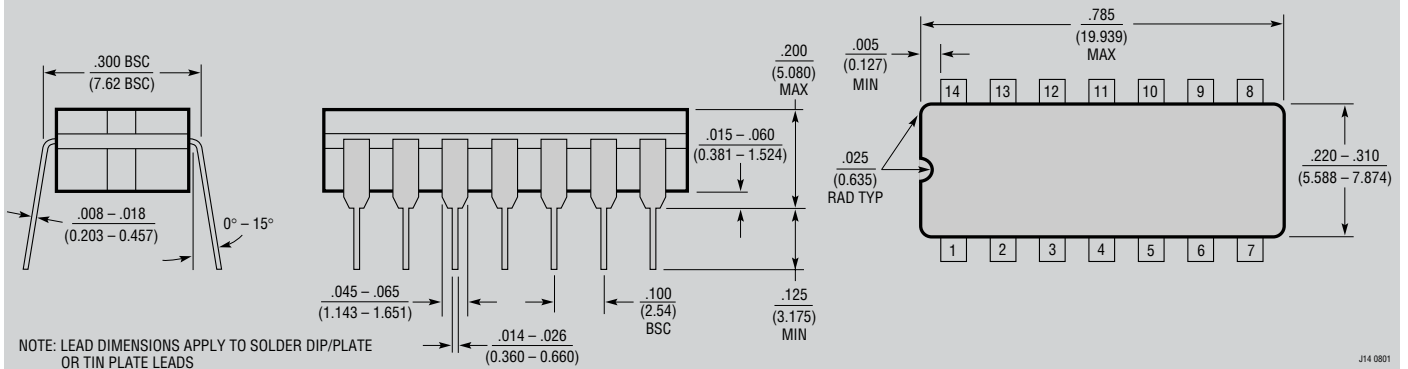
## S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



NOTE:  
1. DIMENSIONS IN  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$   
2. DRAWING NOT TO SCALE  
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

RECOMMENDED SOLDER PAD LAYOUT

## J Package 14-Lead Cerdip (Narrow .300 Inch, Hermetic) (Reference LTC DWG # 05-08-1110)

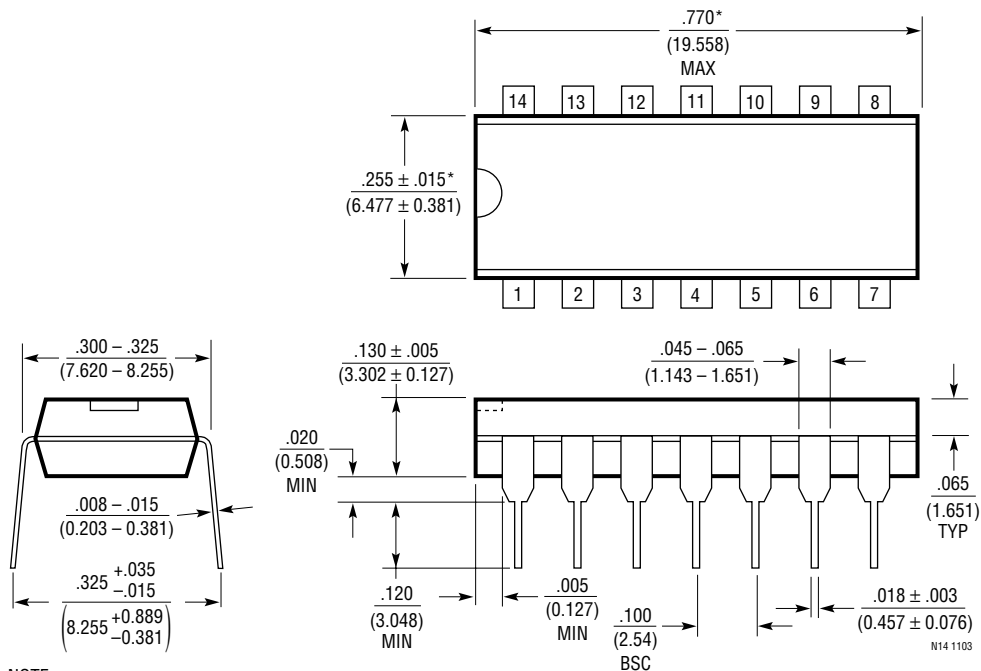


NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS

**OBsolete PACKAGE**

# PACKAGE DESCRIPTION

**N Package**  
**14-Lead PDIP (Narrow .300 Inch)**  
 (Reference LTC DWG # 05-08-1510)

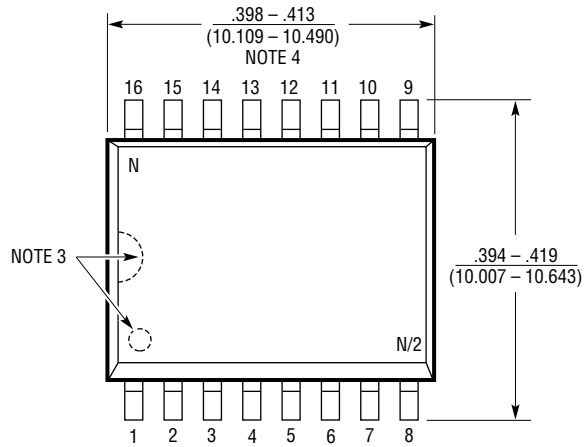


NOTE:  
 1. DIMENSIONS ARE  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

\*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

**PACKAGE DESCRIPTION**

**SW Package**  
**16-Lead Plastic Small Outline (Wide .300 Inch)**  
 (Reference LTC DWG # 05-08-1620)



- NOTE:
1. DIMENSIONS IN  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
  2. DRAWING NOT TO SCALE
  3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
  4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S16 (WIDE) 0502