Power Output Stage Automatic Bias System

FEATURES

- **Set Class AB Bias Currents**
- **Eliminates Adjustments**
- **Eliminates Thermal Runaway of I_Q**
- Corrects for Device Mismatch
- Simplifies Heat Sinking
- Programmable Current Limit
- May Be Paralleled for Higher Current
- Small SO-8 or PDIP Package

APPLICATIONS

- Biasing Power MOSFETs
- High Voltage Amplifiers
- Shaker Table Amplifiers
- Audio Power Amplifiers

DESCRIPTION

The LT®1166 is a bias generating system for controlling class AB output current in high powered amplifiers. When connected with external transistors, the circuit becomes a unity-gain voltage follower. The LT1166 is ideally suited for driving power MOSFET devices because it eliminates all quiescent current adjustments and critical transistor matching. Multiple output stages using the LT1166 can be paralleled to obtain higher output current.

Thermal runaway of the quiescent point is eliminated because the bias system senses the current in each power transistor by using a small external sense resistor. A high speed regulator loop controls the amount of drive applied to each power device. The LT1166 can be biased from a pair of resistors or current sources and because it operates on the drive voltage to the output transistors, it operates on any supply voltage.

TYPICAL APPLICATION

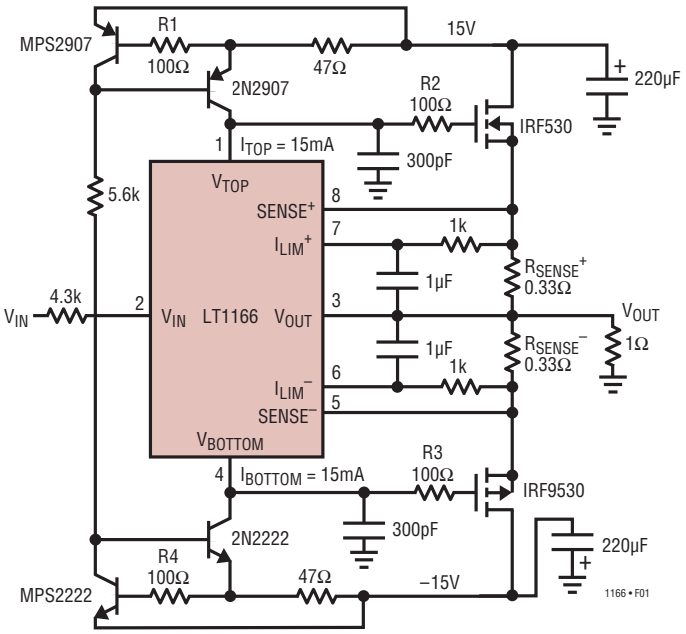
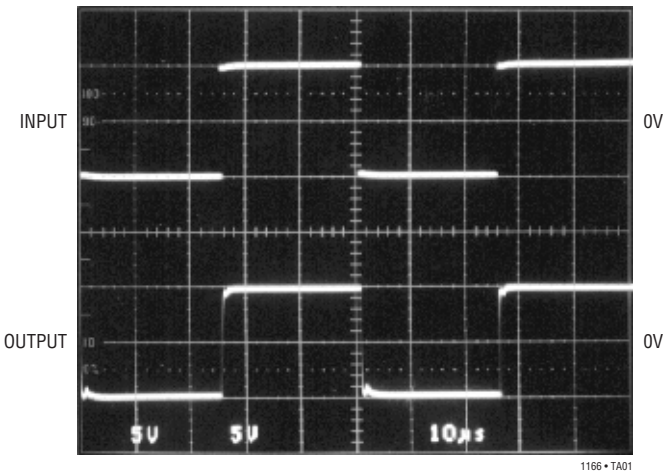


Figure 1. Unity Gain Buffer with Current Limit

Unity Gain Buffer Amp Driving 1Ω Load

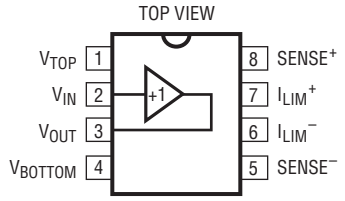


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Current (Pin 1 or Pin 4) 75mA
Differential Voltage (Pin 2 to Pin 3) ..... ±6V
Output Short-Circuit Duration (Note 1) ..... Continuous
Specified Temperature Range (Note 2) ..... 0°C to 70°C
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (Note 3) ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S8)

ORDER INFORMATION

http://www.linear.com/product/LT1166#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1166CN8#PBF	LT1166CN8#TRPBF	1166	8-LEAD PDIP	0°C to 70°C
LT1166CS8#PBF	LT1166CS8#TRPBF	1166	8-LEAD PLASTIC SO	0°C to 70°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Pin 1 = 2V, Pin 4 = –2V, Operating current 15mA and R_{IN} = 20k, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Offset Voltage	Operating Current 15mA to 50mA	●		50	250	mV
Input Bias Current	Operating Current 15mA to 50mA (Note 4)	●		2	10	µA
Input Resistance	Operating Current 15mA to 50mA (Note 5)	●	2	15		MΩ
V_{AB} (Top)	Measure Pin 8 to Pin 3, No Load		14	20	26	mV
V_{AB} (Bottom)	Measure Pin 5 to Pin 3, No Load		–14	–20	–26	mV
Voltage Compliance	Operating Current = 50mA (Notes 6, 9)	●	±2		±10	V
Current Compliance	Operating Voltage = ±2V	●	±4		±50	mA
Transconductance	(Note 7)					
gm_{CC2}	Pin 1 = 2V, Pin 4 = –2V	●	0.08	0.100	0.13	mho
gm_{EE2}	Pin 1 = 2V, Pin 4 = –2V	●	0.08	0.100	0.13	mho
gm_{CC10}	Pin 1 = 10V, Pin 4 = –10V	●	0.09	0.125	0.16	mho
gm_{EE10}	Pin 1 = 10V, Pin 4 = –10V	●	0.09	0.125	0.16	mho
$PSRR_{CC}$	(Note 8)			19		dB
$PSRR_{EE}$	(Note 8)			19		dB
Current Limit Voltage	Operating Current 15mA to 50mA					
	Pin 7 Voltage to Pin 3	●	1.0	1.3	1.5	V
	Pin 6 Voltage to Pin 3	●	–1.0	–1.3	–1.5	V

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Commercial grade parts are designed to operate over the temperature range of –40°C to 85°C but are neither tested nor guaranteed beyond 0°C to 70°C. Industrial grade parts specified and tested over –40°C and 85°C are available on special request, consult factory.

Note 3: T_J calculated from the ambient temperature T_A and the power dissipation P_D according to the following formulas:

LT1166CN8: $T_J = T_A + (P_D \bullet 100°C/W)$

LT1166CS8: $T_J = T_A + (P_D \bullet 150°C/W)$

Note 4: $I_{TOP} = I_{BOTTOM}$

Note 5: The input resistance is typically 15MΩ when the loop is closed. When the loop is open (current limit) the input resistance drops to 200Ω referred to Pin 3.

Note 6: Maximum T_J can be exceeded with 50mA operating current and simultaneous 10V and –10V (20V total).

Note 7: Apply ±200mV to Pin 2 and measure current change in Pin 1 and 4. Pin 3 is grounded.

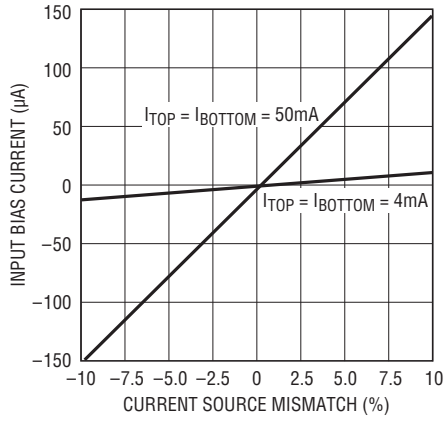
Note 8: $PSRR_{CC} = \dfrac{gm_{CC2} - gm_{CC10}}{gm_{CC2}}$

$PSRR_{EE} = \dfrac{gm_{EE2} - gm_{EE10}}{gm_{EE2}}$

Note 9: For Linear Operation, Pin 1 must not be less than 2V or more than 10V from Pin 3. Similarly, Pin 4 must not be less than 2V or more than 10V from Pin 3.

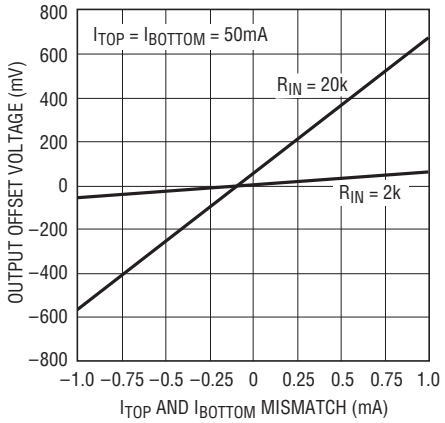
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Current Source Mismatch



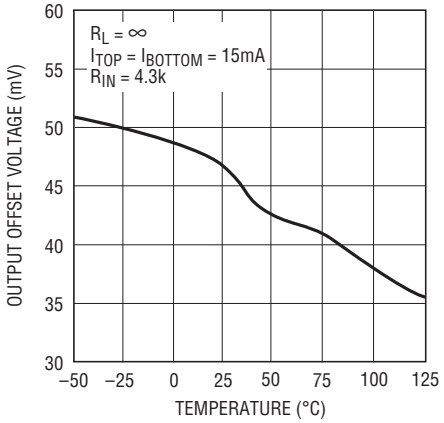
LT1166 • TPC01

Output Offset Voltage vs Current Source Mismatch



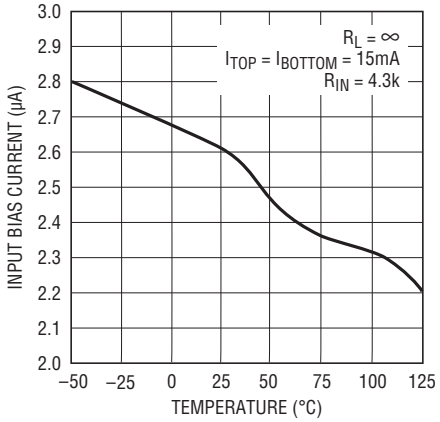
LT1166 • TPC02

Output Offset Voltage vs Temperature



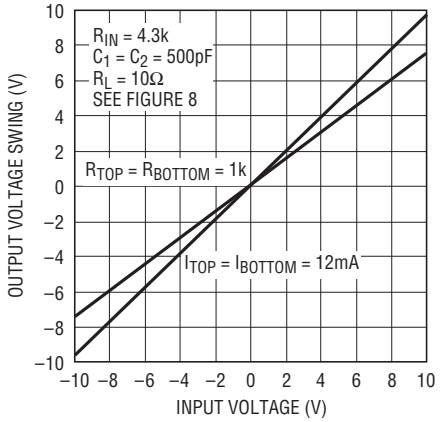
LT1166 • TPC03

Input Bias Current vs Temperature



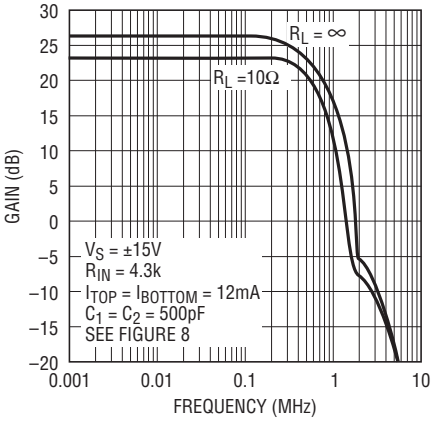
LT1166 • TPC04

Output Voltage vs Input Voltage



LT1166 • TPC05

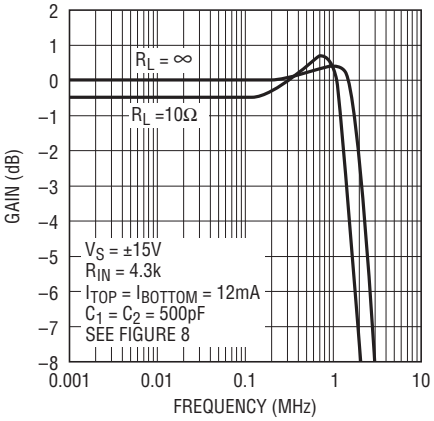
Open-Loop Voltage Gain vs Frequency



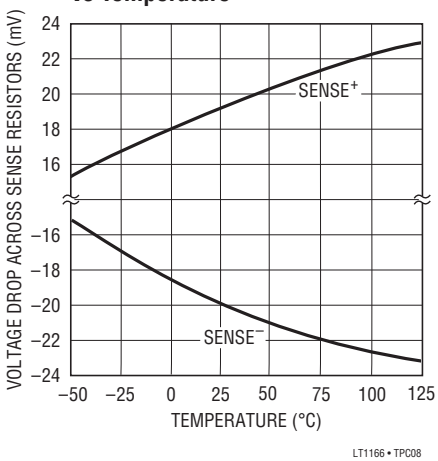
LT1166 • TPC06

TYPICAL PERFORMANCE CHARACTERISTICS

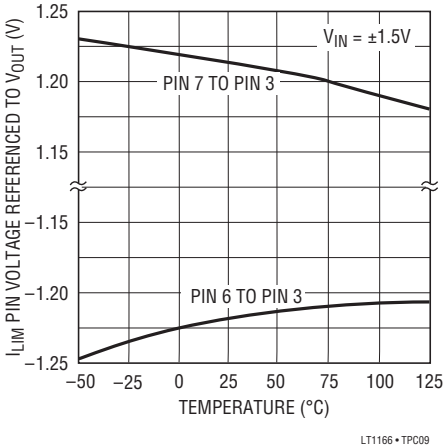
Closed-Loop Voltage Gain vs Frequency



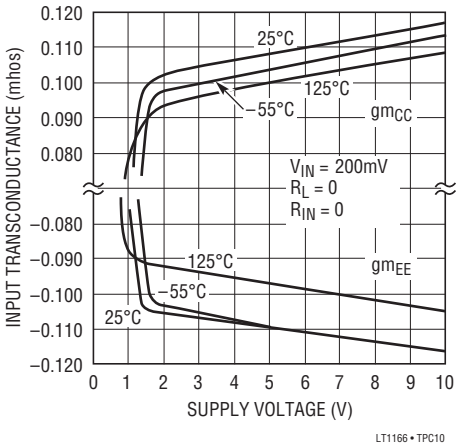
Voltage Across Sense Resistors vs Temperature



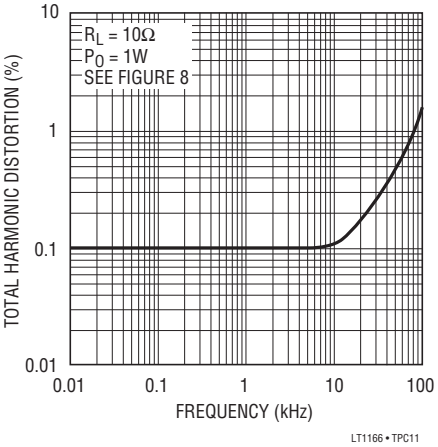
Current Limit Pin Voltage vs Temperature



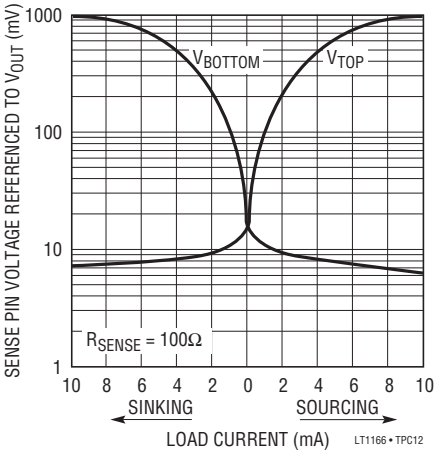
Input Transconductance vs Supply Voltage



Total Harmonic Distortion vs Frequency



Sense Pin Voltage Referenced to V_{OUT} vs Load Current



PIN FUNCTIONS

V_{TOP} (Pin 1): Pin 1 establishes the top side drive voltage for the output transistors. Operating supply current enters Pin 1 and a portion biases internal circuitry; Pin 1 current should be greater than 4mA. Pin 1 voltage is internally clamped to 12V with respect to V_{OUT} and the pin current should be limited to 75mA maximum.

V_{IN} (Pin 2): Pin 2 is the input to a unity gain buffer which drives V_{OUT} (Pin 3). During a fault condition (short-circuit) the input impedance drops to 200Ω and the input current must be limited to 5mA or V_{IN} to V_{OUT} limited to less than ±6V.

V_{OUT} (Pin 3): Pin 3 of the LT1166 is the output of a voltage control loop that maintains the output voltage at the input voltage.

V_{BOTTOM} (Pin 4): Pin 4 establishes the bottom side drive voltage for the output transistors. Operating supply current exits this pin; Pin 4 current should be greater than 4mA. Pin 4 voltage is internally clamped to –12V with respect to V_{OUT} and the pin current should be limited to 75mA maximum.

$SENSE^-$ (Pin 5): The $Sense^-$ pin voltage is established by the current control loop and it controls the output quiescent current in the bottom side power device. Limit the maximum differential voltage between Pin 5 and Pin 3 to ±6V during fault conditions.

I_{LIM}^- (Pin 6): The negative side current limit, limits the voltage at V_{BOTTOM} to V_{OUT} during a negative fault condition. The maximum reverse voltage on Pin 6 with respect to V_{OUT} is 6V.

I_{LIM}^+ (Pin 7): The positive side current limit, limits the voltage at V_{TOP} to V_{OUT} during a positive fault condition. The maximum reverse voltage on Pin 7 with respect to V_{OUT} is –6V.

$SENSE^+$ (Pin 8): The $Sense^+$ pin voltage is established by the current control loop and it controls the output quiescent current in the top side power device. Limit the maximum differential voltage between Pin 8 and Pin 3 to ±6V during fault conditions.

APPLICATIONS INFORMATION

Overvoltage Protection

The supplies V_{TOP} (Pin 1) and V_{BOTTOM} (Pin 4) have clamp diodes that turn on when they exceed ±12V. These diodes act as ESD protection and serve to protect the LT1166 when used with large power MOS devices that produce high V_{GS} voltage. Current into Pin 1 or Pin 4 should be limited to ±75mA maximum.

Multiplier Operation

Figure 2 shows the current multiplier circuit internal to the LT1166 and how it works in conjunction with power output transistors. The supply voltages V_T (top) and V_B (bottom) of the LT1166 are set by the required "on" voltage of the power devices. A reference current I_{REF} sets a constant V_{BE7} and V_{BE8}. This voltage is across emitter base of Q9 and Q10 which are 1/10 the emitter area of Q7 and Q8. The expression for this current multiplier is:

$$V_{BE7} + V_{BE8} = V_{BE9} + V_{BE10}$$

or in terms of current:

$$(I_{C9})(I_{C10}) = (I_{REF})^2/100 = \text{Constant}$$

The product of I_{C9} and I_{C10} is constant. These currents are mirrored and set the voltage on the (+) inputs of a pair of internal op amps. The feedback of the op amps force the same voltage on the (–) inputs and these voltages then appear on the sense resistors in series with the power devices. The product of the two currents in the power devices is constant, as one increases the other decreases. The excellent logging nature of Q9 and Q10 allows this relation to hold over many decades in current.

The total current in Q7 and Q8 is actually the sum of I_{REF} and a small error current from the shunt regulator. During high output current conditions the error current from the regulator decreases. Current conducted by the regulator also decreases allowing V_T or V_B to increase by an amount needed to drive the power devices.

Driving the Input Stage

Figure 3 shows the input transconductance stage of the LT1166 that provides a way to drive V_T and V_B. When a positive voltage V_{IN} is applied to R_{IN}, a small input current flows into R2 and the emitter of Q2. This effect causes V_O to follow V_{IN} within the gain error of the amplifier. The input current is then mirrored by Q3/Q4 and current supplied to Q4's collector is sourced by power device M1. The signal current in Q4's emitter is absorbed by external resistor R_B and this causes V_B to rise by the same amount

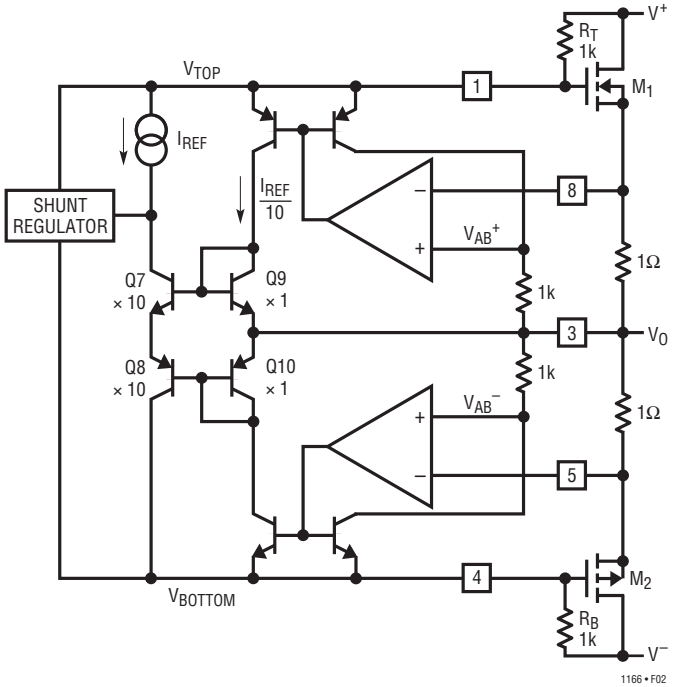


Figure 2. Constant Product Generator

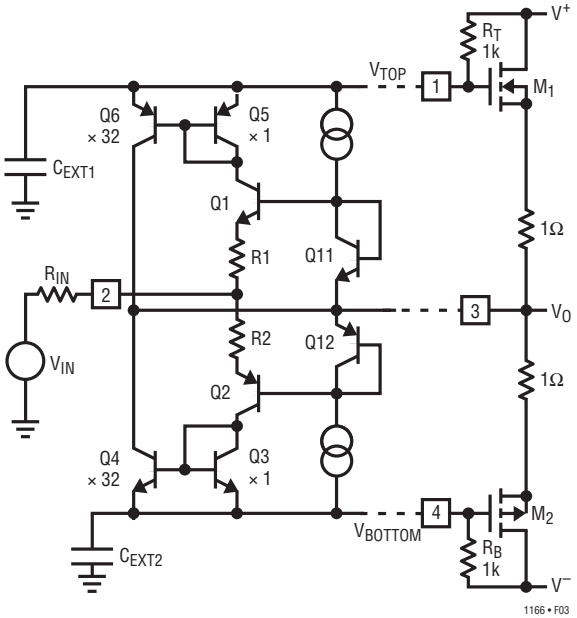


Figure 3. Input Stage Driving Gates

APPLICATIONS INFORMATION

as V_{IN}. Similarly for V_T, when positive voltage is applied to R_{IN}, current that was flowing in R1 and Q1 is now supplied through R_{IN}. This effect reduces the current in mirror Q5/Q6. The reduced current has the effect of reducing the drop on R_T, and V_T rises to make V_O track V_{IN}.

The open-loop voltage gain $V_O/(V_{IN} – V_{PIN2})$ can be increased by replacing R_T and R_B with current sources. The effect of this is to increase the voltage gain V_{OUT}/V_{IN} from approximately 0.8 to 1 (see Typical Performance Characteristics curves). The use of current sources instead of resistors greatly increases loop gain and this compensates for the nonlinearity of the output stage resulting in much lower distortion.

Frequency Compensation and Stability

The input transconductance is set by the input resistor R_{IN} and the 32:1 current mirrors Q3/Q4 and Q5/Q6. The resistors R1 and R2 are small compared to the value of R_{IN}. Current in R_{IN} appears 32 times larger in Q4 or Q6, which drive external compensation capacitors C_{EXT1} and C_{EXT2}. These two input signal paths appear in parallel to give an input transconductance of:

$$g_m = 16/R_{IN}$$

The gain bandwidth is:

$$GBW = \frac{16}{2\pi(R_{IN})(C_{EXT})}$$

Depending on the speed of the output devices, typical values are R_{IN} = 4.3k and $C_{EXT1} = C_{EXT2}$ = 500pF giving a –3dB bandwidth of 1.2MHz (see Typical Performance Characteristics curves).

To prevent instability it is important to provide good supply bypassing as shown in Figure 1. Large supply bypass capacitors (220µF) and short power leads can eliminate instabilities at these high current levels. The 100Ω resistors (R2 and R3) in series with the gates of the output devices stop oscillations in the 100MHz region as do the 100Ω resistors R1 and R4 in Figure 1.

Driving Capacitive Loads

Ideally, amplifiers have enough phase margin that they don't oscillate but just slow down with capacitive loads. Practically, amplifiers that drive significant power require some isolation from heavy capacitive loads to prevent oscillation. This isolation is normally an inductor in series with the output of the amplifier. A 1µH inductor in parallel with a 10Ω resistor is sufficient for many applications.

Setting Output AB Bias Current

Setting the output AB quiescent current requires no adjustments. The internal op amps force V_{AB} = ±20mV between each Sense (Pins 5 and 8) to the Output (Pin 3). At quiescent levels the output current is set by:

$$I_{AB} = 20mV/R_{SENSE}$$

The LT1166 does not require a heat sink or mounting on the heat sink for thermal tracking. The temperature coefficient of V_{AB} is approximately 0.3%/°C and is set by the junction temperature of the LT1166 and not the temperature of the power transistors.

Output Offset Voltage and Input Bias Current

The output offset voltage is a function of the value of R_{IN} and the mismatch between external current sources I_{TOP} and I_{BOTTOM} (see the Typical Performance Characteristics curves). Any error in I_{TOP} and I_{BOTTOM} match is reduced by the 32:1 input current mirror, but is multiplied by the input resistor R_{IN}.

Current Limit

The voltage to activate the current limit is ±1.3V. The simplest way to protect the output transistors is to connect the Current Limit pins 6 and 7 to the Sense pins 5 and 8. A current limit of 1.3A can be set by using 1Ω sense resistors. To keep the current limit circuit from oscillating in hard limit, it is necessary to add an RC (1k and 1µF) between the Sense pin and the I_{LIM} as shown in Figure 1.

The sense resistors can be tapped up or down to increase or decrease the current limit without changing AB bias current in the power transistors. Figure 4 demonstrates

APPLICATIONS INFORMATION

how tapping the sense resistors gives twice the limit current or one half the limit current.

Foldback current limit can be added to the normal or "square" current limit by including two resistors (30k typical) from the power supplies to the I_{LIM} pins as shown in Figure 5. With square current limit the maximum output current is independent of the voltage across the power devices. Foldback limit simply makes the output current dependent on output voltage. This scheme puts dissipation limits on the output devices. The larger the voltage across the power device, the lower the available output current. This is represented in Figure 6, Output Voltage vs Output Current for the circuit of Figure 5.

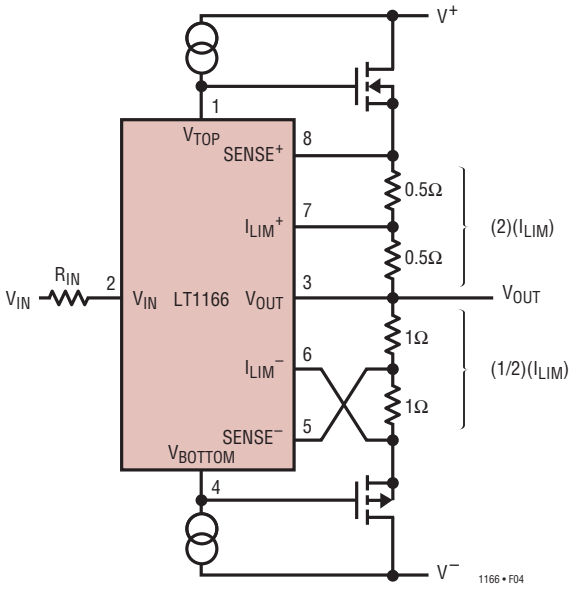


Figure 4. Tapping Current Limit Resistors

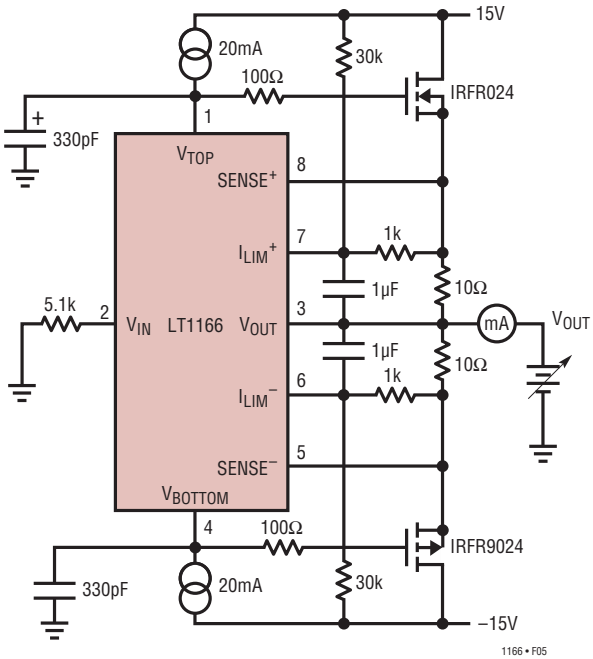


Figure 5. Unity Gain Buffer Amp with Foldback Current Limit

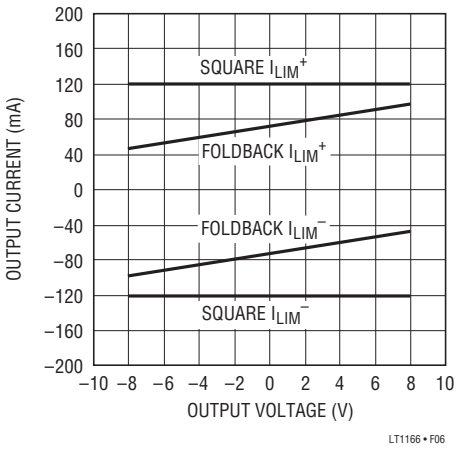


Figure 6. Output Current vs Output Voltage

Driving the Shunt Regulator

It is possible to current drive the shunt regulator directly without driving the input transconductance stage. This has the advantage of higher speed and eliminates the need to compensate the g_m stage. With Pin 2 floating, the LT1166 can be placed inside a feedback loop and driven through the biasing current sources. The input transconductance stage remains biased but has no effect on circuit operation. The R_L in Figure 7 is used to modulate the op amp supply current with input signal. This op amp functions as a V-to-I with the supply leads acting as current source outputs. The load resistor and the positive input of the op amp are connected to the output of the LT1166 for feedback to set A_V = 1V/V. The capacitor C_F eliminates output V_{OS} due to mismatch between I_{TOP} and I_{BOTTOM}, and it also forms a pole at DC and a zero at $1/R_FC_F$. The zero frequency is selected to give a –1V/V gain in the op amp before the phase of the MOSFETs degenerate the stability of the loop.

APPLICATIONS INFORMATION

APPLICATION CIRCUITS

Bipolar Buffer

Similar to the unity gain buffer in Figure 1, the LT1166 can be used to bias bipolar transistors as shown in Figure 8. The minimum operating voltage for the LT1166 is ±2V, so it is necessary to bias the part with adequate voltage from the output stage. The simplest way to do this is to use Darlington drivers and series diodes. There are no thermal tracking circuits or adjustments necessary and the LT1166 does not need to be mounted on the heat sink with the power devices. R_{TOP} and R_{BOTTOM} can be used to replace I_{TOP} and I_{BOTTOM}; see Typical Characteristics curves.

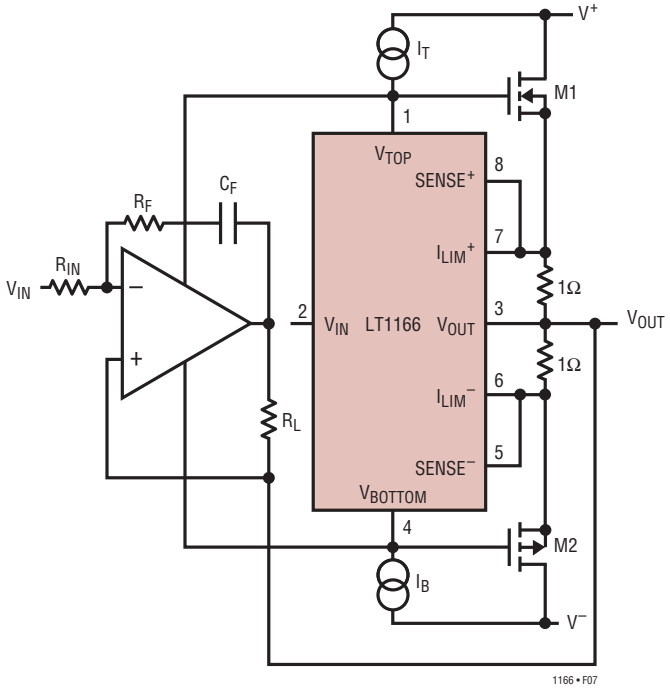


Figure 7. Current Source Drive

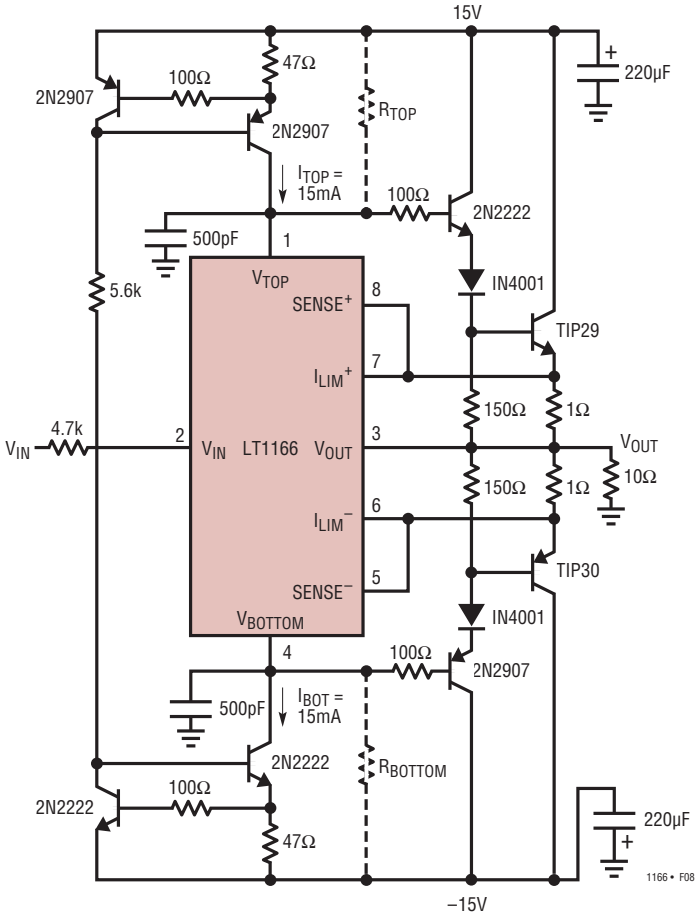


Figure 8. Bipolar Buffer Amp

APPLICATIONS INFORMATION

Adding Voltage Gain

The circuit in Figure 9 adds voltage gain to the circuit in Figure 1. At low frequency the LT1166 is in the feedback loop of the LT1360 so the gain error and the V_{OS} are reduced and the closed-loop gain is 10V/V.

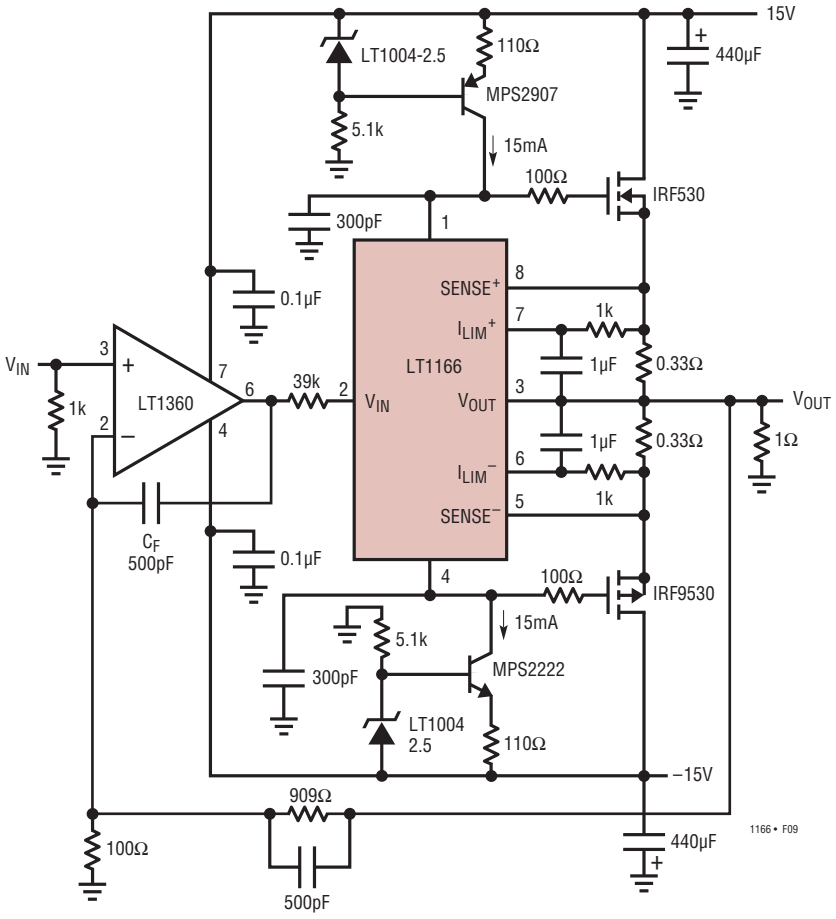


Figure 9. Power Op Amp A_V = 10

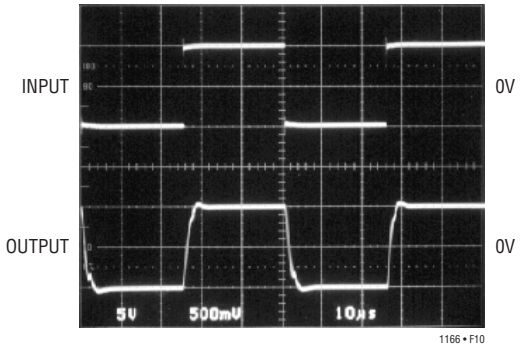


Figure 10. Power Amp Driving 1Ω Load

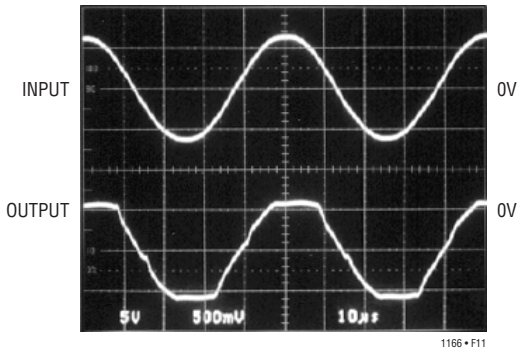


Figure 11. Power Amp at 6A Current Limit

APPLICATIONS INFORMATION

1A Adjustable Voltage Reference

The circuit in Figure 12 uses the LT1166 in a feedback loop with the LT1431 to make a voltage reference with an "attitude." This 5V reference can drive ±1A and maintain 0.4% tolerance at the output. If other output voltages are desired, external resistors can be used instead of the LT1431's internal 5k resistors.

HIGH VOLTAGE APPLICATION CIRCUITS

In order to use op amps in high voltage applications it is necessary to use techniques that confine the amplifier's common mode voltage to its output. The following applications utilize amplifiers operating in suspended-supply operation (Figure 13). See "Linear Technology Magazine" Volume IV Number 2 for a discussion of suspended supplies. The gain setting resistors used in suspended-supply operation must be tight tolerance or the gain will be wrong. For example: with 1% resistors the gain can be as far off as 75%, but with 0.1% resistors that error is cut to less than 5%. Using the values shown in Figure 13, the formula for computing the gain is:

$$A_V = \frac{R8(R9 + R10)}{(R8 \bullet R9) - (R7 \bullet R10)} = -11.22$$

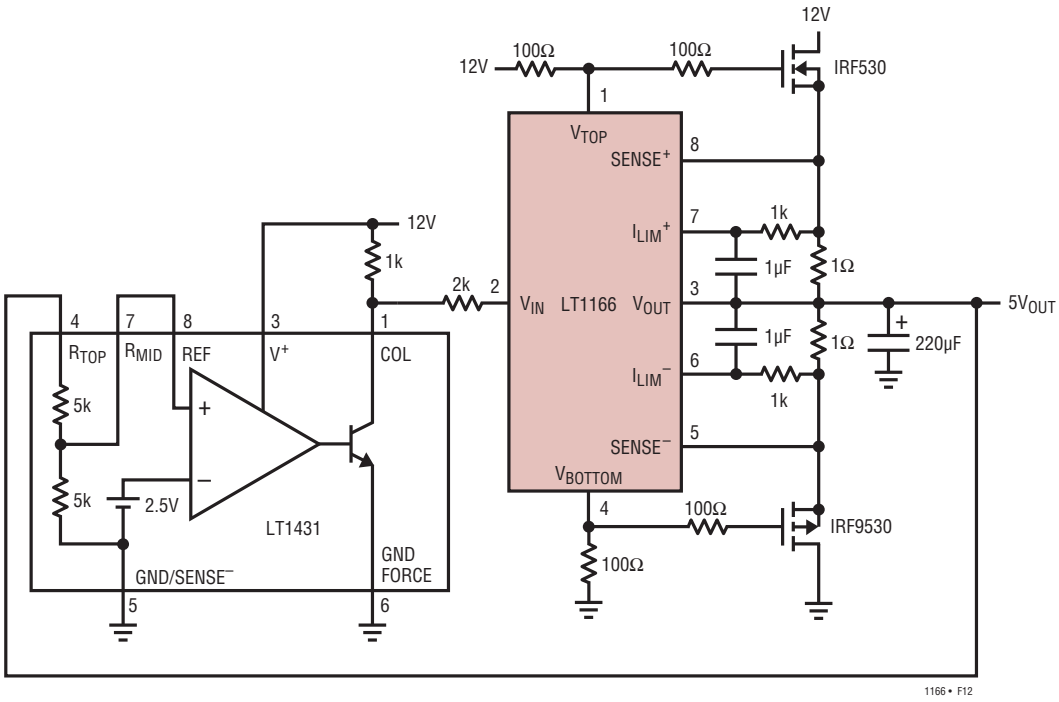


Figure 12. ±1A, 5V Voltage Reference

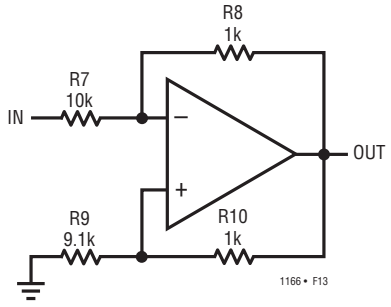
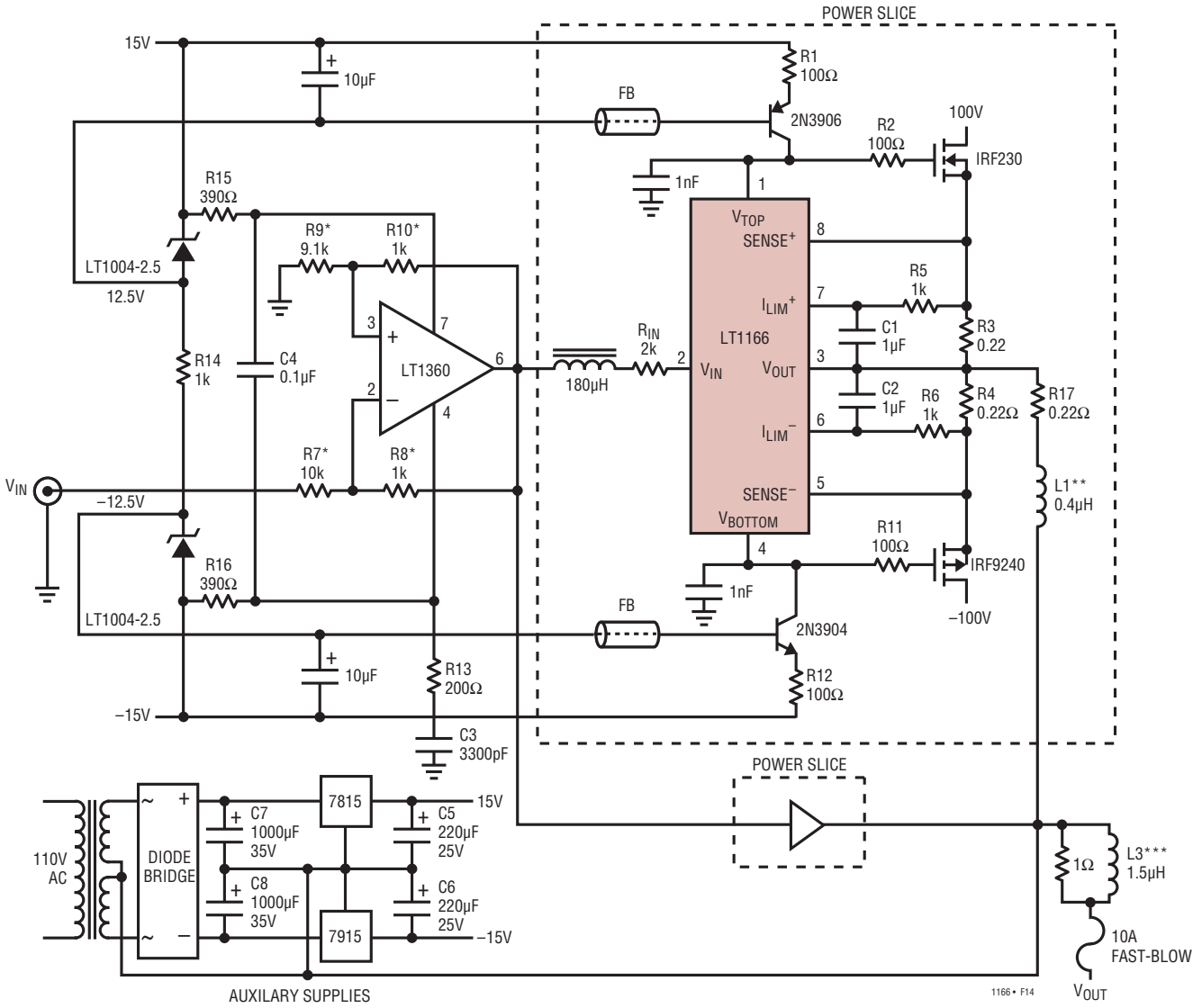


Figure 13. Op Amp in Suspended-Supply Operation

APPLICATIONS INFORMATION

Parallel Operation

Parallel operation is an effective way to get more output power by connecting multiple power drivers. All that is required is a small ballast resistor to ensure current sharing between the drivers and an isolation inductor to keep the drivers apart at high frequency. In Figure 14 one power slice can deliver ±6A at $100V_{PK}$, or 300W RMS into 16Ω. The addition of another slice boosts the power output to 600W RMS into 8Ω and the addition of two or more drivers theoretically raises the power output to 1200W RMS into 4Ω. Due to IR loss across the sense resistors, the FET R_{ON} resistance at 10A, and some sagging of the power supply, the circuit of Figure 14 actually delivers 350W RMS into 8Ω. Performance photos and a THD vs frequency plot are included in Figure 15 through 18. Frequency compensation is provided by the 2k input resistor, 180µH inductor and the 1nF compensation capacitors. The common node in the auxiliary power supplies is connected to amplifier output to generate the floating ±15V supplies.



* 0.1% RESISTORS
** 4 TURNS T37-52 (MICROMETALS)
*** 6 TURNS T80-52 (MICROMETALS)

Figure 14. 350W Shaker Table Amplifier

APPLICATIONS INFORMATION

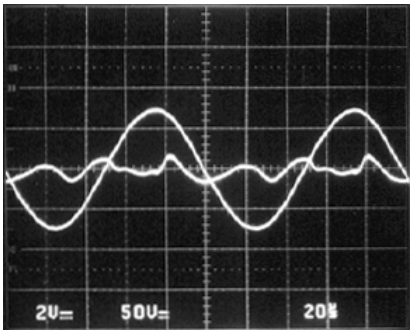


Figure 15. 0.3% THD at 10kHz, P_O = 350W, R_L = 8Ω

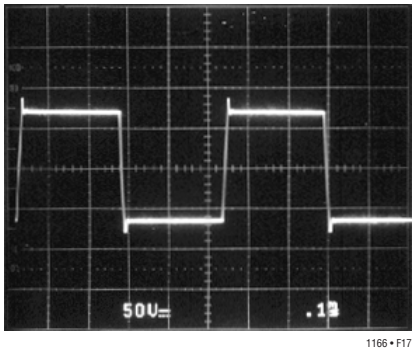


Figure 17. 2kHz Square-Wave, C_L = 1µF

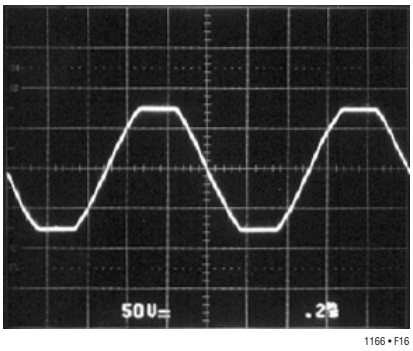


Figure 16. Clipping at 1kHz, R_L = 8Ω

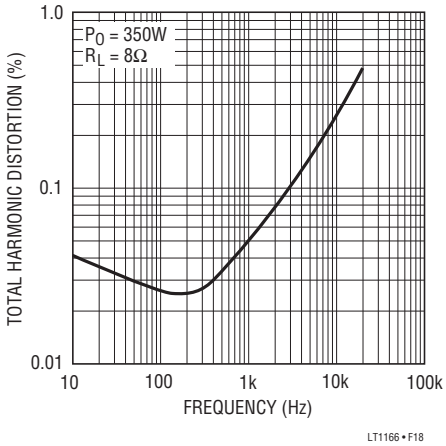


Figure 18. THD vs Frequency

100W Audio Power Amplifier

The details of a low distortion audio amplifier are shown in Figure 19. The LT1360, designated U1, was chosen for its good CMRR and is operated in suspended-supply mode at a closed-loop gain of –26.5V/V. The ±15V supplies of U1 are effectively bootstrapped by the output at point D and are generated as shown in Figure 14. A $3V_{P-P}$ signal at V_{IN} will cause an $80V_{PP}$ output at point A. Resistors 7 to 10 set the gain of –26.5V/V of U1, while C1 compensates for the additional pole generated by the CMRR of U1. The rest of the circuit (point A to point D) is an ultralow distortion unity-gain buffer.

The main component in the unity-gain buffer is U4 (LT1166). This controller performs two important functions, first it modifies the DC voltage between the gates of M1 and M2 by keeping the product of the voltage across R20 and R21 constant. Its secondary role is to perform current limit, protecting M1 and M2 during short-circuit.

The function of U3 is to drive the gates of M1 and M2. This amplifier's real output is not point C as it appears, but rather the Power Supply pins. Current through R6 is used to modulate the supply current and thus provide drive to V_{TOP} and V_{BOTTOM}. Because the output impedance of U3 (through its supply pins) is very high, it is not able to drive the capacitive inputs of M1 and M2 with the combination of speed and accuracy needed to have very low distortion at 20kHz. The purposes of U2 are to drive the gate capacitance of M1 and M2 through its low output impedance and to reduce the nonlinearty of the M1 and M2 transconductance. R24, C4 set a frequency above which U2 no longer looks after U3 and U4, but just looks after itself as its gain goes through unity. R1/R2 and C2/C3 are compensation components for the CMRR feedthough. Curves showing the performance of the amplifier are shown in Figures 20 through 22.

APPLICATIONS INFORMATION

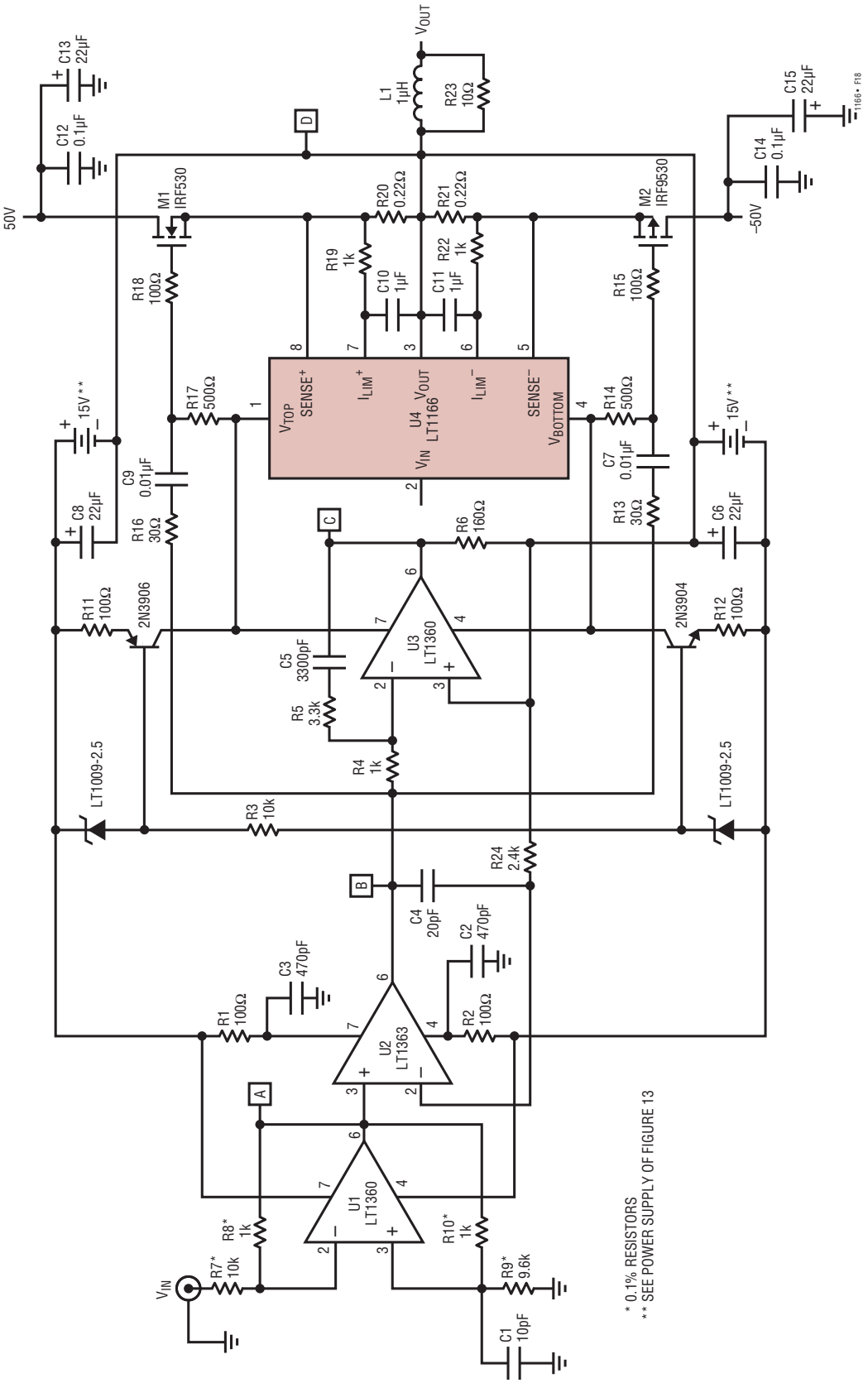
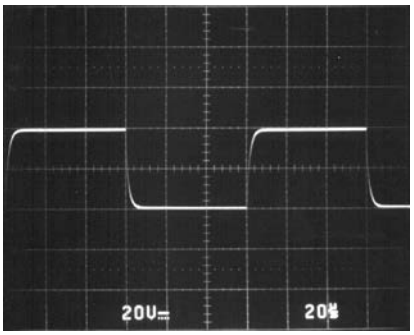


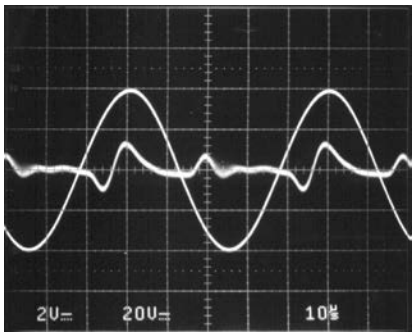
Figure 19. 100W Audio Amplifier

APPLICATIONS INFORMATION



R_L 8Ω
f = 8kHz

Figure 20. Square Wave Response Into 8Ω



R_L 8Ω
f = 20kHz

Figure 21. 100W 20kHz Sine Wave and Its Distortion

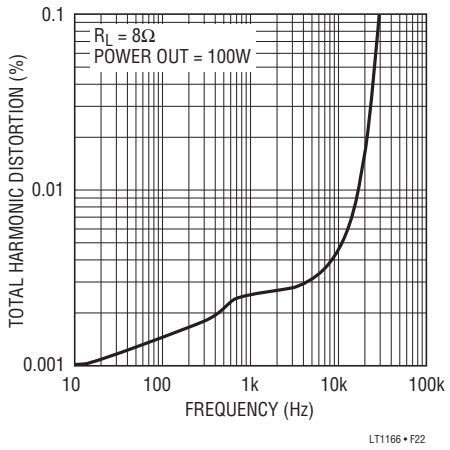
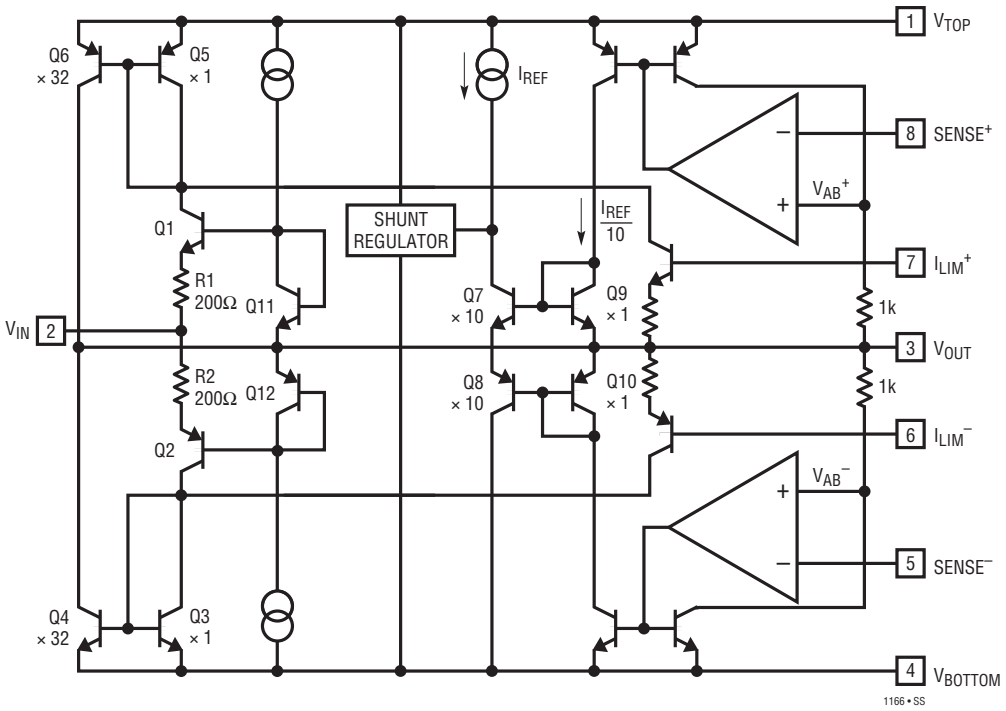


Figure 22. THD vs Frequency

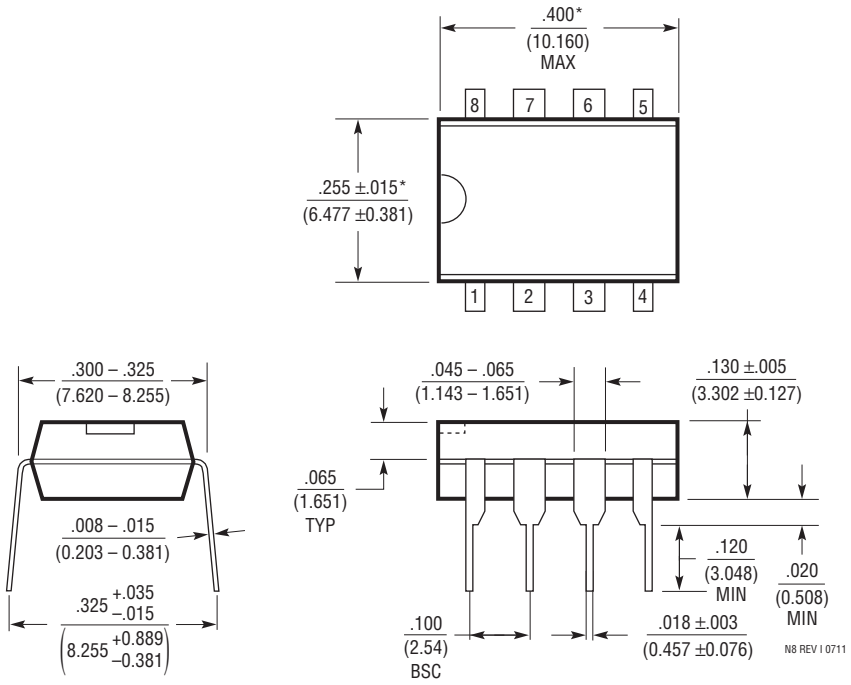
SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT1166#packaging for the most recent package drawings.

N Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510 Rev I)



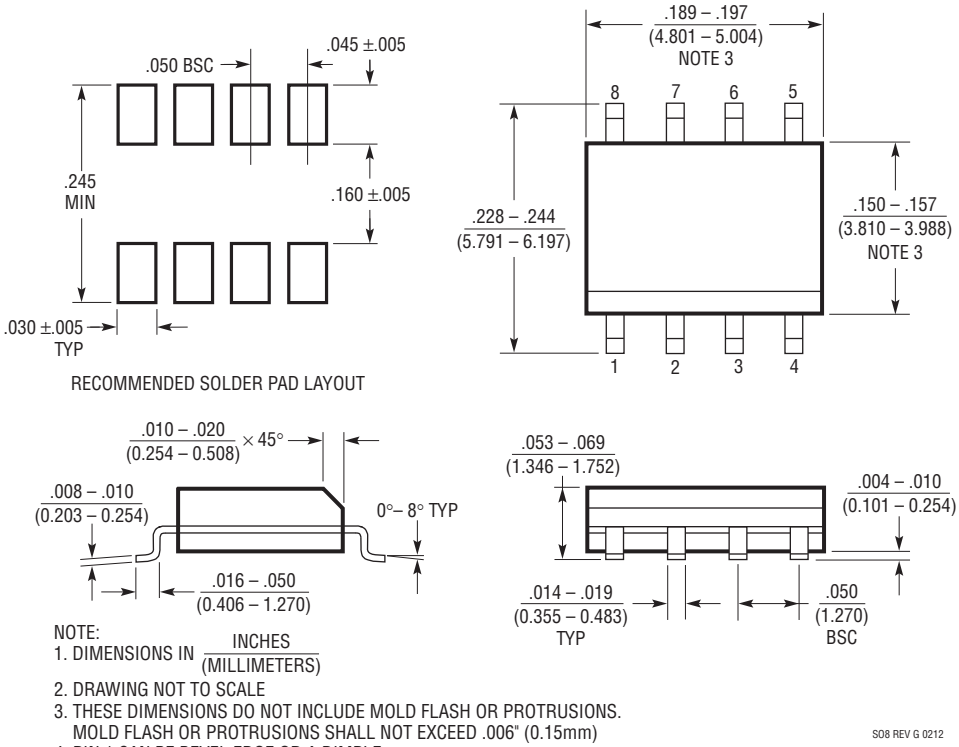
NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT1166#packaging for the most recent package drawings.

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

SO8 REV G 0212

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/17	Updated Order Information.	2
		Corrected pin numbers for U1 and U3.	14