# Very High Speed Operational Amplifier

## FEATURES

- Unity-Gain Stable
- 45MHz Gain-Bandwidth
- 400V/μs Slew Rate
- 7V/mV DC Gain: $R_L$ = 500Ω
- Maximum Input Offset Voltage: 2mV
- ±12V Minimum Output Swing into 500Ω
- Wide Supply Range: ±2.5V to ±15V
- 7mA Supply Current
- 90ns Settling Time to 0.1%, 10V Step
- Drives All Capacitive Loads

## APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- Data Acquisition Systems

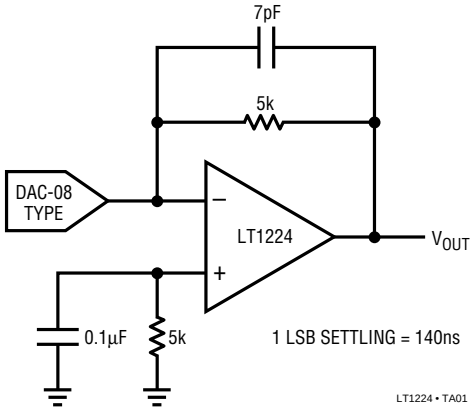
## DESCRIPTION

The LT1224 is a very high speed operational amplifier with excellent DC performance. The LT1224 features reduced input offset voltage and higher DC gain than devices with comparable bandwidth and slew rate. The circuit is a single gain stage with outstanding settling characteristics. The fast settling time makes the circuit an ideal choice for data acquisition systems. The output is capable of driving a 500Ω load to ±12V with ±15V supplies and a 150Ω load to ±3V on ±5V supplies. The circuit is also capable of driving large capacitive loads which makes it useful in buffer or cable driver applications.

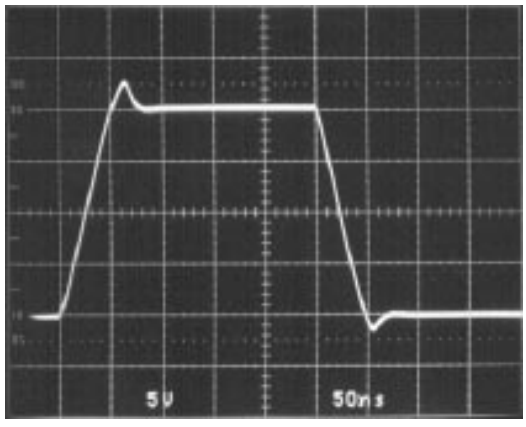
The LT1224 is a member of a family of fast, high performance amplifiers that employ Linear Technology Corporation's advanced bipolar complementary processing.

## TYPICAL APPLICATION

**DAC Current-to-Voltage Converter**



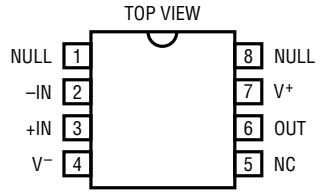

**Inverter Pulse Response**



## ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage ($V^+$ to $V^-$) ..... 36V
Differential Input Voltage ..... ±6V
Input Voltage ..... $\pm V_S$
Output Short Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range
LT1224C ..... 0°C to 70°C
Maximum Junction Temperature
Plastic Package ..... 150°C
Storage Temperature Range ..... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

## PACKAGE/ORDER INFORMATION




N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

LT1224 • POI01

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 100°C/W (N8)
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 150°C/W (S8)

| ORDER PART NUMBER |
|---|
| LT1224CN8<br>LT1224CS8 |
| S8 PART MARKING |
| 1224 |

## ELECTRICAL CHARACTERISTICS

**$V_S$ = ±15V, $T_A$ = 25°C, $R_L$ = 1k, $V_{CM}$ = 0V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | (Note 2) | | 0.5 | 2.0 | mV |
| $I_{OS}$ | Input Offset Current | | | 100 | 400 | nA |
| $I_B$ | Input Bias Current | | | 4 | 8 | µA |
| $e_n$ | Input Noise Voltage | f = 10kHz | | 22 | | nV/√Hz |
| $i_n$ | Input Noise Current | f = 10kHz | | 1.5 | | pA/√Hz |
| $R_{IN}$ | Input Resistance | $V_{CM}$ = ±12V<br>Differential | 24 | 40<br>250 | | MΩ<br>kΩ |
| $C_{IN}$ | Input Capacitance | | | 2 | | pF |
| | Input Voltage Range$^+$ | | 12 | 14 | | V |
| | Input Voltage Range$^-$ | | | –13 | –12 | V |
| CMRR | Common-Mode Rejection Ratio | $V_{CM}$ = ±12V | 86 | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_S$ = ±5V to ±15V | 75 | 84 | | dB |
| $A_{VOL}$ | Large-Signal Voltage Gain | $V_{OUT}$ = ±10V, $R_L$ = 500Ω | 3.3 | 7 | | V/mV |
| $V_{OUT}$ | Output Swing | $R_L$ = 500Ω | ±12.0 | ±13.3 | | V |
| $I_{OUT}$ | Output Current | $V_{OUT}$ = ±12V | 24 | 40 | | mA |
| SR | Slew Rate | $A_{VCL}$ = –2, (Note 3) | 250 | 400 | | V/µs |
| | Full Power Bandwidth | 10V Peak, (Note 4) | | 6.4 | | MHz |
| GBW | Gain-Bandwidth | f = 1MHz | | 45 | | MHz |
| $t_r$, $t_f$ | Rise Time, Fall Time | $A_{VCL}$ = 1, 10% to 90%, 0.1V | | 5 | | ns |
| | Overshoot | $A_{VCL}$ = 1, 0.1V | | 30 | | % |
| | Propagation Delay | 50% $V_{IN}$ to 50% $V_{OUT}$ | | 5 | | ns |
| $t_s$ | Settling Time | 10V Step, 0.1% | | 90 | | ns |
| | Differential Gain | f = 3.58MHz, $R_L$ = 150Ω | | 1 | | % |
| | Differential Phase | f = 3.58MHz, $R_L$ = 150Ω | | 2.4 | | Deg |
| $R_O$ | Output Resistance | $A_{VCL}$ = 1, f = 1MHz | | 2.5 | | Ω |
| $I_S$ | Supply Current | | | 7 | 9 | mA |

## ELECTRICAL CHARACTERISTICS

**$V_S = \pm 5V$, $T_A = 25°C$, $R_L = 1k$, $V_{CM} = 0V$ unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | (Note 2) | | 1 | 4 | mV |
| $I_{OS}$ | Input Offset Current | | | 100 | 400 | nA |
| $I_B$ | Input Bias Current | | | 4 | 8 | µA |
| | Input Voltage Range$^+$ | | 2.5 | 4 | | V |
| | Input Voltage Range$^-$ | | | –3 | –2.5 | V |
| CMRR | Common-Mode Rejection Ratio | $V_{CM} = \pm 2.5V$ | 86 | 98 | | dB |
| $A_{VOL}$ | Large-Signal Voltage Gain | $V_{OUT} = \pm 2.5V$, $R_L = 500\Omega$<br>$V_{OUT} = \pm 2.5V$, $R_L = 150\Omega$ | 2.5 | 7<br>3 | | V/mV<br>V/mV |
| $V_{OUT}$ | Output Swing | $R_L = 500\Omega$<br>$R_L = 150\Omega$ | ±3.0<br>±3.0 | ±3.7<br>±3.3 | | V<br>V |
| $I_{OUT}$ | Output Current | $V_{OUT} = \pm 3V$ | 20 | 40 | | mA |
| SR | Slew Rate | $A_{VCL} = -2$, (Note 3) | | 250 | | V/µs |
| | Full Power Bandwidth | 3V Peak, (Note 4) | | 13.3 | | MHz |
| GBW | Gain-Bandwidth | f = 1MHz | | 34 | | MHz |
| $t_r$, $t_f$ | Rise Time, Fall Time | $A_{VCL} = 1$, 10% to 90%, 0.1V | | 7 | | ns |
| | Overshoot | $A_{VCL} = 1$, 0.1V | | 20 | | % |
| | Propagation Delay | 50% $V_{IN}$ to 50% $V_{OUT}$ | | 7 | | ns |
| $t_s$ | Settling Time | –2.5V to 2.5V, 0.1% | | 90 | | ns |
| $I_S$ | Supply Current | | | 7 | 9 | mA |

## ELECTRICAL CHARACTERISTICS

**$0°C \le T_A \le 70°C$, $R_L = 1k$, $V_{CM} = 0V$ unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V_S = \pm 15V$, (Note 2)<br>$V_S = \pm 5V$, (Note 2) | | 1<br>2 | 4<br>5 | mV<br>mV |
| | Input $V_{OS}$ Drift | | | 25 | | µV/°C |
| $I_{OS}$ | Input Offset Current | $V_S = \pm 15V$ and $V_S = \pm 5V$ | | 100 | 600 | nA |
| $I_B$ | Input Bias Current | $V_S = \pm 15V$ and $V_S = \pm 5V$ | | 4 | 9 | µA |
| CMRR | Common-Mode Rejection Ratio | $V_S = \pm 15V$, $V_{CM} = \pm 12V$ and $V_S = \pm 5V$, $V_{CM} = \pm 2.5V$ | 83 | 98 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_S = \pm 5V$ to $\pm 15V$ | 73 | 84 | | dB |
| $A_{VOL}$ | Large-Signal Voltage Gain | $V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L = 500\Omega$<br>$V_S = \pm 5V$, $V_{OUT} = \pm 2.5V$, $R_L = 500\Omega$ | 2.5<br>2.0 | 7<br>7 | | V/mV<br>V/mV |
| $V_{OUT}$ | Output Swing | $V_S = \pm 15V$, $R_L = 500\Omega$<br>$V_S = \pm 5V$, $R_L = 500\Omega$ or $150\Omega$ | ±12.0<br>±3.0 | ±13.3<br>±3.3 | | V<br>V |
| $I_{OUT}$ | Output Current | $V_S = \pm 15V$, $V_{OUT} = \pm 12V$<br>$V_S = \pm 5V$, $V_{OUT} = \pm 3V$ | 24<br>20 | 40<br>40 | | mA<br>mA |
| SR | Slew Rate | $V_S = \pm 15V$, $A_{VCL} = -2$, (Note 3) | 250 | 400 | | V/µs |
| $I_S$ | Supply Current | $V_S = \pm 15V$ and $V_S = \pm 5V$ | | 7 | 10.5 | mA |

**Note 1:** A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

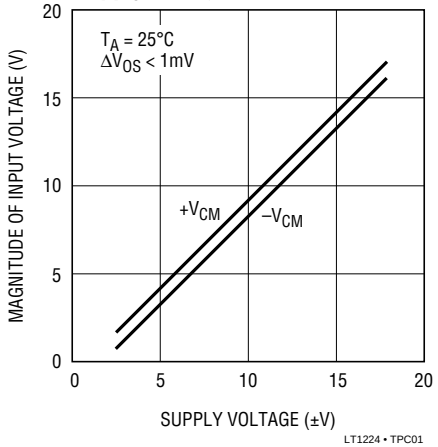
**Note 2:** Input offset voltage is tested with automated test equipment in <1 second.

**Note 3:** Slew rate is measured in a gain of –2 between ±10V on the output with ±6V on the input for ±15V supplies and ±2V on the output with ±1.75V on the input for ±5V supplies.

**Note 4:** Full power bandwidth is calculated from the slew rate measurement: FPBW = SR/2πVp.

# TYPICAL PERFORMANCE CHARACTERISTICS

**Input Common-Mode Range vs Supply Voltage**

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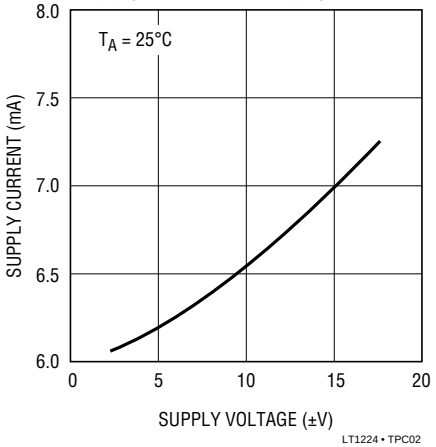
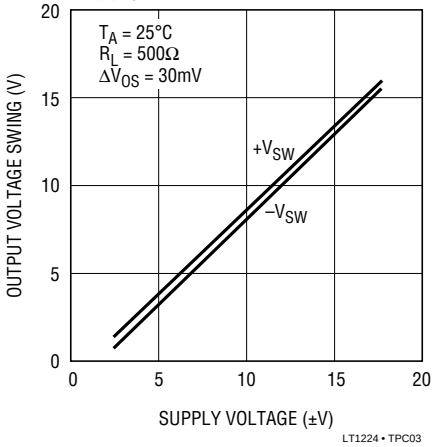
**Supply Current vs Supply Voltage**



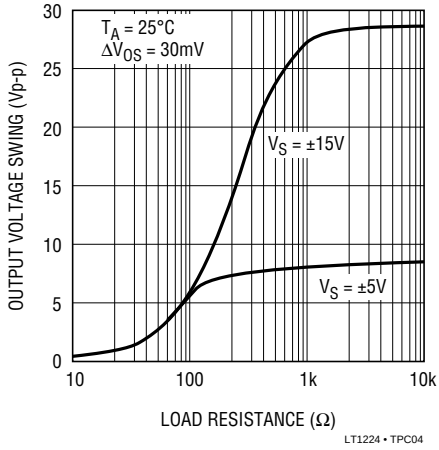

LT1224 • TPC02

**Output Voltage Swing vs Supply Voltage**



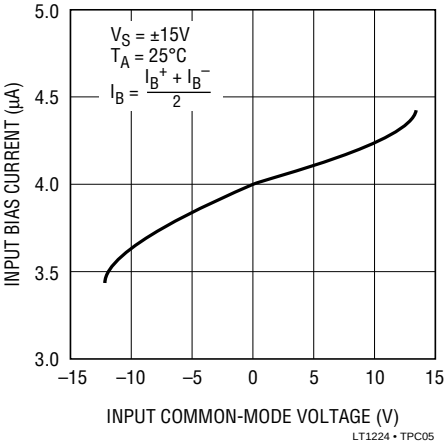

LT1224 • TPC03

**Output Voltage Swing vs Resistive Load**



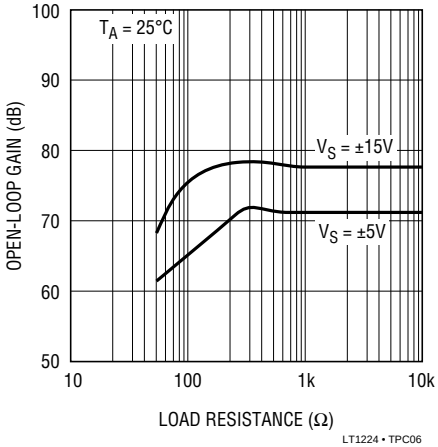

LT1224 • TPC04

**Input Bias Current vs Input Common-Mode Voltage**



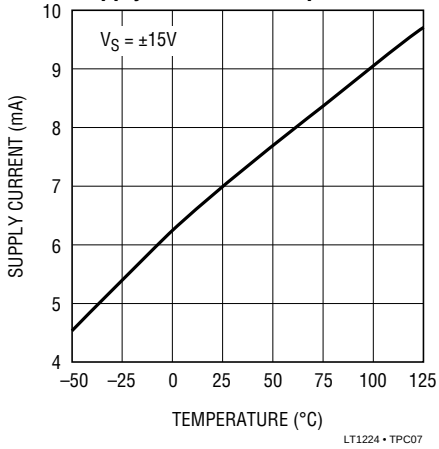

LT1224 • TPC05

**Open-Loop Gain vs Resistive Load**



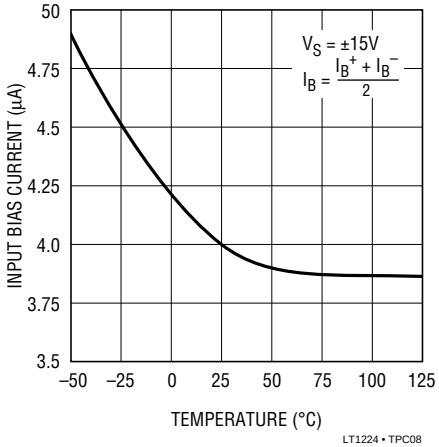

LT1224 • TPC06

**Supply Current vs Temperature**



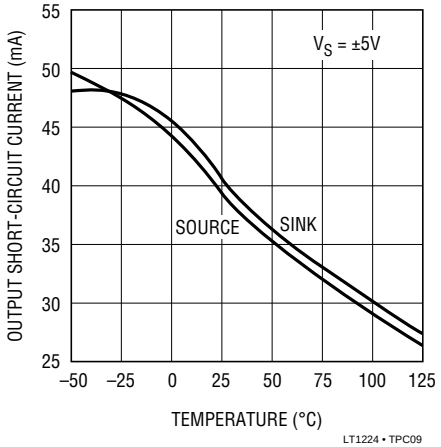

LT1224 • TPC07

**Input Bias Current vs Temperature**




LT1224 • TPC08

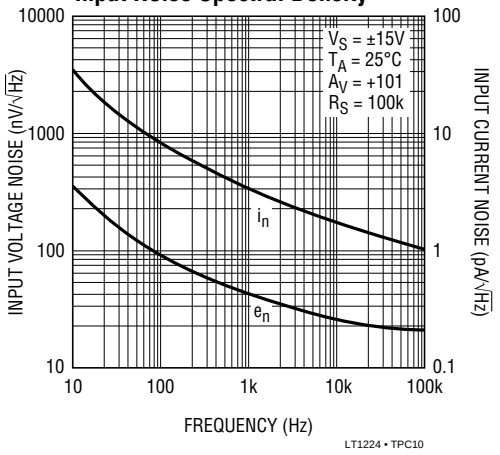
**Output Short Circuit Current vs Temperature**




LT1224 • TPC09

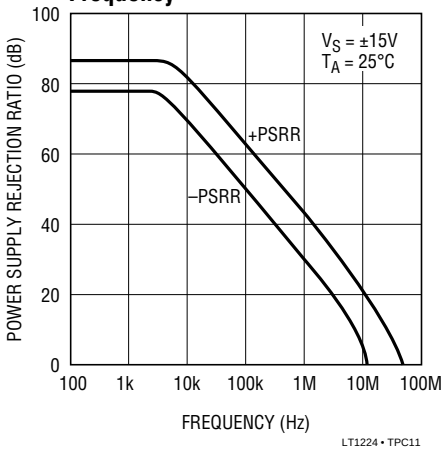
# TYPICAL PERFORMANCE CHARACTERISTICS

### Input Noise Spectral Density



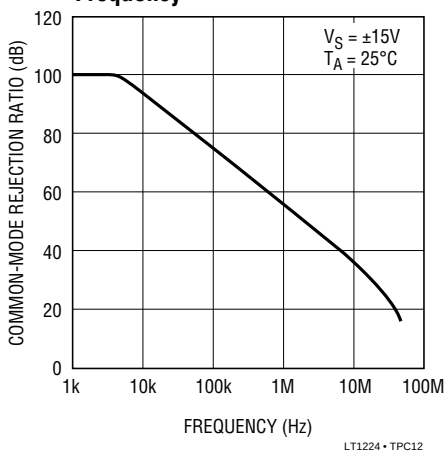

LT1224 • TPC10

### Power Supply Rejection Ratio vs Frequency



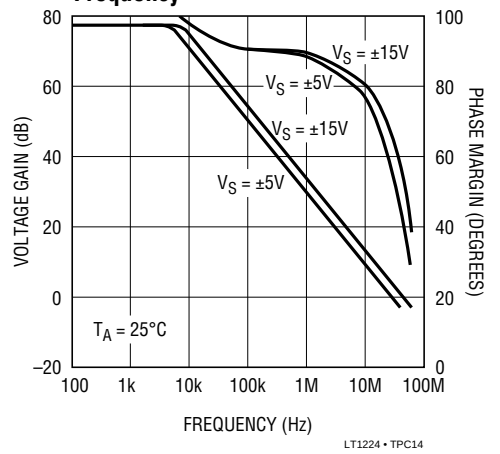

LT1224 • TPC11

### Common Mode Rejection Ratio vs Frequency



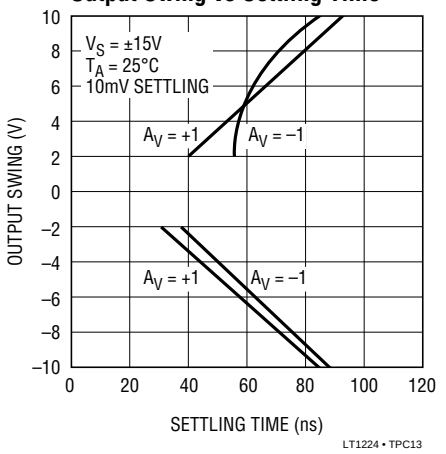

LT1224 • TPC12

### Voltage Gain and Phase vs Frequency



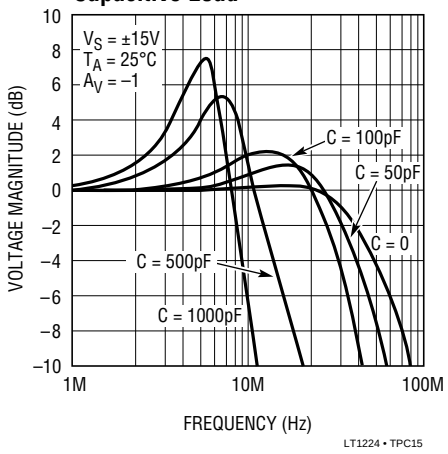

LT1224 • TPC14

### Output Swing vs Settling Time



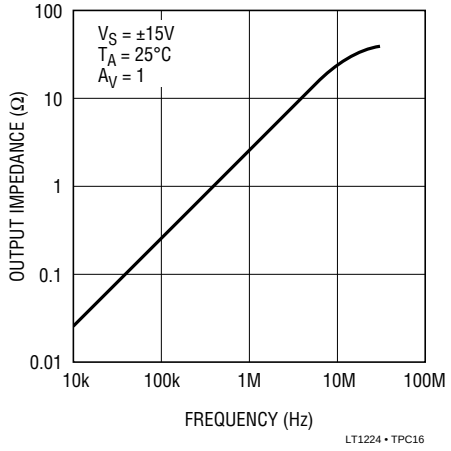

LT1224 • TPC13

### Frequency Response vs Capacitive Load



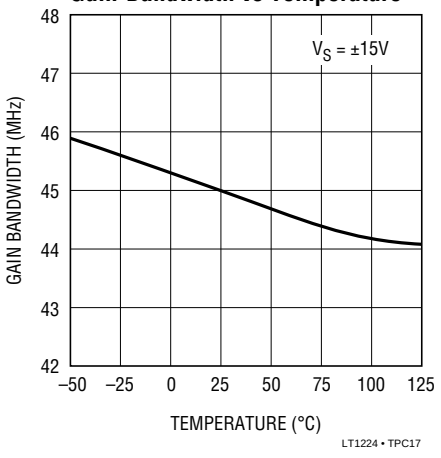

LT1224 • TPC15

### Closed-Loop Output Impedance vs Frequency



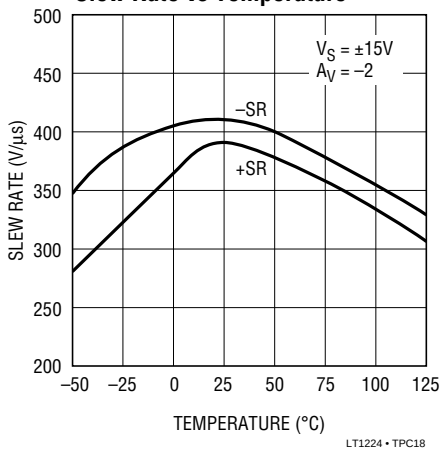

LT1224 • TPC16

### Gain-Bandwidth vs Temperature




LT1224 • TPC17

### Slew Rate vs Temperature

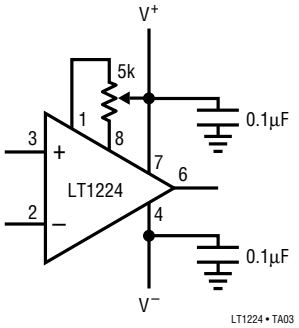



LT1224 • TPC18

## APPLICATIONS INFORMATION

The LT1224 may be inserted directly into HA2541, HA2544, AD847, EL2020 and LM6361 applications, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1224 is shown below.

**Offset Nulling**



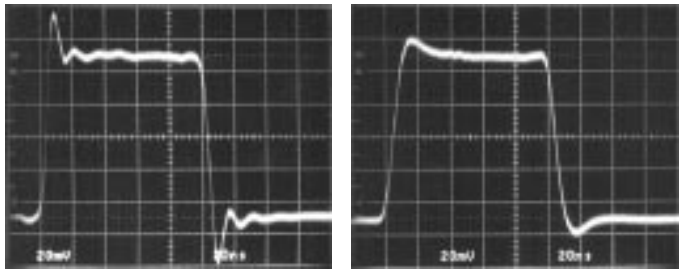

### Layout and Passive Components

As with any high speed operational amplifier, care must be taken in board layout in order to obtain maximum performance. Key layout issues include: use of a ground plane, minimization of stray capacitance at the input pins, short lead lengths, RF-quality bypass capacitors located close to the device (typically 0.01µF to 0.1µF), and use of low ESR bypass capacitors for high drive current applications (typically 1µF to 10µF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50. Feedback resistor values greater than 5k are not recommended because a pole is formed with the input capacitance which can cause peaking. If feedback resistors greater than 5k are used, a parallel capacitor of 5pF to 10pF should be used to cancel the input pole and optimize dynamic performance.

### Transient Response

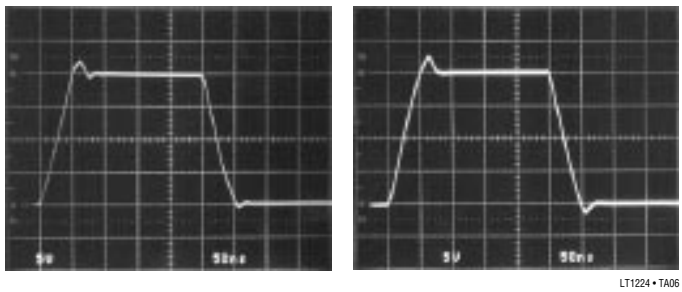
The LT1224 gain bandwidth is 45MHz when measured at f = 1MHz. The actual frequency response in unity-gain is considerably higher than 45MHz due to peaking caused by a second pole beyond the unity-gain crossover. This is reflected in the 50° phase margin and shows up as overshoot in the unity-gain small-signal transient response. Higher noise gain configurations exhibit less overshoot as seen in the inverting gain of one response.

**Small Signal, $A_V = 1$** **Small Signal, $A_V = -1$**




The large-signal responses in both inverting and noninverting gain show symmetrical slewing characteristics. Normally the noninverting response has a much faster rising edge than falling edge due to the rapid change in input common-mode voltage which affects the tail current of the input differential pair. Slew enhancement circuitry has been added to the LT1224 so that the noninverting slew rate response is balanced.

**Large Signal, $A_V = 1$** **Large Signal, $A_V = -1$**




### Input Considerations

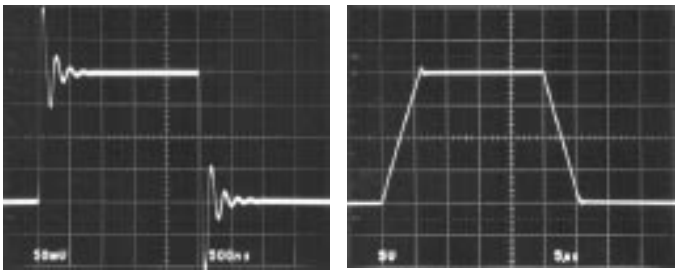
Resistors in series with the inputs are recommended for the LT1224 in applications where the differential input voltage exceeds ±6V continuously or on a transient basis. An example would be in noninverting configurations with high input slew rates or when driving heavy capacitive loads. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

# APPLICATIONS INFORMATION

### Capacitive Loading

The LT1224 is stable with all capacitive loads. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. The photo of the small-signal response with 1000pF load shows 50% peaking. The large-signal response with a 10,000pF load shows the output slew rate being limited by the short-circuit current.

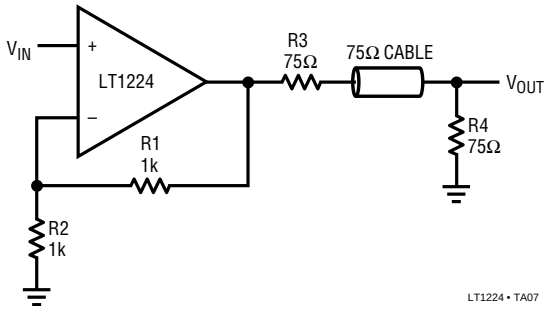
**$A_V = -1$, $C_L = 1000pF$** **$A_V = 1$, $C_L = 10{,}000pF$**



LT1224 • TA06

The LT1224 can drive coaxial cable directly, but for best pulse fidelity the cable should be doubly terminated with a resistor in series with the output.

**Cable Driving**



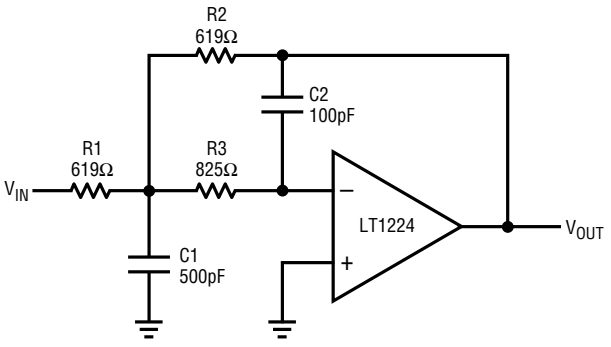

LT1224 • TA07

### DAC Current-to-Voltage Converter

The wide bandwidth, high slew rate and fast settling time of the LT1224 make it well-suited for current-to-voltage conversion after current output D/A converters. A typical application is shown on the first page of this data sheet with a DAC-08 type converter with a full-scale output of 2mA. A compensation capacitor is used across the feedback resistor to null the pole at the inverting input caused by the DAC output capacitance. The combination of the LT1224 and DAC settles to 40mV in 140ns for both a 0V to 10V step and for a 10V to 0V step.

# TYPICAL APPLICATIONS

**1MHz, 2nd Order Butterworth Filter**




–38dB AT 10MHz
SMALL SIGNAL OVERSHOOT = 10%

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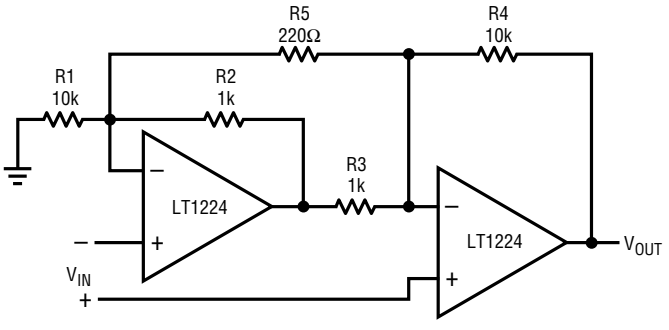
**Two Op Amp Instrumentation Amplifier**




$$A_V = \frac{R4}{R3}\left[1 + \frac{1}{2}\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{R2 + R3}{R5}\right] = 102$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON-MODE REJECTION
BW = 430kHz

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