Half-Bridge N-Channel Power MOSFET Driver with Boost Regulator

FEATURES

- **Floating Top Driver Switches Up to 60V**
- **Internal Boost Regulator for DC Operation**
- **180ns Transition Times Driving 10,000pF**
- **Adaptive Nonoverlapping Gate Drives Prevent Shoot-Through**
- Drives Gate of Top N-Channel MOSFET Above Supply
- Top Drive Maintained at High Duty Cycles
- TTL/CMOS Input Levels
- Undervoltage Lockout with Hysteresis
- Operates at Supply Voltages from 10V to 15V
- Separate Top and Bottom Drive Pins

APPLICATIONS

- PWM of High Current Inductive Loads
- Half-Bridge and Full-Bridge Motor Control
- Synchronous Step-Down Switching Regulators
- 3-Phase Brushless Motor Drive
- High Current Transducer Drivers
- Class D Power Amplifiers

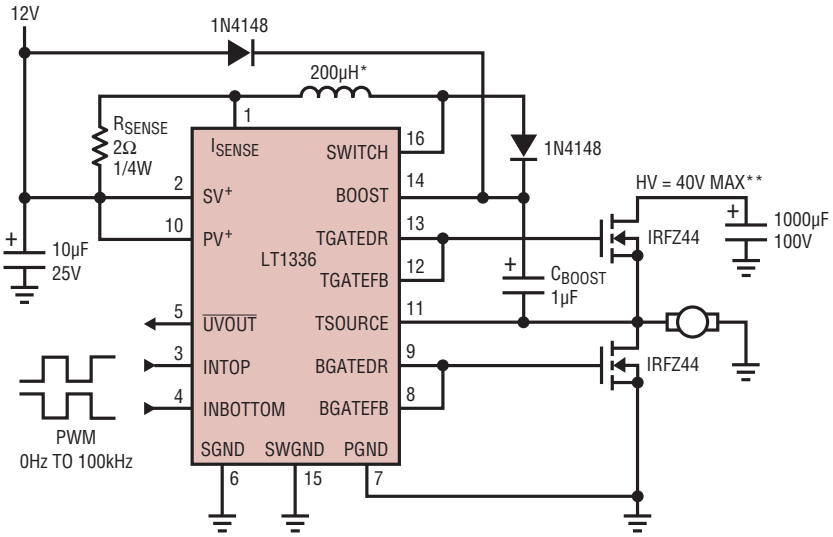
DESCRIPTION

The LT®1336 is a cost effective half-bridge N-channel power MOSFET driver. The floating driver can drive the topside N-channel power MOSFETs operating off a high voltage (HV) rail of up to 60V (absolute maximum). In PWM operation an on-chip switching regulator maintains charge in the bootstrap capacitor even when approaching and operating at 100% duty cycle.

The internal logic prevents the inputs from turning on the power MOSFETs in a half-bridge at the same time. Its unique adaptive protection against shoot-through currents eliminates all matching requirements for the two MOSFETs. This greatly eases the design of high efficiency motor control and switching regulator systems.

During low supply or start-up conditions, the undervoltage lockout actively pulls the driver outputs low to prevent the power MOSFETs from being partially turned on. The 0.5V hysteresis allows reliable operation even with slowly varying supplies.

TYPICAL APPLICATION



INTOP	INBOTTOM	TGATEDR	BGATEDR
L	L	L	L
L	H	L	H
H	L	H	L
H	H	L	L

* SUMIDA RCR-664D-221KC

** FOR HV > 40V SEE "DERIVING THE FLOATING SUPPLY WITH THE FLYBACK TOPOLOGY" IN APPLICATIONS INFORMATION SECTION

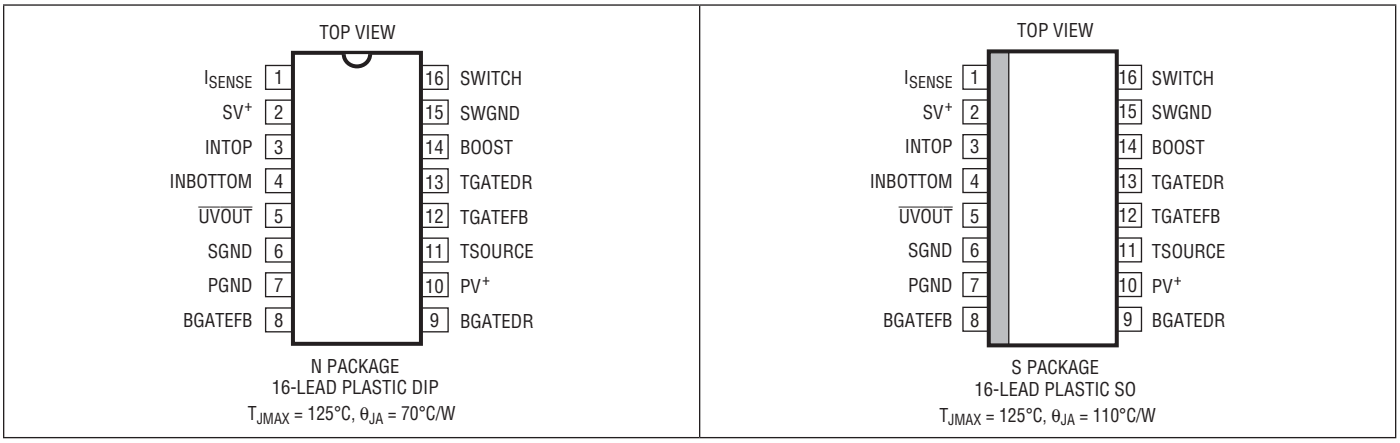
1336 TA01

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (Pins 2, 10) 20V
Boost Voltage 75V
Peak Output Currents (<10µs) 1.5A
Input Pin Voltages ..... –0.3V to V^+ + 0.3V
Top Source Voltage ..... –5V to 60V
Boost-to-Source Voltage
($V_{BOOST} – V_{TSOURCE}$) ..... –0.3V to 20V
Switch Voltage (Pin 16) ..... –0.3V to 60V
Operating Temperature Range
Commercial ..... 0°C to 70°C
Industrial ..... –40°C to 85°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1336CN#PBF	LT1336CN#TRPBF	LT1336CN	16-Lead Plastic DIP	0°C to 70°C
LT1336IN#PBF	LT1336IN#TRPBF	LT1336IN	16-Lead Plastic DIP	–40°C to 85°C
LT1336CS#PBF	LT1336CS#TRPBF	LT1336CS	16-Lead Plastic SO	0°C to 70°C
LT1336IS#PBF	LT1336IS#TRPBF	LT1336IS	16-Lead Plastic SO	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test Circuit, $V^+ = V_{BOOST}$ = 12V, $V_{TSOURCE}$ = 0V and Pins 1, 16 open. Gate Feedback pins connected to Gate Drive pins unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_S	DC Supply Current (Note 3)	V^+ = 15V, V_{INTOP} = 0.8V, $V_{INBOTTOM}$ = 2V V^+ = 15V, V_{INTOP} = 2V, $V_{INBOTTOM}$ = 0.8V V^+ = 15V, V_{INTOP} = 0.8V, $V_{INBOTTOM}$ = 0.8V V^+ = 15V, $V_{TSOURCE}$ = 40V, V_{INTOP} = $V_{INBOTTOM}$ = 0.8V (Note 4)		12 12 12	15 14 15 30	20 20 20 40	mA mA mA mA
I_{BOOST}	Boost Current (Note 3)	V^+ = 15V, $V_{TSOURCE}$ = 60V, V_{BOOST} = 75V, V_{INTOP} = $V_{INBOTTOM}$ = 0.8V		3	5	7	mA
V_{IL}	Input Logic Low		●		1.4	0.8	V
V_{IH}	Input Logic High		●	2	1.7		V
I_{IN}	Input Current	V_{INTOP} = $V_{INBOTTOM}$ = 4V	●		7	25	µA
V^+_{UVH}	V^+ Undervoltage Start-Up Threshold			8.4	9.2	9.75	V
V^+_{UVL}	V^+ Undervoltage Shutdown Threshold			7.8	8.3	8.9	V
V_{BUVH}	V_{BOOST} Undervoltage Start-Up Threshold	$V_{TSOURCE}$ = 60V, $V_{BOOST} - V_{TSOURCE}$		8.8	9.3	9.8	V
V_{BUVL}	V_{BOOST} Undervoltage Shutdown Threshold	$V_{TSOURCE}$ = 60V, $V_{BOOST} - V_{TSOURCE}$		8.2	8.7	9.2	V
$I_{\overline{UVOUT}}$	Undervoltage Output Leakage	V^+ = 15V	●		0.1	5	µA
$V_{\overline{UVOUT}}$	Undervoltage Output Saturation	V^+ = 7.5V, $I_{\overline{UVOUT}}$ = 2.5mA	●		0.2	0.4	V
V_{OH}	Top Gate ON Voltage	V_{INTOP} = 2V, $V_{INBOTTOM}$ = 0.8V, $V_{TGATE\ DR} - V_{TSOURCE}$	●	11	11.3	12	V
	Bottom Gate ON Voltage	V_{INTOP} = 0.8V, $V_{INBOTTOM}$ = 2V, $V_{BGATE\ DR}$	●	11	11.3	12	V
V_{OL}	Top Gate OFF Voltage	V_{INTOP} = 0.8V, $V_{INBOTTOM}$ = 2V, $V_{TGATE\ DR} - V_{TSOURCE}$	●		0.4	0.7	V
	Bottom Gate OFF Voltage	V_{INTOP} = 2V, $V_{INBOTTOM}$ = 0.8V, $V_{BGATE\ DR}$	●		0.4	0.7	V
V_{IS}	I_{SENSE} Peak Current Threshold	$V_{TSOURCE}$ = 60V, V_{BOOST} = 68V, $V^+ - V_{ISENSE}$		310	480	650	mV
V_{ISHYS}	I_{SENSE} Hysteresis	$V_{TSOURCE}$ = 60V, V_{BOOST} = 68V		25	55	85	mV
V_{SAT}	Switch Saturation Voltage	V_{ISENSE} = V^+, $V_{BOOST} - V_{TSOURCE}$ = 9V, I_{SW} = 100mA	●		0.85	1.2	V
V_{BOUT}	V_{BOOST} Regulated Output	$V_{TSOURCE}$ = 40V, V_{INTOP} = $V_{INBOTTOM}$ = 0.8V, I_{BOOST} = 10mA, $V_{BOOST} - V_{TSOURCE}$		10	10.6	11.2	V
t_r	Top Gate Rise Time	V_{INTOP} (+) Transition, $V_{INBOTTOM}$ = 0.8V, Measured at $V_{TGATE\ DR} - V_{TSOURCE}$ (Note 5)	●		130	200	ns
	Bottom Gate Rise Time	$V_{INBOTTOM}$ (+) Transition, V_{INTOP} = 0.8V, Measured at $V_{BGATE\ DR}$ (Note 5)	●		90	200	ns
t_f	Top Gate Fall Time	V_{INTOP} (–) Transition, $V_{INBOTTOM}$ = 0.8V, Measured at $V_{TGATE\ DR} - V_{TSOURCE}$ (Note 5)	●		60	140	ns
	Bottom Gate Fall Time	$V_{INBOTTOM}$ (–) Transition, V_{INTOP} = 0.8V, Measured at $V_{BGATE\ DR}$ (Note 5)	●		60	140	ns
t_{D1}	Top Gate Turn-On Delay	V_{INTOP} (+) Transition, $V_{INBOTTOM}$ = 0.8V, Measured at $V_{TGATE\ DR} - V_{TSOURCE}$ (Note 5)	●		250	500	ns
	Bottom Gate Turn-On Delay	$V_{INBOTTOM}$ (+) Transition, V_{INTOP} = 0.8V, Measured at $V_{BGATE\ DR}$ (Note 5)	●		200	400	ns
t_{D2}	Top Gate Turn-Off Delay	V_{INTOP} (–) Transition, $V_{INBOTTOM}$ = 0.8V, Measured at $V_{TGATE\ DR} - V_{TSOURCE}$ (Note 5)	●		300	600	ns
	Bottom Gate Turn-Off Delay	$V_{INBOTTOM}$ (–) Transition, V_{INTOP} = 0.8V, Measured at $V_{BGATE\ DR}$ (Note 5)	●		200	400	ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test Circuit, $V^+ = V_{BOOST}$ = 12V, $V_{TSOURCE}$ = 0V and Pins 1, 16 open. Gate Feedback pins connected to Gate Drive pins unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{D3}	Top Gate Lockout Delay	$V_{INBOTTOM}$ (+) Transition, V_{INTOP} = 2V, Measured at $V_{TGATE\ DR} - V_{TSOURCE}$ (Note 5)	●		300	600	ns
	Bottom Gate Lockout Delay	V_{INTOP} (+) Transition, $V_{INBOTTOM}$ = 2V, Measured at $V_{BGATE\ DR}$ (Note 5)	●		250	500	ns
t_{D4}	Top Gate Release Delay	$V_{INBOTTOM}$ (–) Transition, V_{INTOP} = 2V, Measured at $V_{TGATE\ DR} - V_{TSOURCE}$ (Note 5)	●		250	500	ns
	Bottom Gate Release Delay	V_{INTOP} (–) Transition, $V_{INBOTTOM}$ = 2V, Measured at $V_{BGATE\ DR}$ (Note 5)	●		200	400	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LT1336CN/LT1336IN: $T_J = T_A + (P_D)(70°C/W)$

LT1336CS/LT1336IS: $T_J = T_A + (P_D)(110°C/W)$

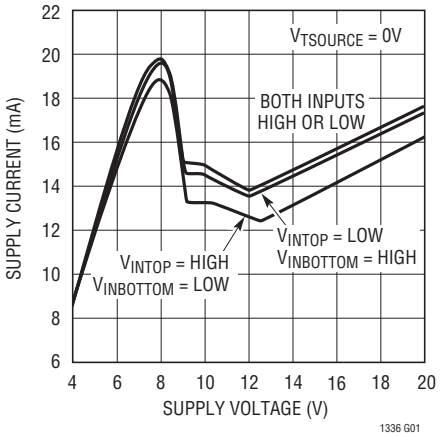
Note 3: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Typical Performance Characteristics and Applications Information sections.

Note 4: Pins 1 and 16 connected to each end of the inductor. Booster is free running.

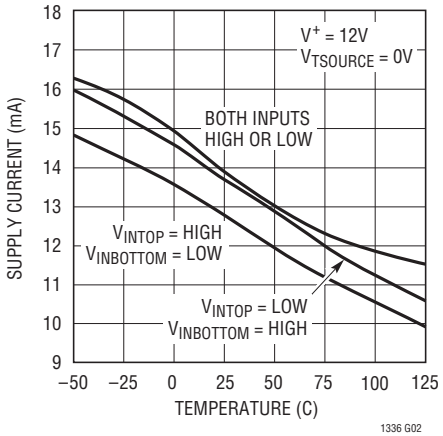
Note 5: See Timing Diagram. Gate rise times are measured from 2V to 10V and fall times are measured from 10V to 2V. Delay times are measured from the input transition to when the gate voltage has risen to 2V or decreased to 10V.

TYPICAL PERFORMANCE CHARACTERISTICS

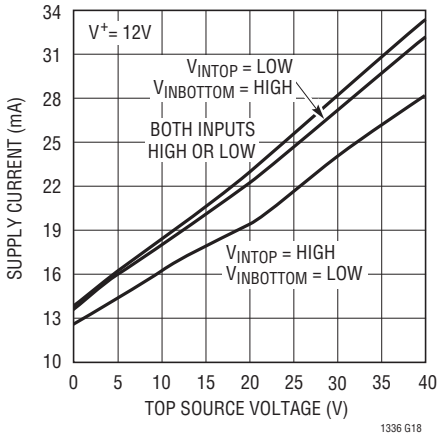
DC Supply Current vs Supply Voltage



DC Supply Current vs Temperature

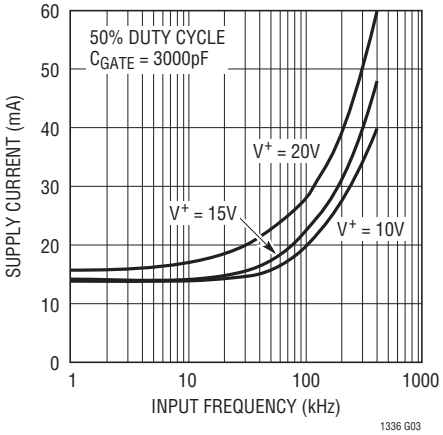


DC Supply Current vs Top Source Voltage

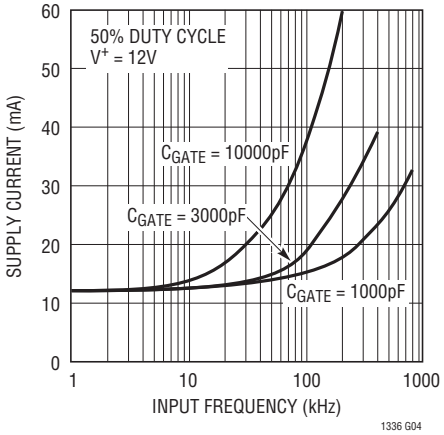


TYPICAL PERFORMANCE CHARACTERISTICS

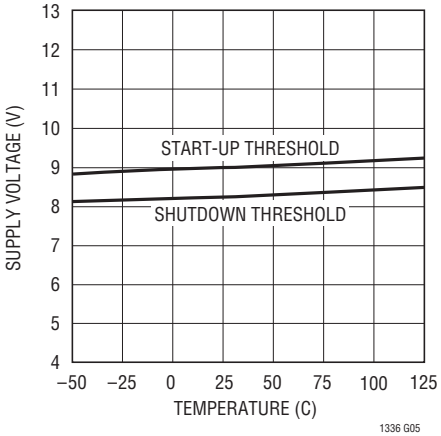
DC + Dynamic Supply Current vs Input Frequency



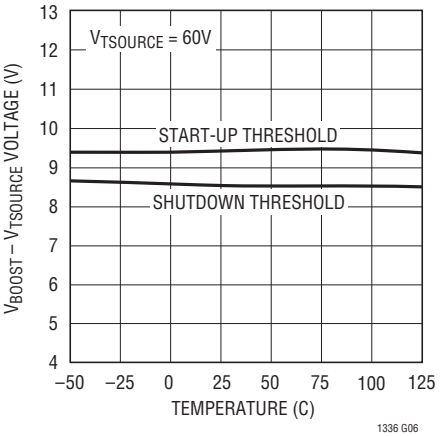
DC + Dynamic Supply Current vs Input Frequency



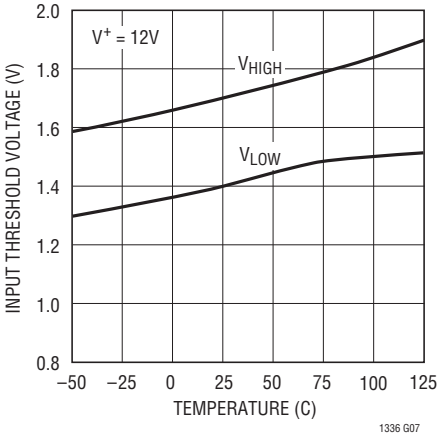
Undervoltage Lockout (V+)



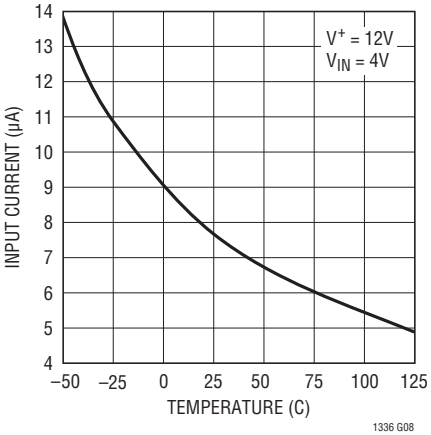
Undervoltage Lockout (V_{BOOST})



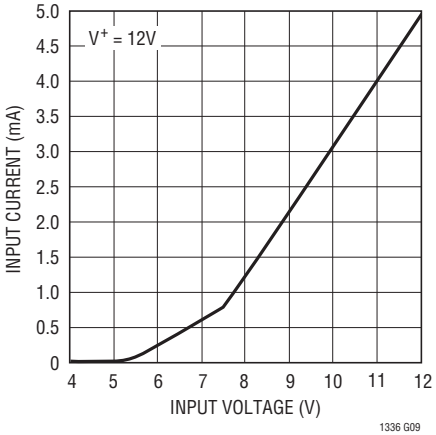
Input Threshold Voltage vs Temperature



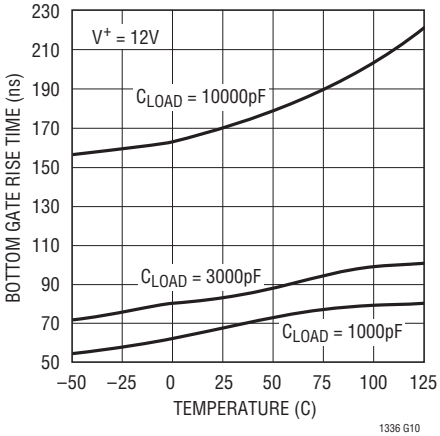
Top or Bottom Input Pin Current vs Temperature



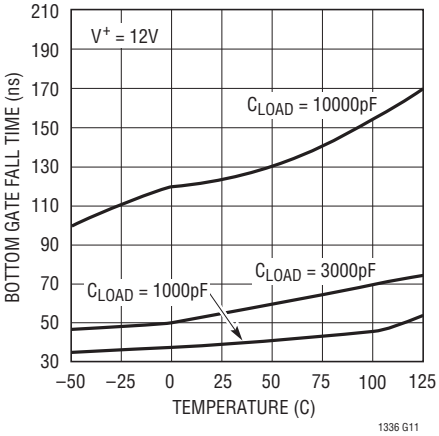
Top or Bottom Input Pin Current vs Input Voltage



Bottom Gate Rise Time vs Temperature

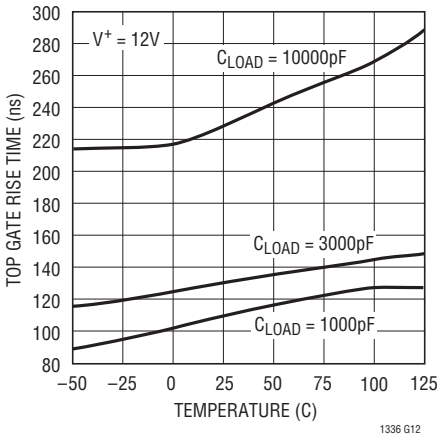


Bottom Gate Fall Time vs Temperature

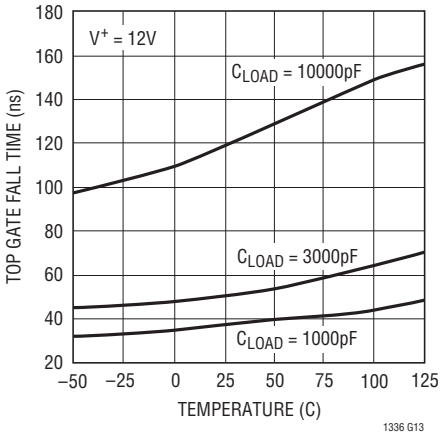


TYPICAL PERFORMANCE CHARACTERISTICS

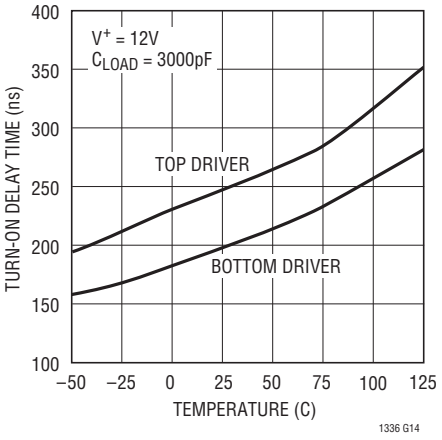
Top Gate Rise Time vs Temperature



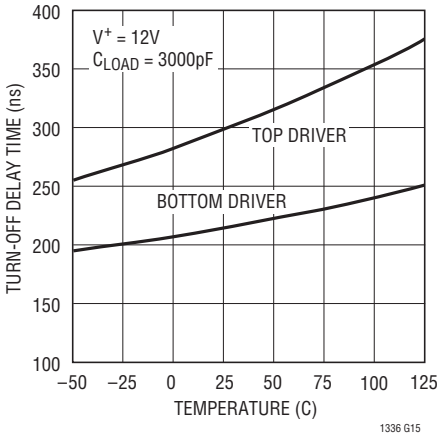
Top Gate Fall Time vs Temperature



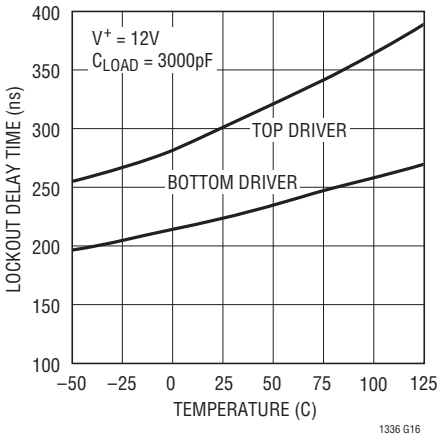
Turn-On Delay Time vs Temperature



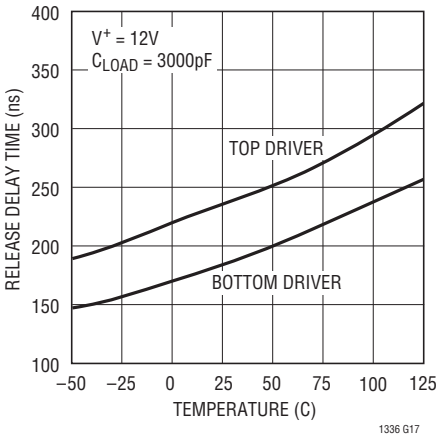
Turn-Off Delay Time vs Temperature



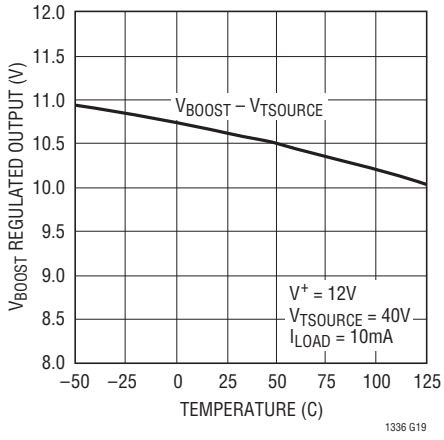
Lockout Delay Time vs Temperature



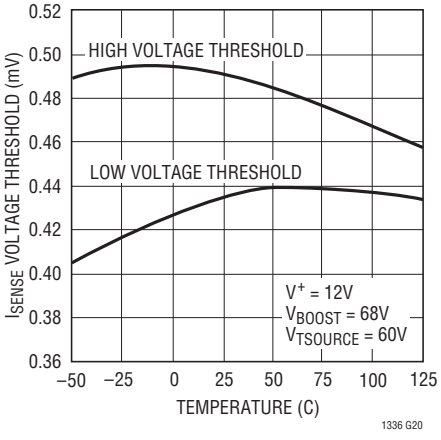
Release Delay Time vs Temperature



V_{BOOST} Regulated Output vs Temperature



I_{SENSE} Voltage Threshold vs Temperature



PIN FUNCTIONS

I_{SENSE} (Pin 1): Boost Regulator I_{SENSE} Comparator Input. An R_{SENSE} placed between Pin 1 and V^+ sets the maximum peak current. Pin 1 can be left open if the boost regulator is not used.

SV^+ (Pin 2): Main Signal Supply. Must be closely decoupled to the signal ground Pin 6.

INTOP (Pin 3): Top Driver Input. Pin 3 is disabled when Pin 4 is high. A 3k input resistor followed by a 5V internal clamp prevents saturation of the input transistors.

INBOTTOM (Pin 4): Bottom Driver Input. Pin 4 is disabled when Pin 3 is high. A 3k input resistor followed by a 5V internal clamp prevents saturation of the input transistors.

$\overline{UVOUT}$ (Pin 5): Undervoltage Output. Open collector NPN output which turns on when V^+ drops below the undervoltage threshold.

SGND (Pin 6): Small-Signal Ground. Must be routed separately from other grounds to the system ground.

PGND (Pin 7): Bottom Driver Power Ground. Connects to source of bottom N-channel MOSFET.

BGATEFB (Pin 8): Bottom Gate Feedback. Must connect directly to the bottom power MOSFET gate. The top MOSFET turn-on is inhibited until Pin 8 has discharged to below 2.5V.

BGATEDR (Pin 9): Bottom Gate Drive. The high current drive point for the bottom MOSFET. When a gate resistor is used it is inserted between Pin 9 and the gate of the MOSFET.

PV^+ (Pin 10): Bottom Driver Supply. Must be connected to the same supply as Pin 2.

TSOURCE (Pin 11): Top Driver Return. Connects to the top MOSFET source and the low side of the bootstrap capacitor.

TGATEFB (Pin 12): Top Gate Feedback. Must connect directly to the top power MOSFET gate. The bottom MOSFET turn-on is inhibited until $V_{TGATE\ FB} – V_{TSOURCE}$ has discharged to below 2.9V.

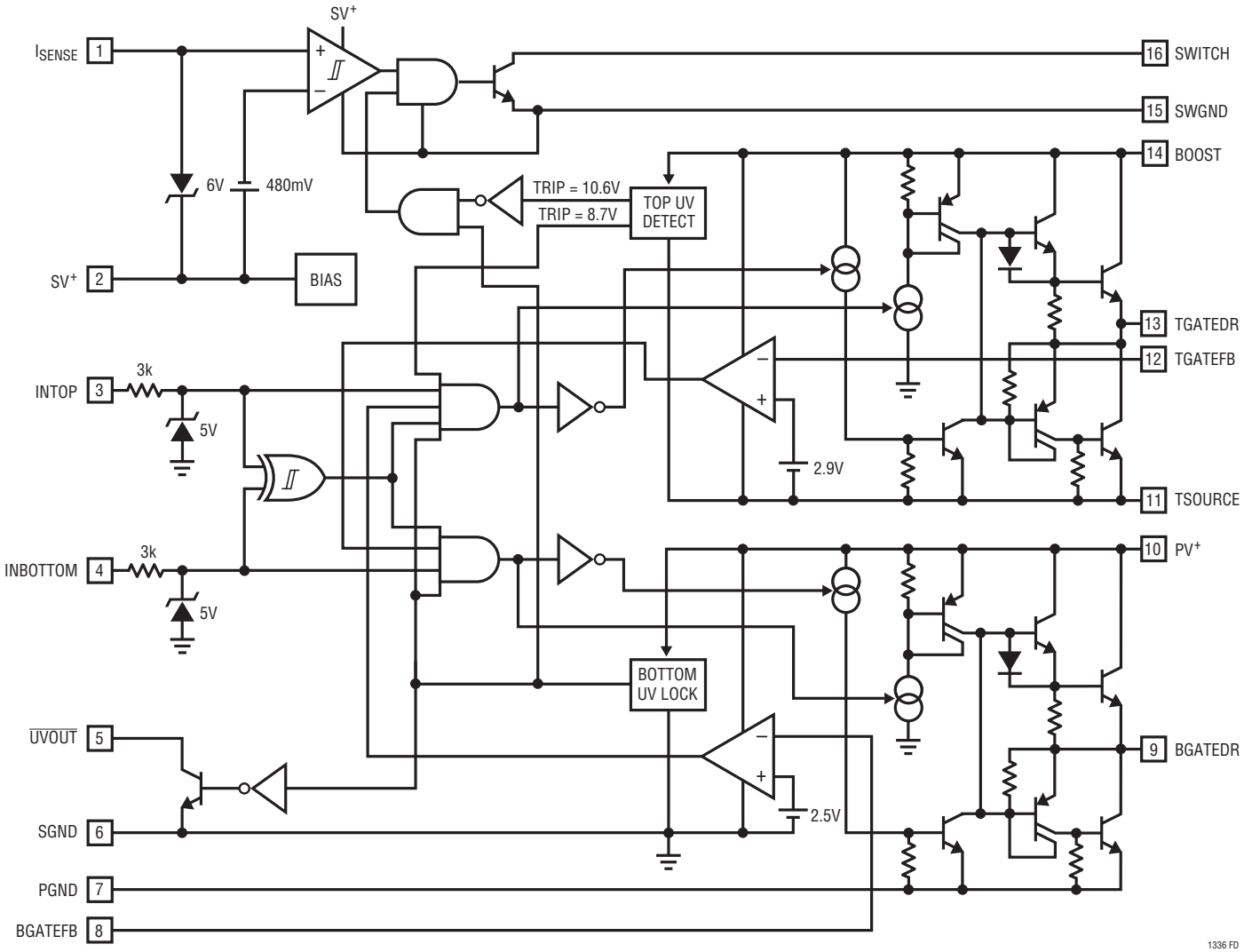
TGATEDR (Pin 13): Top Gate Drive. The high current drive point for the top MOSFET. When a gate resistor is used it is inserted between Pin 13 and the gate of the MOSFET.

BOOST (Pin 14): Top Driver Supply. Connects to the high side of the bootstrap capacitor.

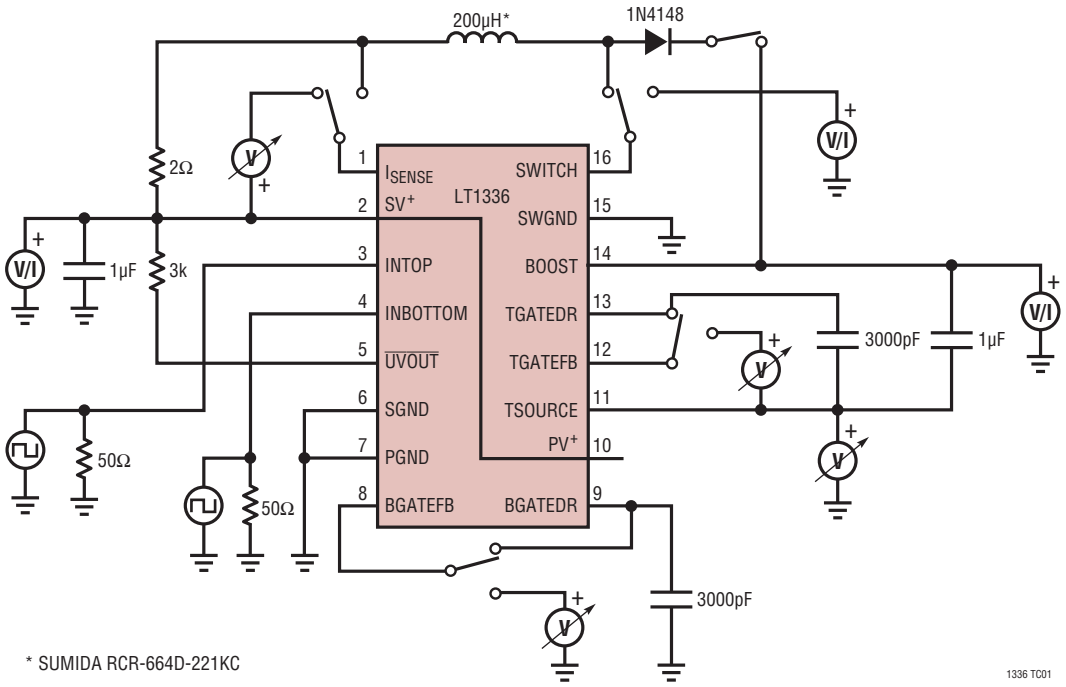
SWGND (Pin 15): Boost Regulator Ground. Must be routed separately from the other grounds to the system ground. Pin 15 can be left open if the boost regulator is not used.

SWITCH (Pin 16): Boost Regulator Switch. Connect this pin to the inductor/diode of the boost regulator network. Pin 16 can be left open if the boost regulator is not used.

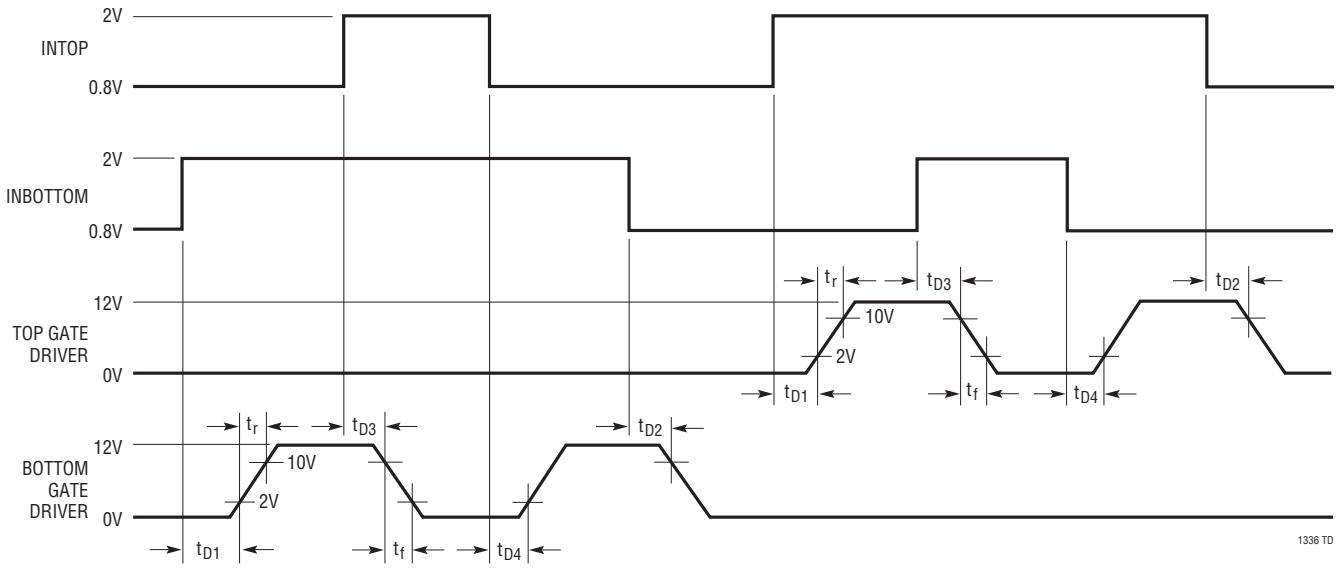
FUNCTIONAL DIAGRAM



TEST CIRCUIT



TIMING DIAGRAM



OPERATION (Refer to Functional Diagram)

The LT1336 incorporates two independent driver channels with separate inputs and outputs. The inputs are TTL/CMOS compatible; they can withstand input voltages as high as V^+. The 1.4V input threshold is regulated and has 300mV of hysteresis. Both channels are noninverting drivers. The internal logic prevents both outputs from simultaneously turning on under any input conditions. When both inputs are high both outputs are actively held low.

An internal switching regulator permits smooth transition from PWM to DC operation. In PWM operation the bootstrap capacitor is recharged each time Top Source pin goes low. As the duty cycle approaches 100% the output pulse width becomes narrower and the time available to produce an elevated upper MOSFET gate supply becomes shorter than required. As the voltage across the bootstrap capacitor drops below 10.6V, an inductor-based switching regulator kicks in and takes over the charging of the floating supply. This allows the output to smoothly transition to 100% duty cycle.

An undervoltage detection circuit disables both channels when V^+ is below the undervoltage trip point. A separate undervoltage detect block disables the high side channel when $V_{BOOST} – V_{TSOURCE}$ is below 9V.

The top and bottom gate drivers in the LT1336 each utilize two gate connections: 1) a Gate Drive pin, which provides the turn-on and turn-off currents through an optional series gate resistor, and 2) a Gate Feedback pin which connects directly to the gate to monitor the gate-to-source voltage.

Whenever there is an input transition to command the outputs to change states, the LT1336 follows a logical sequence to turn off one MOSFET and turn on the other. First, turn-off is initiated, then V_{GS} is monitored until it has decreased below the turn-off threshold, and finally the other gate is turned on.

APPLICATIONS INFORMATION

Deriving the Floating Supply

In a typical half-bridge driver like the LT1158 or the LT1160, the floating supply for the topside driver is provided by a bootstrap capacitor. This capacitor is recharged each time its negative plate goes low in PWM operation. As the duty cycle approaches 100% the output pulse width becomes narrower and the time available to recharge the bootstrap capacitor becomes shorter than required (1µs to 2µs). For instance, at 100kHz and at 95% duty cycle the output pulse width is only 0.5µs; clearly this is insufficient time to recharge the capacitor by bootstrapping. To get around this problem, the LT1336 incorporates a switching regulator to help recharge the bootstrap capacitor under such extreme conditions.

The LT1336 provides all the necessary circuitry to construct a boost or flyback switching regulator. This regulator can charge the bootstrap capacitor when it cannot recharge by bootstrapping. This happens when nearing 100% duty cycle in PWM applications. This is a worst-case condition because the bootstrap capacitor must still provide for the gate charging current of the high side MOSFETs. A diode connected between V^+ and the Boost pin is still needed to allow conventional bootstrapping of the bootstrap capacitor when duty cycles are below 90%.

The LT1336's internal switching regulator can provide enough charge to the bootstrap capacitor to allow the top driver to drive several power MOSFETs in parallel at its maximum operating frequency. The regulated voltage across $V_{BOOST} – V_{TSOURCE}$ is 10.6V; when this voltage is exceeded due to normal bootstrap action, the regulator automatically shuts down.

The switching regulator uses a hysteretic current mode control. This method of control is simple, inherently stable and provides peak inductor current limit in every cycle. It is designed to run at a nominal frequency of around 700kHz which is 7× the maximum PWM operating frequency of the LT1336. Since the hysteretic current mode control has no internal oscillator, the frequency is determined by external conditions such as supply voltage and load currents and external components such as inductor value and current sense resistor value.

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In applications where switching is always above 10kHz and the duty cycle never exceeds 90%, Pins 1, 15 and 16 can be left open. The bootstrap capacitor is then charged by conventional bootstrapping. Only a diode needs to be connected between V^+ and the Boost pin. A 0.1µF bootstrap capacitor is usually adequate using this technique for driving a single MOSFET under 10,000pF. When driving multiple MOSFETs in parallel, if the total gate capacitance exceeds 10,000pF, the bootstrap capacitor should be increased proportionally above 0.1µF (see Paralleling MOSFETs).

Deriving the Floating Supply with the Boost Topology

The advantage of using the boost topology is its simplicity. Only a resistor, a small inductor, a diode and a capacitor are needed. However, the high voltage rail may not exceed 40V to avoid reaching the collector-base breakdown voltage of the internal NPN switch.

The recommended values for the current sense resistor, inductor and bootstrap capacitor are 2Ω, 200µH and 1µF respectively. Using the recommended component values the boost regulator will run at around 700kHz. To lower the frequency the inductor value can be increased and to increase the frequency the inductor value can be decreased. The sense resistor should be at least 1.5Ω to maintain adequate inductor current limit. The bootstrap capacitor value should be 1µF or larger to minimize ripple voltage. An example of a boost regulator is shown in Figure 1.

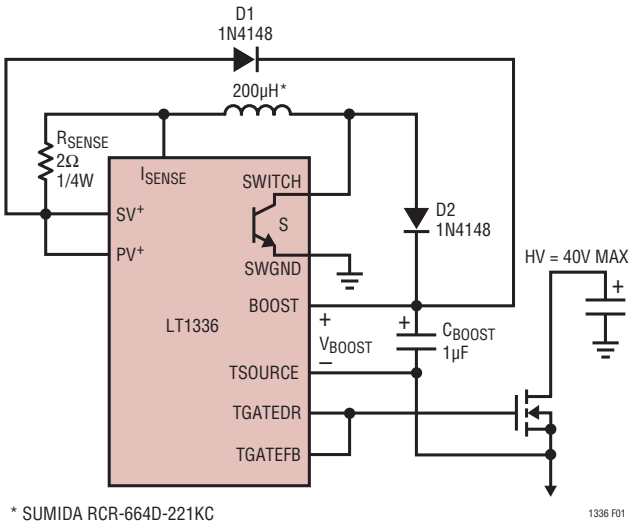


Figure 1. Using the Boost Regulator

The boost regulator works as follows: when switch S is on, the inductor current ramps up as the magnetic field builds up. During this interval energy is being stored in the inductor and no power is transferred to V_{BOOST}. When the inductor peak current is reached, sensed by the 2Ω resistor, the switch is turned off. Energy is no longer transferred to the inductor causing the magnetic field to collapse. The collapsing magnetic field induces a change in voltage across the inductor. The Switch pin voltage rises until diode D2 starts conducting. As the inductor current ramps down, the lower inductor current threshold is reached and switch S is turned off, thus completing the cycle.

Current drawn from V^+ is delivered to V_{BOOST}. Some of this current (~ 1.5mA) flows through the topside driver to the Top Source pin. This current is typically returned to ground via the bottom MOSFET or the output load. If the bottom MOSFET were off and the output load were returned to HV, then the Top Source pin will return the current to HV through the top MOSFET or the output load. If the HV supply cannot sink current and no load drawing greater than 1.5mA is connected to the supply, then a resistor from HV to ground may be needed to prevent voltage buildup on the HV supply.

Note that the current drawn from V^+ and delivered to V_{BOOST} is significantly higher than the current drawn from V_{BOOST} as given by:

$$I_{IN(V^+)} = I_{OUT}\left(\frac{V_{BOOST}}{V^+}\right)$$

Deriving the Floating Supply with the Flyback Topology

For applications where the high voltage rail is greater than 40V, the flyback topology must be used. To configure a flyback regulator, a resistor, a diode, a small 1:1 turns ratio transformer and a capacitor are needed. The maximum voltage across the switch, assuming an ideal transformer, will be about $V^+ + 11.3V$. Leakage inductance in nonideal transformers will induce an overvoltage spike at the switch at the instant when it opens. These spikes can be clamped using a snubbing network or a Zener. Unlike the boost topology, the current drawn from V^+ (assuming no loss) is equal to the current drawn from V_{BOOST}.

APPLICATIONS INFORMATION

Using the components as shown in Figure 2 the flyback regulator will run at around 800kHz. To lower the frequency C_{FILTER} can be increased and to increase the frequency C_{FILTER} can be decreased.

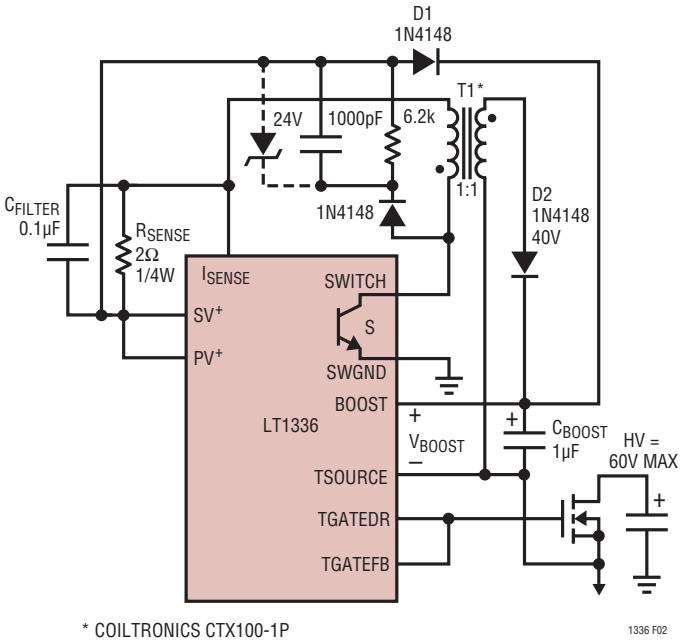


Figure 2. Using the Flyback Regulator

The flyback regulator works as follows: when switch S is on, the primary current ramps up as the magnetic field builds up. The magnetic field in the core induces a voltage on the secondary winding equal to V+. However, no power is transferred to V_{BOOST} because the rectifier diode D2 is reverse biased. The energy is stored in the transformer's magnetic field. When the primary inductor peak current is reached, the switch is turned off. Energy is no longer transferred to the transformer causing the magnetic field to collapse. The collapsing magnetic field induces a change in voltage across the transformer's windings. During this transition the Switch pin's voltage flies to 10.6V plus a diode above V+, the secondary forward biases the rectifier diode D2 and the transformer's energy is transferred to V_{BOOST}. Meanwhile the primary inductor current goes to zero and the voltage at I_{SENSE} decays to the lower inductor current threshold with a time constant of $(R_{SENSE})(C_{FILTER})$, thus completing the cycle.

Power MOSFET Selection

Since the LT1336 inherently protects the top and bottom MOSFETs from simultaneous conduction, there are no size or matching constraints. Therefore, selection can be made based on the operating voltage and $R_{DS(ON)}$ requirements. The MOSFET BV_{DSS} should be at least equal to the LT1336 absolute maximum operating voltage. For a maximum operating HV supply of 60V, the MOSFET BV_{DSS} should be from 60V to 100V.

The MOSFET $R_{DS(ON)}$ is specified at $T_J = 25°C$ and is generally chosen based on the operating efficiency required as long as the maximum MOSFET junction temperature is not exceeded. The dissipation in each MOSFET is given by:

$$P = D\left(I_{DS}\right)^2\left(1+\partial\right)R_{DS(ON)}$$

where D is the duty cycle and ∂ is the increase in $R_{DS(ON)}$ at the anticipated MOSFET junction temperature. From this equation the required $R_{DS(ON)}$ can be derived:

$$R_{DS(ON)} = \frac{P}{D\left(I_{DS}\right)^2\left(1+\partial\right)}$$

For example, if the MOSFET loss is to be limited to 2W when operating at 5A and a 90% duty cycle, the required $R_{DS(ON)}$ would be $0.089\Omega/(1 + \partial)$. $(1 + \partial)$ is given for each MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\partial = 0.007/°C$ can be used as an approximation for low voltage MOSFETs. Thus, if $T_A = 85°C$ and the available heat sinking has a thermal resistance of 20°C/W, the MOSFET junction temperature will be 125°C and $\partial = 0.007(125 – 25) = 0.7$. This means that the required $R_{DS(ON)}$ of the MOSFET will be $0.089\Omega/1.7 = 0.0523\Omega$, which can be satisfied by an IRFZ34 manufactured by International Rectifier.

Transition losses result from the power dissipated in each MOSFET during the time it is transitioning from off to on, or from on to off. These losses are proportional to $(f)(HV)^2$ and vary from insignificant to being a limiting factor on operating frequency in some high voltage applications.

APPLICATIONS INFORMATION

Paralleling MOSFETs

When the above calculations result in a lower $R_{DS(ON)}$ than is economically feasible with a single MOSFET, two or more MOSFETs can be paralleled. The MOSFETs will inherently share the currents according to their $R_{DS(ON)}$ ratio as long as they are thermally connected (e.g., on a common heat sink). The LT1336 top and bottom drivers can each drive five power MOSFETs in parallel with only a small loss in switching speeds (see Typical Performance Characteristics). A low value resistor (10Ω to 47Ω) in series with each individual MOSFET gate may be required to "decouple" each MOSFET from its neighbors to prevent high frequency oscillations (consult manufacturer's recommendations). If gate decoupling resistors are used, the corresponding Gate Feedback pin can be connected to any one of the gates as shown in Figure 3.

Driving multiple MOSFETs in parallel may restrict the operating frequency to prevent overdissipation in the LT1336 (see the following Gate Charge and Driver Dissipation).

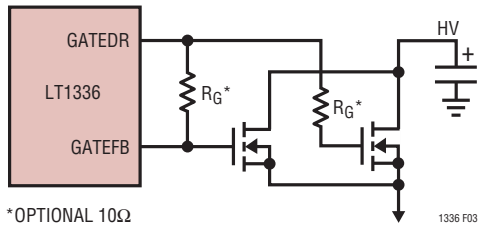


Figure 3. Paralleling MOSFETs

Gate Charge and Driver Dissipation

A useful indicator of the load presented to the driver by a power MOSFET is the total gate charge Q_G, which includes the additional charge required by the gate-to-drain swing. Q_G is usually specified for V_{GS} = 10V and V_{DS} = $0.8V_{DS(MAX)}$. When the supply current is measured in a switching application, it will be larger than given by the DC electrical characteristics because of the additional supply current associated with sourcing the MOSFET gate charge:

$$I_{SUPPLY} = I_{DC} + \left(\frac{dQ_G}{dt}\right)_{TOP} + \left(\frac{dQ_G}{dt}\right)_{BOTTOM}$$

The actual increase in supply current is slightly higher due to LT1336 switching losses and the fact that the gates are being charged to more than 10V. Supply Current vs Switching Frequency is given in the Typical Performance Characteristics.

The LT1336 junction temperature can be estimated by using the equations given in Note 1 of the Electrical Characteristics. For example, the LT1336IS is limited to less than 31mA from a 12V supply:

T_J = 85°C + (31mA)(12V)(110°C/W)
= 126°C exceeds absolute maximum

In order to prevent the maximum junction temperature from being exceeded, the LT1336 supply current must be verified while driving the full complement of the chosen MOSFET type at the maximum switching frequency.

Ugly Transient Issues

In PWM applications the drain current of the top MOSFET is a square wave at the input frequency and duty cycle. To prevent large voltage transients at the top drain, a low ESR electrolytic capacitor must be used and returned to the power ground. The capacitor is generally in the range of 25µF to 5000µF and must be physically sized for the RMS current flowing in the drain to prevent heating and premature failure. In addition, the LT1336 requires a separate 10µF capacitor connected closely between Pins 2 and 6.

The LT1336 top source is internally protected against transients below ground and above supply. However, the Gate Drive pins cannot be forced below ground. In most applications, negative transients coupled from the source to the gate of the top MOSFET do not cause any problems.

Switching Regulator Applications

The LT1336 is ideal as a synchronous switch driver to improve the efficiency of step-down (buck) switching regulators. Most step-down regulators use a high current Schottky diode to conduct the inductor current when the switch is off. The fractions of the oscillator period that the switch is on (switch conducting) and off (diode conducting) are given by:

APPLICATIONS INFORMATION

$$\text{Switch On} = \left(\frac{V_{OUT}}{HV}\right)(\text{Total Period})$$

$$\text{Switch Off} = \left(\frac{HV - V_{OUT}}{HV}\right)(\text{Total Period})$$

Note that for HV > $2V_{OUT}$, the switch is off longer than it is on, making the diode losses more significant than the switch. The worst case for the diode is during a short circuit, when V_{OUT} approaches zero and the diode conducts the short-circuit current almost continuously.

Figure 4 shows the LT1336 used to synchronously drive a pair of power MOSFETs in a step-down regulator application, where the top MOSFET is the switch and the bottom MOSFET replaces the Schottky diode. Since both conduction paths have low losses, this approach can result in very high efficiency (90% to 95%) in most applications. For regulators under 10A, using low $R_{DS(ON)}$ N-channel MOSFETs eliminates the need for heat sinks. R_{GS} holds the top MOSFET off when HV is applied before the 12V supply.

One fundamental difference in the operation of a step-down regulator with synchronous switching is that it never becomes discontinuous at light loads. The inductor current doesn't stop ramping down when it reaches zero, but actually reverses polarity, resulting in a constant ripple current independent of load. This does not cause a significant efficiency loss (as might be expected) since the negative inductor current is returned to HV when the switch turns back on. However, I^2R losses will occur under these conditions due to the recirculating currents.

The LT1336 performs the synchronous MOSFET drive in a step-down switching regulator. A reference and PWM are required to complete the regulator. Any voltage mode or current mode PWM controller may be used but the LT3526 is particularly well-suited to high power, high efficiency applications such as the 10A circuit shown in Figure 6. In higher current regulators a small Schottky diode across the bottom MOSFET helps to reduce reverse- recovery switching losses.

Motor Drive Applications

In applications where rotation is always in the same direction, a single LT1336 controlling a half-bridge can be used to drive a DC motor. One end of the motor may be connected either to supply or to ground. A motor in this configuration is controlled by its inputs which give three alternatives: run, free running stop (coasting) and fast stop ("plugging" braking with the motor shorted by one of the MOSFETs).

Whenever possible, returning one end of the motor to ground is preferable. When the motor is returned to supply and the boost topology is used to charge the bootstrap capacitor, the return current from the top driver will find its way to the high voltage rail through the top MOSFET. Since most power supplies cannot sink current, this

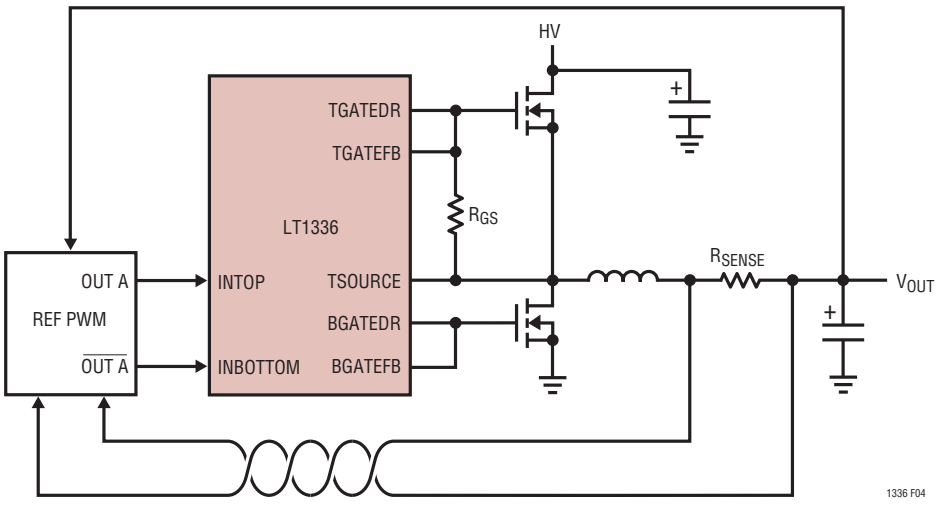


Figure 4. Adding Synchronous Switching to a Step-Down Switching Regulator

APPLICATIONS INFORMATION

current can raise the voltage of the high voltage rail. This can be avoided by placing a discharge resistor between HV supply and ground to divert the return current to ground as shown in Figure 5. For a high voltage rail of 40V, a 26k resistor or smaller should be used, since the top driver will return about 1.5mA.

For applications where using a discharge resistor is undesirable, use the flyback regulator topology instead of the boost regulator topology (see Deriving the Floating Supply with the Flyback Topology).

To drive a DC motor in both directions, two LT1336s can be used to drive an H-bridge output stage. In this configuration the motor can be made to run clockwise, counterclockwise, stop rapidly ("plugging" braking) or free run (coast) to a stop. A very rapid stop may be achieved by reversing the current, though this requires more careful design to stop the motor dead. In practice a closed-loop control system with tachometric feedback is usually necessary.

The motor speed in these examples can be controlled by switching the drivers with pulse width modulated square waves. This approach is particularly suitable for microcomputers/DSP control loops.

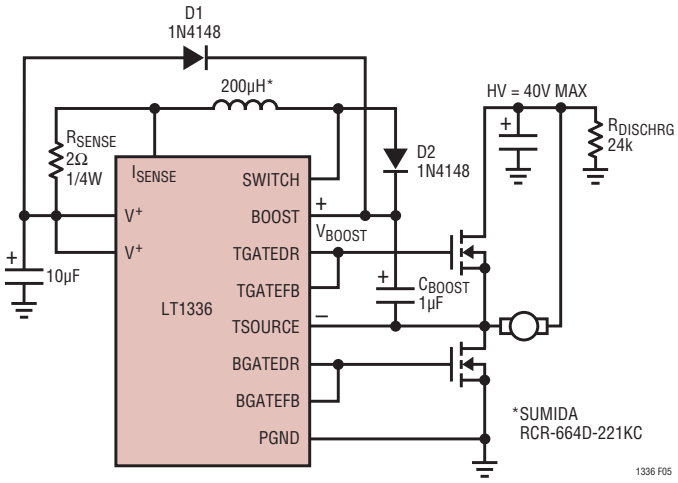
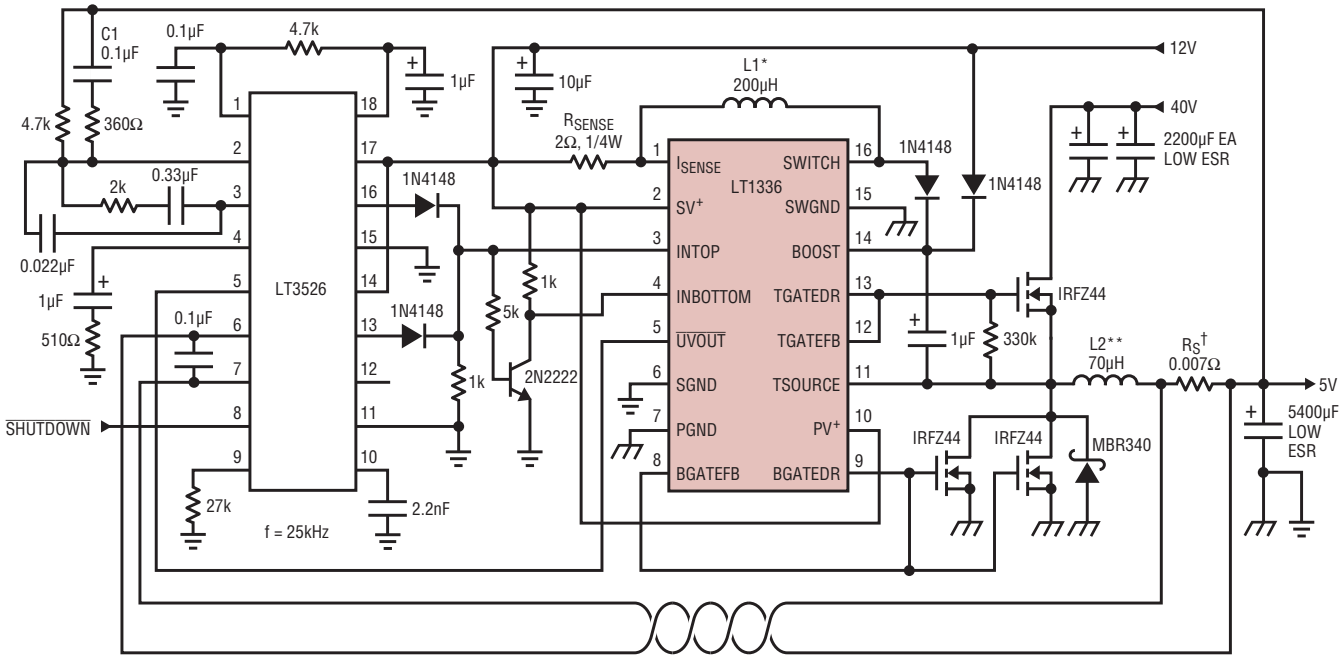


Figure 5. Driving a Supply Referenced Motor

TYPICAL APPLICATIONS



* SUMIDA RCR-664D-221KC
** MAGNETICS CORE #55585-A2 30 TURNS 14GA MAGNET WIRE
† DALE TYPE LVR-3 ULTRONIX RCS01

1336 F06

Figure 6. 90% Efficiency, 40V to 5V, 10A, Low Dropout Voltage Mode Switching Regulator

TYPICAL APPLICATIONS

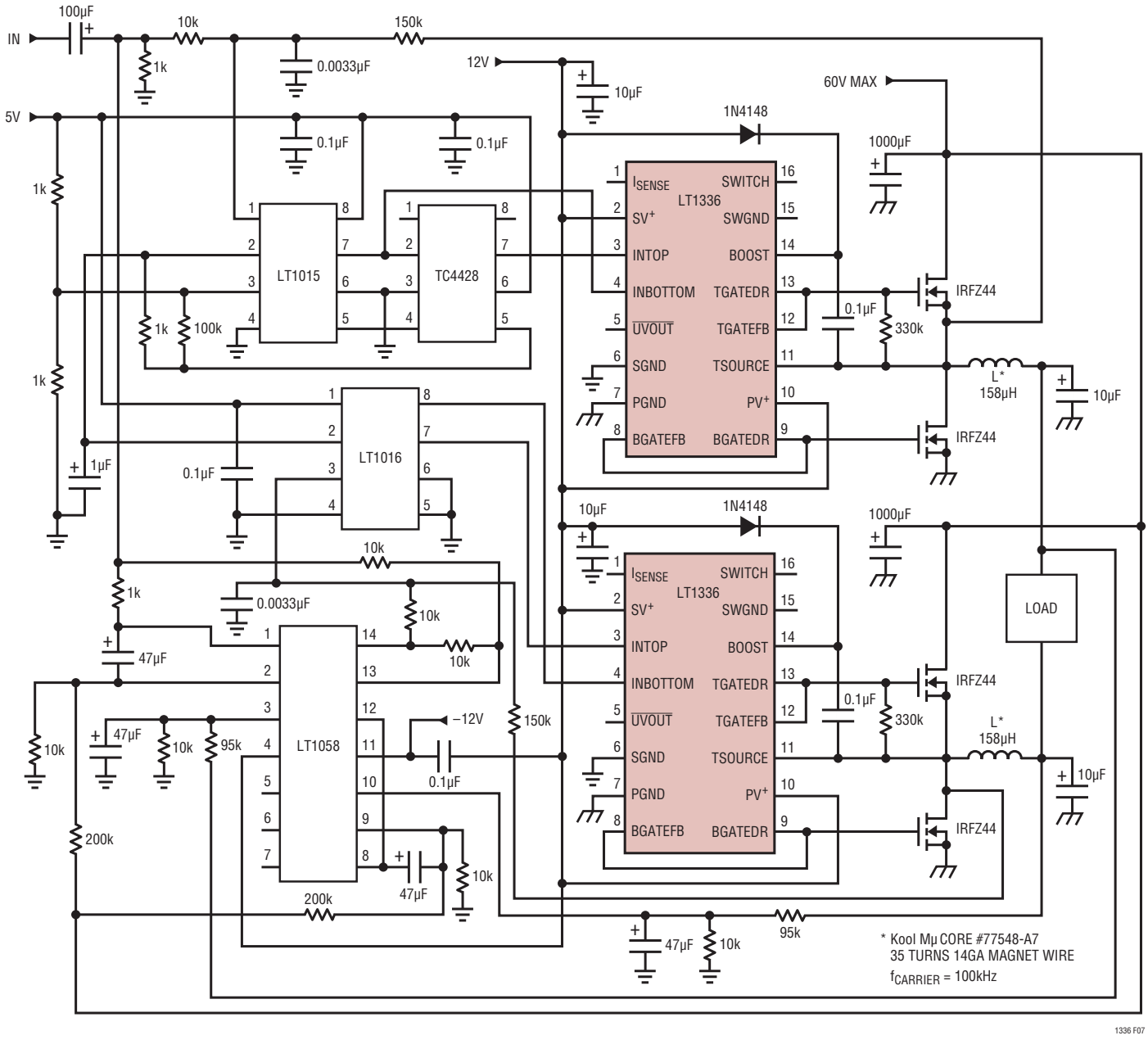
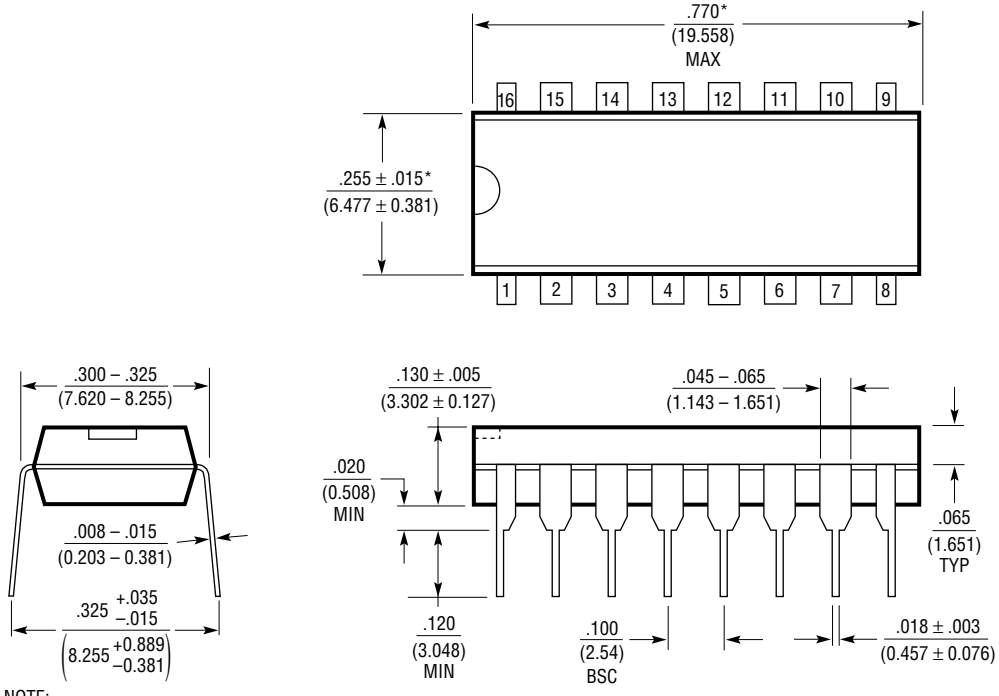


Figure 7. 200W Class D, 10Hz to 1kHz Amplifier

PACKAGE DESCRIPTION

N Package
16-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)

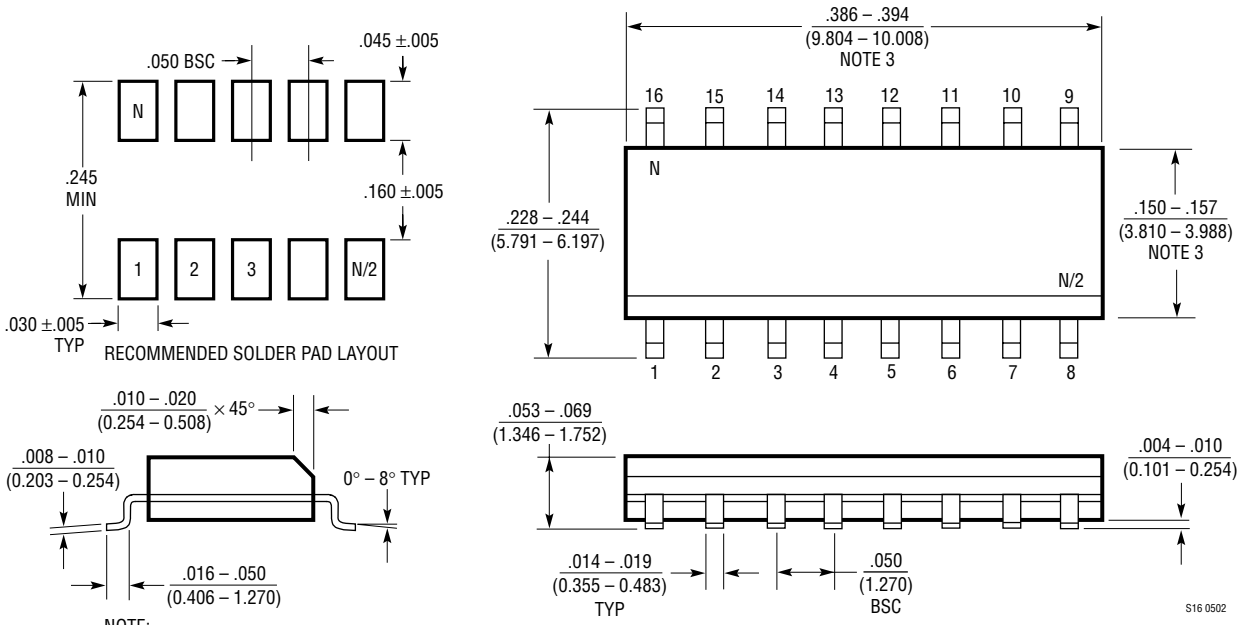


NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

S Package
16-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/10	Change to Undervoltage Start-Up Threshold and Undervoltage Shutdown Threshold max limits in Electrical Characteristics section.	3
		Updated Notes in Electrical Characteristics section.	4
		Updated Related Parts.	20