Dual and Quad 12MHz, 400V/µs Op Amps

FEATURES

- **12MHz Gain Bandwidth**
- **400V/µs Slew Rate**
- **1.25mA Maximum Supply Current per Amplifier**
- Unity-Gain Stable
- C-Load™ Op Amp Drives All Capacitive Loads
- 10nV/√Hz Input Noise Voltage
- 800µV Maximum Input Offset Voltage
- 300nA Maximum Input Bias Current
- 70nA Maximum Input Offset Current
- 12V/mV Minimum DC Gain, R_L = 1k
- 230ns Settling Time to 0.1%, 10V Step
- 280ns Settling Time to 0.01%, 10V Step
- ±12V Minimum Output Swing into 500Ω
- ±2.75V Minimum Output Swing into 150Ω
- Specified at ±2.5V, ±5V, and ±15V

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Data Acquisition Systems
- Photodiode Amplifiers

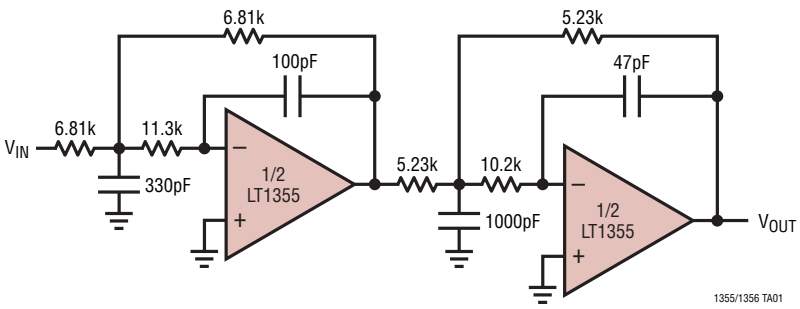
DESCRIPTION

The LT®1355/LT1356 are dual and quad low power high speed operational amplifiers with outstanding AC and DC performance. The amplifiers feature much lower supply current and higher slew rate than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with matched high impedance inputs and the slewing performance of a current feedback amplifier. The high slew rate and single stage design provide excellent settling characteristics which make the circuit an ideal choice for data acquisition systems. Each output drives a 500Ω load to ±12V with ±15V supplies and a 150Ω load to ±2.75V on ±5V supplies. The amplifiers are stable with any capacitive load making them useful in buffer applications.

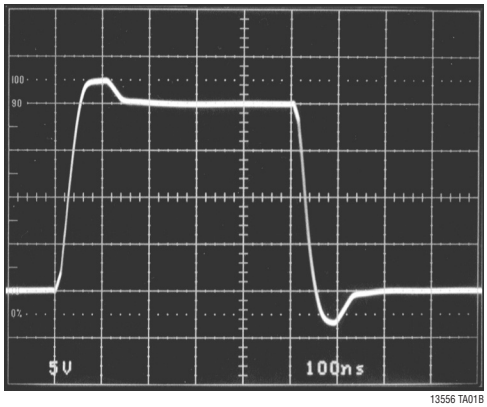
The LT1355/LT1356 are members of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For a single amplifier version of the LT1355/LT1356 see the LT1354 data sheet. For higher bandwidth devices with higher supply currents see the LT1357 through LT1365 data sheets. Bandwidths of 25MHz, 50MHz, and 70MHz are available with 2mA, 4mA, and 6mA of supply current per amplifier. Singles, duals, and quads of each amplifier are available.

TYPICAL APPLICATION

100kHz, 4th Order Butterworth Filter



A_V = –1 Large-Signal Response



13556 TA01B

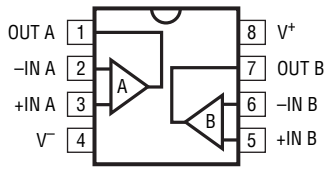
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage (Transient Only)
(Note 2) ..... ±10V
Input Voltage ..... $\pm V_S$
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 7)
LT1355C/LT1356C/LT1356I ..... –40°C to 85°C
LT1356H (T_C) ..... –40°C to 125°C
Specified Temperature Range (Note 8)
LT1355C/LT1356C ..... 0°C to 70°C
LT1356I ..... –40°C to 85°C
LT1356H (T_C) ..... –40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION

LT1355

TOP VIEW

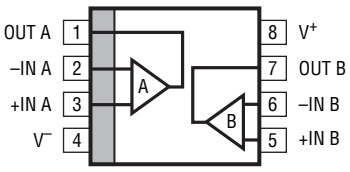


N8 PACKAGE
8-LEAD PDIP

T_{JMAX} = 150°C, θ_{JA} = 130°C/W

LT1355

TOP VIEW

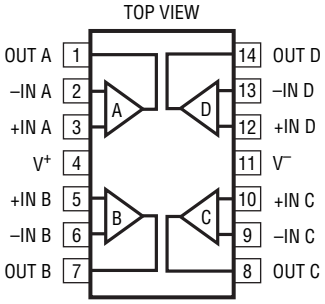


S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 190°C/W

LT1356

TOP VIEW

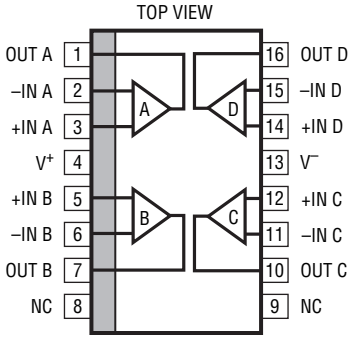


N PACKAGE
14-LEAD PDIP

T_{JMAX} = 150°C, θ_{JA} = 110°C/W

LT1356

TOP VIEW



S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 150°C/W, θ_{JC} = 30°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1355CN8#PBF	LT1355CN8#TRPBF	LT1355CN8	8-Lead PDIP	0°C to 70°C
LT1355CS8#PBF	LT1355CS8#TRPBF	1355	8-Lead Plastic SO	0°C to 70°C
LT1356CN#PBF	LT1356CN#TRPBF	LT1356CN	14-Lead PDIP	0°C to 70°C
LT1356CS#PBF	LT1356CS#TRPBF	LT1356CS	16-Lead Plastic SO	0°C to 70°C
LT1356IS#PBF	LT1356IS#TRPBF	LT1356S	16-Lead Plastic SO	–40°C to 85°C
LT1356HS#PBF	LT1356HS#TRPBF	LT1356S	16-Lead Plastic SO	–40°C < T_C < 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V ±5V ±2.5V		0.3 0.3 0.4	0.8 0.8 1.0	mV mV mV
I_{OS}	Input Offset Current		±2.5V to ±15V		20	70	nA
I_B	Input Bias Current		±2.5V to ±15V		80	300	nA
e_n	Input Noise Voltage	f = 10kHz	±2.5V to ±15V		10		nV/√Hz
i_n	Input Noise Current	f = 10kHz	±2.5V to ±15V		0.6		pA/√Hz
R_{IN}	Input Resistance	V_{CM} = ±12V	±15V	70	160		MΩ
	Input Resistance	Differential	±15V		11		MΩ
C_{IN}	Input Capacitance		±15V		3		pF
	Input Voltage Range$^+$		±15V ±5V ±2.5V	12.0 2.5 0.5	13.4 3.5 1.1		V V V
	Input Voltage Range$^-$		±15V ±5V ±2.5V		–13.2 –3.4 –0.9	–12.0 –2.5 –0.5	V V V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12V V_{CM} = ±2.5V V_{CM} = ±0.5V	±15V ±5V ±2.5V	83 78 68	97 84 75		dB dB dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		92	106		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 1k V_{OUT} = ±10V, R_L = 500Ω V_{OUT} = ±2.5V, R_L = 1k V_{OUT} = ±2.5V, R_L = 500Ω V_{OUT} = ±2.5V, R_L = 150Ω V_{OUT} = ±1V, R_L = 500Ω	±15V ±15V ±5V ±5V ±5V ±2.5V	12 5 12 5 1 5	36 15 36 15 4 20		V/mV V/mV V/mV V/mV V/mV V/mV
V_{OUT}	Output Swing	R_L = 1k, V_{IN} = ±40mV R_L = 500Ω, V_{IN} = ±40mV R_L = 500Ω, V_{IN} = ±40mV R_L = 150Ω, V_{IN} = ±40mV R_L = 500Ω, V_{IN} = ±40mV	±15V ±15V ±5V ±5V ±2.5V	13.3 12.0 3.5 2.75 1.3	13.8 13.0 4.0 3.3 1.7		±V ±V ±V ±V ±V
I_{OUT}	Output Current	V_{OUT} = ±12.0V V_{OUT} = ±2.75V	±15V ±5V	24.0 18.3	30 25		mA mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±3V	±15V	30	42		mA
SR	Slew Rate	A_V = –2 (Note 4)	±15V ±5V	200 70	400 120		V/µs V/µs
	Full-Power Bandwidth	10V Peak (Note 5) 3V Peak (Note 5)	±15V ±5V		6.4 6.4		MHz MHz
GBW	Gain Bandwidth	f = 200kHz, R_L = 2k	±15V ±5V ±2.5V	9.0 7.5	12.0 10.5 9.0		MHz MHz MHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10% to 90%, 0.1V	±15V ±5V		14 17		ns ns
	Overshoot	A_V = 1, 0.1V	±15V ±5V		20 18		% %
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V	±15V ±5V		16 19		ns ns
t_s	Settling Time	10V Step, 0.1%, A_V = –1 10V Step, 0.01%, A_V = –1 5V Step, 0.1%, A_V = –1 5V Step, 0.01%, A_V = –1	±15V ±15V ±5V ±5V		230 280 240 380		ns ns ns ns

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
	Differential Gain	f = 3.58MHz, A_V = 2, R_L = 1k	±15V ±5V		2.2 2.1		% %
	Differential Phase	f = 3.58MHz, A_V = 2, R_L = 1k	±15V ±5V		3.1 3.1		Deg Deg
R_O	Output Resistance	A_V = 1, f = 100kHz	±15V		0.7		Ω
	Channel Separation	V_{OUT} = ±10V, R_L = 500Ω	±15V	100	113		dB
I_S	Supply Current	Each Amplifier Each Amplifier	±15V ±5V		1.0 0.9	1.25 1.20	mA mA

The ● denotes the specifications which apply over the temperature range 0°C ≤ T_A ≤ 70°C, V_{CM} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V ±5V ±2.5V	● ● ●			1.0 1.0 1.2	mV mV mV
	Input V_{OS} Drift	(Note 6)	±2.5V to ±15V	●		5	8	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			100	nA
I_B	Input Bias Current		±2.5V to ±15V	●			450	nA
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12V V_{CM} = ±2.5V V_{CM} = ±0.5V	±15V ±5V ±2.5V	● ● ●	81 77 67			dB dB dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		●	90			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 1k V_{OUT} = ±10V, R_L = 500Ω V_{OUT} = ±2.5V, R_L = 1k V_{OUT} = ±2.5V, R_L = 500Ω V_{OUT} = ±2.5V, R_L = 150Ω V_{OUT} = ±1V, R_L = 500Ω	±15V ±15V ±5V ±5V ±5V ±2.5V	● ● ● ● ● ●	10.0 3.3 10.0 3.3 0.6 3.3			V/mV V/mV V/mV V/mV V/mV V/mV
V_{OUT}	Output Swing	R_L = 1k, V_{IN} = ±40mV R_L = 500Ω, V_{IN} = ±40mV R_L = 500Ω, V_{IN} = ±40mV R_L = 150Ω, V_{IN} = ±40mV R_L = 500Ω, V_{IN} = ±40mV	±15V ±15V ±5V ±5V ±2.5V	● ● ● ● ●	13.2 11.5 3.4 2.5 1.2			±V ±V ±V ±V ±V
I_{OUT}	Output Current	V_{OUT} = ±11.5V V_{OUT} = ±2.5V	±15V ±5V	● ●	23.0 16.7			mA mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±3V	±15V	●	24			mA
SR	Slew Rate	A_V = –2, (Note 4)	±15V ±5V	● ●	150 60			V/µs V/µs
GBW	Gain Bandwidth	f = 200kHz, R_L = 2k	±15V ±5V	● ●	7.5 6.0			MHz MHz
	Channel Separation	V_{OUT} = ±10V, R_L = 500Ω	±15V	●	98			dB
I_S	Supply Current	Each Amplifier Each Amplifier	±15V ±5V	● ●			1.45 1.40	mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C ≤ T_A ≤ 85°C and –40°C ≤ T_C ≤ 125°C temperature ranges, V_{CM} = 0V unless otherwise noted. (Note 8)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V ±5V ±2.5V	● ● ●			1.8 1.8 2.0	mV mV mV
I_{OS}	Input Offset Current		±2.5V to ±15V	●			250	nA
I_B	Input Bias Current		±2.5V to ±15V	●			600	nA
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12V V_{CM} = ±2.5V V_{CM} = ±0.5V	±15V ±5V ±2.5V	● ● ●	80 76 66			dB dB dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		●	90			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 1k V_{OUT} = ±2.5V, R_L = 1k V_{OUT} = ±2.5V, R_L = 500Ω V_{OUT} = ±1V, R_L = 500Ω	±15V ±5V ±5V ±2.5V	● ● ● ●	6.0 4.0 1.7 1.7			V/mV V/mV V/mV V/mV
V_{OUT}	Output Swing	R_L = 1k, V_{IN} = ±40mV R_L = 500Ω, V_{IN} = ±40mV R_L = 500Ω, V_{IN} = ±40mV	±15V ±5V ±2.5V	● ● ●	12.7 3.3 1.2			±V ±V ±V
I_{OUT}	Output Current	V_{OUT} = ±12.7V V_{OUT} = ±3.3V	±15V ±5V	● ●	12.7 6.6			mA mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±3V	±15V	●	16			mA
SR	Slew Rate	A_V = –2, (Note 4)	±15V ±5V	● ●	110 43			V/µs V/µs
GBW	Gain Bandwidth	f = 200kHz, R_L = 2k	±15V ±5V	● ●	6.0 4.6			MHz MHz
	Channel Separation	V_{OUT} = ±10V, R_L = 500Ω	±15V	●	96			dB
I_S	Supply Current	Each Amplifier Each Amplifier	±15V ±5V	● ●			1.55 1.50	mA mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Differential inputs of ±10V are appropriate for transient operation only, such as during slewing. Large, sustained differential inputs will cause excessive power dissipation and may damage the part. See Input Considerations in the Applications Information section of this data sheet for more details.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: Slew rate is measured between ±10V on the output with ±6V input for ±15V supplies and ±1V on the output with ±1.75V input for ±5V supplies.

Note 5: Full power bandwidth is calculated from the slew rate measurement: FPBW = (SR)/2πV_P.

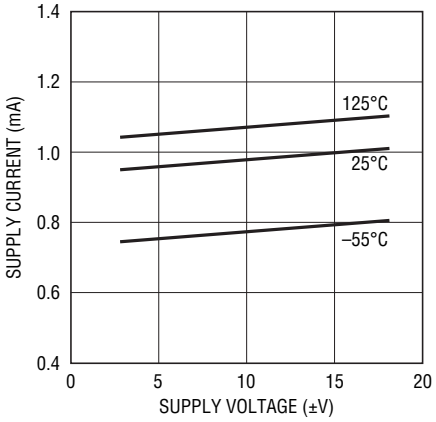
Note 6: This parameter is not 100% tested.

Note 7: The LT1355C/LT1356C/LT1356I are guaranteed functional over the operating temperature range of –40°C to 85°C. The LT1356H is guaranteed functional over the operating temperature range of –40°C to 125°C case temperature (T_C).

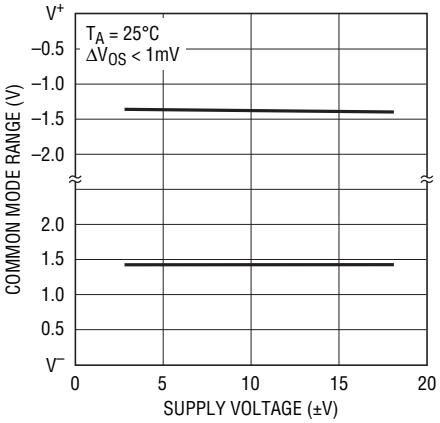
Note 8: The LT1355C/LT1356C are guaranteed to meet specified performance from 0°C to 70°C. The LT1355C/LT1356C are designed, characterized and expected to meet specified performance from –40°C to 85°C, but are not tested or QA sampled at these temperatures. The LT1356I is guaranteed to meet specified performance from –40°C to 85°C. The LT1356H is guaranteed to meet specified performance from –40°C to 125°C case temperature (T_C). The parts are pulse tested at these temperatures. Internal warm-up drift must be taken into account separately. Care must be taken not to exceed the maximum junction temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

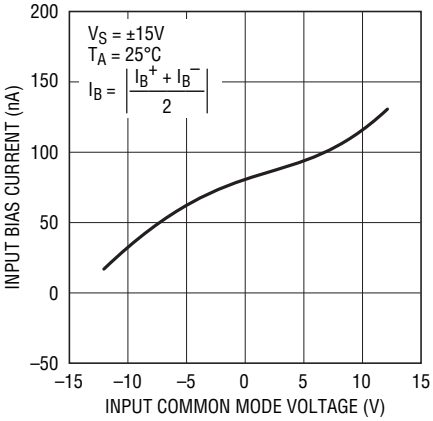
Supply Current vs Supply Voltage and Temperature



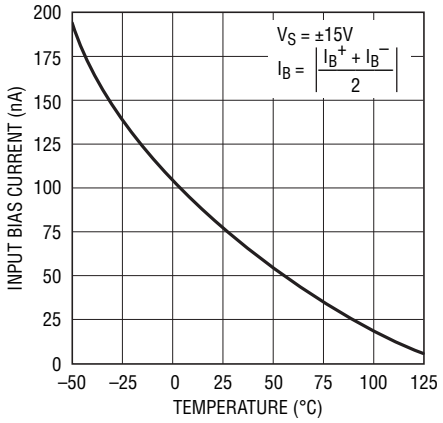
Input Common Mode Range vs Supply Voltage



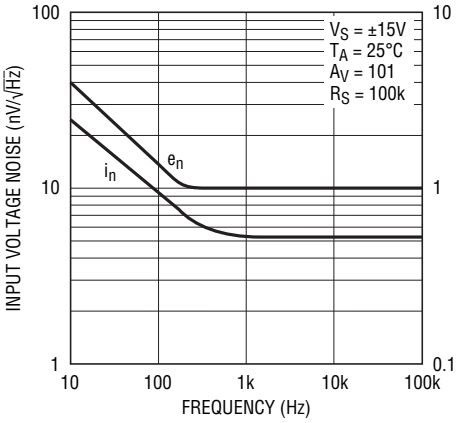
Input Bias Current vs Input Common Mode Voltage



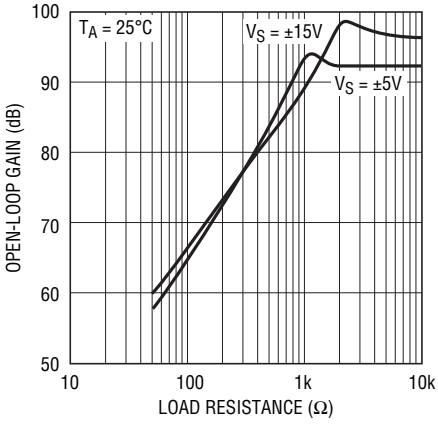
Input Bias Current vs Temperature



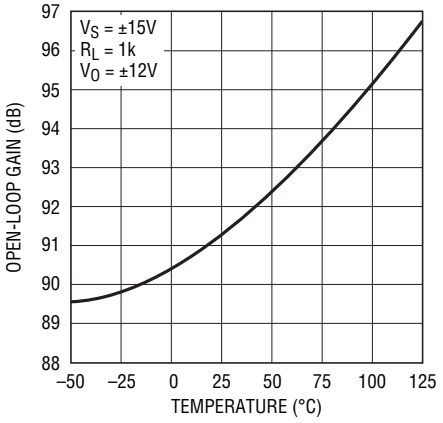
Input Noise Spectral Density



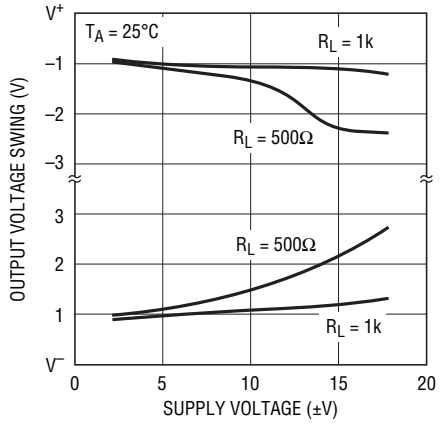
Open-Loop Gain vs Resistive Load



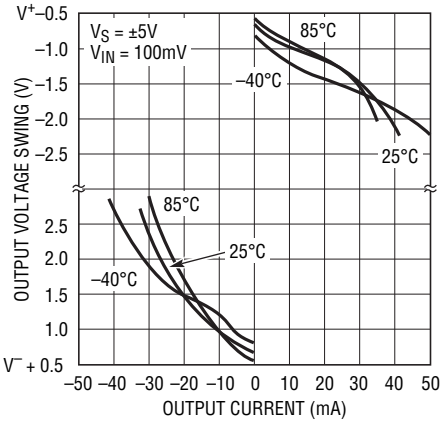
Open-Loop Gain vs Temperature



Output Voltage Swing vs Supply Voltage

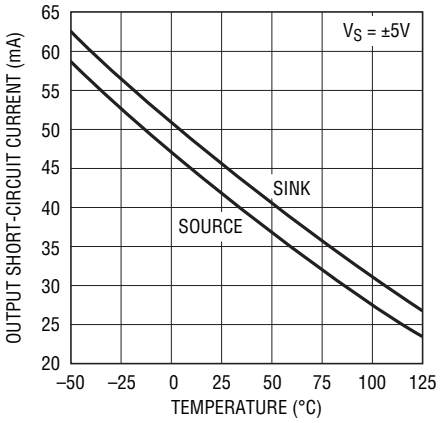


Output Voltage Swing vs Load Current



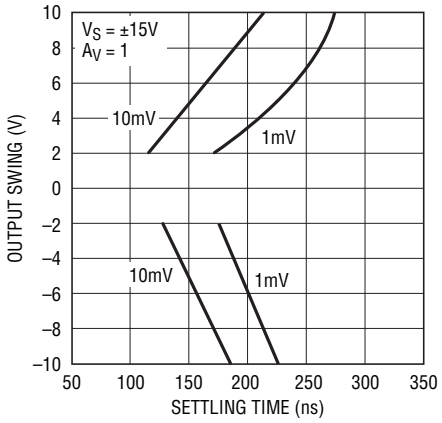
TYPICAL PERFORMANCE CHARACTERISTICS

Output Short-Circuit Current vs Temperature



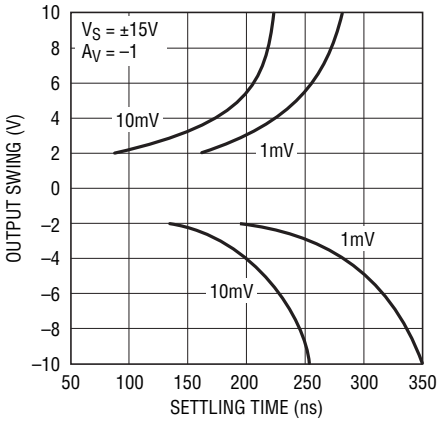
1355/1356 G10

Settling Time vs Output Step (Noninverting)



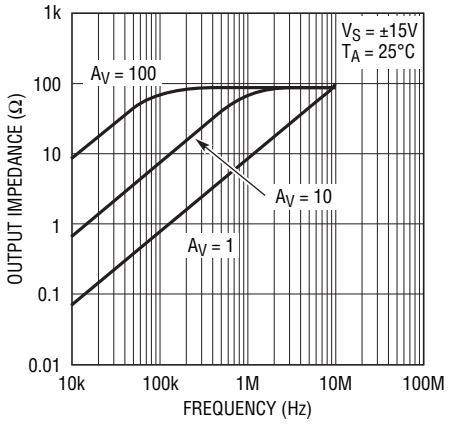
1355/1356 G11

Settling Time vs Output Step (Inverting)



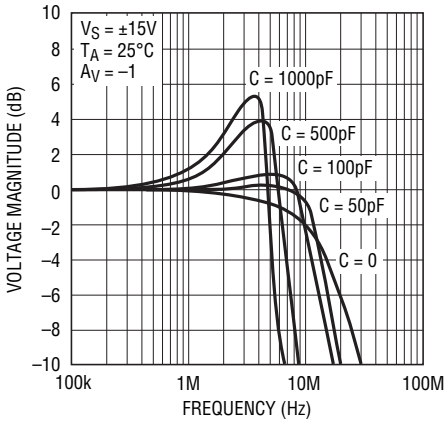
1355/1356 G12

Output Impedance vs Frequency



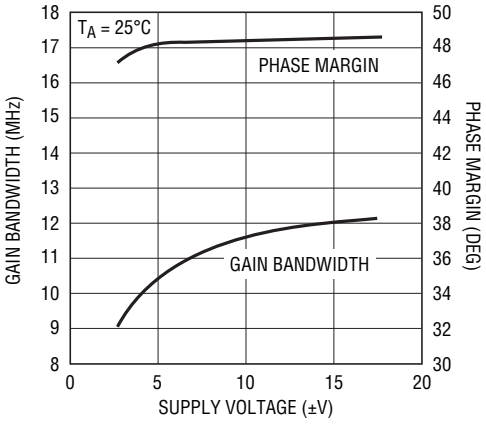
1355/1356 G13

Frequency Response vs Capacitive Load



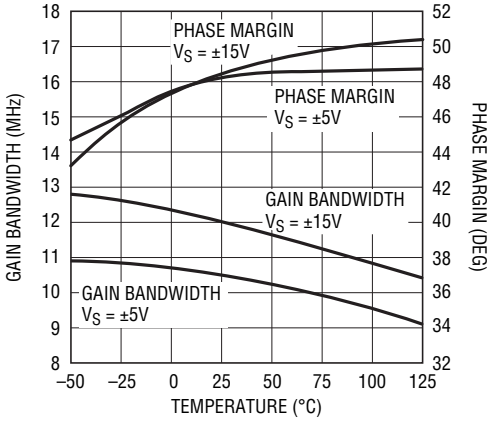
1355/1356 G19

Gain Bandwidth and Phase Margin vs Supply Voltage



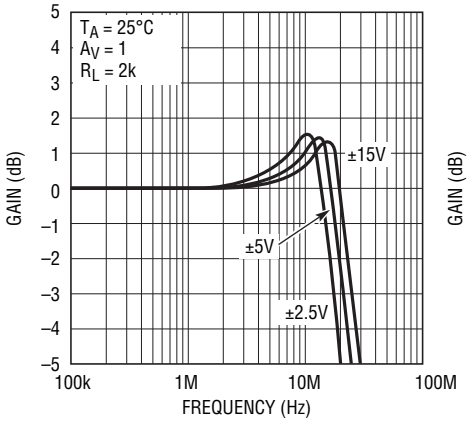
1355/1356 G15

Gain Bandwidth and Phase Margin vs Temperature



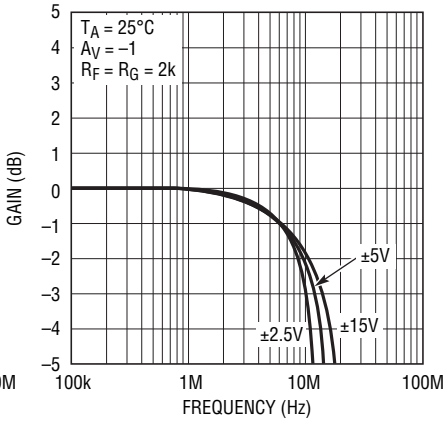
1355/1356 G16

Frequency Response vs Supply Voltage (A_V = 1)



1355/1356 G17

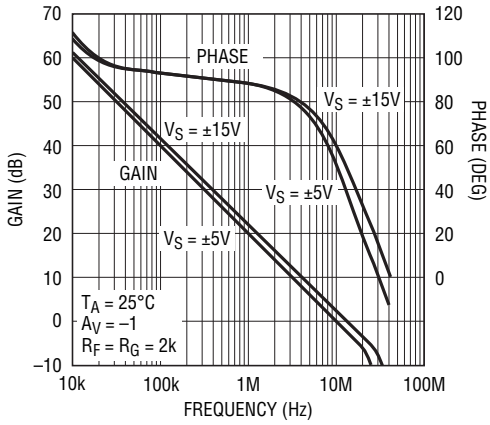
Frequency Response vs Supply Voltage (A_V = –1)



1355/1356 G18

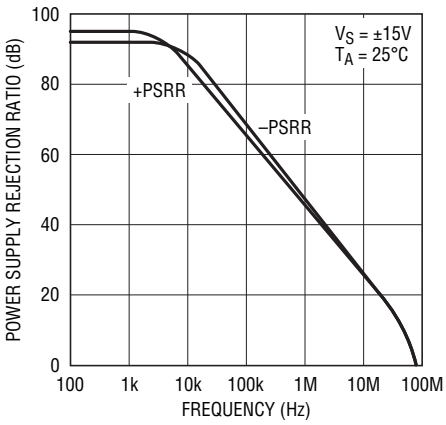
TYPICAL PERFORMANCE CHARACTERISTICS

Gain and Phase vs Frequency



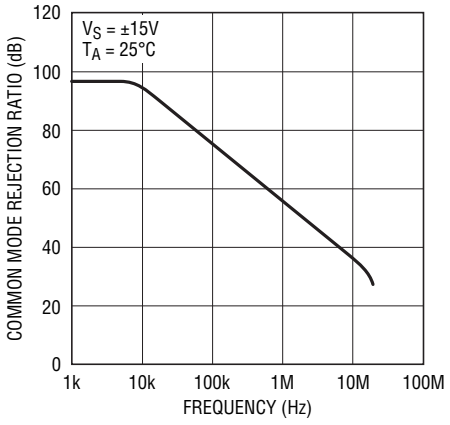
1355/1356 G14

Power Supply Rejection Ratio vs Frequency



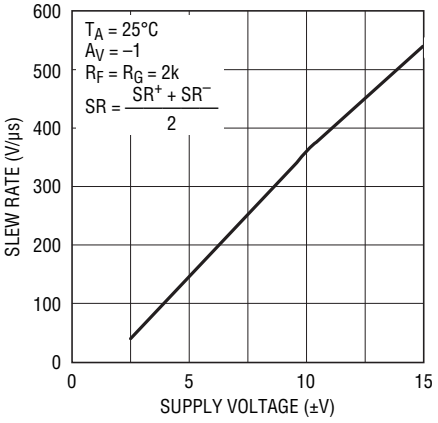
1355/1356 G20

Common Mode Rejection Ratio vs Frequency



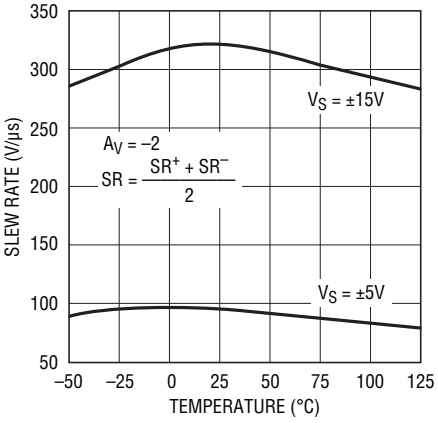
1355/1356 G21

Slew Rate vs Supply Voltage



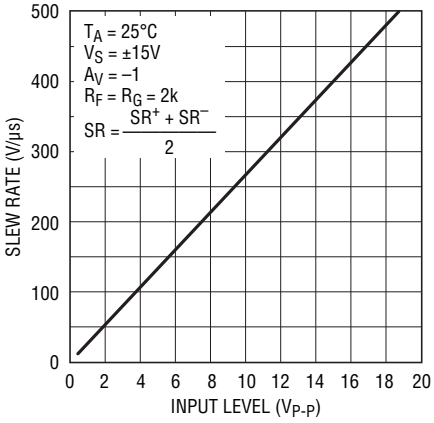
1355/1356 G22

Slew Rate vs Temperature



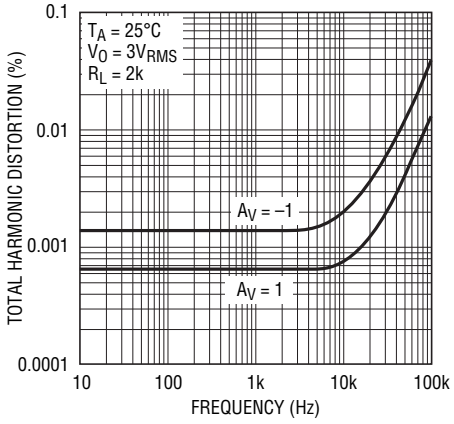
1355/1356 G23

Slew Rate vs Input Level



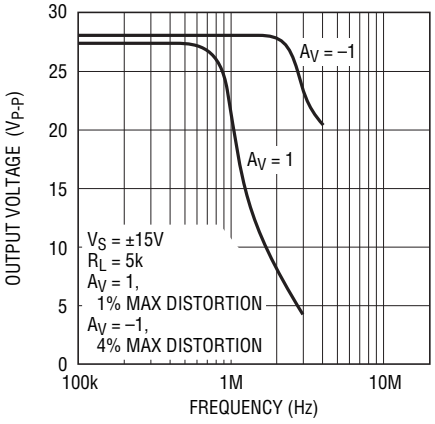
1355/1356 G24

Total Harmonic Distortion vs Frequency



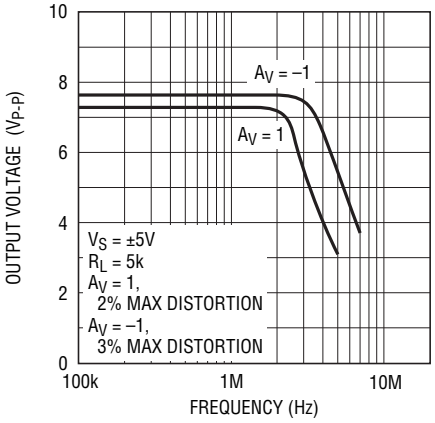
1355/1356 G25

Undistorted Output Swing vs Frequency (±15V)



1355/1356 G26

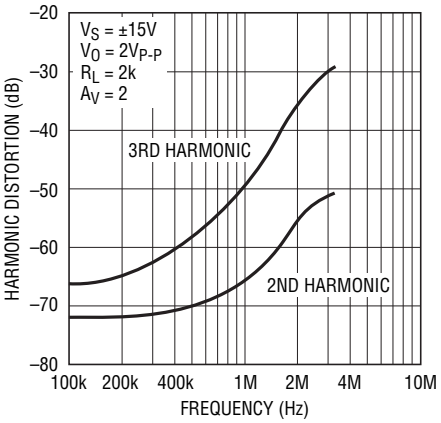
Undistorted Output Swing vs Frequency (±5V)



1355/1356 G27

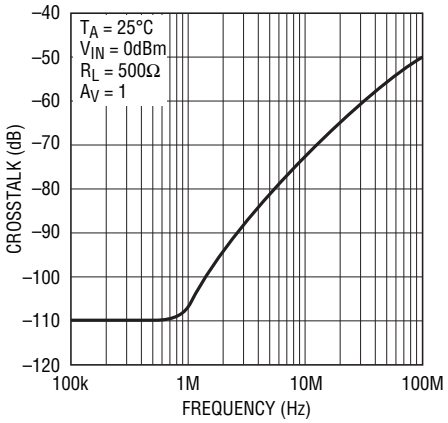
TYPICAL PERFORMANCE CHARACTERISTICS

2nd and 3rd Harmonic Distortion vs Frequency



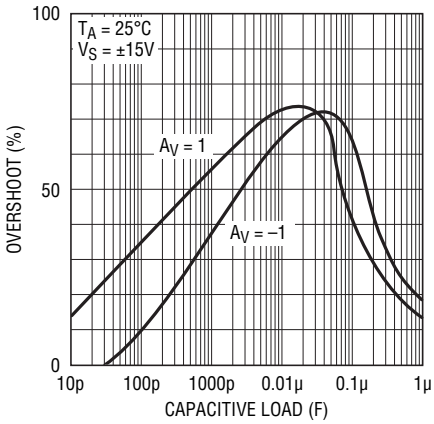
1355/1356 G28

Crosstalk vs Frequency



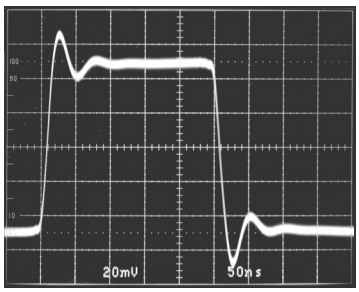
1355/1356 G29

Capacitive Load Handling



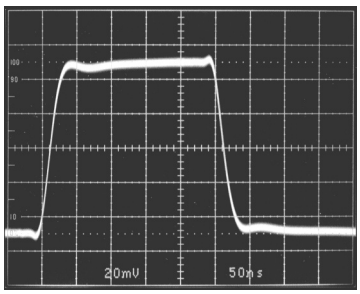
1355/1356 G30

Small-Signal Transient (A_V = 1)



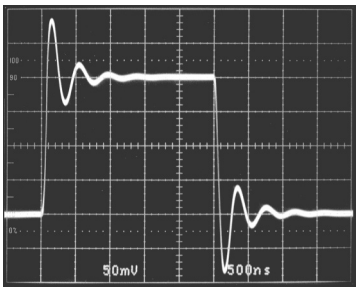
12556 G31

Small-Signal Transient (A_V = –1)



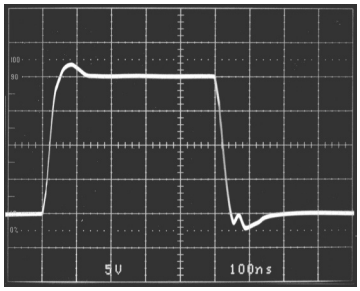
12556 G32

Small-Signal Transient (A_V = –1, C_L = 1000pF)



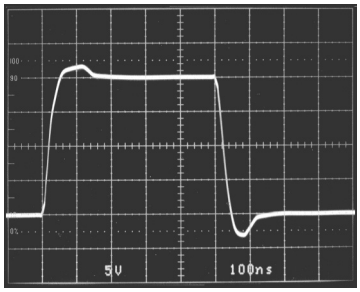
12556 G33

Large-Signal Transient (A_V = 1)



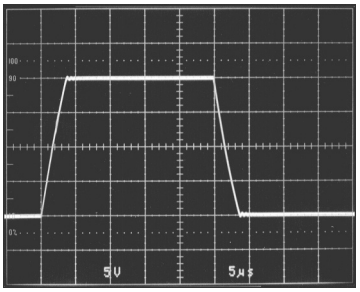
12556 G34

Large-Signal Transient (A_V = –1)



12556 G35

Large-Signal Transient (A_V = 1, C_L = 10,000pF)



12556 G36

APPLICATIONS INFORMATION

Layout and Passive Components

The LT1355/LT1356 amplifiers are easy to use and tolerant of less than ideal layouts. For maximum performance (for example, fast 0.01% settling) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications use low ESR bypass capacitors (1µF to 10µF tantalum).

The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole which can cause peaking or oscillations. If feedback resistors greater than 5k are used, a parallel capacitor of value:

$$C_F > R_G \times C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Capacitive Loading

The LT1355/LT1356 are stable with any capacitive load. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

Input Considerations

Each of the LT1355/LT1356 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on NPN/PNP beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

The inputs can withstand transient differential input voltages up to 10V without damage and need no clamping or source resistance for protection. Differential inputs, however, generate large supply currents (tens of mA) as required for high slew rates. If the device is used with sustained differential inputs, the average supply current will increase, excessive power dissipation will result and the part may be damaged. **The part should not be used as a comparator, peak detector or other open-loop application with large, sustained differential inputs.** Under normal, closed-loop operation, an increase of power dissipation is only noticeable in applications with large slewing outputs and is proportional to the magnitude of the differential input voltage and the percent of the time that the inputs are apart. Measure the average supply current for the application in order to calculate the power dissipation.

Circuit Operation

The LT1355/LT1356 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive an 800Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step, whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1355/LT1356 are tested for slew rate in a gain of –2 so higher slew rates can be expected in gains of 1 and –1, and lower slew rates in higher gain configurations.

APPLICATIONS INFORMATION

The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity-gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

Power Dissipation

The LT1355/LT1356 combine high speed and large output drive in small packages. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient or case temperature (T_A or T_C) and power dissipation (P_D) as follows:

LT1355CN8: $T_J = T_A + (P_D \bullet 130°C/W)$
LT1355CS8: $T_J = T_A + (P_D \bullet 190°C/W)$
LT1356CN: $T_J = T_A + (P_D \bullet 110°C/W)$
LT1356CS: $T_J = T_A + (P_D \bullet 150°C/W)$
LT1356HS: $T_J = T_C + (P_D \bullet 30°C/W)$

Worst-case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). For each amplifier P_{DMAX} is:

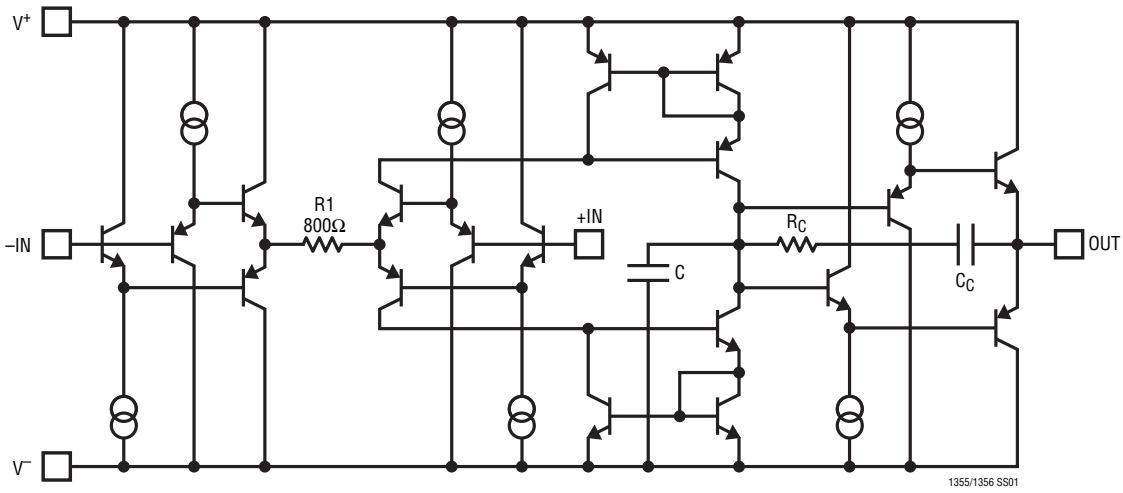
$$P_{DMAX} = (V^+ - V^-)(I_{SMAX}) + (V^+/2)^2/R_L$$

Example: LT1356 in S16 at $T_A = 70°C$, $V_S = \pm 15V$, $R_L = 1k$

$$P_{DMAX} = (30V)(1.45mA) + (7.5V)^2/1k\Omega = 99.8mW$$

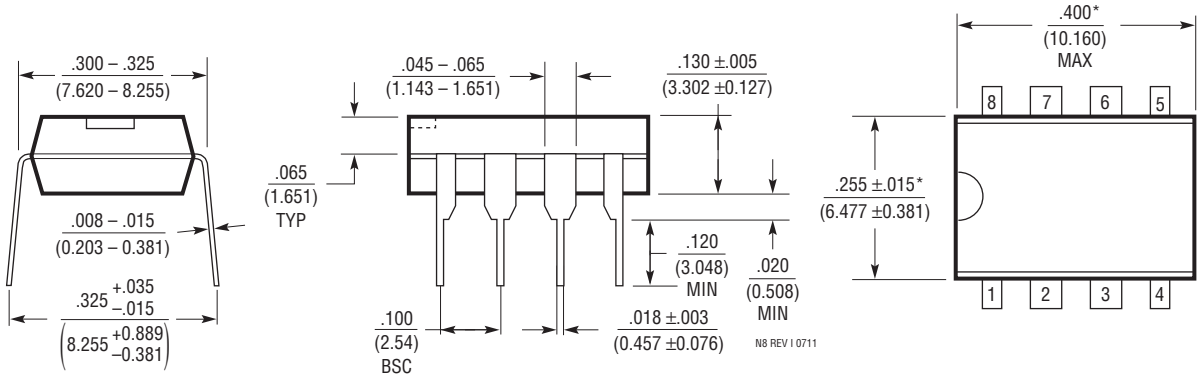
$$T_{JMAX} = 70°C + (4 \bullet 99.8mW)(150°C/W) = 130°C$$

SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

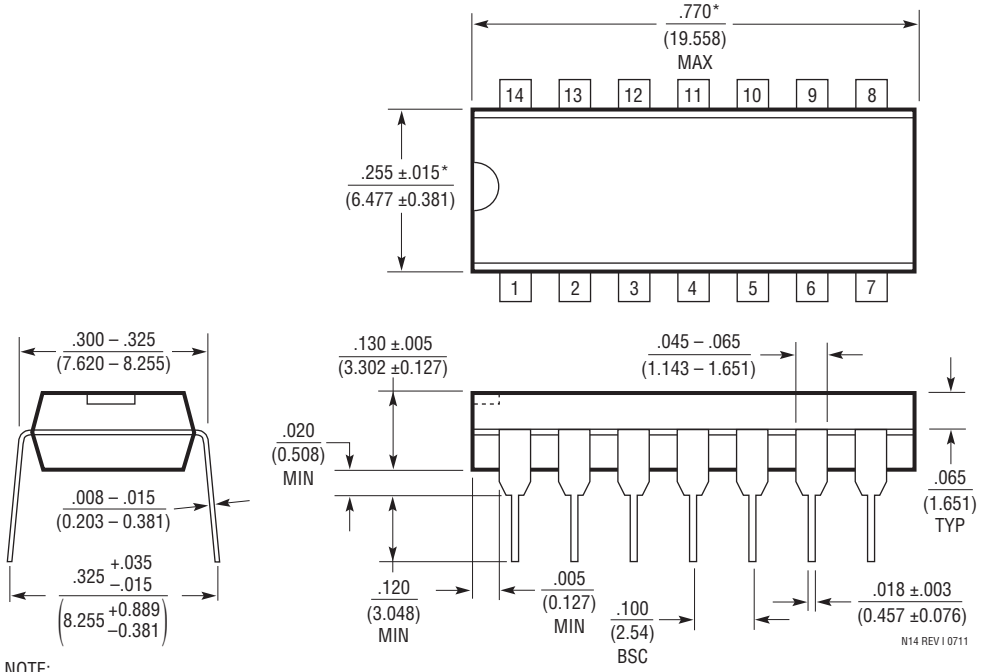
N Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510 Rev I)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

N Package
14-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510 Rev I)

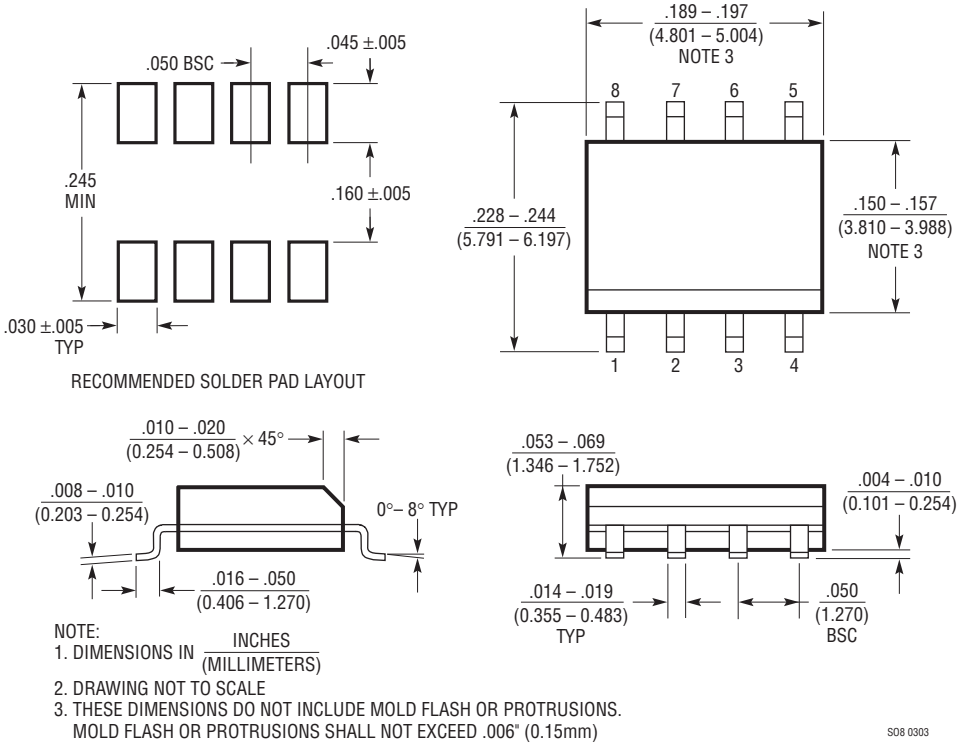


NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

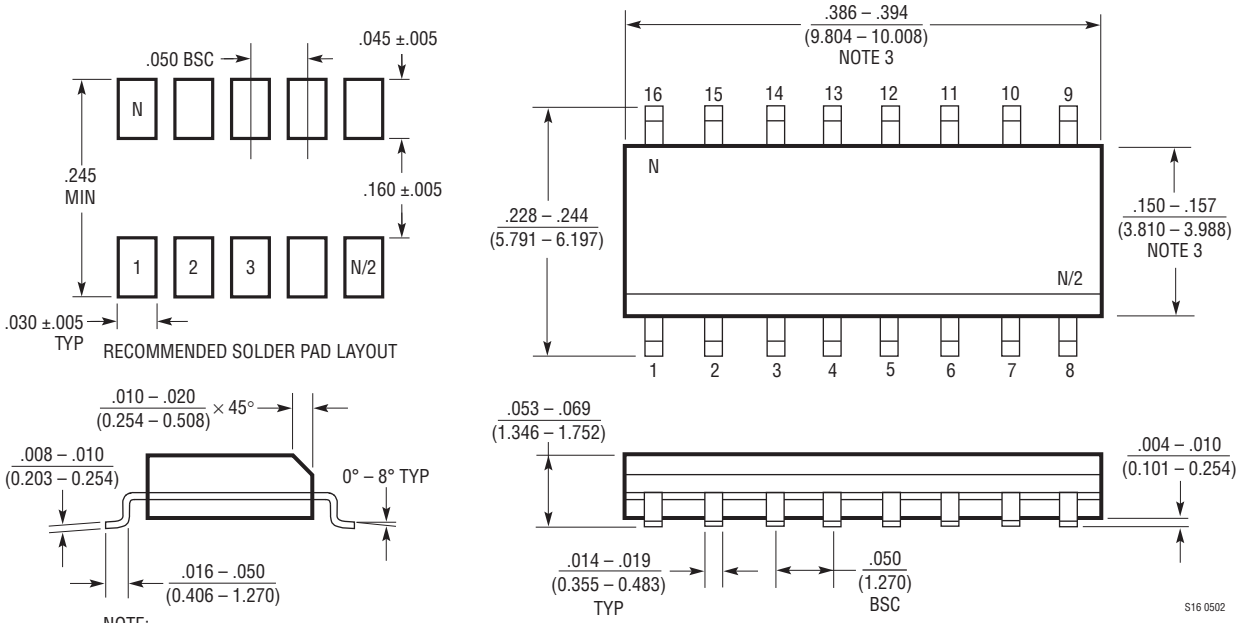


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

PACKAGE DESCRIPTION

S Package
16-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	05/12	Added H- and I-grades	2, 5, 11