

FEATURES

- 50MHz Gain Bandwidth
- 800V/ μ s Slew Rate
- 5mA Maximum Supply Current per Amplifier
- Unity-Gain Stable
- C-Load™ Op Amp Drives All Capacitive Loads
- 9nV/ $\sqrt{\text{Hz}}$ Input Noise Voltage
- 1mV Maximum Input Offset Voltage
- 1 μ A Maximum Input Bias Current
- 250nA Maximum Input Offset Current
- $\pm 13\text{V}$ Minimum Output Swing into 500 Ω
- $\pm 3.2\text{V}$ Minimum Output Swing into 150 Ω
- 4.5V/mV Minimum DC Gain, $R_L=1\text{k}$
- 60ns Settling Time to 0.1%, 10V Step
- 0.2% Differential Gain, $A_V=2$, $R_L=150\Omega$
- 0.3° Differential Phase, $A_V=2$, $R_L=150\Omega$
- Specified at $\pm 2.5\text{V}$, $\pm 5\text{V}$, and $\pm 15\text{V}$

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- Data Acquisition Systems

DESCRIPTION

The LT1361/LT1362 are dual and quad low power high speed operational amplifiers with outstanding AC and DC performance. The amplifiers feature much lower supply current and higher slew rate than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with matched high impedance inputs and the slewing performance of a current feedback amplifier. The high slew rate and single stage design provide excellent settling characteristics which make the circuit an ideal choice for data acquisition systems. Each output drives a 500 Ω load to $\pm 13\text{V}$ with $\pm 15\text{V}$ supplies and a 150 Ω load to $\pm 3.2\text{V}$ on $\pm 5\text{V}$ supplies. The amplifiers are stable with any capacitive load making them useful in buffer or cable driving applications.

The LT1361/LT1362 are members of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For a single amplifier version of the LT1361/LT1362 see the LT1360 data sheet. For higher bandwidth devices with higher supply currents see the LT1363 through LT1365 data sheets. For lower supply current amplifiers see the LT1354 to LT1359 data sheets. Singles, duals, and quads of each amplifier are available.

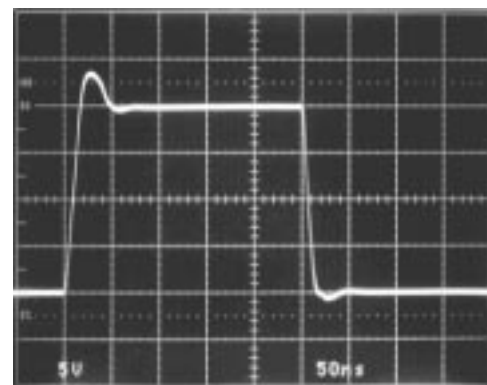
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 C-Load is a trademark of Linear Technology Corporation

TYPICAL APPLICATION

Cable Driver Frequency Response



$A_V = -1$ Large-Signal Response



1361/1362 TA02

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-)	36V	Operating Temperature Range (Note 8) ...	-40°C to 85°C
Differential Input Voltage (Transient Only) (Note 2)	$\pm 10\text{V}$	Specified Temperature Range (Note 9)	-40°C to 85°C
Input Voltage	$\pm V_S$	Maximum Junction Temperature (See Below) Plastic Package	150°C
Output Short-Circuit Duration (Note 3)	Indefinite	Storage Temperature Range	-65°C to 150°C
		Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

 <p>TOP VIEW</p> <p>OUT A 1, -IN A 2, +IN A 3, V^- 4, 8 V^+, 7 OUT B, 6 -IN B, 5 +IN B</p> <p>N8 PACKAGE 8-LEAD PDIP</p> <p>$T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 130^{\circ}\text{C/W}$</p>	<p>ORDER PART NUMBER</p> <p>LT1361CN8</p>	 <p>TOP VIEW</p> <p>OUT A 1, -IN A 2, +IN A 3, V^- 4, 8 V^+, 7 OUT B, 6 -IN B, 5 +IN B</p> <p>S8 PACKAGE 8-LEAD PLASTIC SO</p> <p>$T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 190^{\circ}\text{C/W}$</p>	<p>ORDER PART NUMBER</p> <p>LT1361CS8</p> <p>S8 PART MARKING</p> <p>1361</p>
 <p>TOP VIEW</p> <p>OUT A 1, -IN A 2, +IN A 3, V^+ 4, +IN B 5, -IN B 6, OUT B 7, 14 OUT D, 13 -IN D, 12 +IN D, 11 V^-, 10 +IN C, 9 -IN C, 8 OUT C</p> <p>N PACKAGE 14-LEAD PDIP</p> <p>$T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 110^{\circ}\text{C/W}$</p>	<p>ORDER PART NUMBER</p> <p>LT1362CN</p>	 <p>TOP VIEW</p> <p>OUT A 1, -IN A 2, +IN A 3, V^+ 4, +IN B 5, -IN B 6, OUT B 7, NC 8, 16 OUT D, 15 -IN D, 14 +IN D, 13 V^-, 12 +IN C, 11 -IN C, 10 OUT C, 9 NC</p> <p>S PACKAGE 16-LEAD PLASTIC SO</p> <p>$T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 150^{\circ}\text{C/W}$</p>	<p>ORDER PART NUMBER</p> <p>LT1362CS</p>

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)	$\pm 15\text{V}$	0.3	1.0		mV
			$\pm 5\text{V}$	0.3	1.0		mV
			$\pm 2.5\text{V}$	0.4	1.2		mV
I_{OS}	Input Offset Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	80	250		nA
I_B	Input Bias Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	0.3	1.0		μA
e_n	Input Noise Voltage	$f = 10\text{kHz}$	$\pm 2.5\text{V}$ to $\pm 15\text{V}$		9		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current	$f = 10\text{kHz}$	$\pm 2.5\text{V}$ to $\pm 15\text{V}$		0.9		$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	$V_{CM} = \pm 12\text{V}$	$\pm 15\text{V}$	20	50		$\text{M}\Omega$
					5		$\text{M}\Omega$
C_{IN}	Input Capacitance		$\pm 15\text{V}$	3			pF

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
	Input Voltage Range ⁺		$\pm 15\text{V}$	12.0	13.4		V
			$\pm 5\text{V}$	2.5	3.4		V
			$\pm 2.5\text{V}$	0.5	1.1		V
	Input Voltage Range ⁻		$\pm 15\text{V}$		-13.2	-12.0	V
			$\pm 5\text{V}$		-3.2	-2.5	V
			$\pm 2.5\text{V}$		-0.9	-0.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$	$\pm 15\text{V}$	86	92		dB
		$V_{CM} = \pm 2.5\text{V}$	$\pm 5\text{V}$	79	84		dB
		$V_{CM} = \pm 0.5\text{V}$	$\pm 2.5\text{V}$	68	74		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V}$ to $\pm 15\text{V}$		93	105		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$, $R_L = 1\text{k}$	$\pm 15\text{V}$	4.5	9.0		V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L = 500\Omega$	$\pm 15\text{V}$	3.0	6.5		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 500\Omega$	$\pm 5\text{V}$	3.0	6.4		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 150\Omega$	$\pm 5\text{V}$	1.5	4.2		V/mV
		$V_{OUT} = \pm 1\text{V}$, $R_L = 500\Omega$	$\pm 2.5\text{V}$	2.5	5.2		V/mV
V_{OUT}	Output Swing	$R_L = 1\text{k}$, $V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	13.5	13.9		$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	13.0	13.6		$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	3.5	4.0		$\pm\text{V}$
		$R_L = 150\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	3.2	3.8		$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 40\text{mV}$	$\pm 2.5\text{V}$	1.3	1.7		$\pm\text{V}$
I_{OUT}	Output Current	$V_{OUT} = \pm 13\text{V}$	$\pm 15\text{V}$	26	34		mA
		$V_{OUT} = \pm 3.2\text{V}$	$\pm 5\text{V}$	21	29		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	40	54		mA
SR	Slew Rate	$A_V = -2$, (Note 5)	$\pm 15\text{V}$	600	800		V/ μs
			$\pm 5\text{V}$	250	350		V/ μs
	Full Power Bandwidth	10V Peak, (Note 6) 3V Peak, (Note 6)	$\pm 15\text{V}$		12.7		MHz
			$\pm 5\text{V}$		18.6		MHz
GBW	Gain Bandwidth	$f = 200\text{kHz}$	$\pm 15\text{V}$	35	50		MHz
			$\pm 5\text{V}$	25	37		MHz
			$\pm 2.5\text{V}$		32		MHz
t_r , t_f	Rise Time, Fall Time	$A_V = 1$, 10%-90%, 0.1V	$\pm 15\text{V}$		3.1		ns
			$\pm 5\text{V}$		4.3		ns
	Overshoot	$A_V = 1$, 0.1V	$\pm 15\text{V}$		35		%
			$\pm 5\text{V}$		27		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT} , 0.1V	$\pm 15\text{V}$		5.2		ns
			$\pm 5\text{V}$		6.4		ns
t_s	Settling Time	10V Step, 0.1%, $A_V = -1$	$\pm 15\text{V}$		60		ns
		10V Step, 0.01%, $A_V = -1$	$\pm 15\text{V}$		90		ns
		5V Step, 0.1%, $A_V = -1$	$\pm 5\text{V}$		65		ns
	Differential Gain	$f = 3.58\text{MHz}$, $A_V = 2$, $R_L = 150\Omega$	$\pm 15\text{V}$		0.20		%
			$\pm 5\text{V}$		0.20		%
		$f = 3.58\text{MHz}$, $A_V = 2$, $R_L = 1\text{k}$	$\pm 15\text{V}$		0.04		%
			$\pm 5\text{V}$		0.02		%
	Differential Phase	$f = 3.58\text{MHz}$, $A_V = 2$, $R_L = 150\Omega$	$\pm 15\text{V}$		0.40		Deg
			$\pm 5\text{V}$		0.30		Deg
		$f = 3.58\text{MHz}$, $A_V = 2$, $R_L = 1\text{k}$	$\pm 15\text{V}$		0.07		Deg
			$\pm 5\text{V}$		0.26		Deg
R_0	Output Resistance	$A_V = 1$, $f = 1\text{MHz}$	$\pm 15\text{V}$		1.4		Ω
	Channel Separation	$V_{OUT} = \pm 10\text{V}$, $R_L = 500\Omega$	$\pm 15\text{V}$	100	113		dB
I_S	Supply Current	Each Amplifier	$\pm 15\text{V}$		4.0	5.0	mA
			$\pm 5\text{V}$		3.8	4.8	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range

0°C ≤ T_A ≤ 70°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V _{SUPPLY}	MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	(Note 4)	±15V	●		1.5	mV
			±5V	●		1.5	mV
			±2.5V	●		1.7	mV
	Input V _{OS} Drift	(Note 7)	±2.5V to ±15V	●	9	12	μV/°C
I _{OS}	Input Offset Current		±2.5V to ±15V	●		350	nA
I _B	Input Bias Current		±2.5V to ±15V	●		1.5	μA
CMRR	Common Mode Rejection Ratio	V _{CM} = ±12V	±15V	●	84		dB
		V _{CM} = ±2.5V	±5V	●	77		dB
		V _{CM} = ±0.5V	±2.5V	●	66		dB
PSRR	Power Supply Rejection Ratio	V _S = ±2.5V to ±15V		●	91		dB
A _{VOL}	Large-Signal Voltage Gain	V _{OUT} = ±12V, R _L = 1k	±15V	●	3.6		V/mV
		V _{OUT} = ±10V, R _L = 500Ω	±15V	●	2.4		V/mV
		V _{OUT} = ±2.5V, R _L = 500Ω	±5V	●	2.4		V/mV
		V _{OUT} = ±2.5V, R _L = 150Ω	±5V	●	1.0		V/mV
		V _{OUT} = ±1V, R _L = 500Ω	±2.5V	●	2.0		V/mV
V _{OUT}	Output Swing	R _L = 1k, V _{IN} = ±40mV	±15V	●	13.4		±V
		R _L = 500Ω, V _{IN} = ±40mV	±15V	●	12.8		±V
		R _L = 500Ω, V _{IN} = ±40mV	±5V	●	3.4		±V
		R _L = 150Ω, V _{IN} = ±40mV	±5V	●	3.1		±V
		R _L = 500Ω, V _{IN} = ±40mV	±2.5V	●	1.2		±V
I _{OUT}	Output Current	V _{OUT} = ±12.8V	±15V	●	25		mA
		V _{OUT} = ±3.1V	±5V	●	20		mA
I _{SC}	Short-Circuit Current	V _{OUT} = 0V, V _{IN} = ±3V	±15V	●	32		mA
SR	Slew Rate	A _V = -2, (Note 5)	±15V	●	475		V/μs
			±5V	●	185		V/μs
GBW	Gain Bandwidth	f = 200kHz	±15V	●	31		MHz
			±5V	●	22		MHz
	Channel Separation	V _{OUT} = ±10V, R _L = 500Ω	±15V	●	98		dB
I _S	Supply Current	Each Amplifier	±15V	●		5.8	mA
		Each Amplifier	±5V	●		5.6	mA

The ● denotes the specifications which apply over the temperature range -40°C ≤ T_A ≤ 85°C, V_{CM} = 0V unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS	V _{SUPPLY}	MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	(Note 4)	±15V	●		2.0	mV
			±5V	●		2.0	mV
			±2.5V	●		2.2	mV
	Input V _{OS} Drift	(Note 7)	±2.5V to ±15V	●	9	12	μV/°C
I _{OS}	Input Offset Current		±2.5V to ±15V	●		400	nA
I _B	Input Bias Current		±2.5V to ±15V	●		1.8	μA
CMRR	Common Mode Rejection Ratio	V _{CM} = ±12V	±15V	●	84		dB
		V _{CM} = ±2.5V	±5V	●	77		dB
		V _{CM} = ±0.5V	±2.5V	●	66		dB
PSRR	Power Supply Rejection Ratio	V _S = ±2.5V to ±15V		●	90		dB
A _{VOL}	Large-Signal Voltage Gain	V _{OUT} = ±12V, R _L = 1k	±15V	●	2.5		V/mV
		V _{OUT} = ±10V, R _L = 500Ω	±15V	●	1.5		V/mV
		V _{OUT} = ±2.5V, R _L = 500Ω	±5V	●	1.5		V/mV
		V _{OUT} = ±2.5V, R _L = 150Ω	±5V	●	0.6		V/mV
		V _{OUT} = ±1V, R _L = 500Ω	±2.5V	●	1.3		V/mV

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the temperature range $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS	V _{SUPPLY}	MIN	TYP	MAX	UNITS
V _{OUT}	Output Swing	R _L = 1k, V _{IN} = ±40mV	±15V	●	13.4		±V
		R _L = 500Ω, V _{IN} = ±40mV	±15V	●	12.0		±V
		R _L = 500Ω, V _{IN} = ±40mV	±5V	●	3.4		±V
		R _L = 150Ω, V _{IN} = ±40mV	±5V	●	3.0		±V
		R _L = 500Ω, V _{IN} = ±40mV	±2.5V	●	1.2		±V
I _{OUT}	Output Current	V _{OUT} = ±12.0V	±15V	●	24		mA
		V _{OUT} = ±3.0V	±5V	●	20		mA
I _{SC}	Short-Circuit Current	V _{OUT} = 0V, V _{IN} = ±3V	±15V	●	30		mA
SR	Slew Rate	A _V = -2, (Note 5)	±15V	●	450		V/μs
			±5V	●	175		V/μs
GBW	Gain Bandwidth	f = 200kHz	±15V	●	30		MHz
			±5V	●	20		MHz
	Channel Separation	V _{OUT} = ±10V, R _L = 500Ω	±15V	●	98		dB
I _S	Supply Current	Each Amplifier	±15V	●		6.0	mA
		Each Amplifier	±5V	●		5.8	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Differential inputs of ±10V are appropriate for transient operation only, such as during slewing. Large, sustained differential inputs will cause excessive power dissipation and may damage the part. See Input Considerations in the Applications Information section of this data sheet for more details.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: Input offset voltage is pulse tested and is exclusive of warm-up drift.

Note 5: Slew rate is measured between ±10V on the output with ±6V input for ±15V supplies and ±1V on the output with ±1.75V input for ±5V supplies.

Note 6: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi V_p$.

Note 7: This parameter is not 100% tested.

Note 8: The LT1361C/LT1362C are guaranteed functional over the operating temperature range of -40°C to 85°C .

Note 9: The LT1361C/LT1362C are guaranteed to meet specified performance from 0°C to 70°C . The LT1361C/LT1362C are designed, characterized and expected to meet specified performance from -40°C to 85°C , but are not tested or QA sampled at these temperatures. For guaranteed I-grade parts, consult the factory.

TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage and Temperature



1361/1362 G01

Input Common Mode Range vs Supply Voltage



1361/1362 G02

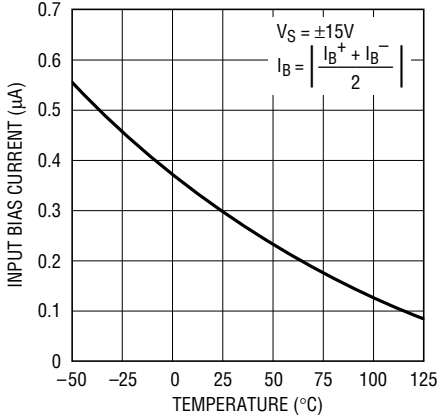
Input Bias Current vs Input Common Mode Voltage



1361/1362 G03

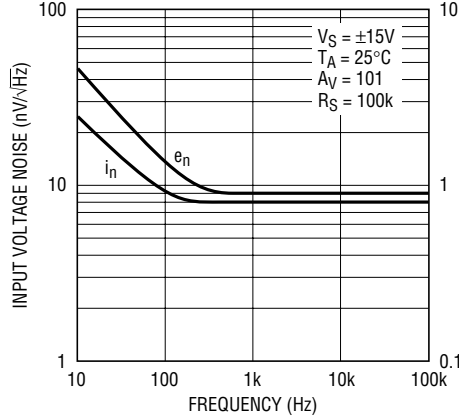
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Temperature



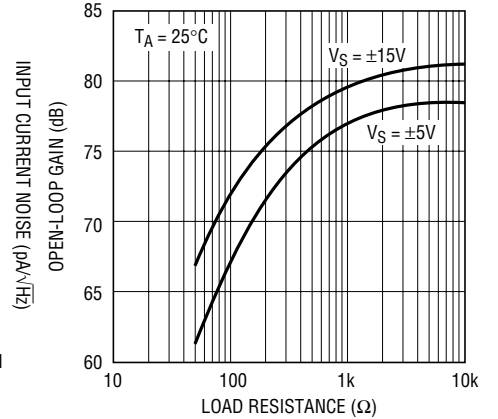
1361/1362 G04

Input Noise Spectral Density



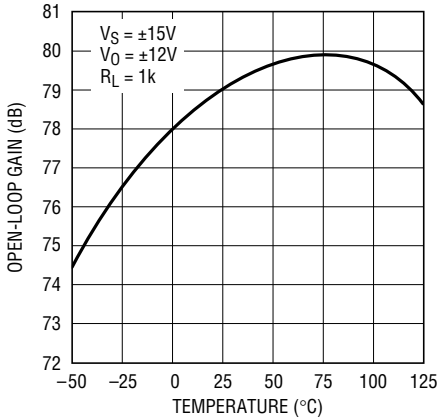
1361/1362 G05

Open-Loop Gain vs Resistive Load



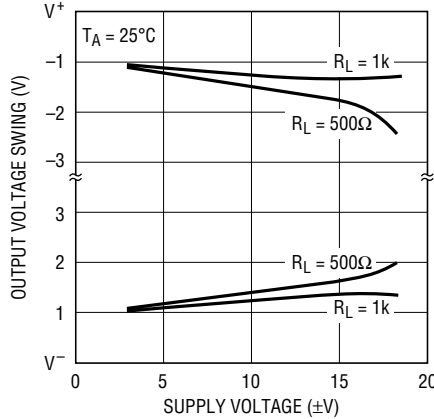
1361/1362 G06

Open-Loop Gain vs Temperature



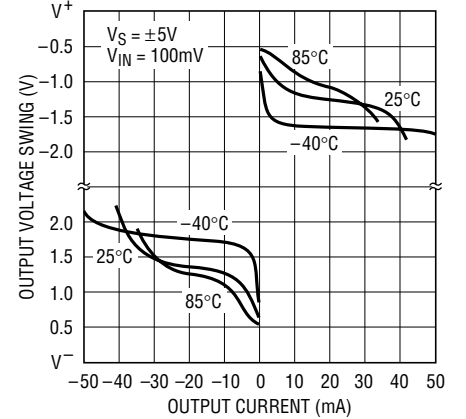
1361/1362 G07

Output Voltage Swing vs Supply Voltage



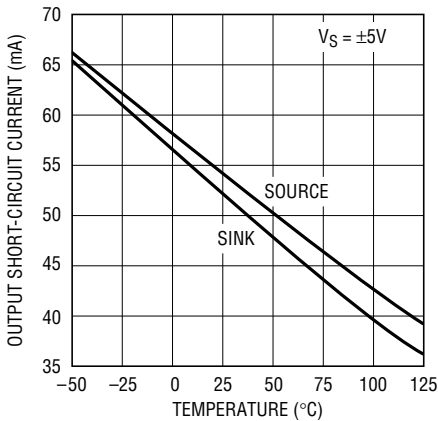
1361/1362 G08

Output Voltage Swing vs Load Current



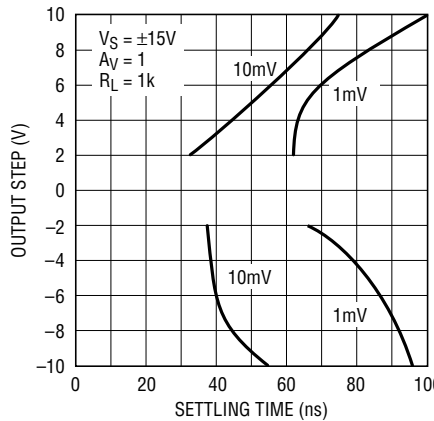
1361/1362 G09

Output Short-Circuit Current vs Temperature



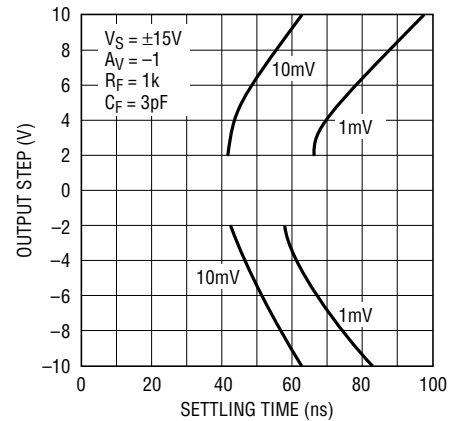
1361/1362 G10

Settling Time vs Output Step (Noninverting)



1361/1362 G11

Settling Time vs Output Step (Inverting)



1361/1362 G12

TYPICAL PERFORMANCE CHARACTERISTICS

Output Impedance vs Frequency



1361/1362 G13

Gain and Phase vs Frequency



1361/1362 G14

Crosstalk vs Frequency



1361/1362 G15

Gain Bandwidth and Phase Margin vs Temperature



1361/1362 G16

Frequency Response vs Supply Voltage (AV = 1)



1361/1362 G17

Frequency Response vs Capacitive Load



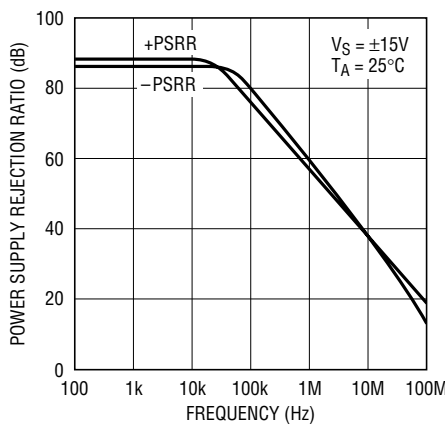
1361/1362 G18

Gain Bandwidth and Phase Margin vs Supply Voltage



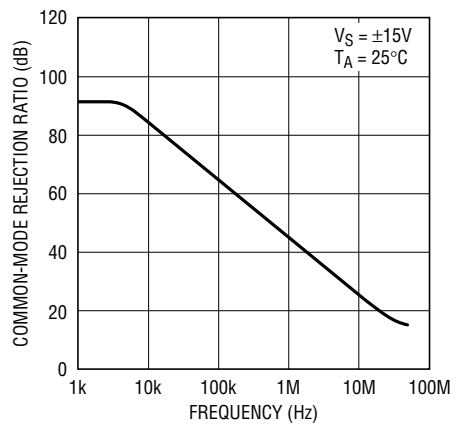
1361/1362 G19

Power Supply Rejection Ratio vs Frequency



1361/1362 G20

Common Mode Rejection Ratio vs Frequency



1361/1362 G20

TYPICAL PERFORMANCE CHARACTERISTICS

Slew Rate vs Supply Voltage



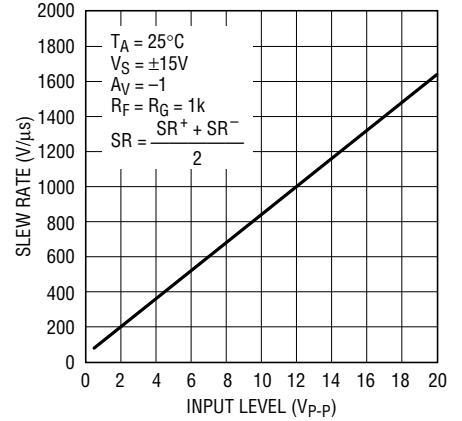
1361/1362 G22

Slew Rate vs Temperature



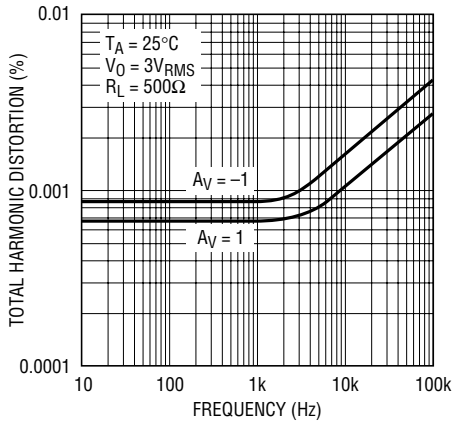
1361/1362 G23

Slew Rate vs Input Level



1361/1362 G24

Total Harmonic Distortion vs Frequency



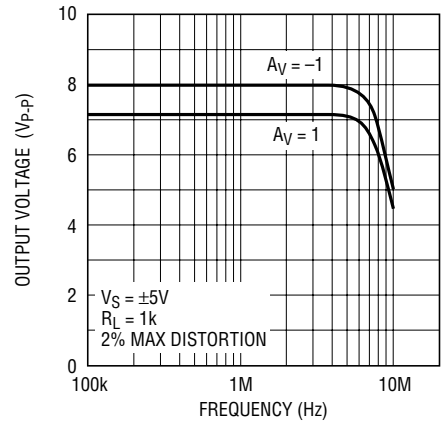
1361/1362 G25

Undistorted Output Swing vs Frequency (±15V)



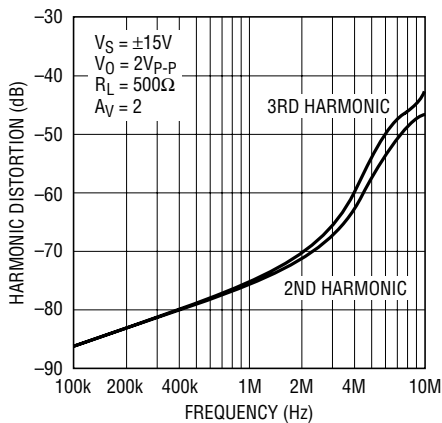
1361/1362 G26

Undistorted Output Swing vs Frequency (±5V)



1361/1362 G27

2nd and 3rd Harmonic Distortion vs Frequency



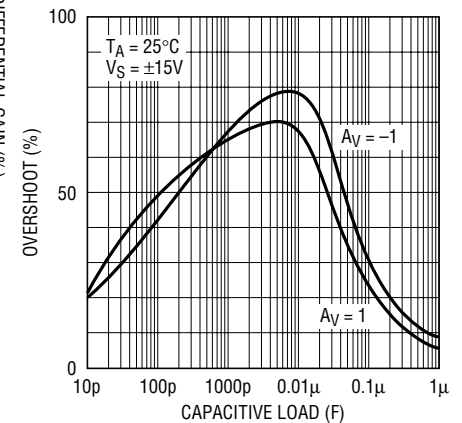
1361/1362 G28

Differential Gain and Phase vs Supply Voltage



1361/1362 G29

Capacitive Load Handling



1361/1362 G30

TYPICAL PERFORMANCE CHARACTERISTICS

Small-Signal Transient
($A_V = 1$)



1361/1362 TA31

Small-Signal Transient
($A_V = -1$)



1361/1362 TA32

Small-Signal Transient
($A_V = -1, C_L = 500\text{pF}$)



1361/1362 TA33

Large-Signal Transient
($A_V = 1$)



1361/1362 TA34

Large-Signal Transient
($A_V = -1$)



1361/1362 TA35

Large-Signal Transient
($A_V = 1, C_L = 10,000\text{pF}$)



1361/1362 TA36

APPLICATIONS INFORMATION

Layout and Passive Components

The LT1361/LT1362 amplifiers are easy to use and tolerant of less than ideal layouts. For maximum performance (for example, fast 0.01% settling) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01 μF to 0.1 μF). For high drive current applications use low ESR bypass capacitors (1 μF to 10 μF tantalum). The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole which can cause peaking or oscillations. If feedback resistors greater than 5k Ω are used, a parallel capacitor of value

$$C_F > R_G \times C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN} .

Input Considerations

Each of the LT1361/LT1362 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on NPN/PNP beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

The inputs can withstand transient differential input voltages up to 10V without damage and need no clamping or source resistance for protection. Differential inputs, however, generate large supply currents (tens of mA) as required for high slew rates. If the device is used with sustained differential inputs, the average supply current will increase, excessive power dissipation will result and the part may be damaged. **The part should not be used as a comparator, peak detector or other open-loop applica-**

APPLICATIONS INFORMATION

tion with large, sustained differential inputs. Under normal, closed-loop operation, an increase of power dissipation is only noticeable in applications with large slewing outputs and is proportional to the magnitude of the differential input voltage and the percent of the time that the inputs are apart. Measure the average supply current for the application in order to calculate the power dissipation.

Capacitive Loading

The LT1361/LT1362 are stable with any capacitive load. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response as shown in the typical performance curves. The photo of the small signal response with 500pF load shows 60% peaking. The large signal response shows the output slew rate being limited to 5V/μs by the short-circuit current. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

Circuit Operation

The LT1361/LT1362 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive a 500Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step,

whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1361/LT1362 are tested for slew rate in a gain of -2 so higher slew rates can be expected in gains of 1 and -1, and lower slew rates in higher gain configurations.

The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity-gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

Power Dissipation

The LT1361/LT1362 combine high speed and large output drive in small packages. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

$$\text{LT1361CN8: } T_J = T_A + (P_D \times 130^\circ\text{C/W})$$

$$\text{LT1361CS8: } T_J = T_A + (P_D \times 190^\circ\text{C/W})$$

$$\text{LT1362CN: } T_J = T_A + (P_D \times 110^\circ\text{C/W})$$

$$\text{LT1362CS: } T_J = T_A + (P_D \times 150^\circ\text{C/W})$$

Worst case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). For each amplifier $P_{D\text{MAX}}$ is:

$$P_{D\text{MAX}} = (V^+ - V^-)(I_{S\text{MAX}}) + (V^+/2)^2/R_L$$

Example: LT1362 in S16 at 70°C, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$

$$P_{D\text{MAX}} = (10\text{V})(5.6\text{mA}) + (2.5\text{V})^2/100\Omega = 119\text{mW}$$

$$T_{J\text{MAX}} = 70^\circ\text{C} + (4 \times 119\text{mW})(150^\circ\text{C/W}) = 141^\circ\text{C}$$

SIMPLIFIED SCHEMATIC

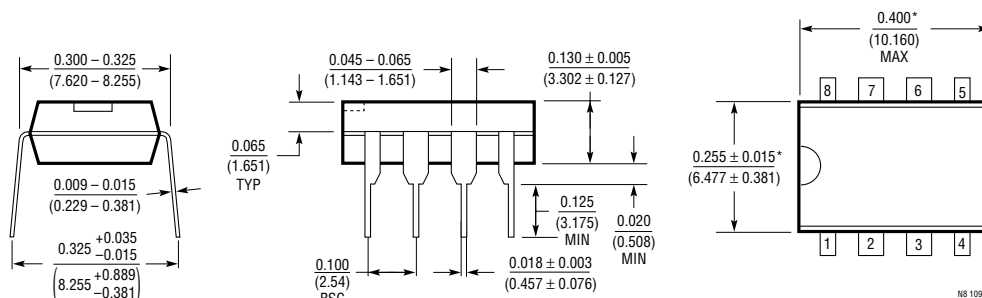


1361/1362 SS01

PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

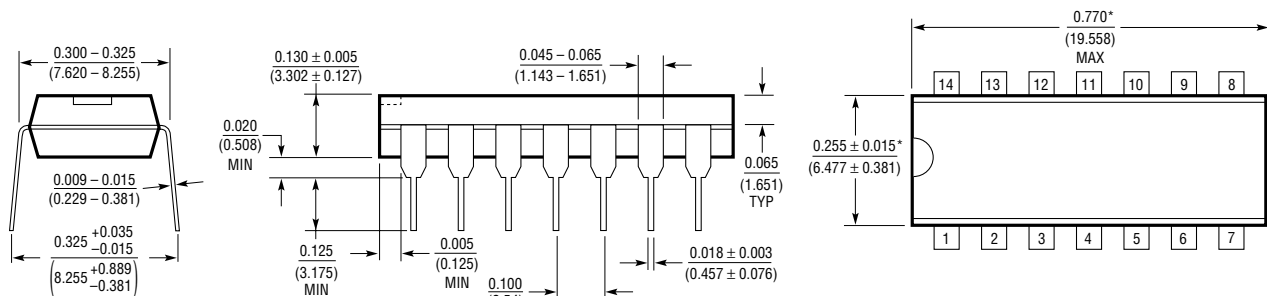
N8 Package 8-Lead PDIP (Narrow 0.300) (LTC DWG # 05-08-1510)



MS 1098

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N Package 14-Lead PDIP (Narrow 0.300) (LTC DWG # 05-08-1510)



MS 1098

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)