Micropower Dual/Quad Precision Rail-to-Rail Input and Output Op Amps

FEATURES

- **Rail-to-Rail Input and Output**
- **Low Supply Current: 75μA Max**
- **390μV $V_{OS(MAX)}$ for $V_{CM} = V^-$ to V^+**
- **High Common Mode Rejection Ratio: 83dB Min**
- High A_{VOL}: 400V/mV Min
- Wide Supply Range: 2V to ±5V
- Low Input Bias Current: 6nA Typ
- 120kHz Gain Bandwidth Product

APPLICATIONS

- Supply Current Sensing
- Driving A/D Converters
- Test Equipment Amplifiers

DESCRIPTION

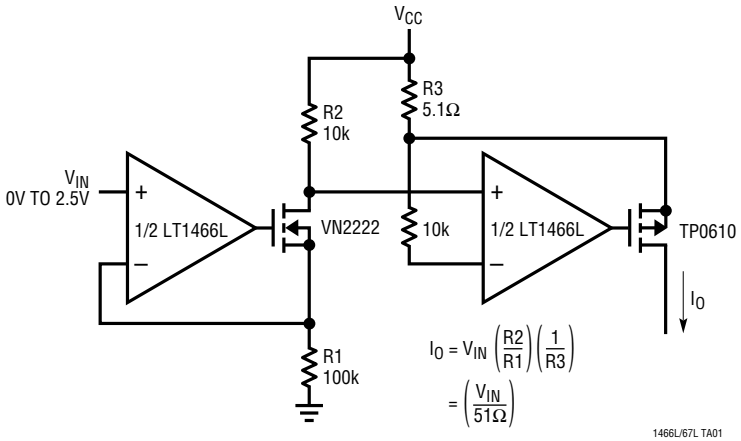
The LT®1466L/LT1467L are dual/quad bipolar op amps that combine rail-to-rail input and output operation with precision specifications. Using a patented technique, both input stages of the LT1466L/LT1467L are trimmed: one at the negative supply and the other at the positive supply. The resulting common mode rejection of 83dB minimum is much better than other rail-to-rail input op amps. A minimum open-loop gain of 400V/mV into a 10k load virtually eliminates all gain error. Operation is specified for 3V, 5V and ±5V supplies.

Unlike other rail-to-rail amplifiers, the input offset voltage of 390μV maximum is guaranteed across the entire rail-to-rail input range, not just at half supply. The graph below contrasts the V_{OS} specifications of the LT1466L/LT1467L to a competitive part that is specified only at half supply. As can be seen, the LT1466L/LT1467L's limits are much tighter for inputs near either supply.

The LT1466L is available in 8-lead PDIP and SO-8 packages with the standard dual pinout. The LT1467L features the standard quad pinout and is available in a 16-lead narrow SO package.

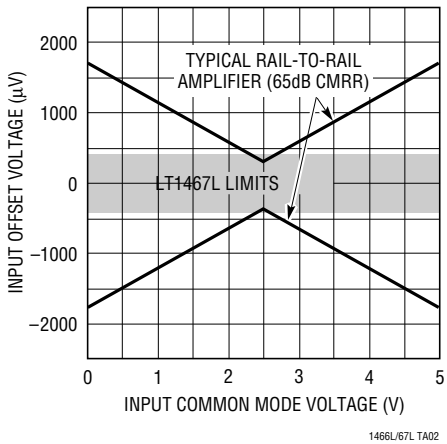
TYPICAL APPLICATION

Variable Current Source



1466L/67L TA01

Worst-Case V_{OS} vs Input Common Mode Voltage



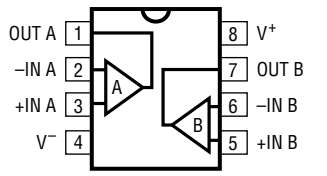
1466L/67L TA02

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±8V
Input Current ..... ±15mA
Output Short-Circuit Duration (Note 1) ..... Continuous
Specified Temperature Range ..... 0°C to 70°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW



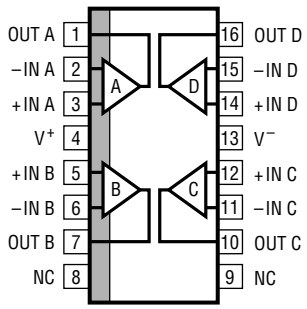
N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 190°C/W (S)

ORDER PART NUMBER
LT1466LCN8 LT1466LCS8
S8 PART MARKING
1466L

TOP VIEW



S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1467LCS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_O = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^-$			110 110	390 390	µV µV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+			75	345	µV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^-$, V^+ (Notes 3, 4)			150	550	µV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^-$		 –14	3 –6	14	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^-$ to V^+			9	28	nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^-$			0.6 0.4	3.6 3.6	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+			0.9	5.1	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+$ (Note 4) $V_{CM} = V^-$ (Note 4)			0.6 0.6	5.1 5.1	nA nA
e_n	Input Noise Voltage Density	f = 1kHz			45		nV/√Hz
i_n	Input Noise Current Density	f = 1kHz			0.05		pA/√Hz
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.4V, R_L = 10k V_S = 3V, V_O = 0.5V to 2.4V, R_L = 10k		400 250	1500 1000		V/mV V/mV

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_O = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	V_{CM} = V^- to V^+, V_S = 5V		83	96		dB
	CMRR Match (Channel-to-Channel)	V_{CM} = V^- to V^+, V_S = 5V (Note 4)		80	93		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.3V to 12V, V_{CM} = V_O = 0.5V		90	105		dB
	PSRR Match (Channel-to-Channel)	V_S = 2.3V to 12V, V_{CM} = V_O = 0.5V (Note 4)		84	105		dB
V_{OL}	Output Voltage Swing LOW	No Load			32	60	mV
		I_{SINK} = 0.5mA			135	270	mV
		I_{SINK} = 2.5mA			235	470	mV
V_{OH}	Output Voltage Swing HIGH	No Load		V^+ – 0.052	V^+ – 0.026		V
		I_{SOURCE} = 0.5mA		V^+ – 0.270	V^+ – 0.135		V
		I_{SOURCE} = 2.5mA		V^+ – 0.570	V^+ – 0.265		V
I_{SC}	Short-Circuit Current			10	17		mA
I_S	Supply Current per Amplifier				60	75	µA

0°C ≤ T_A ≤ 70°C, V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_O = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V^+	●		140	585	µV
		V_{CM} = V^-	●		140	585	µV
V_{OS} TC	Input Offset Voltage Drift (Note 2)		●		2	7	µV/°C
ΔV_{OS}	Input Offset Voltage Shift	V_{CM} = V^- to V^+	●		80	500	µV
	Input Offset Voltage Match (Channel-to-Channel)	V_{CM} = V^-, V^+ (Notes 3, 4)	●		170	825	µV
I_B	Input Bias Current	V_{CM} = V^+	●		8	16	nA
		V_{CM} = V^-	●	–16	–8		nA
ΔI_B	Input Bias Current Shift	V_{CM} = V^- to V^+	●		16	32	nA
I_{OS}	Input Offset Current	V_{CM} = V^+	●		0.7	5.3	nA
		V_{CM} = V^-	●		0.5	5.3	nA
ΔI_{OS}	Input Offset Current Shift	V_{CM} = V^- to V^+	●		0.8	7.5	nA
	Input Bias Current Match (Channel-to-Channel)	V_{CM} = V^+ (Note 4)	●		0.7	7.5	nA
		V_{CM} = V^- (Note 4)	●		0.6	7.5	nA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.4V, R_L = 10k	●	100	500		V/mV
		V_S = 3V, V_O = 0.5V to 2.4V, R_L = 10k	●	70	400		V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = V^- to V^+, V_S = 5V	●	80	96		dB
	CMRR Match (Channel-to-Channel)	V_{CM} = V^- to V^+, V_S = 5V (Note 4)	●	75	93		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.3V to 12V, V_{CM} = V_O = 0.5V	●	80	105		dB
	PSRR Match (Channel-to-Channel)	V_S = 2.3V to 12V, V_{CM} = V_O = 0.5V (Note 4)	●	80	105		dB
V_{OL}	Output Voltage Swing LOW	No Load	●		42	80	mV
		I_{SINK} = 0.5mA	●		150	300	mV
		I_{SINK} = 2.5mA	●		270	540	mV
V_{OH}	Output Voltage Swing HIGH	No Load	●	V^+ – 0.065	V^+ – 0.033		V
		I_{SOURCE} = 0.5mA	●	V^+ – 0.305	V^+ – 0.155		V
		I_{SOURCE} = 2.5mA	●	V^+ – 0.620	V^+ – 0.310		V
I_{SC}	Short-Circuit Current		●	7	16		mA
I_S	Supply Current per Amplifier		●		70	85	µA

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±5V, V_{CM} = V_O = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$			120	475	µV
		$V_{CM} = V^-$			120	475	µV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+			80	390	µV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^-$, V^+ (Notes 3, 4)			150	685	µV
I_B	Input Bias Current	$V_{CM} = V^+$			3	14	nA
		$V_{CM} = V^-$		–14	–6		nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^-$ to V^+			9	28	nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$			0.6	3.6	nA
		$V_{CM} = V^-$			0.4	3.6	nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+			0.9	5.1	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+$ (Note 4)			0.6	5.1	nA
		$V_{CM} = V^-$ (Note 4)			0.6	5.1	nA
A_{VOL}	Large-Signal Voltage Gain	V_O = ±4.25V, R_L = 10k		250	450		V/mV
	Channel Separation	V_O = ±4.25V, R_L = 10k		120	130		dB
SR	Slew Rate	A_V = –1, R_L = ∞		0.018	0.04		V/µs
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to V^+		88	102		dB
	CMRR Match (Channel-to-Channel)	$V_{CM} = V^-$ to V^+ (Note 4)		82	99		dB
V_{OL}	Output Voltage Swing LOW	No Load			V^- + 0.032	V^- + 0.060	V
		I_{SINK} = 0.5mA			V^- + 0.135	V^- + 0.270	V
		I_{SINK} = 2.5mA			V^- + 0.235	V^- + 0.470	V
V_{OH}	Output Voltage Swing HIGH	No Load		V^+ – 0.052	V^+ – 0.026		V
		I_{SOURCE} = 0.5mA		V^+ – 0.270	V^+ – 0.135		V
		I_{SOURCE} = 2.5mA		V^+ – 0.570	V^+ – 0.265		V
I_{SC}	Short-Circuit Current			10	18		mA
I_S	Supply Current per Amplifier				70	80	µA
GBW	Gain Bandwidth Product	f = 1kHz			120		kHz

0°C ≤ T_A ≤ 70°C, V_S = ±5V, V_{CM} = V_O = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$	●		150	660	µV
		$V_{CM} = V^-$	●		150	660	µV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+	●		90	500	µV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^-$, V^+ (Notes 3, 4)	●		180	900	µV
I_B	Input Bias Current	$V_{CM} = V^+$	●		8	16	nA
		$V_{CM} = V^-$	●	–16	–8		nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^-$ to V^+	●		16	32	nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$	●		0.8	5.3	nA
		$V_{CM} = V^-$	●		0.6	5.3	nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+	●		0.9	7.5	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+$ (Note 4)	●		0.7	7.5	nA
		$V_{CM} = V^-$ (Note 4)	●		0.6	7.5	nA
A_{VOL}	Large-Signal Voltage Gain	V_O = ±4.25V, R_L = 10k	●	100	250		V/mV
	Channel Separation	V_O = ±4.25V, R_L = 10k	●	120	130		dB
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to V^+	●	86	101		dB
	CMRR Match (Channel-to-Channel)	$V_{CM} = V^-$ to V^+ (Note 4)	●	80	98		dB

ELECTRICAL CHARACTERISTICS

$0°C \le T_A \le 70°C$, $V_S = \pm 5V$, $V_{CM} = V_O = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Output Voltage Swing LOW	No Load	●		$V^- + 0.042$	$V^- + 0.080$	V
		$I_{SINK} = 0.5mA$	●		$V^- + 0.150$	$V^- + 0.300$	V
		$I_{SINK} = 2.5mA$	●		$V^- + 0.270$	$V^- + 0.540$	V
V_{OH}	Output Voltage Swing HIGH	No Load	●	$V^+ - 0.065$	$V^+ - 0.033$		V
		$I_{SOURCE} = 0.5mA$	●	$V^+ - 0.305$	$V^+ - 0.155$		V
		$I_{SOURCE} = 2.5mA$	●	$V^+ - 0.620$	$V^+ - 0.310$		V
I_{SC}	Short-Circuit Current		●	7	18		mA
I_S	Supply Current per Amplifier		●		70	90	µA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: A heat sink may be required to keep the junction temperature below the Absolute Maximum Rating when the output is shorted indefinitely.

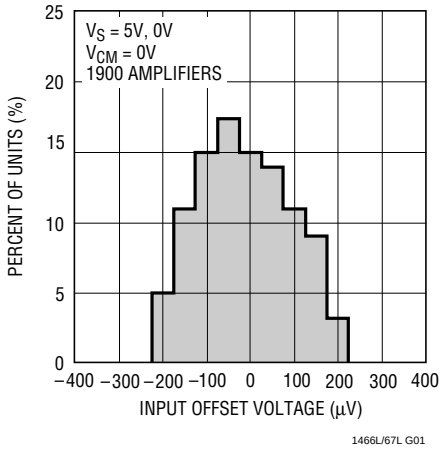
Note 2: This parameter is not 100% tested.

Note 3: Input offset match is the difference in offset voltage between amplifiers measured at both $V_{CM} = V^-$ and $V_{CM} = V^+$.

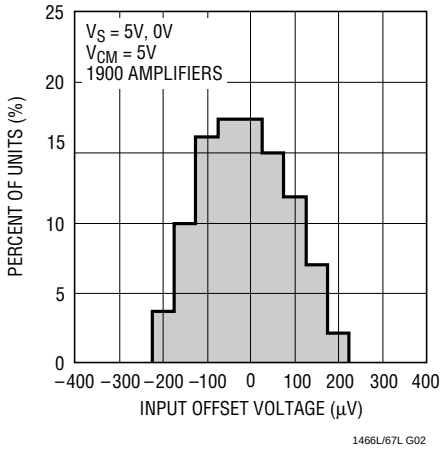
Note 4: Matching parameters are the difference between amplifiers A and D and between B and C.

TYPICAL PERFORMANCE CHARACTERISTICS

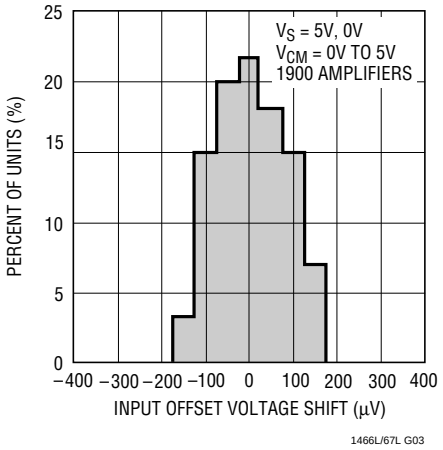
V_{OS} Distribution, $V_{CM} = 0V$



V_{OS} Distribution, $V_{CM} = 5V$

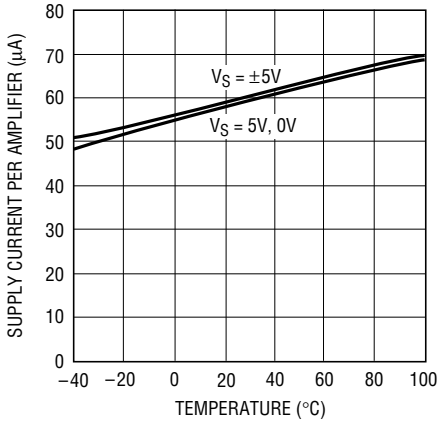


V_{OS} Shift, $V_{CM} = 0V$ to $5V$



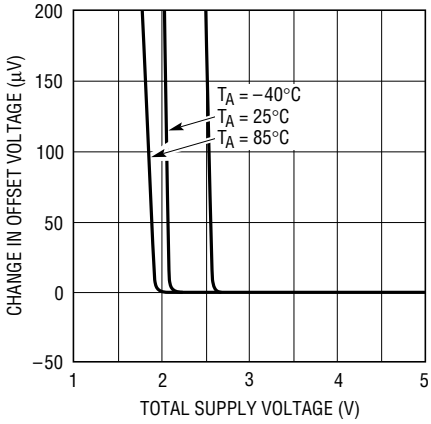
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Temperature



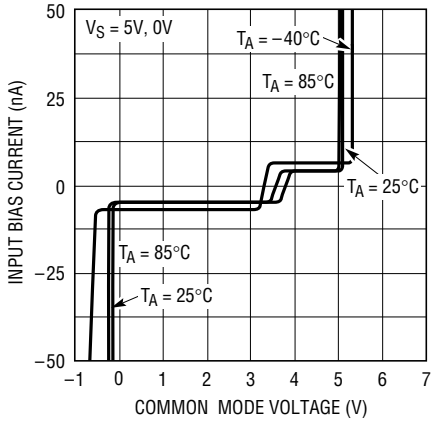
1466L/67L G04

Minimum Supply Voltage



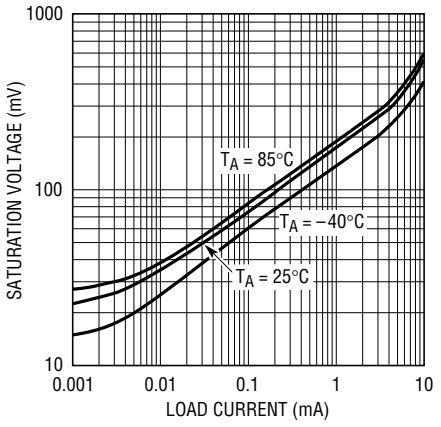
1466L/67L G05

Input Bias Current vs Common Mode Voltage



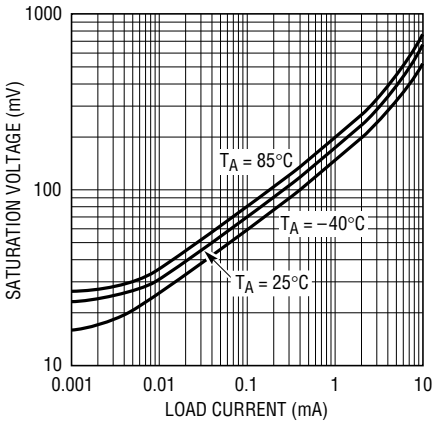
1466L/67L G06

Output Saturation Voltage vs Load Current (Output Low)



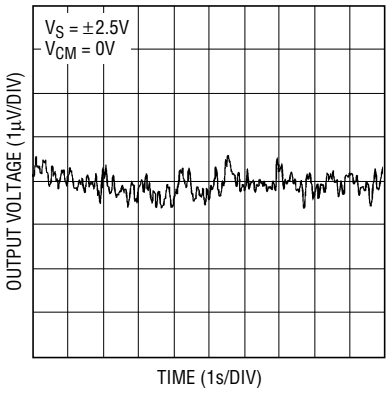
1466L/67L G07

Output Saturation Voltage vs Load Current (Output High)



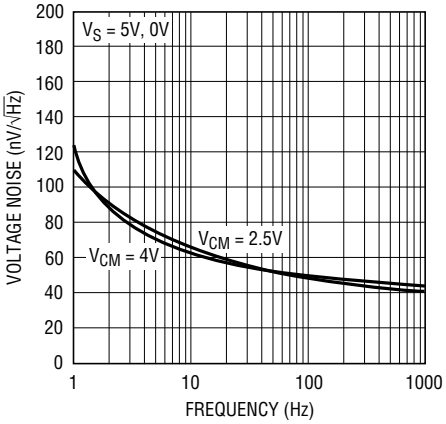
1466L/67L G08

0.1Hz to 10Hz Output Voltage Noise



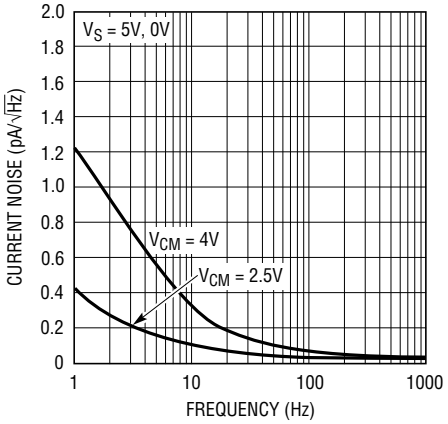
1466L/67L G09

Voltage Noise Spectrum



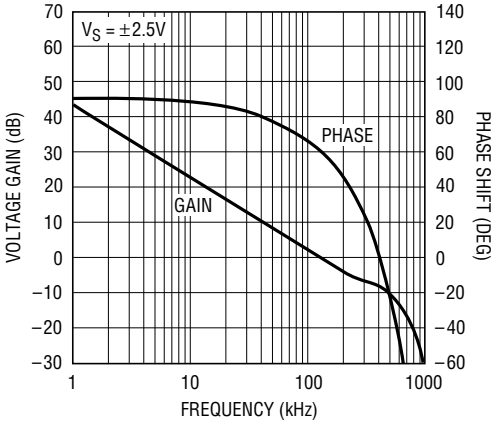
1466L/67L G10

Current Noise Spectrum



1466L/67L G11

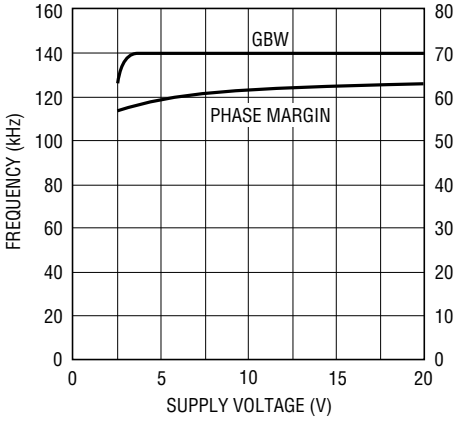
Gain and Phase Shift vs Frequency



1466L/67L G12

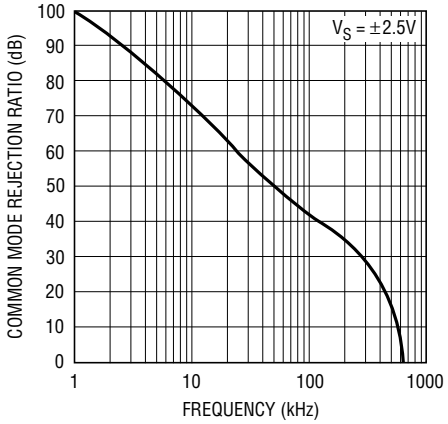
TYPICAL PERFORMANCE CHARACTERISTICS

Gain Bandwidth and Phase Margin vs Supply Voltage



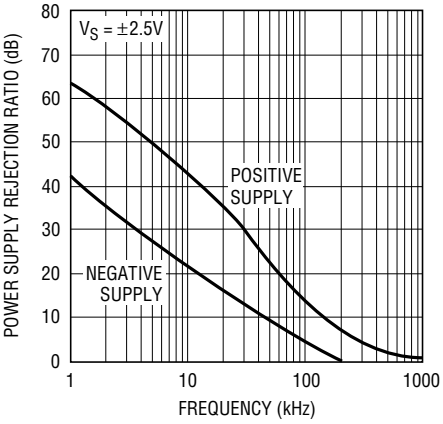
1466L/67L G13

Common Mode Rejection Ratio vs Frequency



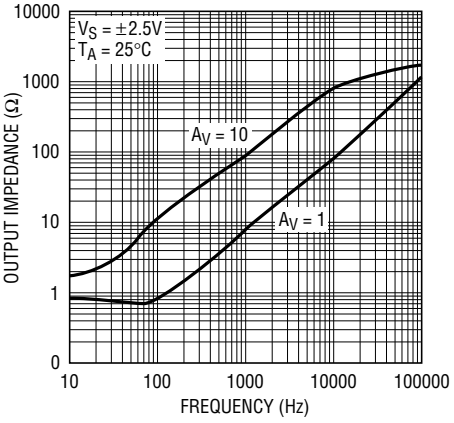
1466L/67L G14

Power Supply Rejection Ratio vs Frequency



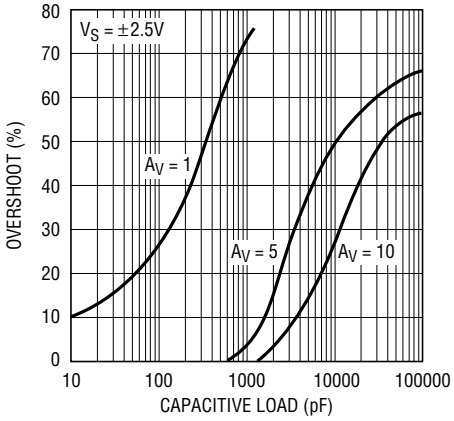
1466L/67L G15

Closed-Loop Output Impedance vs Frequency



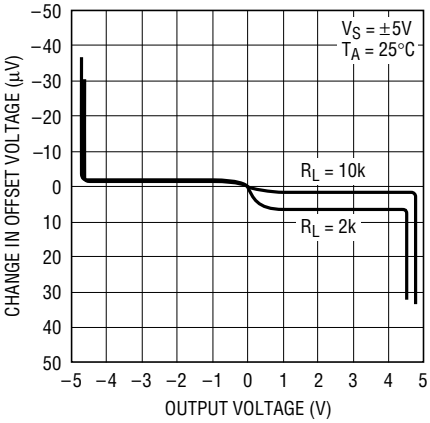
1466L/67 G16

Capacitive Load Handling



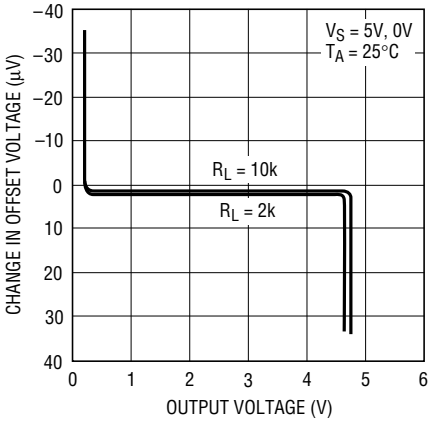
1466L/67L G17

Voltage Gain, $V_S = \pm 5V$



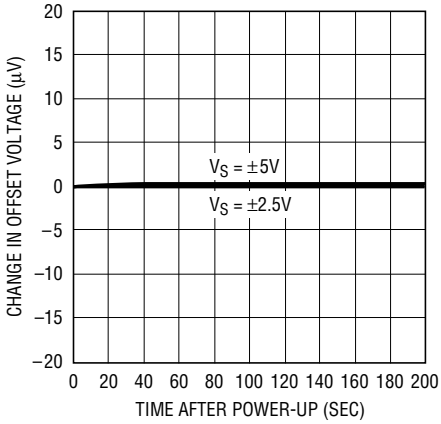
1466L/67L G18

Voltage Gain, $V_S = 5V, 0V$



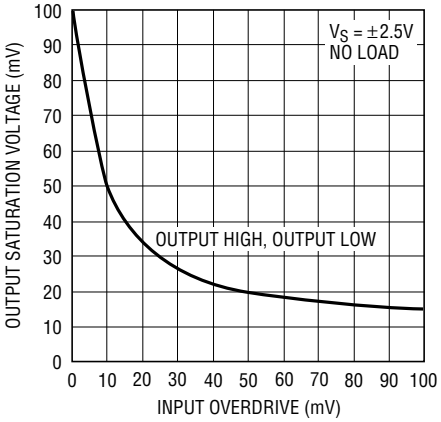
1466L/67L G19

Input Offset Drift vs Time



1466L/67L G20

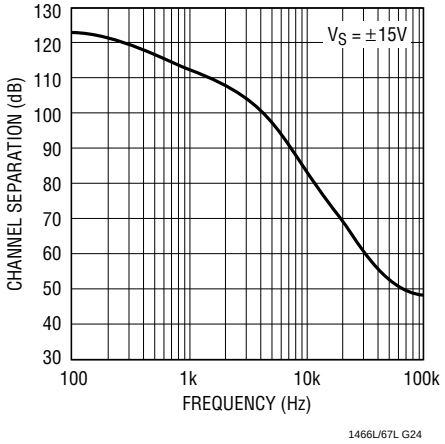
Output Saturation Voltage vs Input Overdrive



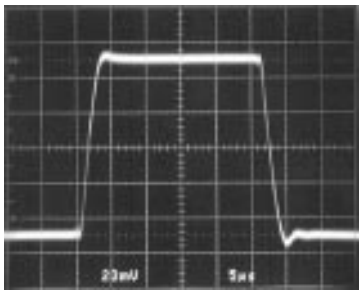
1466L/67/ G21

TYPICAL PERFORMANCE CHARACTERISTICS

Channel Separation vs Frequency

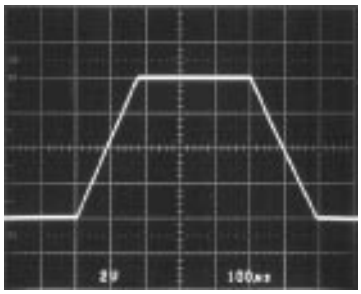


Small-Signal Response
$V_S = \pm 2.5V$



$V_S = \pm 2.5V$
$A_V = 1$

Large-Signal Response
$V_S = \pm 5V$



$V_S = \pm 5V$
$A_V = 1$

APPLICATIONS INFORMATION

Rail-to-Rail Operation

The LT1466L/LT1467L differ from conventional op amps in the design of both the input and output stages. Figure 1 shows a simplified schematic. The input stage consists of two differential amplifiers, a PNP stage Q1-Q2 and an NPN stage Q3-Q4, that are active over different portions of the input common mode range. Each input stage is trimmed for offset voltage. A complementary output configuration (Q12-Q13) is employed to create an output stage with rail-to-rail swing. The devices are fabricated on Linear Technology's proprietary complementary bipolar process, which ensures very similar DC and AC characteristics for the output devices Q12 and Q13.

First, looking at the input stage, Q5 switches the current from current source I_1 between the two input stages. When the input common mode voltage V_{CM} is near the negative supply, Q5 is reverse biased, so the current from I_1 becomes the tail current for the PNP differential pair Q1-Q2. At the other extreme, when V_{CM} is near the positive supply, the PNPs Q1-Q2 are biased off. The current from

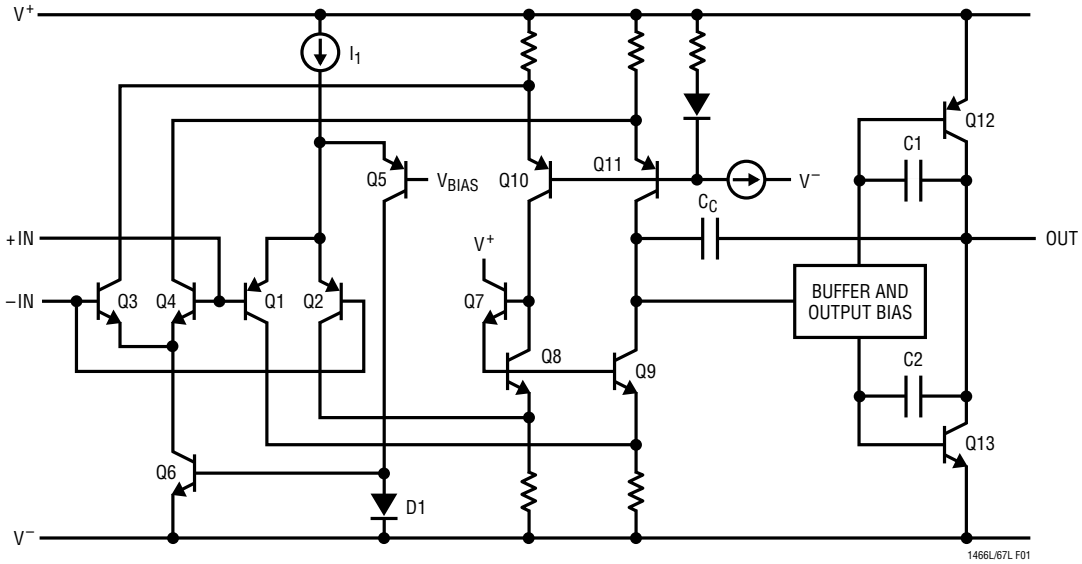


Figure 1. Simplified Schematic

APPLICATIONS INFORMATION

I_1 then flows through Q5 to the current mirror D3-Q6, furnishing the tail current for the NPN differential pair Q3-Q4. The switchover point between stages occurs when V_{CM} is equal to the base voltage of Q5, which is biased approximately 1.3V below the positive supply.

The collector currents of the two input pairs are combined in the second stage, consisting of Q7-Q11. Most of the voltage gain in the amplifier is contained in this stage. The output of the second stage is buffered and applied to the output devices Q12 and Q13. Capacitors C1 and C2 form local feedback loops around the output devices, lowering the output impedance at high frequencies. Capacitor C_C sets the amplifier bandwidth.

Input Offset Voltage

Since the amplifier has two input stages, the input offset voltage changes depending upon which stage is active. When the amplifier switches between stages, the offset voltage may go up, down or remain flat. Both stages of the LT1466L/LT1467L are trimmed; one at the negative supply and the other at the positive supply. The resulting common mode rejection ratio of 83dB minimum is much better than typical rail-to-rail amplifiers.

Overdrive Protection

The LT1466L/LT1467L contain circuits that prevent the output from reversing polarity when the input voltage exceeds either supply. For these circuits to work properly, the input current should be limited to –10mA when the input is below the negative supply, and 0.5mA when the input is above the positive supply. If the amplifier is to be severely overdriven, an external resistor should be used to limit the current.

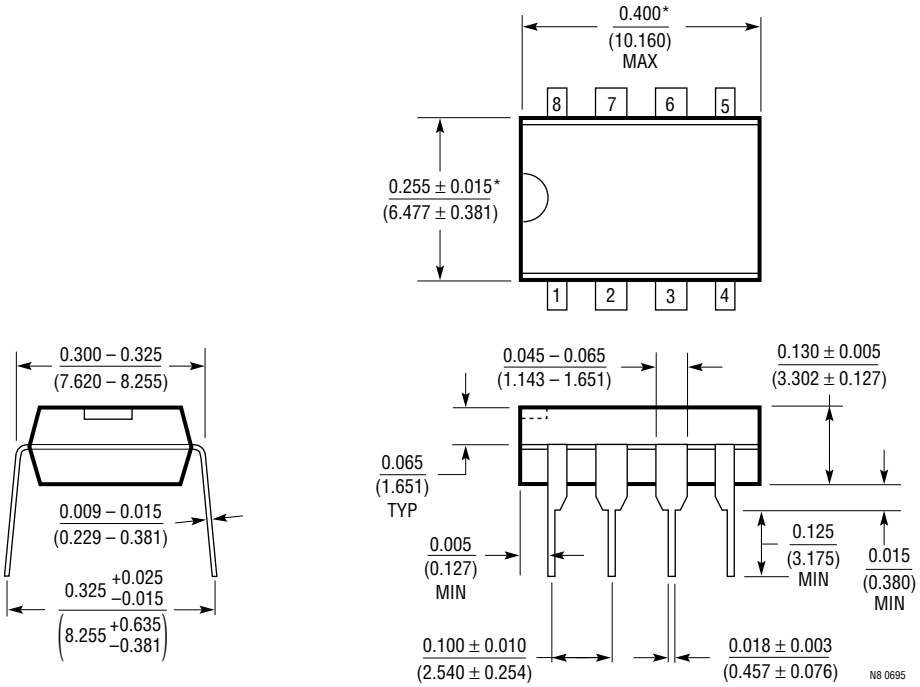
Output

The output voltage swing and current sinking capability of the LT1466L/LT1467L are affected by input overdrive as shown in the Typical Performance Characteristics. When monitoring voltages within 100mV of either rail, gain should be taken to keep the output from clipping.

PACKAGE DESCRIPTION

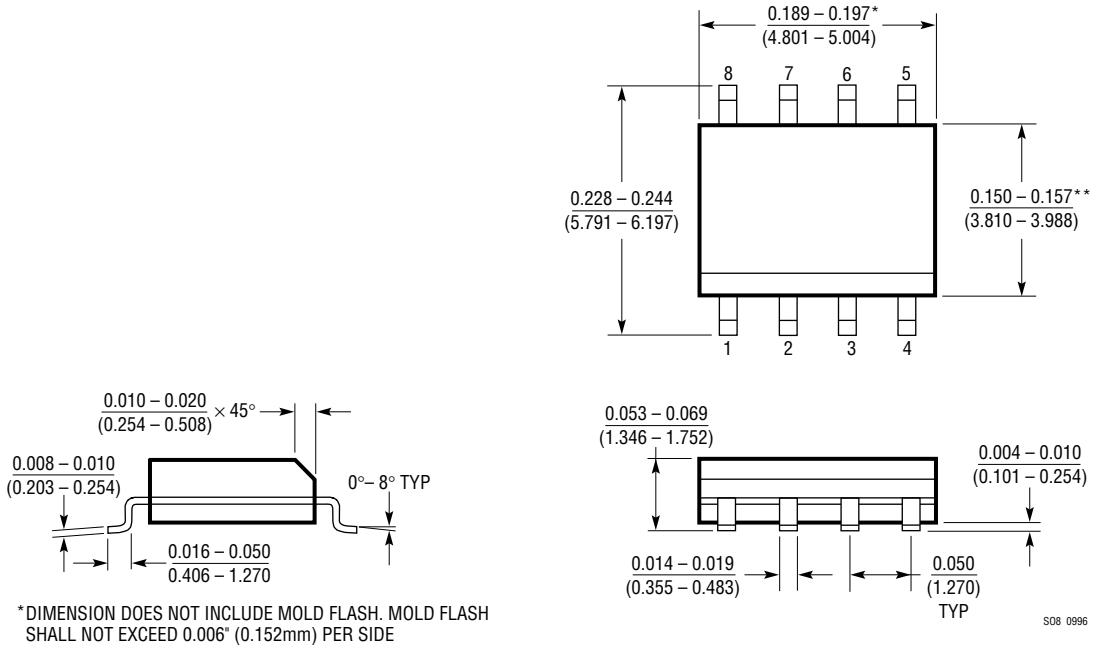
Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



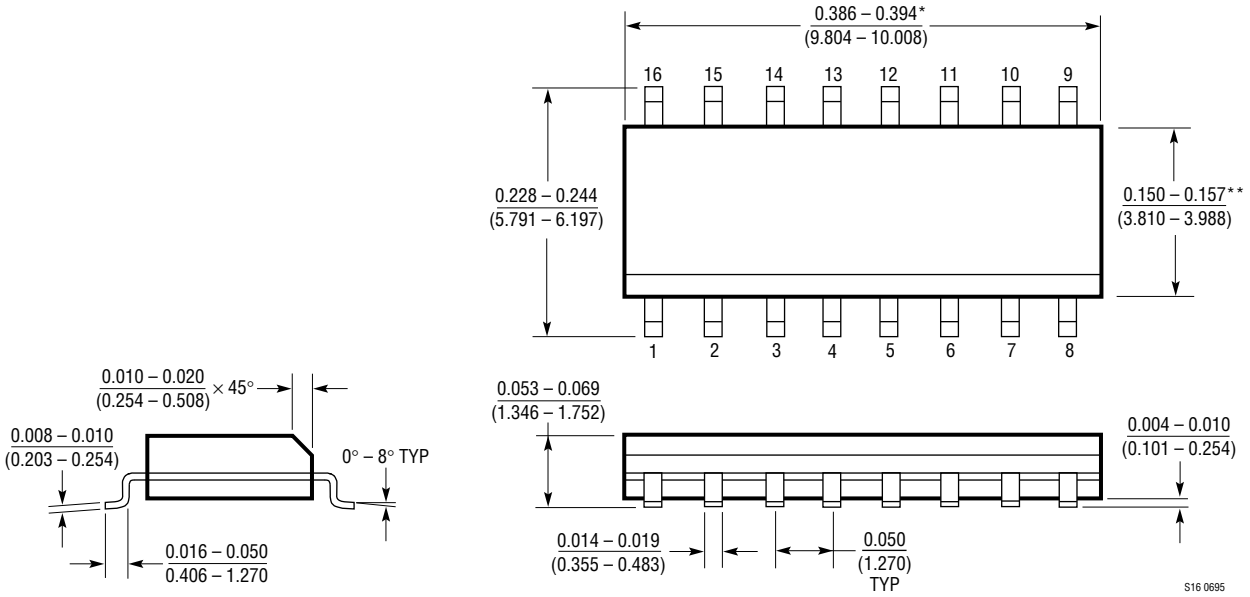
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE