

FEATURES

- Stable in Gain $A_V \geq 2$ ($A_V = -1$)
- 200MHz Gain Bandwidth Product
- 30V/ μ s Slew Rate
- Settling Time: 800ns (10V Step, 150 μ V)
- Specified at $\pm 5V$ and $\pm 15V$ Supplies
- Low Distortion, $-96.5dB$ for 100kHz, 10V_{P-P}
- Maximum Input Offset Voltage: 75 μ V
- Maximum Input Offset Voltage Drift: 2 μ V/ $^{\circ}C$
- Maximum (-) Input Bias Current: 10nA
- Minimum DC Gain: 1000V/mV
- Minimum Output Swing into 2k: $\pm 12.8V$
- Input Noise Voltage: 5nV/ \sqrt{Hz}
- Input Noise Current: 0.6pA/ \sqrt{Hz}
- Total Input Noise Optimized for $1k < R_S < 20k$
- Available in an 8-Lead Plastic SO Package and 8-Lead DFN Package

APPLICATIONS

- 16-Bit DAC Current-to-Voltage Converter
- Precision Instrumentation
- ADC Buffer
- Low Distortion Active Filters
- High Accuracy Data Acquisition Systems
- Photodiode Amplifiers

DESCRIPTION

The LT[®]1468-2 is a precision high speed operational amplifier with 16-bit accuracy, decompensated to be stable in a gain of 2 or greater. The combination of precision and AC performance makes the LT1468-2 the optimum choice for high accuracy applications such as DAC current-to-voltage conversion and ADC buffers. The initial accuracy and drift characteristics of the input offset voltage and inverting input bias current are tailored for inverting applications.

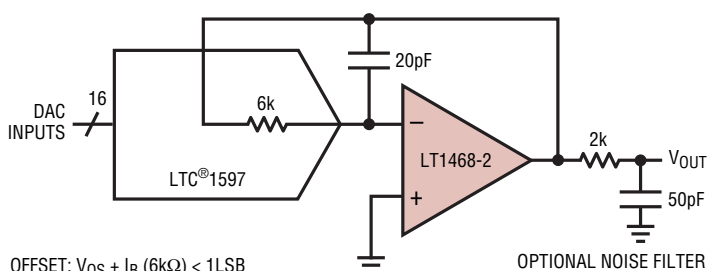
The 200MHz gain bandwidth ensures high open-loop gain at frequency for reducing distortion. In noninverting applications such as an ADC buffer, the low distortion and DC accuracy allow full 16-bit AC and DC performance. The high slew rate of the LT1468-2 improves large-signal performance in applications such as active filters and instrumentation amplifiers compared to other precision op amps.

The LT1468-2 is specified on power supply voltages of $\pm 5V$ and $\pm 15V$ and from $-40^{\circ}C$ to $85^{\circ}C$. For a unity-gain stable op amp with same DC performance, see the LT1468 data sheet.

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TYPICAL APPLICATION

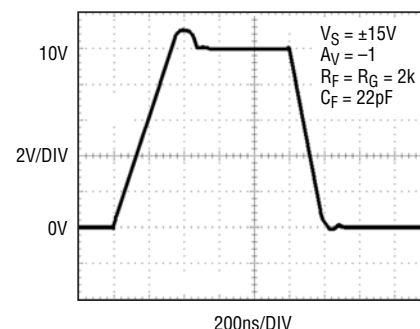
16-Bit DAC I-to-V Converter



OFFSET: $V_{OS} + I_B(6k\Omega) < 1LSB$
 SETTLE TIME TO 150 μ V = 1.6 μ s
 SETTLE TIME LIMITED BY 6k AND 20pF TO COMPENSATE DAC OUTPUT CAPACITANCE

14682 TA01

Large Signal Transient, $A_V = -1$



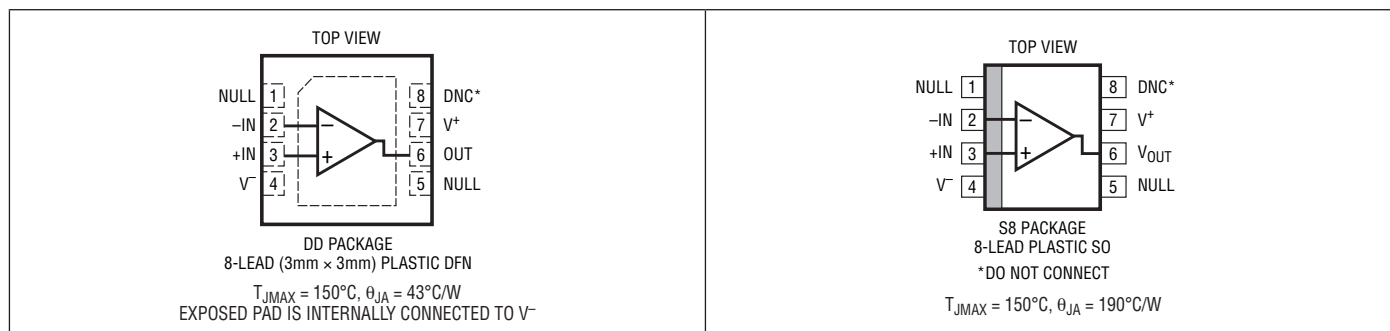
14682 TA02

LT1468-2

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-).....	36V	Specified Temperature Range (Note 4)	-40°C to 85°C
Maximum Input Current (Note 2).....	10mA	Junction Temperature	150°C
Output Short-Circuit Duration (Note 3)	Indefinite	Storage Temperature.....	-65°C to 150°C
Operating Temperature Range	-40°C to 85°C	Lead Temperature (Soldering, 10 sec) for S8 Only.....	300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1468CS8-2#PBF	LT1468CS8-2#TRPBF	14682	8-Lead Plastic Small Outline	0°C to 70°C
LT1468IS8-2#PBF	LT1468IS8-2#TRPBF	14682	8-Lead Plastic Small Outline	-40°C to 85°C
LT1468ACDD-2#PBF	LT1468ACDD-2#TRPBF	LDSY	8-Lead (3mm \times 3mm) Plastic DFN	0°C to 70°C
LT1468AIDD-2#PBF	LT1468AIDD-2#TRPBF	LDSY	8-Lead (3mm \times 3mm) Plastic DFN	-40°C to 85°C
LT1468CDD-2#PBF	LT1468CDD-2#TRPBF	LDSY	8-Lead (3mm \times 3mm) Plastic DFN	0°C to 70°C
LT1468IDD-2#PBF	LT1468IDD-2#TRPBF	LDSY	8-Lead (3mm \times 3mm) Plastic DFN	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	S8 Package	$\pm 15\text{V}$	30	75	μV	
			$\pm 5\text{V}$	50	175	μV	
		LT1468A, DD Package	$\pm 15\text{V}$	30	75	μV	
			$\pm 5\text{V}$	50	175	μV	
		LT1468, DD Package	$\pm 15\text{V}$	100	200	μV	
			$\pm 5\text{V}$	150	300	μV	
I_{OS}	Input Offset Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	13	50	nA	

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ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
I_{B^-}	Inverting Input Bias Current		$\pm 5\text{V}$ to $\pm 15\text{V}$			3	± 10	nA
I_{B^+}	Noninverting Input Bias Current		$\pm 5\text{V}$ to $\pm 15\text{V}$			-10	± 40	nA
	Input Noise Voltage	0.1Hz to 10Hz	$\pm 5\text{V}$ to $\pm 15\text{V}$			0.3		μV_{P-P}
e_n	Input Noise Voltage	$f = 10\text{kHz}$	$\pm 5\text{V}$ to $\pm 15\text{V}$			5		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Voltage	$f = 10\text{kHz}$	$\pm 5\text{V}$ to $\pm 15\text{V}$			0.6		$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	$V_{CM} = \pm 12.5\text{V}$ Differential	$\pm 15\text{V}$ $\pm 15\text{V}$		100 50	240 150		$\text{M}\Omega$ $\text{k}\Omega$
C_{IN}	Input Capacitance		$\pm 15\text{V}$			4		pF
	Input Voltage Range +		$\pm 15\text{V}$ $\pm 5\text{V}$		12.5 2.5	13.5 3.5		V V
	Input Voltage Range -		$\pm 15\text{V}$ $\pm 5\text{V}$			-14.3 -4.3	-12.5 -2.5	V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12.5\text{V}$	$\pm 15\text{V}$		96	110		dB
		$V_{CM} = \pm 2.5\text{V}$	$\pm 5\text{V}$		96	112		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5\text{V}$ to $\pm 15\text{V}$			100	112		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12.5\text{V}$, $R_L = 10\text{k}$	$\pm 15\text{V}$		1000	9000		V/mV
		$V_{OUT} = \pm 12.5\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$		500	5000		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 10\text{k}$	$\pm 5\text{V}$		1000	6000		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 5\text{V}$		500	3000		V/mV
V_{OUT}	Output Swing	$R_L = 10\text{k}$	$\pm 15\text{V}$		± 13.0	± 13.6		V
		$R_L = 2\text{k}$	$\pm 15\text{V}$		± 12.8	± 13.5		V
		$R_L = 10\text{k}$	$\pm 5\text{V}$		± 3.0	± 3.6		V
		$R_L = 2\text{k}$	$\pm 5\text{V}$		± 2.8	± 3.5		V
I_{OUT}	Output Current	$V_{OUT} = \pm 12.5\text{V}$	$\pm 15\text{V}$		± 15	± 22		mA
		$V_{OUT} = \pm 2.5\text{V}$	$\pm 5\text{V}$		± 15	± 22		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 0.2\text{V}$	$\pm 15\text{V}$		± 25	± 40		mA
SR	Slew Rate	$R_L = 2\text{k}$ (Note 5)	$\pm 15\text{V}$ $\pm 5\text{V}$		20 15	30 22		$\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$
	Full-Power Bandwidth	10V Peak, (Note 6) 3V Peak, (Note 6)	$\pm 15\text{V}$ $\pm 5\text{V}$			475 1160		kHz kHz
GBW	Gain Bandwidth	$f = 100\text{kHz}$, $R_L = 2\text{k}$	$\pm 15\text{V}$		140	200		MHz
			$\pm 5\text{V}$		130	190		MHz
t_s	Settling Time	10V Step, 0.01%, $A_V = -1$	$\pm 15\text{V}$			650		ns
		10V Step, $150\mu\text{V}$, $A_V = -1$	$\pm 15\text{V}$			800		ns
		5V Step, 0.01%, $A_V = -1$	$\pm 5\text{V}$			550		ns
R_O	Output Resistance	$A_V = -1$, $f = 100\text{kHz}$	$\pm 15\text{V}$			0.02		Ω
I_S	Supply Current		$\pm 15\text{V}$			3.9	5.2	mA
			$\pm 5\text{V}$			3.6	5.0	mA

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	S8 Package	$\pm 15\text{V}$	●			150	μV
			$\pm 5\text{V}$	●			250	μV
		LT1468A, DD Package	$\pm 15\text{V}$	●			150	μV
			$\pm 5\text{V}$	●			250	μV
LT1468, DD Package	$\pm 15\text{V}$	●			300	μV		
	$\pm 5\text{V}$	●			400	μV		

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
	Input V_{OS} Drift	(Note 7)	$\pm 5\text{V}$ to $\pm 15\text{V}$	●		0.7	2.0	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			65	nA
	Input Offset Current Drift		$\pm 5\text{V}$ to $\pm 15\text{V}$			60		$\text{pA}/^\circ\text{C}$
I_{B^-}	Inverting Input Bias Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			± 15	nA
	Negative Input Current Drift		$\pm 5\text{V}$ to $\pm 15\text{V}$			40		$\text{pA}/^\circ\text{C}$
I_{B^+}	Noninverting Input Bias Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			± 50	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12.5\text{V}$ $V_{CM} = \pm 2.5\text{V}$	$\pm 15\text{V}$ $\pm 5\text{V}$	● ●	94 94			dB dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5\text{V}$ to $\pm 15\text{V}$		●	98			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12.5\text{V}$, $R_L = 10\text{k}$ $V_{OUT} = \pm 12.5\text{V}$, $R_L = 2\text{k}$ $V_{OUT} = \pm 2.5\text{V}$, $R_L = 10\text{k}$ $V_{OUT} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$ $\pm 15\text{V}$ $\pm 5\text{V}$ $\pm 5\text{V}$	● ● ● ●	500 250 500 250			V/mV V/mV V/mV V/mV
V_{OUT}	Output Swing	$R_L = 10\text{k}$ $R_L = 2\text{k}$ $R_L = 10\text{k}$ $R_L = 2\text{k}$	$\pm 15\text{V}$ $\pm 15\text{V}$ $\pm 5\text{V}$ $\pm 5\text{V}$	● ● ● ●	± 12.9 ± 12.7 ± 2.9 ± 2.7			V V V V
I_{OUT}	Output Current	$V_{OUT} = \pm 12.5\text{V}$ $V_{OUT} = \pm 2.5\text{V}$	$\pm 15\text{V}$ $\pm 5\text{V}$	● ●	± 12.5 ± 12.5			mA mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 0.2\text{V}$	$\pm 15\text{V}$	●	± 17			mA
SR	Slew Rate	$R_L = 2\text{k}$ (Note 5)	$\pm 15\text{V}$ $\pm 5\text{V}$	● ●	18 13			V/ μs V/ μs
GBW	Gain Bandwidth	$f = 100\text{kHz}$, $R_L = 2\text{k}$	$\pm 15\text{V}$ $\pm 5\text{V}$	● ●	130 120	200 190		MHz MHz
I_S	Supply Current		$\pm 15\text{V}$ $\pm 5\text{V}$	● ●			6.5 6.3	mA mA

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	S8 Package	$\pm 15\text{V}$ $\pm 5\text{V}$	● ●			230 330	μV μV
		LT1468A, DD Package	$\pm 15\text{V}$ $\pm 5\text{V}$	● ●			230 330	μV μV
		LT1468, DD Package	$\pm 15\text{V}$ $\pm 5\text{V}$	● ●			400 500	μV μV
	Input V_{OS} Drift	(Note 7)	$\pm 5\text{V}$ to $\pm 15\text{V}$	●		0.7	2.5	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			80	nA
	Input Offset Current Drift		$\pm 5\text{V}$ to $\pm 15\text{V}$			120		$\text{pA}/^\circ\text{C}$
I_{B^-}	Inverting Input Bias Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			± 30	nA
	Negative Input Current Drift		$\pm 5\text{V}$ to $\pm 15\text{V}$			80		$\text{pA}/^\circ\text{C}$
I_{B^+}	Noninverting Input Bias Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●			± 60	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12.5\text{V}$ $V_{CM} = \pm 2.5\text{V}$	$\pm 15\text{V}$ $\pm 5\text{V}$	● ●	92 92			dB dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5\text{V}$ to $\pm 15\text{V}$		●	96			dB

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$, $R_L = 10\text{k}$	$\pm 15\text{V}$	●	300		V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	●	150		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 10\text{k}$	$\pm 5\text{V}$	●	300		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 5\text{V}$	●	150		V/mV
V_{OUT}	Output Swing	$R_L = 10\text{k}$	$\pm 15\text{V}$	●	± 12.8		V
		$R_L = 2\text{k}$	$\pm 15\text{V}$	●	± 12.6		V
		$R_L = 10\text{k}$	$\pm 5\text{V}$	●	± 2.8		V
		$R_L = 2\text{k}$	$\pm 5\text{V}$	●	± 2.6		V
I_{OUT}	Output Current	$V_{OUT} = \pm 12.5\text{V}$	$\pm 15\text{V}$	●	± 7		mA
		$V_{OUT} = \pm 2.5\text{V}$	$\pm 5\text{V}$	●	± 7		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 0.2\text{V}$	$\pm 15\text{V}$	●	± 12		mA
SR	Slew Rate	$R_L = 2\text{k}$ (Note 5)	$\pm 15\text{V}$	●	15		V/ μs
			$\pm 5\text{V}$	●	11		V/ μs
GBW	Gain Bandwidth	$f = 100\text{kHz}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	●	110	200	MHz
			$\pm 5\text{V}$	●	100	190	MHz
I_S	Supply Current		$\pm 15\text{V}$	●		7.0	mA
			$\pm 5\text{V}$	●		6.8	mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by back-to-back diodes and two 100 Ω series resistors. If the differential input voltage exceeds 0.7V, the input current should be limited to 10mA. Input voltages outside the supplies will be clamped by ESD protection devices and input currents should also be limited to 10mA.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: The LT1468C-2 is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet these extended temperature limits, but is not tested at -40°C and at 85°C. The LT1468I-2 is guaranteed to meet the extended temperature limits.

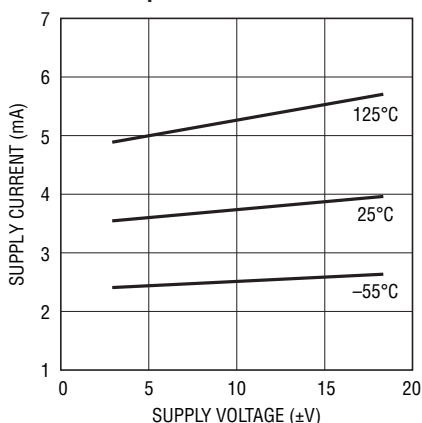
Note 5: Slew rate is measured between $\pm 8\text{V}$ on the output with $\pm 12\text{V}$ input for $\pm 15\text{V}$ supplies and $\pm 2\text{V}$ on the output with $\pm 3\text{V}$ input for $\pm 5\text{V}$ supplies.

Note 6: Full power bandwidth is calculated from the slew rate measurement: $\text{FPBW} = \text{SR}/2\pi V_P$

Note 7: This parameter is not 100% tested.

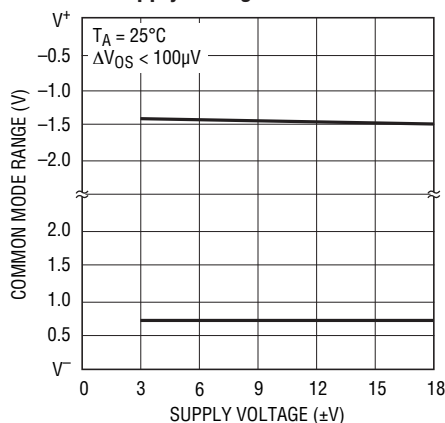
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage and Temperature



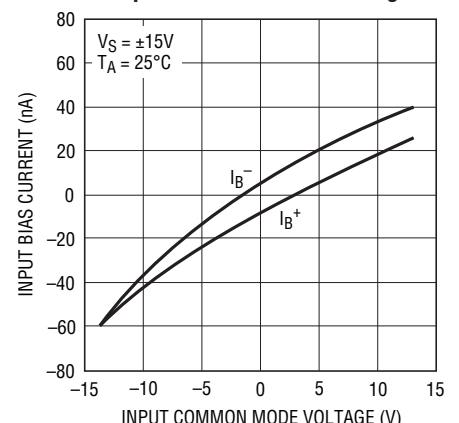
14682 G01

Input Common Mode Range vs Supply Voltage



14682 G02

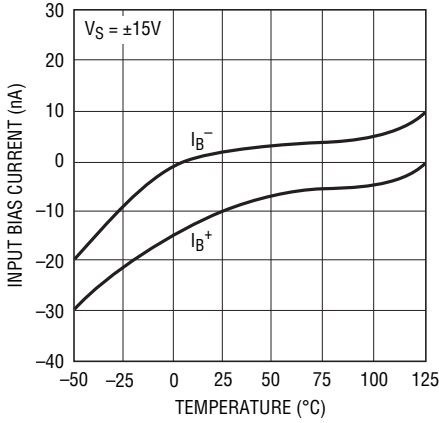
Input Bias Current vs Input Common Mode Voltage



14682 G03

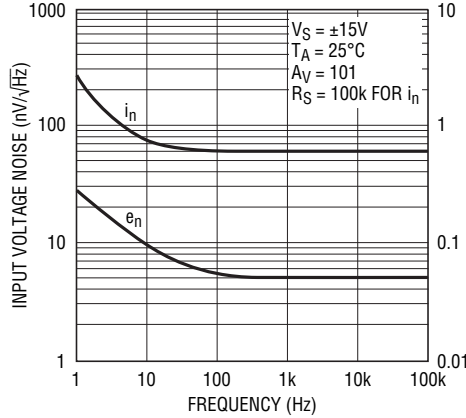
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Temperature



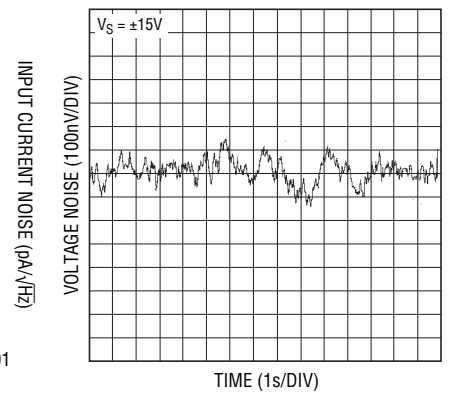
14682 G04

Input Noise Spectral Density



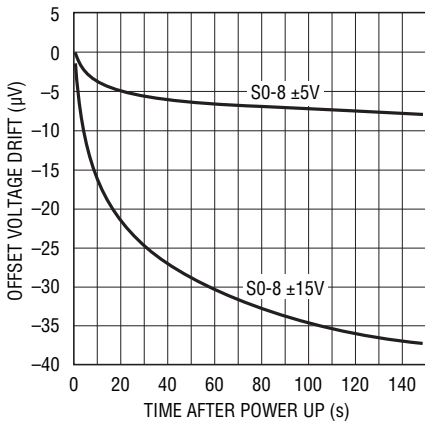
14682 G05

0.1Hz to 10Hz Voltage Noise



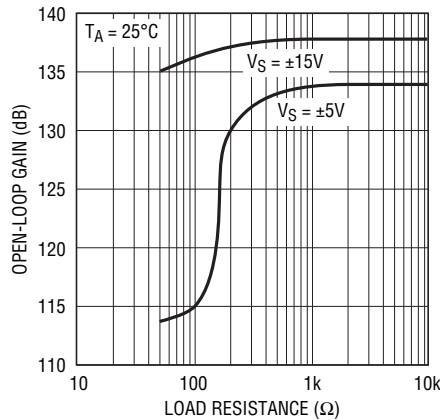
14682 G06

Warm-Up Drift vs Time



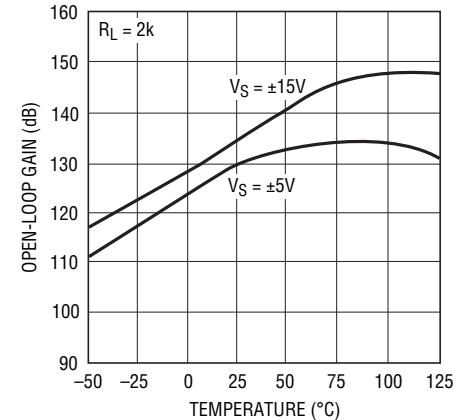
14682 G07

Open-Loop Gain vs Resistive Load



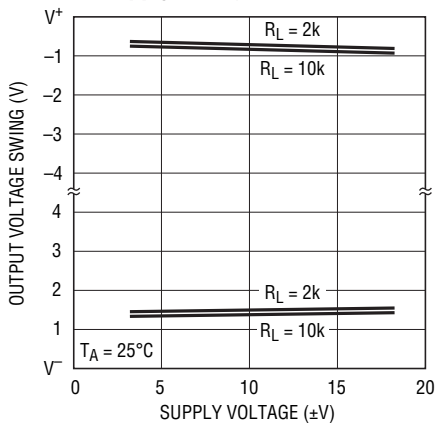
14682 G08

Open-Loop Gain vs Temperature



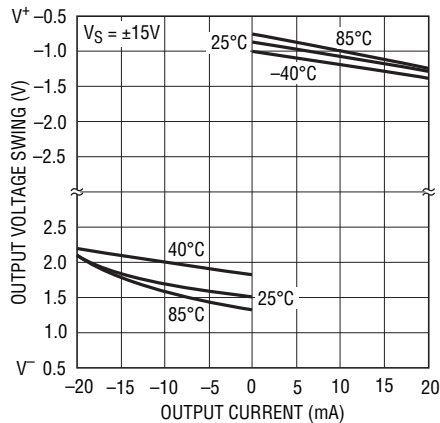
14682 G09

Output Voltage Swing vs Supply Voltage



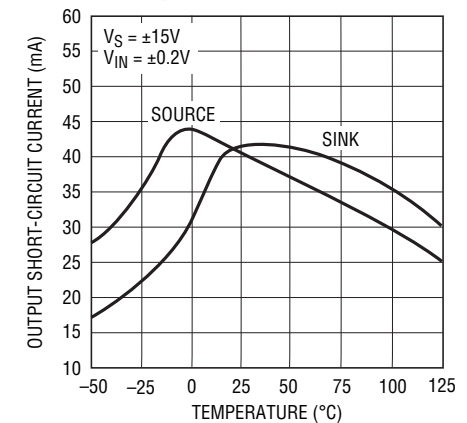
14682 G10

Output Voltage Swing vs Load Current



14682 G11

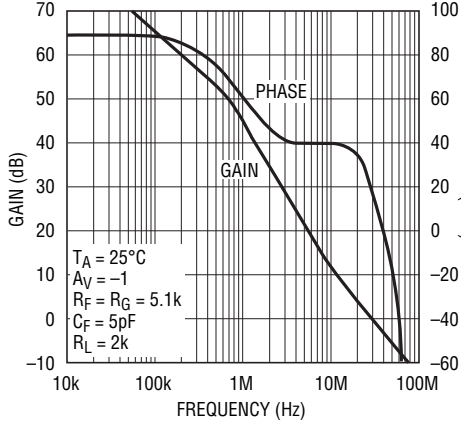
Output Short-Circuit Current vs Temperature



14682 G12

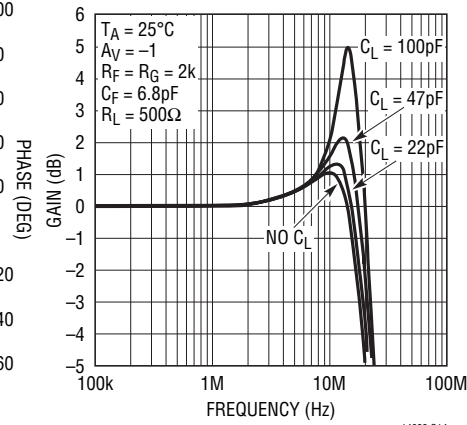
TYPICAL PERFORMANCE CHARACTERISTICS

Open-Loop Gain and Phase vs Frequency



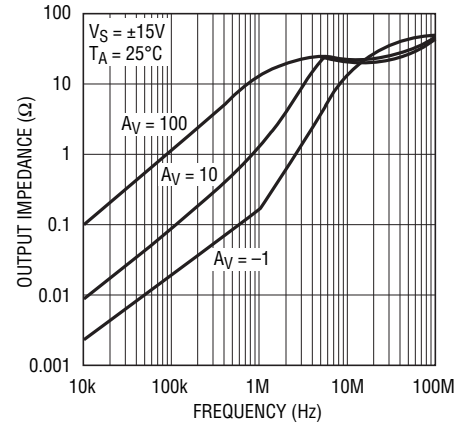
14682 G13

Gain vs Frequency, $A_V = -1$



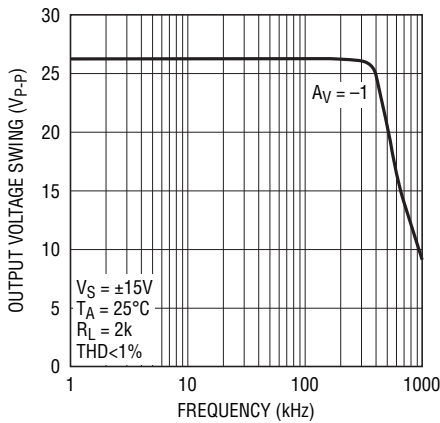
14682 G14

Output Impedance vs Frequency



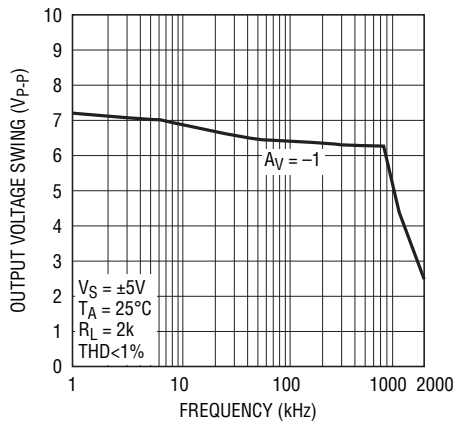
14682 G15

Undistorted Output Swing vs Frequency, $V_S = \pm 15V$



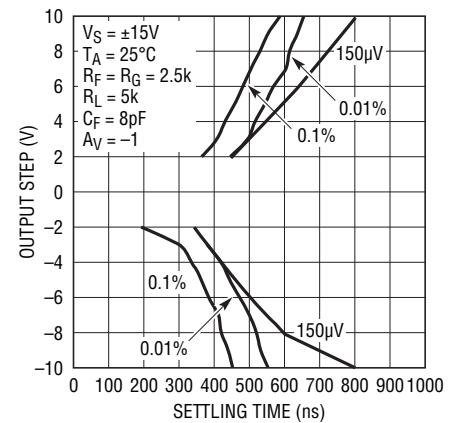
14682 G16

Undistorted Output Swing vs Frequency, $V_S = \pm 5V$



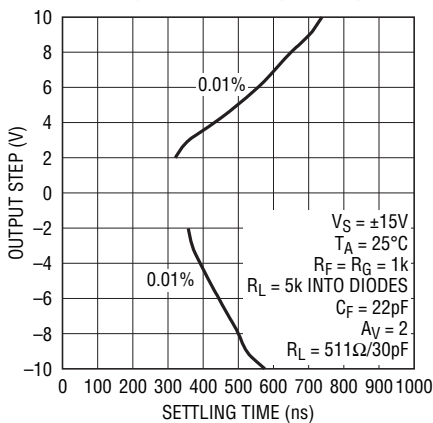
14682 G17

Settling Time vs Output Step



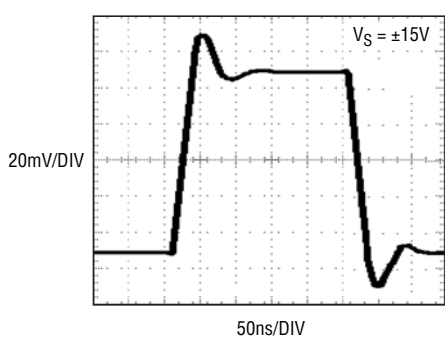
14682 G18

Settling Time vs Output Step



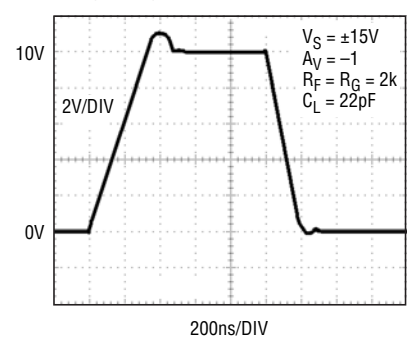
14682 G19

Small-Signal Transient, $A_V = -1$



14682 G20

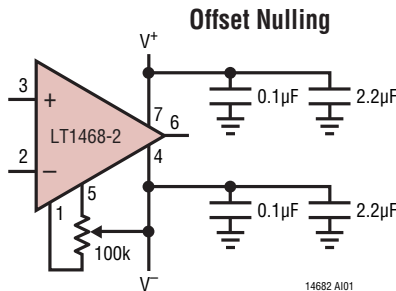
Large-Signal Transient, $A_V = -1$



14682 G21

APPLICATIONS INFORMATION

The LT1468-2 may be inserted directly into many operational amplifier applications improving both DC and AC performance, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1468-2 is shown below.



Gain of 2 Stable

The LT1468-2 is a decompensated version of the LT1468. The precision DC performance is identical, but the internal compensation capacitors have been reduced to a point where the op amp needs a gain of 2 or greater in order to be stable.

In general, for applications where the gain around the op amp is ≥ 2 , the decompensated version should be used, because it will give the best AC performance. In applications where the gain is < 2 , the unity-gain stable version should be used.

The appropriate way to define the ‘gain’ is as the inverse of the feedback ratio from output to differential input, including all relevant parasitics. Moreover, as with all feedback loops, the stability of the loop depends on the value of that feedback ratio at frequencies where the total loop-gain would cross unity. Therefore, it is possible to have circuits in which the gain at DC is lower than the gain at high frequency, and these circuits can be stable even with a non unity-gain stable op amp. An example is many current-output DAC buffer applications.

Layout and Passive Components

The LT1468 requires attention to detail in board layout in order to maximize DC and AC performance. For best AC results (for example fast settling time) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01µF to 0.1µF) in parallel with low ESR bypass capacitors (1µF to 10µF tantalum). For best DC performance, use “star” grounding techniques, equalize input trace lengths

and minimize leakage (i.e., 1.5GΩ of leakage between an input and a 15V supply will generate 10nA—equal to the maximum I_B^- specification.)

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs. For inverting configurations tie the ring to ground, in noninverting connections tie the ring to the inverting input (note the input capacitance will increase which may require a compensating capacitor as discussed below.)

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the inputs can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

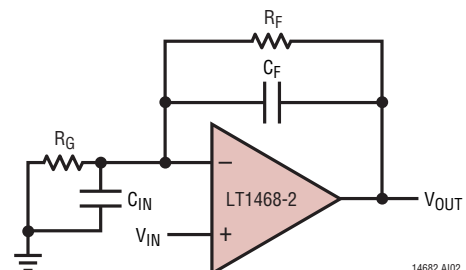
Make no connection to Pin 8. This pin is used for factory trim of the inverting input current.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole that can cause peaking or even oscillations. A feedback capacitor of the value:

$$C_F = (R_G)(C_{IN}/R_F)$$

may be used to cancel the input pole and optimize dynamic performance. For applications where the DC noise gain is one, and a large feedback resistor is used, C_F should be less than or equal to one half of C_{IN} . An example would be a DAC I-to-V converter as shown on the front page of this data sheet where the DAC can have many tens of pF of output capacitance.

Nulling Input Capacitance



APPLICATIONS INFORMATION

Input Considerations

Each input of the LT1468-2 is protected with a 100Ω series resistor and back-to-back diodes across the bases of the input devices. If the inputs can be pulled apart, the input current should be limited to less than 10mA with an external series resistor. Each input also has two ESD clamp diodes—one to each supply. If an input is driven above the supply, limit the current with an external resistor to less than 10mA.

The LT1468-2 employs bias current cancellation at the inputs. The inverting input current is trimmed at zero common mode voltage to minimize errors in inverting applications such as I-to-V converters. The noninverting input current is not trimmed and has a wider variation and therefore a larger maximum value. As the input offset current can be greater than either input current, the use of balanced source resistance is NOT recommended as it actually degrades DC accuracy and also increases noise.

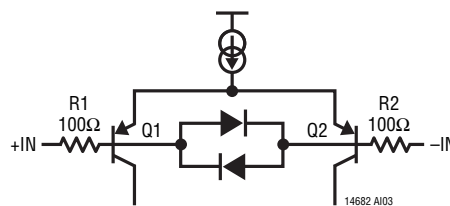
The input bias currents vary with common mode voltage as shown in the Typical Performance Characteristics. The cancellation circuitry was not designed to track this common mode voltage because the settling time would have been adversely affected.

The LT1468 inputs can be driven to the negative supply and to within 0.5V of the positive supply without phase reversal. As the input moves closer than 0.5V to the positive supply, the output reverses phase.

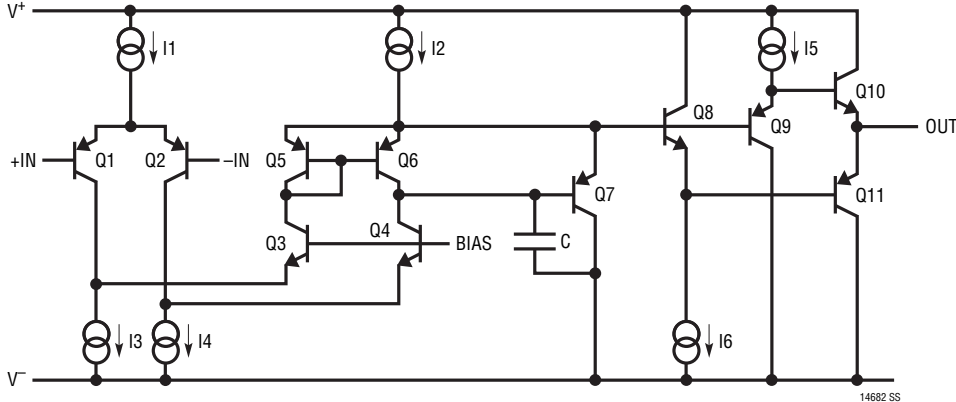
Total Input Noise

The curve of Total Noise vs Unmatched Source Resistance in the Typical Performance Characteristics shows that with source resistance below 1k, the voltage noise of the amplifier dominates. In the 1k to 20k region the increase in noise is due to the source resistance. Above 20k the input current noise component is larger than the resistor noise.

Input Stage Protection



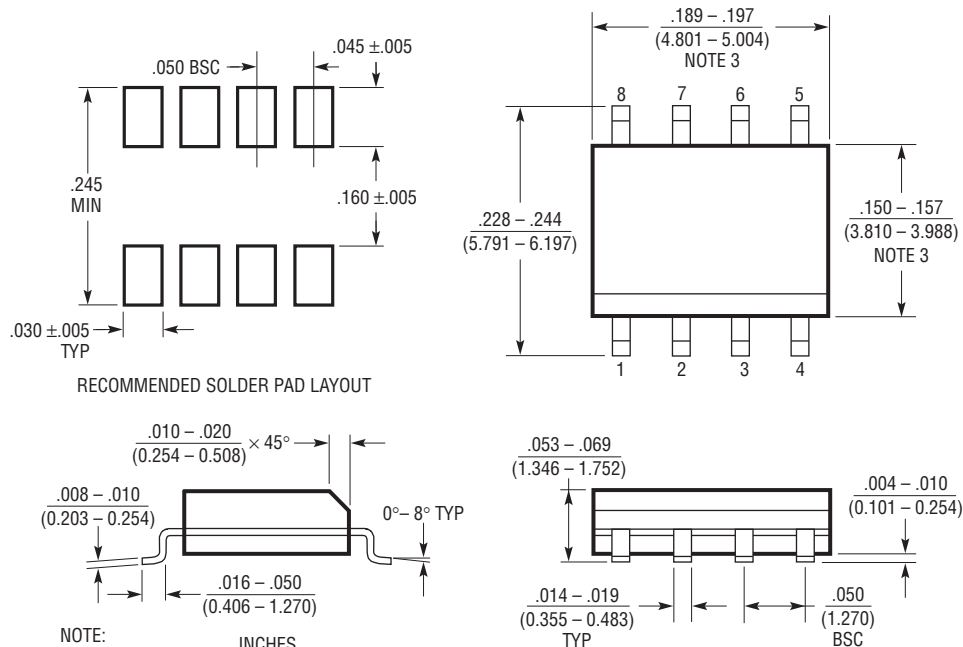
SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610 Rev G)



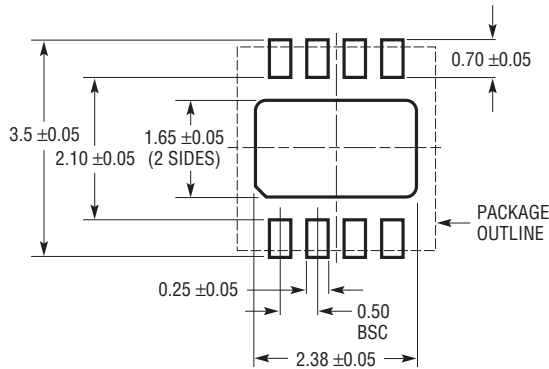
- NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
 2. DRAWING NOT TO SCALE
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED $.006''$ (0.15mm)
 4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

S08 REV G 0212

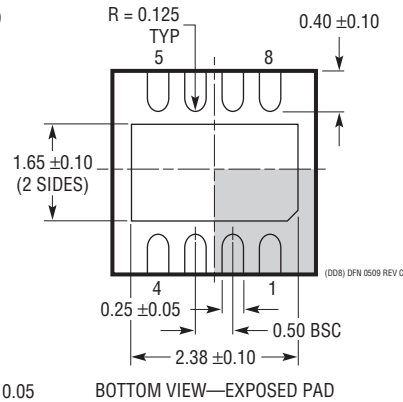
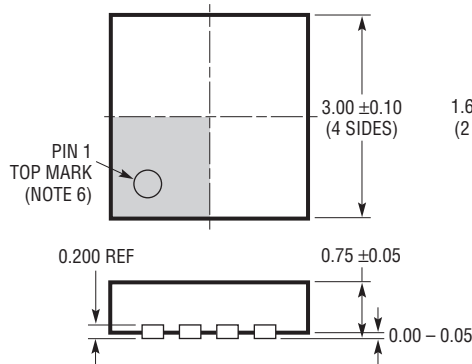
PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

DD Package
8-Lead Plastic DFN (3mm × 3mm)
 (Reference LTC DWG # 05-08-1698 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
 APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



- NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
 2. DRAWING NOT TO SCALE
 3. ALL DIMENSIONS ARE IN MILLIMETERS
 4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
 5. EXPOSED PAD SHALL BE SOLDER PLATED
 6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/09	Change to Both Packages in Pin Configuration.	2
B	11/12	Updated S8 and DD packages in the Package Description section.	11-12