200MHz, 30V/µs 16-Bit Accurate $A_V \geq 2$ Op Amp

FEATURES

- **Stable in Gain $A_V \geq 2$ ($A_V = -1$)**
- **200MHz Gain Bandwidth Product**
- **30V/µs Slew Rate**
- **Settling Time: 800ns (10V Step, 150µV)**
- **Specified at ±5V and ±15V Supplies**
- Low Distortion, –96.5dB for 100kHz, $10V_{P-P}$
- Maximum Input Offset Voltage: 75µV
- Maximum Input Offset Voltage Drift: 2µV/°C
- Maximum (–) Input Bias Current: 10nA
- Minimum DC Gain: 1000V/mV
- Minimum Output Swing into 2k: ±12.8V
- Input Noise Voltage: $5nV/\sqrt{Hz}$
- Input Noise Current: $0.6pA/\sqrt{Hz}$
- Total Input Noise Optimized for $1k < R_S < 20k$
- Available in an 8-Lead Plastic SO Package and 8-Lead DFN Package

APPLICATIONS

- 16-Bit DAC Current-to-Voltage Converter
- Precision Instrumentation
- ADC Buffer
- Low Distortion Active Filters
- High Accuracy Data Acquisition Systems
- Photodiode Amplifiers

DESCRIPTION

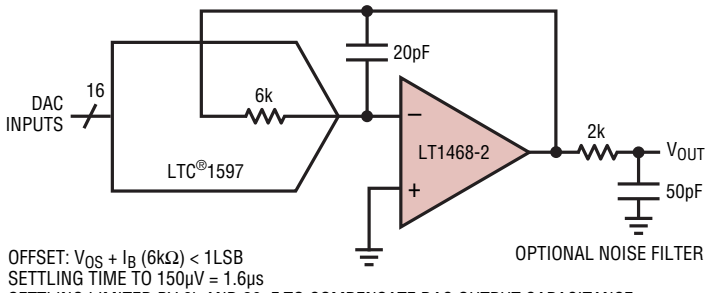
The LT®1468-2 is a precision high speed operational amplifier with 16-bit accuracy, decompensated to be stable in a gain of 2 or greater. The combination of precision and AC performance makes the LT1468-2 the optimum choice for high accuracy applications such as DAC current-to-voltage conversion and ADC buffers. The initial accuracy and drift characteristics of the input offset voltage and inverting input bias current are tailored for inverting applications.

The 200MHz gain bandwidth ensures high open-loop gain at frequency for reducing distortion. In noninverting applications such as an ADC buffer, the low distortion and DC accuracy allow full 16-bit AC and DC performance. The high slew rate of the LT1468-2 improves large-signal performance in applications such as active filters and instrumentation amplifiers compared to other precision op amps.

The LT1468-2 is specified on power supply voltages of ±5V and ±15V and from –40°C to 85°C. For a unity-gain stable op amp with same DC performance, see the LT1468 data sheet.

TYPICAL APPLICATION

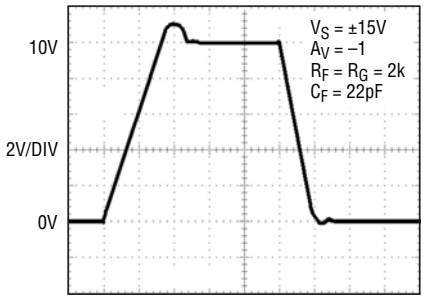
16-Bit DAC I-to-V Converter



OFFSET: $V_{OS} + I_B$ (6kΩ) < 1LSB
SETTLING TIME TO 150µV = 1.6µs
SETTLING LIMITED BY 6k AND 20pF TO COMPENSATE DAC OUTPUT CAPACITANCE

14682 TA01

Large Signal Transient, $A_V = -1$

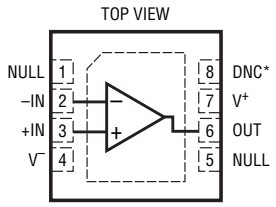


14682 TA02

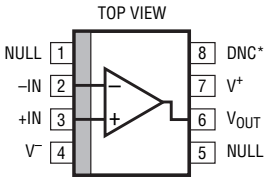
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-).....36V
Maximum Input Current (Note 2).....10mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range (Note 4) .... –40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
for S8 Only..... 300°C

PIN CONFIGURATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD IS INTERNALLY CONNECTED TO V^-



S8 PACKAGE
8-LEAD PLASTIC SO
*DO NOT CONNECT
T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1468CS8-2#PBF	LT1468CS8-2#TRPBF	14682	8-Lead Plastic Small Outline	0°C to 70°C
LT1468IS8-2#PBF	LT1468IS8-2#TRPBF	14682	8-Lead Plastic Small Outline	–40°C to 85°C
LT1468ACDD-2#PBF	LT1468ACDD-2#TRPBF	LDSY	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT1468AIDD-2#PBF	LT1468AIDD-2#TRPBF	LDSY	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT1468CDD-2#PBF	LT1468CDD-2#TRPBF	LDSY	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT1468IDD-2#PBF	LT1468IDD-2#TRPBF	LDSY	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	S8 Package	±15V ±5V			30 50	75 175	µV µV
		LT1468A, DD Package	±15V ±5V			30 50	75 175	µV µV
		LT1468, DD Package	±15V ±5V			100 150	200 300	µV µV
I_{OS}	Input Offset Current		±5V to ±15V			13	50	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
I_B^-	Inverting Input Bias Current		±5V to ±15V			3	±10	nA
I_B^+	Noninverting Input Bias Current		±5V to ±15V			–10	±40	nA
	Input Noise Voltage	0.1Hz to 10Hz	±5V to ±15V			0.3		μV_{P-P}
e_n	Input Noise Voltage	f = 10kHz	±5V to ±15V			5		$nV/\sqrt{Hz}$
i_n	Input Noise Voltage	f = 10kHz	±5V to ±15V			0.6		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12.5V Differential	±15V ±15V		100 50	240 150		MΩ kΩ
C_{IN}	Input Capacitance		±15V			4		pF
	Input Voltage Range +		±15V ±5V		12.5 2.5	13.5 3.5		V V
	Input Voltage Range –		±15V ±5V			–14.3 –4.3	–12.5 –2.5	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12.5V V_{CM} = ±2.5V	±15V ±5V		96 96	110 112		dB dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±15V			100	112		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12.5V, R_L = 10k V_{OUT} = ±12.5V, R_L = 2k V_{OUT} = ±2.5V, R_L = 10k V_{OUT} = ±2.5V, R_L = 2k	±15V ±15V ±5V ±5V		1000 500 1000 500	9000 5000 6000 3000		V/mV V/mV V/mV V/mV
V_{OUT}	Output Swing	R_L = 10k R_L = 2k R_L = 10k R_L = 2k	±15V ±15V ±5V ±5V		±13.0 ±12.8 ±3.0 ±2.8	±13.6 ±13.5 ±3.6 ±3.5		V V V V
I_{OUT}	Output Current	V_{OUT} = ±12.5V V_{OUT} = ±2.5V	±15V ±5V		±15 ±15	±22 ±22		mA mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±0.2V	±15V		±25	±40		mA
SR	Slew Rate	R_L = 2k (Note 5)	±15V ±5V		20 15	30 22		V/µs V/µs
	Full-Power Bandwidth	10V Peak, (Note 6) 3V Peak, (Note 6)	±15V ±5V			475 1160		kHz kHz
GBW	Gain Bandwidth	f = 100kHz, R_L = 2k	±15V ±5V		140 130	200 190		MHz MHz
t_s	Settling Time	10V Step, 0.01%, A_V = –1 10V Step, 150µV, A_V = –1 5V Step, 0.01%, A_V = –1	±15V ±15V ±5V			650 800 550		ns ns ns
R_O	Output Resistance	A_V = –1, f = 100kHz	±15V			0.02		Ω
I_S	Supply Current		±15V ±5V			3.9 3.6	5.2 5.0	mA mA

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. 0°C ≤ T_A ≤ 70°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	S8 Package	±15V ±5V	● ●			150 250	µV µV
		LT1468A, DD Package	±15V ±5V	● ●			150 250	µV µV
		LT1468, DD Package	±15V ±5V	● ●			300 400	µV µV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. 0°C ≤ T_A ≤ 70°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
	Input V_{OS} Drift	(Note 7)	±5V to ±15V	●		0.7	2.0	µV/°C
I_{OS}	Input Offset Current		±5V to ±15V	●			65	nA
	Input Offset Current Drift		±5V to ±15V			60		pA/°C
I_B^-	Inverting Input Bias Current		±5V to ±15V	●			±15	nA
	Negative Input Current Drift		±5V to ±15V			40		pA/°C
I_B^+	Noninverting Input Bias Current		±5V to ±15V	●			±50	nA
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12.5V V_{CM} = ±2.5V	±15V ±5V	● ●	94 94			dB dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±15V		●	98			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12.5V, R_L = 10k V_{OUT} = ±12.5V, R_L = 2k V_{OUT} = ±2.5V, R_L = 10k V_{OUT} = ±2.5V, R_L = 2k	±15V ±15V ±5V ±5V	● ● ● ●	500 250 500 250			V/mV V/mV V/mV V/mV
V_{OUT}	Output Swing	R_L = 10k R_L = 2k R_L = 10k R_L = 2k	±15V ±15V ±5V ±5V	● ● ● ●	±12.9 ±12.7 ±2.9 ±2.7			V V V V
I_{OUT}	Output Current	V_{OUT} = ±12.5V V_{OUT} = ±2.5V	±15V ±5V	● ●	±12.5 ±12.5			mA mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±0.2V	±15V	●	±17			mA
SR	Slew Rate	R_L = 2k (Note 5)	±15V ±5V	● ●	18 13			V/µs V/µs
GBW	Gain Bandwidth	f = 100kHz, R_L = 2k	±15V ±5V	● ●	130 120	200 190		MHz MHz
I_S	Supply Current		±15V ±5V	● ●			6.5 6.3	mA mA

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. –40°C ≤ T_A ≤ 85°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	S8 Package	±15V ±5V	● ●			230 330	µV µV
		LT1468A, DD Package	±15V ±5V	● ●			230 330	µV µV
		LT1468, DD Package	±15V ±5V	● ●			400 500	µV µV
	Input V_{OS} Drift	(Note 7)	±5V to ±15V	●		0.7	2.5	µV/°C
I_{OS}	Input Offset Current		±5V to ±15V	●			80	nA
	Input Offset Current Drift		±5V to ±15V			120		pA/°C
I_B^-	Inverting Input Bias Current		±5V to ±15V	●			±30	nA
	Negative Input Current Drift		±5V to ±15V			80		pA/°C
I_B^+	Noninverting Input Bias Current		±5V to ±15V	●			±60	nA
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12.5V V_{CM} = ±2.5V	±15V ±5V	● ●	92 92			dB dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±15V		●	96			dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. –40°C ≤ T_A ≤ 85°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 10k	±15V	●	300			V/mV
		V_{OUT} = ±10V, R_L = 2k	±15V	●	150			V/mV
		V_{OUT} = ±2.5V, R_L = 10k	±5V	●	300			V/mV
		V_{OUT} = ±2.5V, R_L = 2k	±5V	●	150			V/mV
V_{OUT}	Output Swing	R_L = 10k	±15V	●	±12.8			V
		R_L = 2k	±15V	●	±12.6			V
		R_L = 10k	±5V	●	±2.8			V
		R_L = 2k	±5V	●	±2.6			V
I_{OUT}	Output Current	V_{OUT} = ±12.5V	±15V	●	±7			mA
		V_{OUT} = ±2.5V	±5V	●	±7			mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±0.2V	±15V	●	±12			mA
SR	Slew Rate	R_L = 2k (Note 5)	±15V	●	15			V/µs
			±5V	●	11			V/µs
GBW	Gain Bandwidth	f = 100kHz, R_L = 2k	±15V	●	110	200		MHz
			±5V	●	100	190		MHz
I_S	Supply Current		±15V	●			7.0	mA
			±5V	●			6.8	mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by back-to-back diodes and two 100Ω series resistors. If the differential input voltage exceeds 0.7V, the input current should be limited to 10mA. Input voltages outside the supplies will be clamped by ESD protection devices and input currents should also be limited to 10mA.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: The LT1468C-2 is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet these extended temperature limits, but is not tested at –40°C and at 85°C. The LT1468I-2 is guaranteed to meet the extended temperature limits.

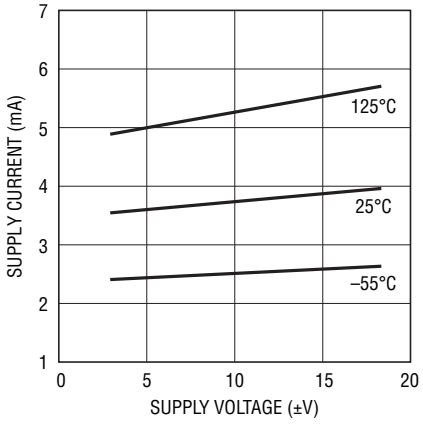
Note 5: Slew rate is measured between ±8V on the output with ±12V input for ±15V supplies and ±2V on the output with ±3V input for ±5V supplies.

Note 6: Full power bandwidth is calculated from the slew rate measurement: FPBW = SR/2πV_P

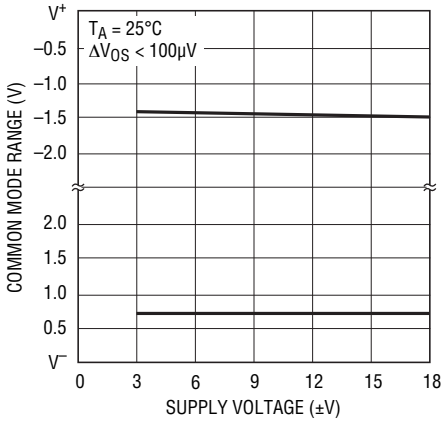
Note 7: This parameter is not 100% tested.

TYPICAL PERFORMANCE CHARACTERISTICS

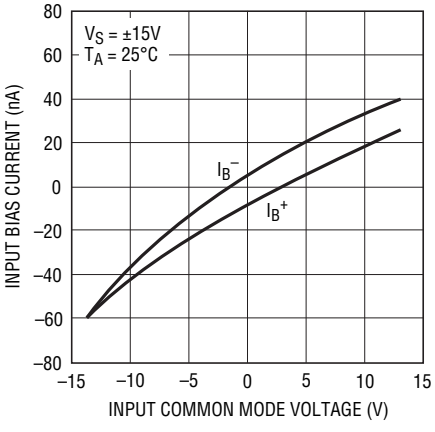
Supply Current vs Supply Voltage and Temperature



Input Common Mode Range vs Supply Voltage

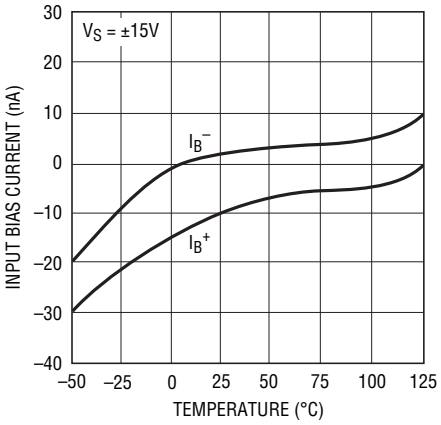


Input Bias Current vs Input Common Mode Voltage



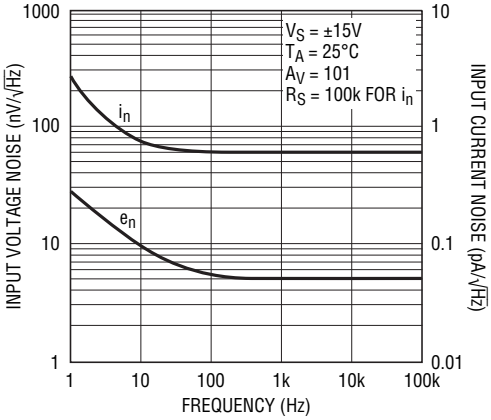
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Temperature



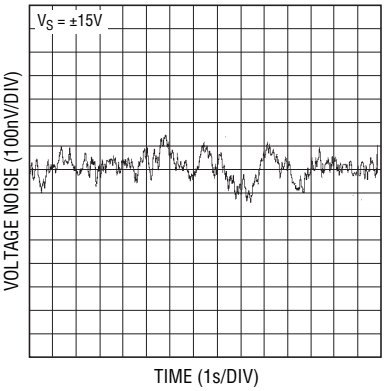
14682 G04

Input Noise Spectral Density



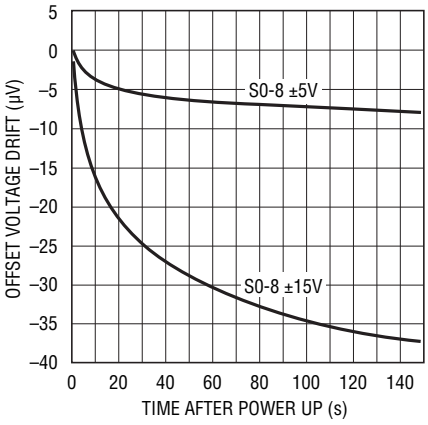
14682 G05

0.1Hz to 10Hz Voltage Noise



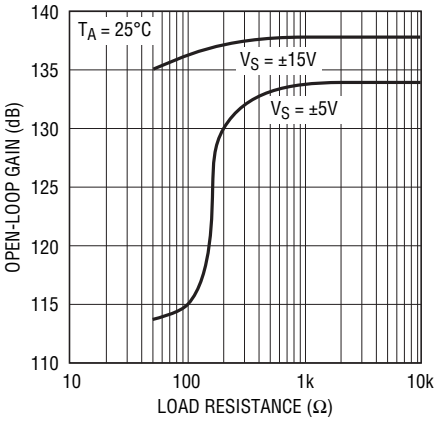
14682 G06

Warm-Up Drift vs Time



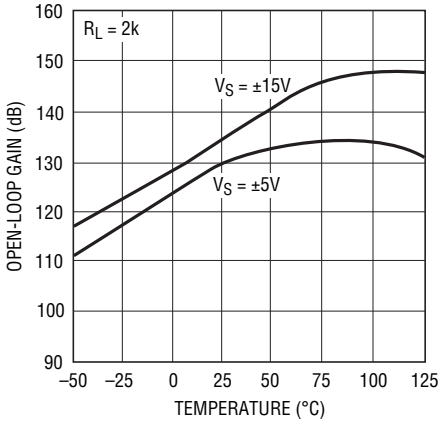
14682 G07

Open-Loop Gain vs Resistive Load



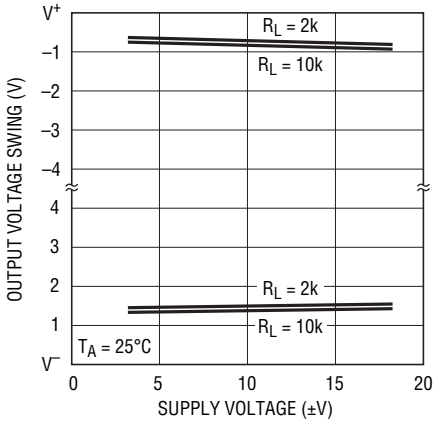
14682 G08

Open-Loop Gain vs Temperature



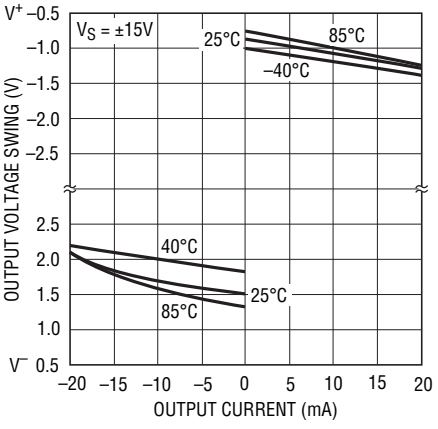
14682 G09

Output Voltage Swing vs Supply Voltage



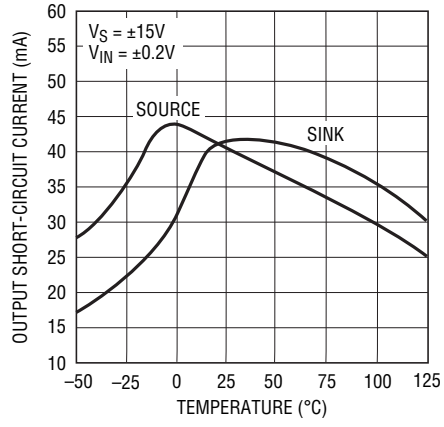
14682 G10

Output Voltage Swing vs Load Current



14682 G11

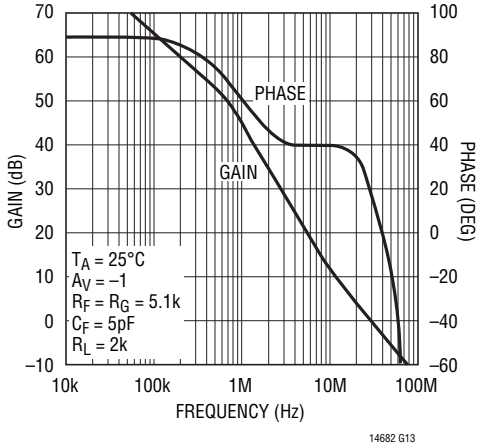
Output Short-Circuit Current vs Temperature



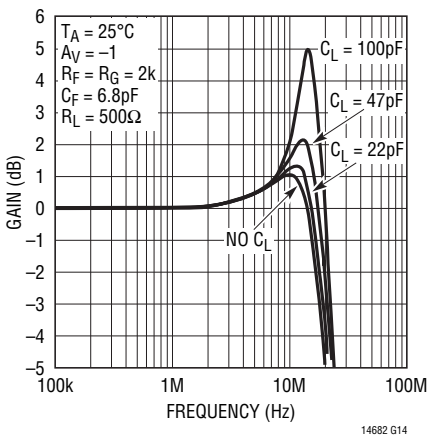
14682 G12

TYPICAL PERFORMANCE CHARACTERISTICS

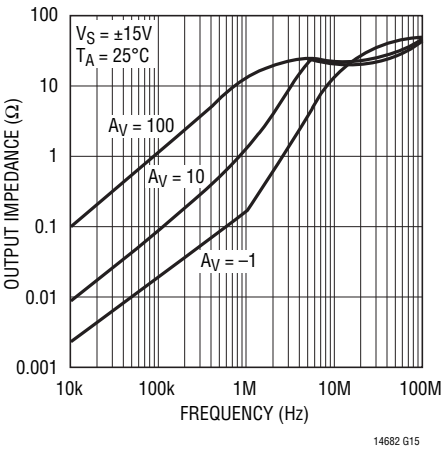
Open-Loop Gain and Phase vs Frequency



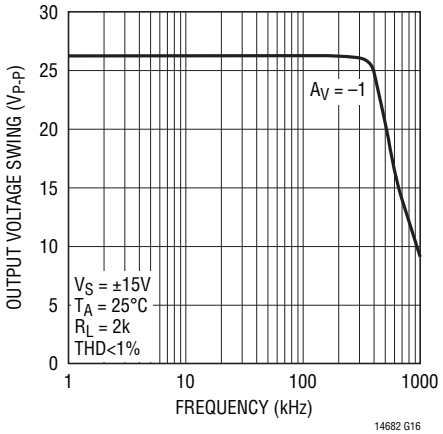
Gain vs Frequency, $A_V = -1$



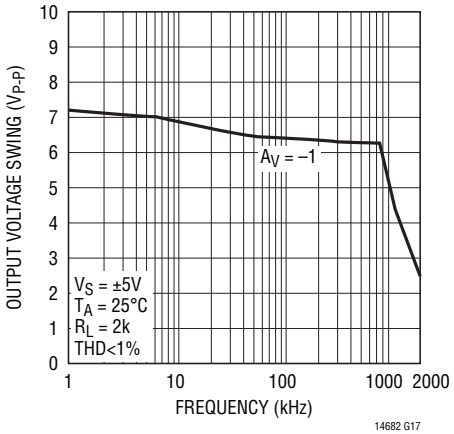
Output Impedance vs Frequency



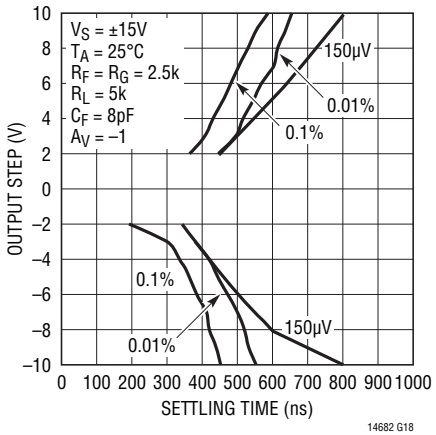
Undistorted Output Swing vs Frequency, $V_S = \pm 15V$



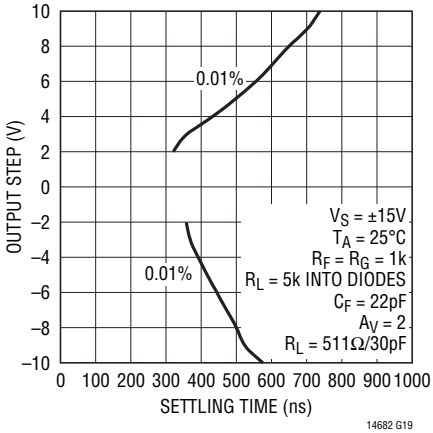
Undistorted Output Swing vs Frequency, $V_S = \pm 5V$



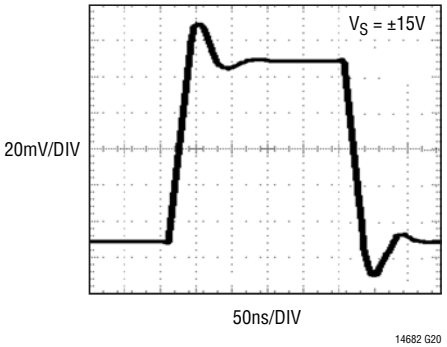
Settling Time vs Output Step



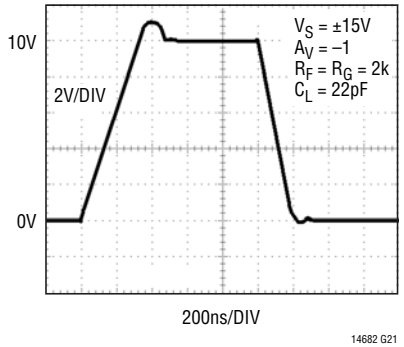
Settling Time vs Output Step



Small-Signal Transient, $A_V = -1$



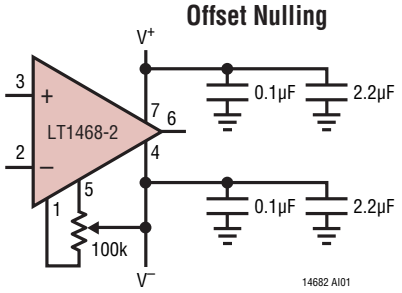
Large-Signal Transient, $A_V = -1$



APPLICATIONS INFORMATION

The LT1468-2 may be inserted directly into many operational amplifier applications improving both DC and AC performance, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1468-2 is shown below.

Offset Nulling



Gain of 2 Stable

The LT1468-2 is a decompensated version of the LT1468. The precision DC performance is identical, but the internal compensation capacitors have been reduced to a point where the op amp needs a gain of 2 or greater in order to be stable.

In general, for applications where the gain around the op amp is ≥ 2, the decompensated version should be used, because it will give the best AC performance. In applications where the gain is < 2, the unity-gain stable version should be used.

The appropriate way to define the 'gain' is as the inverse of the feedback ratio from output to differential input, including all relevant parasitics. Moreover, as with all feedback loops, the stability of the loop depends on the value of that feedback ratio at frequencies where the total loop-gain would cross unity. Therefore, it is possible to have circuits in which the gain at DC is lower than the gain at high frequency, and these circuits can be stable even with a non unity-gain stable op amp. An example is many current-output DAC buffer applications.

Layout and Passive Components

The LT1468 requires attention to detail in board layout in order to maximize DC and AC performance. For best AC results (for example fast settling time) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01µF to 0.1µF) in parallel with low ESR bypass capacitors (1µF to 10µF tantalum). For best DC performance, use "star" grounding techniques, equalize input trace lengths and minimize leakage (i.e., 1.5GΩ of leakage between an input and a 15V supply will generate 10nA—equal to the maximum I_B^- specification.)

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs. For inverting configurations tie the ring to ground, in noninverting connections tie the ring to the inverting input (note the input capacitance will increase which may require a compensating capacitor as discussed below.)

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the inputs can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

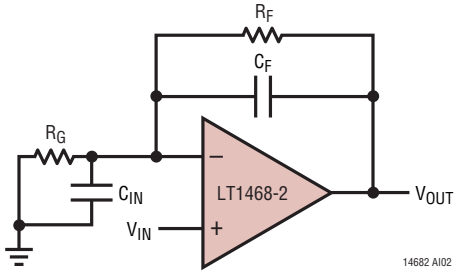
Make no connection to Pin 8. This pin is used for factory trim of the inverting input current.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole that can cause peaking or even oscillations. A feedback capacitor of the value:

$$C_F = (R_G)(C_{IN}/R_F)$$

may be used to cancel the input pole and optimize dynamic performance. For applications where the DC noise gain is one, and a large feedback resistor is used, C_F should be less than or equal to one half of C_{IN}. An example would be a DAC I-to-V converter as shown on the front page of this data sheet where the DAC can have many tens of pF of output capacitance.

Nulling Input Capacitance



APPLICATIONS INFORMATION

Input Considerations

Each input of the LT1468-2 is protected with a 100Ω series resistor and back-to-back diodes across the bases of the input devices. If the inputs can be pulled apart, the input current should be limited to less than 10mA with an external series resistor. Each input also has two ESD clamp diodes—one to each supply. If an input is driven above the supply, limit the current with an external resistor to less than 10mA.

The LT1468-2 employs bias current cancellation at the inputs. The inverting input current is trimmed at zero common mode voltage to minimize errors in inverting applications such as I-to-V converters. The noninverting input current is not trimmed and has a wider variation and therefore a larger maximum value. As the input offset current can be greater than either input current, the use of balanced source resistance is NOT recommended as it actually degrades DC accuracy and also increases noise.

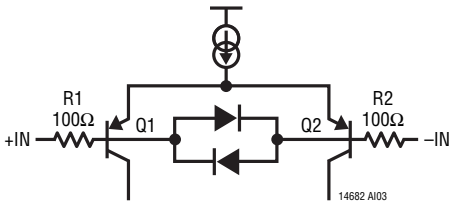
The input bias currents vary with common mode voltage as shown in the Typical Performance Characteristics. The cancellation circuitry was not designed to track this common mode voltage because the settling time would have been adversely affected.

The LT1468 inputs can be driven to the negative supply and to within 0.5V of the positive supply without phase reversal. As the input moves closer than 0.5V to the positive supply, the output reverses phase.

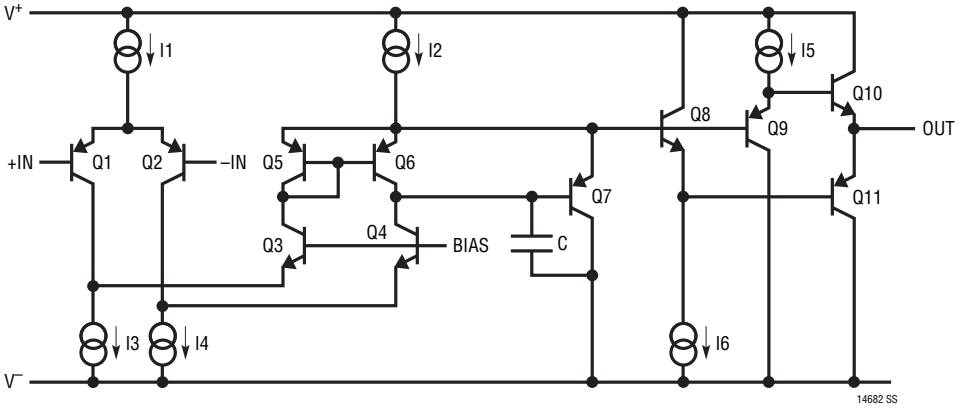
Total Input Noise

The curve of Total Noise vs Unmatched Source Resistance in the Typical Performance Characteristics shows that with source resistance below 1k, the voltage noise of the amplifier dominates. In the 1k to 20k region the increase in noise is due to the source resistance. Above 20k the input current noise component is larger than the resistor noise.

Input Stage Protection



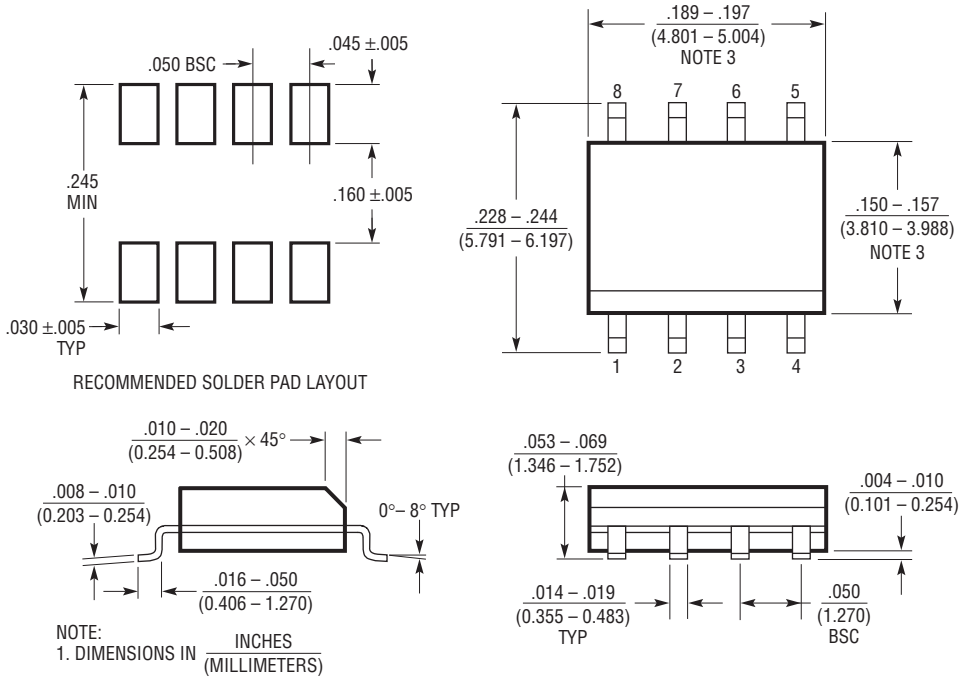
SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610 Rev G)



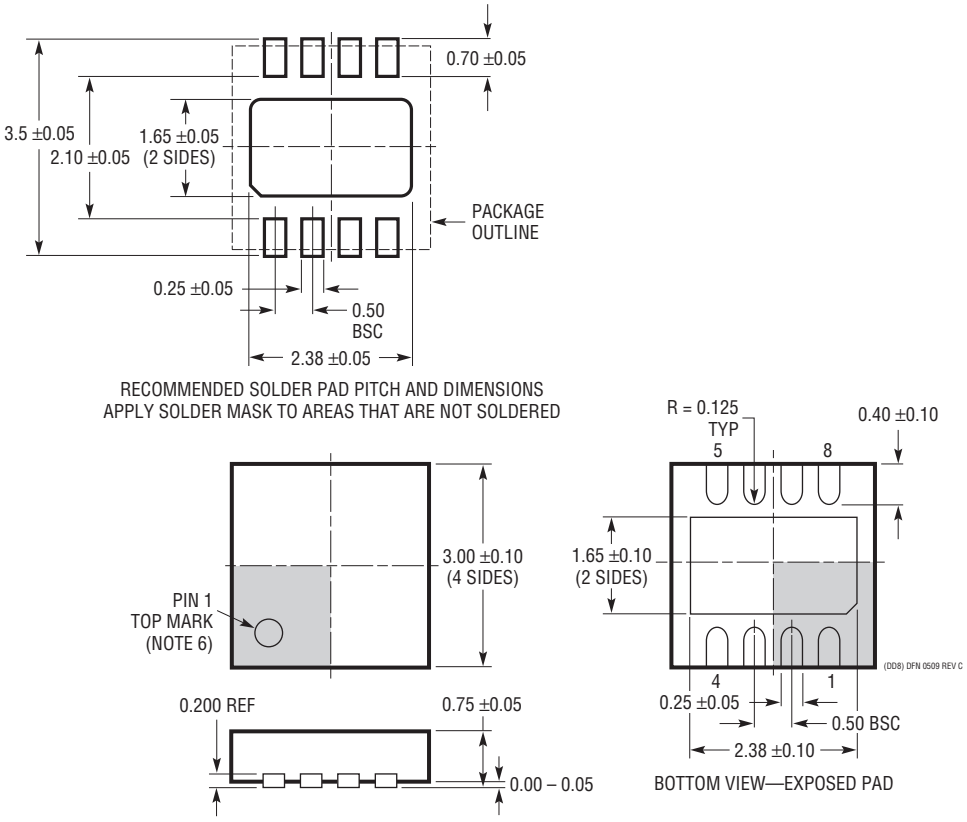
NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

S08 REV G 0212

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/09	Change to Both Packages in Pin Configuration.	2
B	11/12	Updated S8 and DD packages in the Package Description section.	11-12