Power Factor and PWM Controller

FEATURES

- **PFC and PWM Single Chip Solution**
- Synchronized Operation up to 300kHz
- 99% Power Factor over 20:1 Load Current Range
- **Current Mode PWM**
- **Instantaneous Overvoltage Protection**
- Dedicated Overvoltage Protection (OVP Pin)
- Minimal Line Current Dead Zone
- Typical 250μA Start-Up Supply Current
- Line Switching Noise Filter
- Low Quiescent Current: 13mA
- Fast 2A Peak Current Gate Drivers
- Separate Soft Start Controls

APPLICATIONS

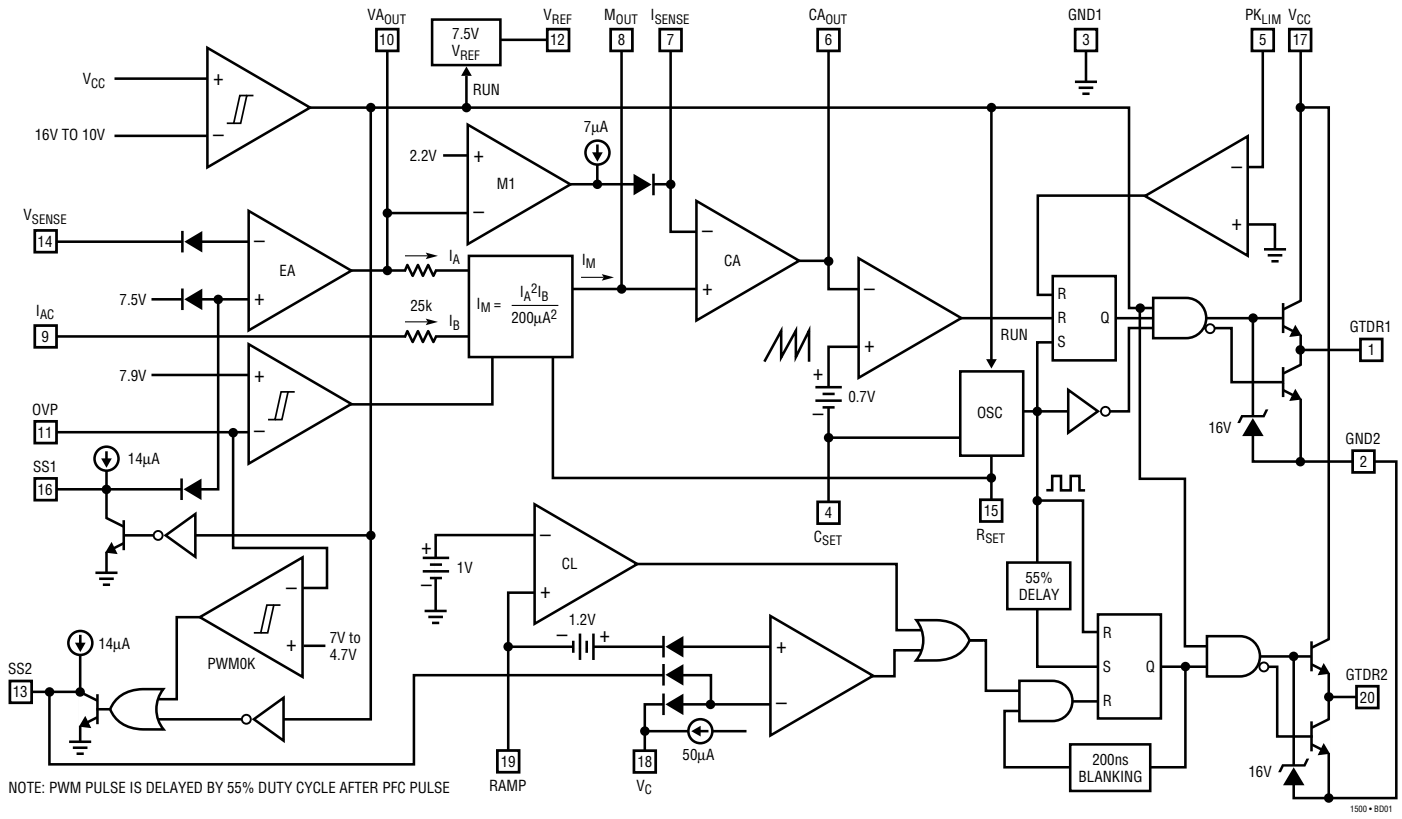
- Universal Power Factor Corrected Power Supplies and Preregulators

DESCRIPTION

The LT®1509 is a complete solution for universal off-line switching power supplies utilizing active power factor correction. The PFC section is identical to the LT1248 PFC controller except the EN/SYNC pin is removed because PFC and PWM are synchronized internally.

The current mode PWM section (the LT1508 is the voltage-mode counterpart) contains all the primary side functions to convert the PFC preregulated high voltage output to an isolated low voltage output. The PWM duty cycle is internally limited to 47% (maximum 50%) to prevent transformer saturation. PWM soft start begins when PFC output reaches the preset voltage. In the event of brief line loss, the PWM will be shut off when the PFC output voltage drops below 73% of the preset value.

BLOCK DIAGRAM



DESCRIPTION

By using fixed high frequency PWM current averaging without the need for slope compensation, the LT1509 achieves far lower line current distortion with a smaller magnetic element than systems that use either peak current detection, or zero current switching approach, in both continuous and discontinuous modes of operation.

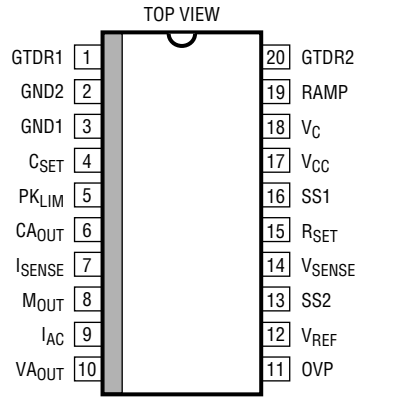
The LT1509 also provides filtering capability to reject line switching noise which can cause instability when fed into the multiplier. Line current dead zone is minimized with low bias voltage at the current input to the multiplier.

The LT1509 provides many protection features including peak current limiting and overvoltage protection. Implemented with a very high speed process, the LT1509 can be operated at frequencies as high as 300kHz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 27V
GTDR Current Continuous 0.5A
GTDR Output Energy 5μJ
I_{AC}, R_{SET}, PK_{LIM} Input Current 20mA
V_{SENSE}, OVP Input Voltage ..... V_{MAX}
RAMP, V_C Input Voltage 8V
I_{SENSE}, M_{OUT} Input Current ..... ±5mA
Operating Junction Temperature Range
  Commercial ..... 0°C to 100°C
  Industrial ..... –40°C to 125°C
Thermal Resistance (Junction-to-Ambient)
  N Package ..... 100°C/W
  SW Package ..... 120°C/W

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LT1509CN
LT1509CSW
LT1509IN
LT1509ISW

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

Maximum operating voltage (V_{MAX}) = 25V, V_{CC} = 18V, R_{SET} = 15k to GND, C_{SET} = 1nF to GND, I_{AC} = 100μA, I_{SENSE} = 0V, CA_{OUT} = 3.5V, VA_{OUT} = 5V, OVP = V_{REF}. No load on any outputs unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Overall						
Supply Current (V_{CC} in Undervoltage Lockout)	V_{CC} = Lockout Voltage –0.2V	●		0.25	0.45	mA
Supply Current On	11.5V ≤ V_{CC} ≤ V_{MAX}	●		13	19	mA
V_{CC} Turn-On Threshold (Undervoltage Lockout)		●	15.5	16.5	17.5	V
V_{CC} Turn-Off Threshold		●	9.5	10.5	11.5	V
Voltage Amplifier (PFC Section)						
Voltage Amp Offset	VA_{OUT} = 3.5V	●	–10		10	mV
Input Bias Current	V_{SENSE} = 0V to 7V	●		–25	–250	nA
Voltage Gain			70	100		dB
Voltage Amp Unity-Gain Bandwidth				3		MHz
Voltage Amp Output High (Internally Clamped)		●	11.3	13.3		V
Voltage Amp Output Low		●		1.1	2	V
Voltage Amp Short-Circuit Current	VA_{OUT} = 0V	●	3	8	17	mA

ELECTRICAL CHARACTERISTICS

Maximum operating voltage (V_{MAX}) = 25V, V_{CC} = 18V, R_{SET} = 15k to GND, C_{SET} = 1nF to GND, I_{AC} = 100μA, I_{SENSE} = 0V, CA_{OUT} = 3.5V, VA_{OUT} = 5V, OVP = V_{REF}. No load on any outputs unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Amplifier (PFC Section)						
Current Amp Offset Voltage		●		±1	±4	mV
I_{SENSE} Bias Current		●		–25	–250	nA
Current Amp Voltage Gain			80	110		dB
Current Amp Unity-Gain Bandwidth				3		MHz
Current Amp Output High		●	7.2	8.5		V
Current Amp Output Low		●		1.1	2	V
Current Amp Short-Circuit Current	CA_{OUT} = 0V	●	3	8	17	mA
Input Range, I_{SENSE}, M_{OUT} (Linear Operation)		●	–0.3		1	V
Reference						
Reference Output Voltage	I_{REF} = 0mA, T_A = 25°C		7.39	7.50	7.60	V
V_{REF} Load Regulation	–5mA < I_{REF} < 0mA			5		mV
V_{REF} Line Regulation	11.5V < V_{CC} < V_{MAX}	●	–20	5	20	mV
V_{REF} Short-Circuit Current	V_{REF} = 0V	●	12	28	50	mA
V_{REF} Worst Case	Load, Line, Temperature	●	7.32	7.5	7.68	V
Current Limit						
PK_{LIM} Offset Voltage		●	–25		25	mV
PK_{LIM} Input Current	PK_{LIM} = –0.1V	●		–50	–100	μA
PK_{LIM} to GTDR Propagation Delay	PK_{LIM} Falling from 50mV to –50mV			400		ns
Multiplier						
Multiplier Output Current	I_{AC} = 100μA, R_{SET} = 15k			35		μA
Multiplier Output Current Offset	R_{AC} = 1M from I_{AC} to GND	●		–0.05	–0.5	μA
Multiplier Maximum Output Current	I_{AC} = 450μA, R_{SET} = 15k, VA_{OUT} = 7V, M_{OUT} = 0V	●	–286	–260	–235	μA
Multiplier Gain Constant (Note 1)				0.035		V^{-2}
I_{AC} Input Resistance	I_{AC} from 50μA to 1mA		15	25	35	kΩ
Oscillator						
Oscillator Frequency	R_{SET} = 15k, C_{SET} = 1000pF R_{SET} = 15k, C_{SET} = 1500pF	● ●	85 58	100 68	115 78	kHz kHz
C_{SET} Ramp Peak-to-Peak Amplitude			4.35	4.7	5.0	V
C_{SET} Ramp Valley Voltage			1.15	1.3	1.55	V
Overvoltage Comparator (PFC Section)						
Comparator Trip Voltage Ratio (V_{TRIP}/V_{REF})		●	1.04	1.05	1.06	
Hysteresis				0.35		V
OVP Bias Current	OVP = 7.5V	●		0.2	1	μA
OVP Propagation Delay				100		ns
Gate Drivers (GTDR1 and GTDR2)						
Max Output Voltage	0mA Load, 18V < V_{CC}	●	12	15	17.5	V
Output High	–200mA Load, 11.5V ≤ V_{CC} ≤ 15V	●	V_{CC} – 3.0			V
Output Low (Device Unpowered)	V_{CC} = 0V, 50mA Load (Sinking)	●		0.9	1.5	V
Output Low (Device Active)	200mA Load (Sinking) 10mA Load	● ●		0.5 0.2	1.0 0.4	V V
Peak Output Current	10nF from GTDR to GND			2		A
Rise and Fall Time	1nF from GTDR to GND			25		ns
Max Duty Cycle (PFC)			90	96		%
Max Duty Cycle (PWM) (Note 2)			44		50	%

ELECTRICAL CHARACTERISTICS

V_{CC} = 18V, R_{SET} = 15k to GND, C_{SET} = 1nF to GND, I_{AC} = 100µA, I_{SENSE} = 0V, CA_{OUT} = 3.5V, VA_{OUT} = 5V, OVP = V_{REF}. No load on any outputs, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Soft Start Current						
SS1 Current (PFC)	SS1 = 2.5V	●	5	12	30	µA
SS2 Current (PWM)	SS2 = 1V	●	5	12	30	µA
Comparators in PWM Section						
RAMP Input Current	RAMP = 0V, V_C = 1.6V	●		–0.3	–2	µA
Current Limit Comparator (CL) Threshold	V_C > 2.6V	●	0.95	1.1	1.2	V
GTDR2 Switching Off Threshold at V_C or at SS2	RAMP = 0V	●	1			V
V_C Input Current	V_C = 0V	●	–20		–80	µA
PWMOK Comparator Low Threshold (in Terms of V_{REF})		●	0.57	0.63	0.70	
V_C Pin High Voltage (LT1509)	1mA into V_C Pin	●	2.6	3.2	3.8	V
GTDR2 Turn-On Blanking Time				180		ns

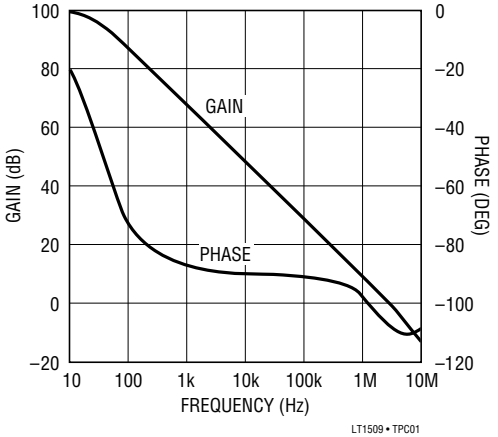
The ● denotes specifications which apply over the full operating temperature range.

Note 1: Multiplier Gain Constant: $K = \frac{I_M}{I_{AC}\,(VA_{OUT} - 2)^2}$

Note 2: GTDR2 (PWM) pulse is delayed by 53% duty cycle after GTDR1 (PFC) is set. See PFC/PWM Synchronization graph in the Typical Performance Characteristics section.

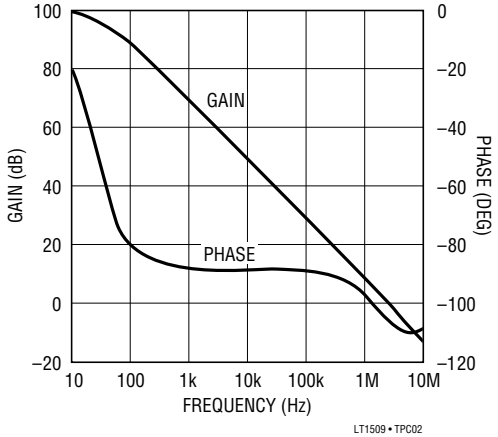
TYPICAL PERFORMANCE CHARACTERISTICS

PFC Voltage Amplifier Open-Loop Gain and Phase



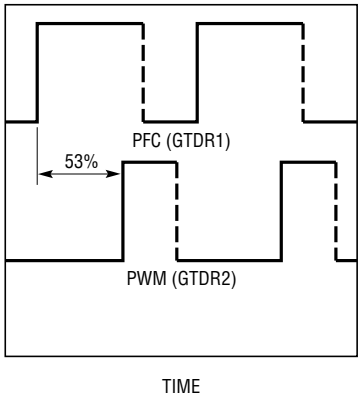
LT1509 • TPC01

PFC Current Amplifier Open-Loop Gain and Phase



LT1509 • TPC02

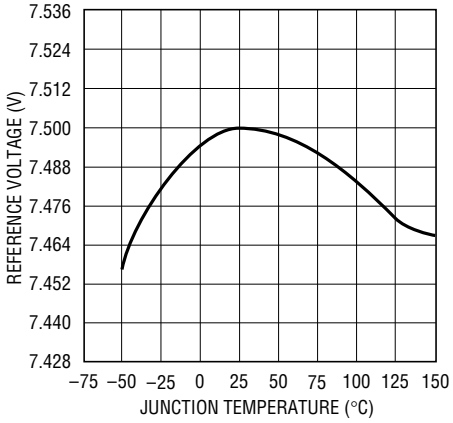
PFC/PWM Synchronization



LT1509 TPC03

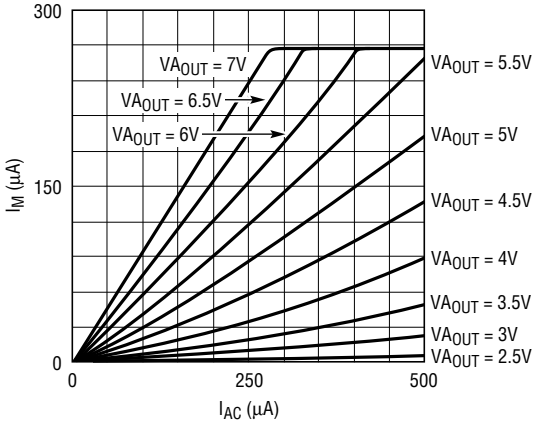
TYPICAL PERFORMANCE CHARACTERISTICS

Reference Voltage vs Temperature



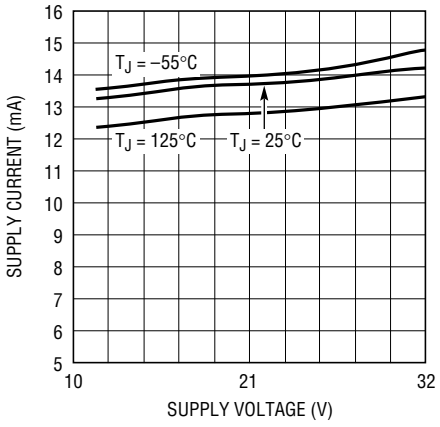
LT1509 • TPC04

Multiplier Current



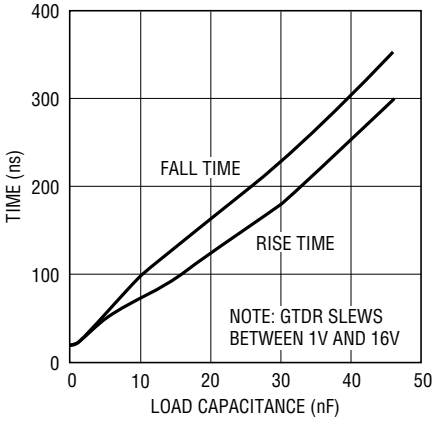
LT1509 • TPC05

Supply Current vs Supply Voltage



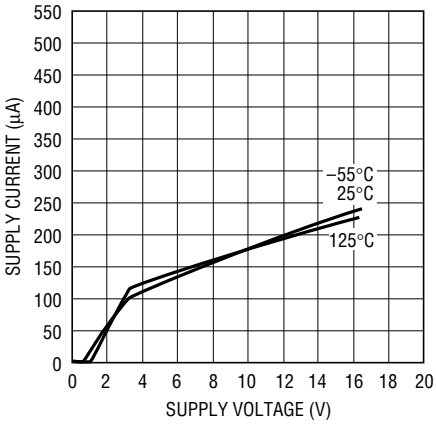
LT1509 • TPC06

GTDR Rise and Fall Time



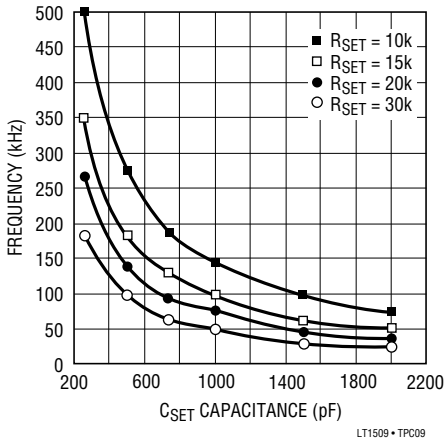
LT1509 • TPC07

Start-Up Supply Current vs Supply Voltage



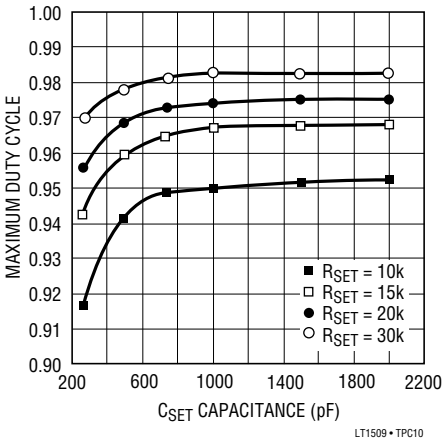
LT1509 • TPC08

Frequency vs R_{SET} and C_{SET}



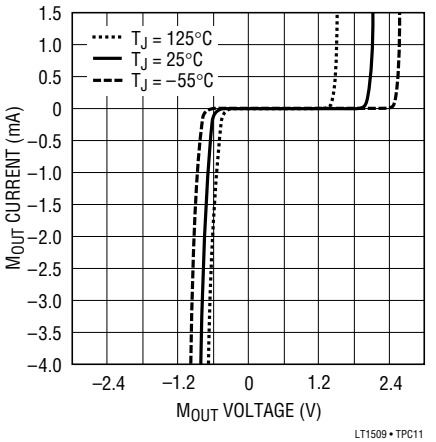
LT1509 • TPC09

GTDR1 Maximum Duty Cycle vs R_{SET} and C_{SET}



LT1509 • TPC10

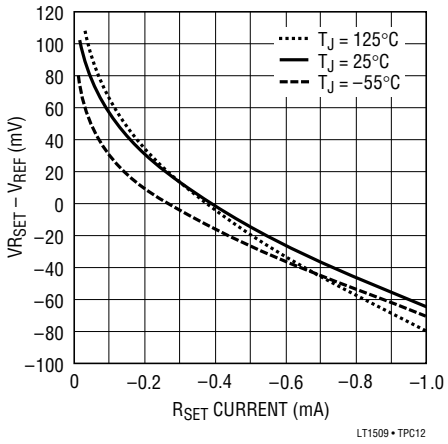
M_{OUT} Pin Characteristics



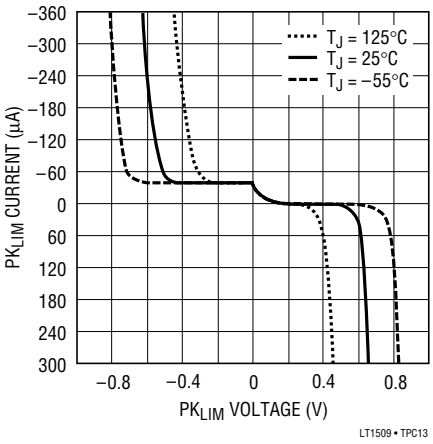
LT1509 • TPC11

TYPICAL PERFORMANCE CHARACTERISTICS

R_{SET} Voltage vs Current



PK_{LIM} Pin Characteristics



PIN FUNCTIONS (For application help with the PFC portion of this chip, see the LT1248 data sheet)

PFC SECTION

GTDR1 (Pin 1): The PFC MOSFET gate driver is a fast totem pole output which is clamped at 15V. Capacitive loads like the MOSFET gates may cause overshoot. A gate series resistor of at least 5Ω will prevent the overshoot.

GND2 (Pin 2): Power Ground. High current spikes occur in this line when either GTDR1 or GTDR2 switches low.

GND1 (Pin 3): Analog Ground.

C_{SET} (Pin 4): The capacitor from this pin to GND and R_{SET} determines oscillator frequency. The oscillator ramp is 5V and the frequency = $1.5/(R_{SET}\ C_{SET})$.

PK_{LIM} (Pin 5): The threshold of the peak current limit comparator is GND. To set current limit, a resistor divider can be connected from V_{REF} to current sense resistor.

CA_{OUT} (Pin 6): This is the output of the current amplifier that senses and forces the line current to follow the reference signal that comes from the multiplier by commanding the pulse width modulator. When CA_{OUT} is low, the modulator has zero duty cycle.

I_{SENSE} (Pin 7): This is the inverting input of the current amplifier. This pin is clamped at –0.6V by an ESD protection diode.

M_{OUT} (Pin 8): This is the multiplier high impedance current output and the noninverting input of the current amplifier. This pin is clamped at –0.6V and 3V.

I_{AC} (Pin 9): This is the AC line voltage sensing input to the multiplier. It is a current input that is biased at 2V to minimize the crossover dead zone caused by low line voltage. At the pin, a 25k resistor is in series with the current input, so that a lowpass RC can be used to filter out the switching noise coming down from the line with a high line impedance environment.

VA_{OUT} (Pin 10): This is the output of the voltage error amplifier. The output is clamped at 13.5V. When the output goes below 2.5V, the multiplier output current is zero.

OVP (Pin 11): This is the input to the overvoltage comparator. The threshold is 1.05 times the reference voltage. When the comparator trips, the multiplier, which is quickly inhibited, blanks PFC switching to prevent further overshoot. This pin is also the input to the PWMOK comparator that releases the PWM soft start (SS2) after the PFC output gets close to the final voltage and has a hysteresis of approximately 150V for 382V PFC output.

V_{REF} (Pin 12): This is the 7.5V reference. When V_{CC} goes low, V_{REF} will stay at 0V. V_{REF} biases most of the internal circuitry and can source up to 5mA externally.

V_{SENSE} (Pin 14): This is the inverting input to the voltage amplifier.

PIN FUNCTIONS (For application help with the PFC portion of this chip, see the LT1248 data sheet)

R_{SET} (Pin 15): A resistor from R_{SET} to GND sets the oscillator charging current and the maximum multiplier output current which is used to limit the maximum line current.

$I_{M(MAX)} = 3.75V/R_{SET}$

SS1 (Pin 16): Soft Start. SS1 is reset to zero for low V_{CC}. When V_{CC} rises above lockout threshold, SS1 is released to ramp up at a rate set by the internal 12μA current source and an external capacitor. During this ramp up, PFC reference voltage is equal to SS1 voltage. After SS1 rises past 7.5V, reference voltage remains at 7.5V.

V_{CC} (Pin 17): This is the supply for the chip. The LT1509 has two fast gate drivers required to fast charge high power MOSFET gate capacitances. Good supply bypassing is required consisting of a 0.1μF ceramic capacitor in parallel with a low ESR electrolytic capacitor (56μF or higher) in close proximity to IC GND.

PWM SECTION

SS2 (Pin 13): PWM Soft Start. The comparator PWMOK monitors the OVP pin and releases the SS2 after the PFC output gets close to the final voltage.

V_C (Pin 18): PWM current mode control voltage. Normally connects to the optocoupler amplifier output. A pull-up current of 50μA flows out of the pin.

RAMP (Pin 19): PWM current mode current sense input with current limit set to 1V.

GTDR2 (Pin 20): The PWM MOSFET gate driver is a 1.5A fast totem pole output. It is clamped at 15V. Capacitive loads like the MOSFET gates may cause overshoot. A gate series resistor of at least 5Ω will prevent the overshoot.

APPLICATIONS INFORMATION

Voltage Error Amplifier (PFC Section)

The voltage error amplifier has a 100dB DC gain and 3MHz unity-gain frequency. The output is internally clamped at 13.3V with V_{CC} = 18V. Maximum error amp output voltage decreases to V_{CC} – 1.5V for V_{CC} less than 12V. The noninverting input is tied to the 7.5V_{REF} through a diode and can be pulled down with the SS1 pin. Referring to Figure 1, $V_{OUT} = V_{REF}[(R1 + R2)/R2]$. With R1 = 1M and R2 = 20k, V_{OUT} = 382V. R1 through R4, C1 and C2 form the compensation for the voltage loop. Gain of the voltage error amp with the values shown is given by:

$$\frac{VA_{OUT}}{V_{OUT}} = -\frac{1 + j\frac{f}{1}}{(j)(f)(6.6)\left(1 + j\frac{f}{11}\right)}$$

The small-signal gain for the remaining portion of the voltage loop for frequencies below the current loop bandwidth is (see Figure 2):

$$\frac{V_{OUT}}{VA_{OUT}} = \frac{V_{IN}}{(5\pi)(j)(f)(C_{OUT})(V_{OUT})}\sqrt{\frac{(R_{REF})(P_{IN})}{R_S(R_{IAC} + 25k)}}$$

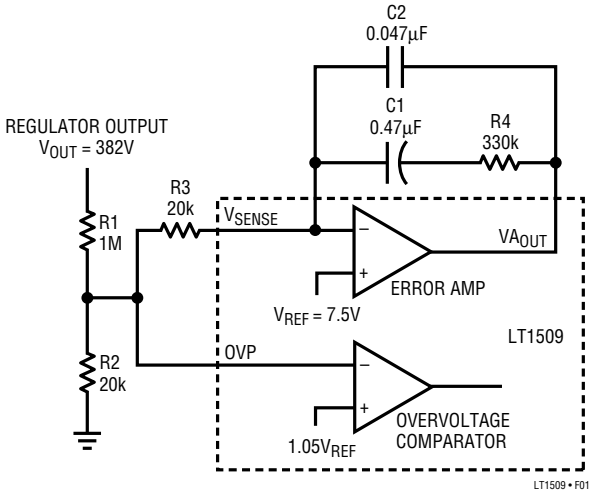


Figure 1

With V_{IN} = 120VAC, P_{IN} = 150W, R_S = 0.15Ω, R_{REF} = 4k, R_{IAC} = 1M, V_{OUT} = 382V and C_{OUT} = 470μF, V_{OUT}/VA_{OUT} = 85/(j)(f). At very low frequencies, the loop has a –40dB/decade slope. Additional zero-pole compensation is added at 1Hz and 11Hz. The resulting loop gain and phase margin is shown in Figure 3. The unity-gain bandwidth is low compared to 120Hz, which results in low distortion and a high power factor.

APPLICATIONS INFORMATION

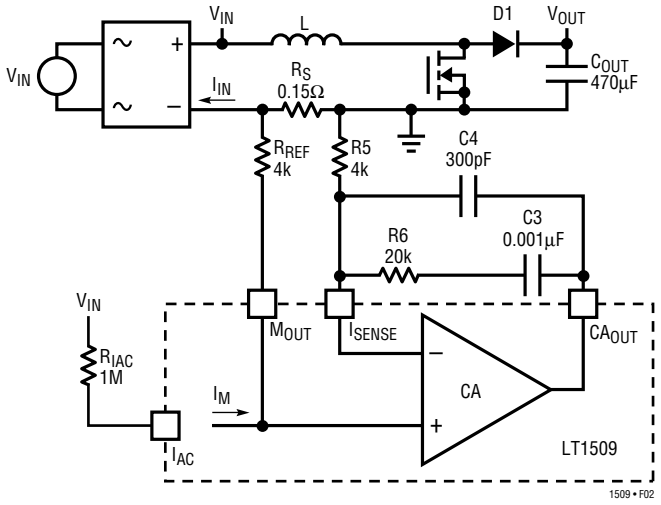


Figure 2

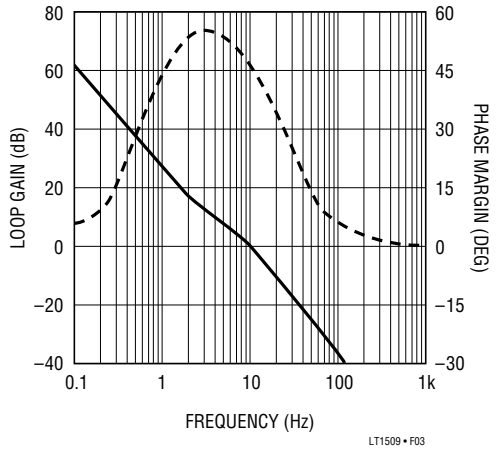


Figure 3

Current Amplifier (PFC Section)

The current amplifier has a 110dB DC gain, 3MHz unity-gain frequency and a 2V/µs slew rate. It is internally clamped at 8.5V. Note that in the current averaging operation, high gain at twice the line frequency is necessary to minimize line current distortion. Because CA_{OUT} may need to swing 5V over one line cycle at high line condition, 20mV AC will be needed at the inputs of the current amplifier for a gain of 260 at 120Hz. Especially at light load when the current loop reference signal is small, lower gain will distort the reference signal and line current. But, if signal gain at switching frequency is too high, the system behaves more like a current mode system and can cause subharmonic oscillation.

To avoid subharmonic oscillations, the amplified downslope of the inductor current must be less than the slope of the oscillator ramp.

$$\frac{V_{CA(OUT)}}{V_{RS}} \leq \frac{(V_{OSC})(L)(f_{SW})}{(V_{OUT})(R_S)}$$

$$= \frac{(5V)(500\mu H)(100k)}{(382V)(0.15\Omega)} = 4.4$$

If the current amplifier gain at 100kHz is less than 4.4, there will be no subharmonic oscillation. The open-loop gain of the current loop is given by:

$$\frac{V_{RS}}{V_{CA(OUT)}} = \frac{(V_{OUT})(R_S)}{(j)(2\pi f)(L)(V_{OSC})}$$

$$= \frac{(382V)(0.15\Omega)}{(j)(2\pi f)(500\mu H)(5V)} = \frac{3648}{(j)(f)}$$

The current error amp, with R5 = 4k, R6 = 20k, C3 = 0.001µF and C4 = 300pF, provides zero pole compensation resulting in 16kHz loop crossover frequency. The current amp gain at 100kHz is 1.7. The resulting current loop gain and phase margin is shown in Figure 4.

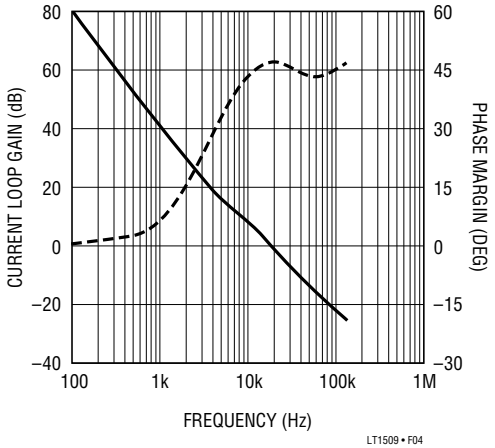


Figure 4

Multiplier

The multiplier has high noise immunity and superior linearity over its full operating range. The current gain is $I_M = (I_{AC}I_{EA}^2)/(200\mu A^2)$ with $I_{EA} = (VA_{OUT} – 2V)/ 25k$. The error amplifier output voltage required at the input to the multiplier is:

APPLICATIONS INFORMATION

$$VA_{OUT} = 2 + \sqrt{\frac{(P_{IN})(R_S)(25)(R_{IAC} + 25k)}{(V_{IN}^2)(R_{REF})}}$$

See Figure 2 for R_{REF}.

VA_{OUT} is squared in the multiplier, resulting in excellent performance over a wide range of output power and input voltage without the addition of feedforward line frequency ripple. Care must be taken to avoid feeding switching frequency noise into the multiplier from the I_{AC} pin. An internal 25k is provided in series with the low impedance multiplier input so that only a capacitor from the I_{AC} pin to GND1 is required to filter noise. The maximum multiplier output current, which ultimately limits the input line current, is set by a resistor from the R_{SET} pin to GND1 according to the formula: $I_{M(MAX)} = 3.75V/R_{SET}$. Figure 5 shows I_M versus I_{AC} for various values of VA_{OUT}. Note that Figure 5 data was taken with R_{SET} = 15k.

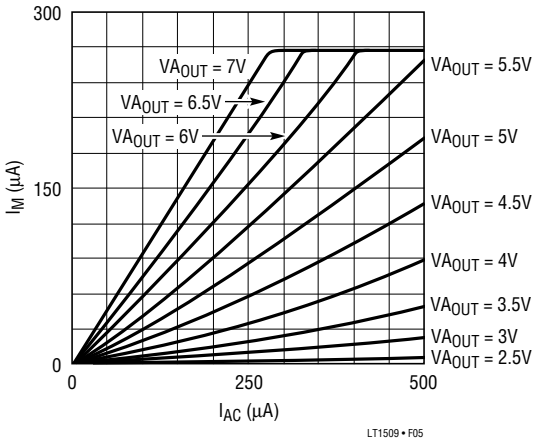


Figure 5. Multiplier Current I_M vs I_{AC} and VA_{OUT}

Oscillator Frequency and Maximum Line Current Setting

The oscillator frequency is set by R_{SET} and C_{SET}. R_{SET} is the resistor from the R_{SET} pin to GND1 and C_{SET} is the capacitor from the C_{SET} pin to GND1. R_{SET} should be determined first. The oscillator frequency, which is equal to the switching frequency for both the PFC and PWM section, is determined by:

$$f_{OSC} = \frac{1.5}{(R_{SET})(C_{SET})}$$

The multiplier output acts as the command signal to the current loop error amplifier. During steady-state operation the voltage across $R_{REF} = (I_M)(R_{REF}) = (I_{IN})(R_S)$. Based on this the value for R_S is determined by:

$$R_S \leq \frac{(I_{M(MAX)})(R_{REF})(V_{IN})(eff)}{P_{OUT}\sqrt{2}}$$

with R_{SET} = 15k, $I_{M(MAX)} = 3.75/15k = 250\mu A$. For a 300W converter with an efficiency (eff) of 0.8 at low line ($90V_{RMS}$) and R_{REF} set to 4k, R_S should be less than:

$$\frac{(250\mu A)(4k)(90VAC)(0.8)}{300W\sqrt{2}} = 0.169\Omega$$

A 0.15Ω resistor will yield a maximum peak input current of $(I_{M(MAX)})(R_{REF}/R_S) = (250\mu A)(4k)/0.15\Omega = 6.67A$. For a 100kHz switching frequency with R_{SET} = 15k, $C_{SET} = 1.5/(100kHz)(15k) = 1nF$. For added protection the LT1509 provides a second independent current limit comparator. When the input voltage to the comparator (PK_{LIM} pin) dips below 0V, GTDR1 pin quickly goes low turning off the PFC power switch. A resistor divider from V_{REF} to R_S (Figure 6) senses the voltage across the line current sense resistor (R_S) and limits the peak input line current to [(7.5V/R1) + 50µA] (R2/R_S). The 50µA represents the PK_{LIM} input current which flows out of the PK_{LIM} pin. With R1 = 10k and R2 = 1.8k, I_{IN} = 9.6A peak above the 6.67A peak average plus the input inductor peak ripple current.

Always use R_{SET} to set the primary line current limit. The PK_{LIM} comparator is only for secondary protection. When the line current reaches the primary limit, V_{OUT} can no longer be supported with the given input current and begins to fall. System stability is maintained by the current loop which is controlled by the current amplifier. When the

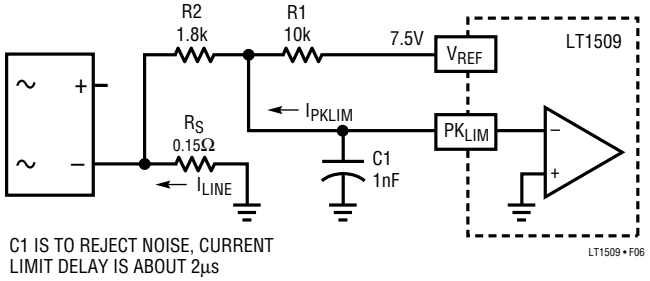


Figure 6

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line current reaches the secondary limit, the comparator takes over control and hysteresis may occur causing audible noise.

Overvoltage Protection (PFC Section)

Because of the slow loop response necessary for power factor correction, output overshoot can occur following a sudden load reduction or removal. To protect downstream components, the LT1509 provides an overvoltage comparator which senses the output voltage and quickly reduces the line current demand. Referring back to Figure 1, V_{OUT} is 382V and during normal operation, since no current flows in R3, 7.5V appears at both the V_{SENSE} and OVP pins. When V_{OUT} overshoots its preset value, the overcurrent from R1 will flow through R2 as well as R3. The voltage amplifier feedback will keep V_{SENSE} at 7.5V. Therefore, the equivalent AC resistance seen by the OVP pin is R2 in parallel with R3 or 10k. With these values and the overvoltage comparator trip level internally set at $1.05V_{REF}$, the comparator trips when V_{OUT} overshoots 10%. Overvoltage trip level is given by:

$$(\%)V_{OUT} = 5\%\left(\frac{R2 + R3}{R3}\right)$$

For additional protection, the OVP pin can be connected to V_{OUT} through an independent resistor divider (see Figure 7). This ensures overvoltage protection during safety agency abnormal testing conditions, such as opening R1 or shorting R2.

The output of the multiplier looks like a high impedance current source. In the current loop, offset line current is determined by multiplier offset current and input offset voltage of the current error amplifier. A –4mV current amplifier V_{OS} translates to 27mA line current and 6.7W input power for 250VAC line if a 0.15Ω sense resistor is used. Under a no-load condition or when the load power is less than the offset output power, the offset line current could slowly charge the output to an overvoltage level. This is because the best the overvoltage comparator can do is to reduce the multiplier output current to zero. Unfortunately, this does not guarantee zero output current if the current amplifier has offset. To regulate V_{OUT} under

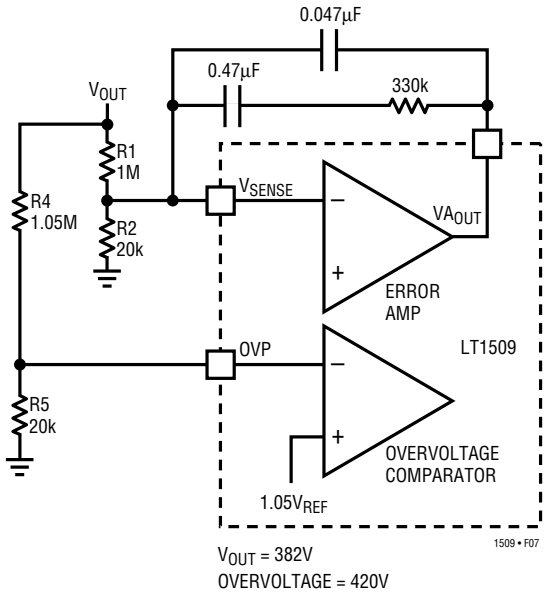

Figure 7

this condition, the amplifier M1 (see Block Diagram) becomes active. When VA_{OUT} reduces to 2.2V, M1 supplies up to 7µA of current to the resistor at the I_{SENSE} pin in order to cancel a negative V_{OS} and keep V_{OUT} error to within 2V.

Undervoltage Lockouts and Soft Start

The LT1509 turns on when V_{CC} reaches 16V and remains on until V_{CC} falls below 10V, whereupon the chip enters the lockout state. In the lockout state, the oscillator is off and the V_{REF} and gate driver pins remain low. A capacitor from SS1 to GND1 determines the ramp-up time of the PFC section. SS1 is released from a zero when V_{CC} rises above the lockout threshold. Once released, an internal 14µA current source ramps the voltage error amplifier's reference voltage to 7.5V. SS1 voltage then continues beyond 7.5V. A second capacitor from SS2 to GND1 determines the start-up time from the PWM section. A PWMOK comparator (see Block Diagram) holds SS2 low until the OVP pin reaches 7V. This corresponds to the PFC output voltage reaching approximately 93% of its preset voltage. SS2 is diode coupled to the PMW comparator which is connected to the V_C pin by a second diode. Holding SS2 low at any time will disable PWM output. Once released, the 14µA current source ramps the PWM comparator

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input up to V_C and then the SS2 voltage continues beyond V_C. The PWMOK comparator contains hysteresis and will pull SS2 low disabling the PWM section if the PFC output voltage falls below approximately 62% of its preset value (240V with nominal 382V output).

Start Up and Supply Voltage

The LT1509 draws only 250μA before the chip starts at 16V on V_{CC}. To trickle start, a 91k resistor from the power line to V_{CC} supplies trickle current, and C4 holds V_{CC} up while switching starts (see Figure 8); then the auxiliary winding takes over and supplies the operating current. Note that D3 and the larger values of C3 are only necessary for systems that have sudden large load variations down to minimum load and/or very light load conditions. Under these conditions the loop may exhibit a start/restart mode because switching remains off long enough for C4 to discharge below 10V. Large values for C3 will hold V_{CC} up until switching resumes. For less severe load variations D3 is replaced with a short and C3 is omitted. The turns ratio between the primary winding determines V_{CC} according to :

$$\frac{V_{OUT}}{V_{CC} - 2V} = \frac{N_P}{N_S}$$

for 382V V_{OUT} and 18V V_{CC}, Np/Ns ≈ 19.

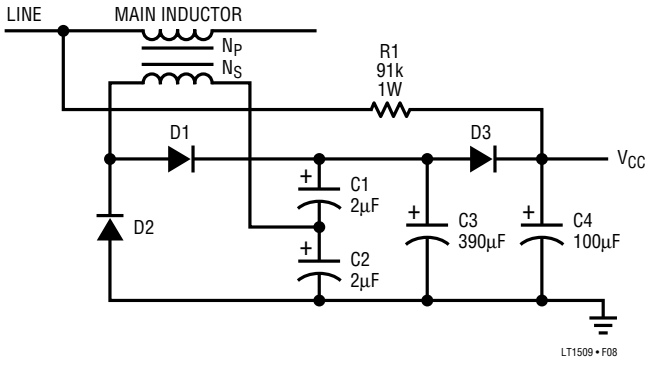

Figure 8

Output Capacitor (PFC Section)

GTDR2 (PWM) pulse is synchronized to GTDR1 (PFC) pulse with 53% duty cycle delay to reduce RMS ripple current in the output capacitor. See PFC/PWM Synchronization graph in the Typical Performance Characteristics section.

The peak-to-peak 120Hz PFC output ripple is determined by:

$$V_{P-P} = 2I_{LOAD(DC)}(Z)$$

where $I_{LOAD(DC)}$ is the DC load current of the PWM stage and Z is the capacitor impedance at 120Hz.

For 470μF, impedance is 2.8Ω at 120Hz. At 335W load, $I_{LOAD(DC)}$ = 335V/382V = 0.88A, V_{P-P} = (2)(0.88)(2.8Ω) = 5V. If less ripple is desired higher capacitance should be used. The selection of the output capacitor is based on voltage ripple, hold-up time and ripple current. Assuming the DC converter (PWM section) is designed to operate with 240V to 382V_{IN} , the minimum hold-up time is a function of the energy storage capacity of the capacitor:

$$t_{HOLD} = \frac{(0.5)C_{OUT}}{P_{OUT}}\left[(382V - 0.5V_{P-P})^2 - 240V^2\right]$$

with C_{OUT} = 470μF, V_{P-P} = 11.5V, and P_{OUT} = 335W, t_{HOLD} = 60ms which is 3.6 line cycles at 60Hz. The ripple current can be divided into two major components. The first is the 120Hz component which is related to the DC load current as follows:

$$I_{120HZ} \approx I_{LOAD(DC)}\sqrt{2}$$

The second component is made up of switching frequency components due to the PFC stage charging the capacitor and the PWM stage discharging the capacitor. For a 300W output PFC forward converter running from an input voltage of 100V_{RMS}, the total high frequency ripple current was measured to be 1.79A_{RMS}.

For the United Chemicon KMH 450V capacitor series, ripple current at 100kHz is specified 1.43 times higher than the 120Hz limit.

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The total equivalent 120Hz ripple in the output capacitor can be calculated by:

$$I_{RMS} = \sqrt{I_{120HZ}^2 + \left(\frac{I_{HF}}{1.43}\right)^2}$$

I_{HF} = 100kHz Ripple Current.

For $I_{LOAD(DC)}$ = 0.88A, 1_{120Hz} = 0.62A and the equivalent 120Hz ripple current is:

$$I_{RMS} = \sqrt{0.62^2 + \left(\frac{1.79}{1.43}\right)^2} = 1.4A_{RMS}$$

Table 1 lists the ripple current components from lab measurements for various output powers and line voltages. The 120Hz ripple current rating at 105°C ambient is 1.72A for the 470µF KMH 35mm × 50mm capacitor. The expected life of the output capacitor may be calculated from thermal stress analysis:

$$L = (L_O)2^{\left[\frac{(105°C + \Delta T_K) - (T_A + \Delta T_O)}{10}\right]}$$

where

L = Expected life time

L_O = Hours of load life at rated ripple current and rated ambient temperature

ΔT_K = Capacitor internal temperature rise at rated condition. $\Delta T_K = (I^2R)/(KA)$, where I is the rated current, R is capacitor ESR and KA is a volume constant.

T_A = Operating ambient temperature

ΔT_O = Capacitor internal temperature rise at operating condition

Table 1. PFC Capacitor RMS Ripple Current

	100W		200W		300W	
V_{INRMS}	I_{120HZ}	I_{HF}	I_{120HZ}	I_{HF}	I_{120HZ}	I_{HF}
100	0.2	0.6	0.41	1.18	0.62	1.79
120	0.2	0.5	0.41	0.97	0.62	1.45
230	0.2	0.53	0.41	0.87	0.62	1.26

In our example, L_O = 2000 hours assuming ΔT_K = 5°C at rated 1.72A. ΔT_O can then be calculated from:

$$\Delta T_O = \Delta T_K \left(\frac{I_{RMS}}{1.72A}\right)^2 = 5°C\left(\frac{1.4A}{1.72A}\right)^2 = 3.3°C$$

Assuming the operating ambient temperature is 60°C, the approximate lifetime is:

$$L = (2000)(2)^{\left[\frac{(105°C + 5°C) - (60 + 3.3°C)}{10}\right]}$$

= 50,870 Hours

For longer life a capacitor with a higher ripple current rating or parallel capacitors should be used.

PWM Comparators

The LT1509 includes two comparators in the PWM section which implement peak current mode control. The primary current sense voltage is fed into the RAMP pin. The V_C or Control Voltage pin sets the primary peak current level. An additional current limit comparator turns GTDR2 off in the event the RAMP pin voltage exceeds 1V. Referring to the Block Diagram, there is a 1.2V offset between the RAMP and V_C pin. This feature simplifies the connection to an optocoupler because the V_C pin no longer has to be pulled all the way to ground to inhibit switching. On-chip blanking avoids reset due to leading edge noise.

Typical Application

Figure 9 shows a 24VDC, 300W power factor corrected, universal input supply. The 2-transistor forward converter offers many benefits including low peak currents, nondissipative snubber, 500VDC switches and automatic core reset guaranteed by the LT1509's 50% maximum duty cycle.

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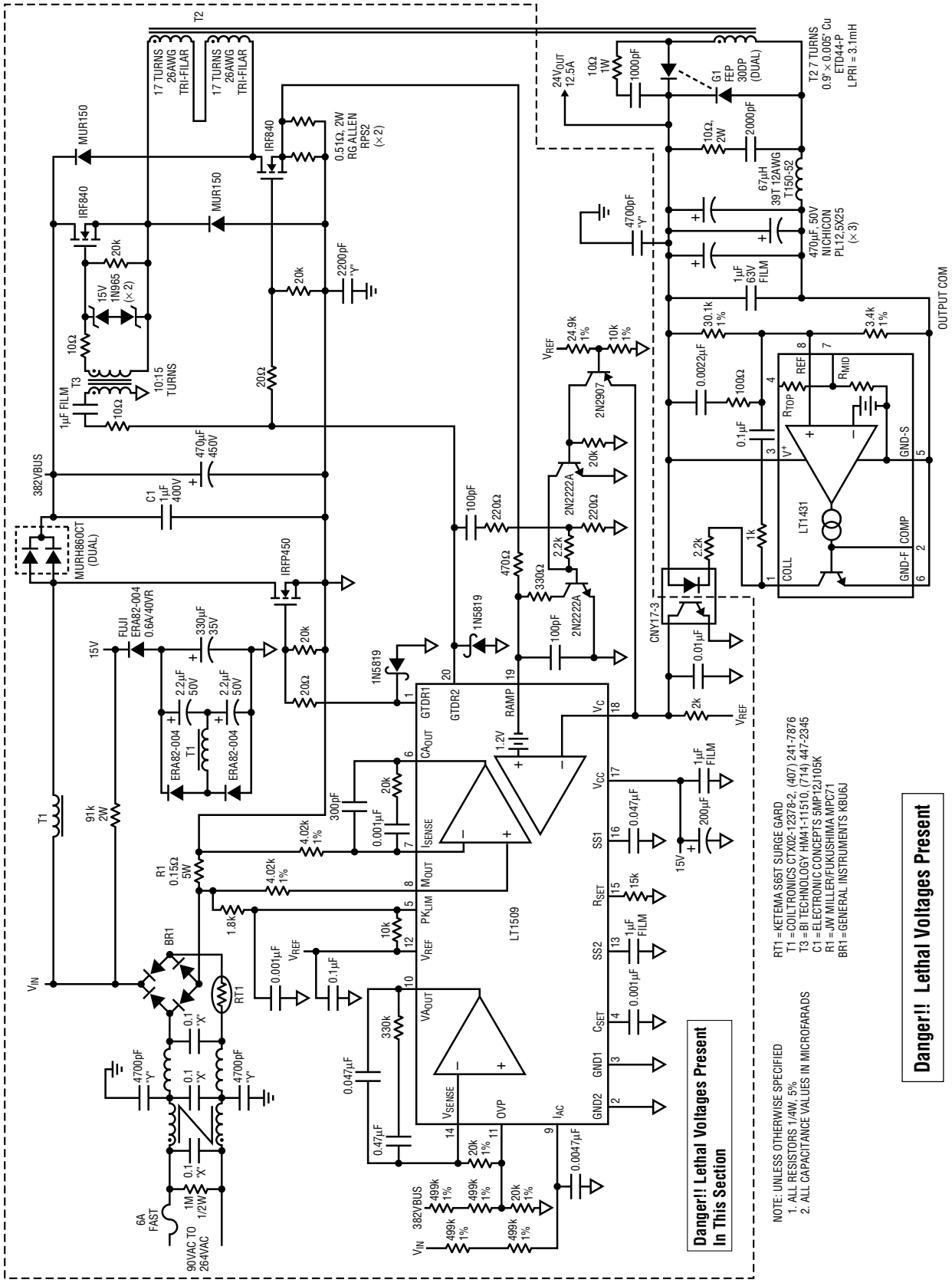

Figure 9. 24V, 300W Off-Line PFC Supply

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An LT1431 reference/amplifier coupled to a low cost optoisolator closes the loop from secondary side to primary side. Unity loop frequency is a conservative 3kHz. Figure 10 shows the output voltage's response with a 2A to almost 10A current step. Output voltage is maintained to within 0.5V during the load step. Efficiency versus power and line voltage is shown in Figure 11. The PFC preregulator alone has efficiency numbers between 90% and 97% over line and load.

A 3-turn secondary added to the 70-turn primary of T1 bootstraps V_{CC} to about 15V supplying the chip's 13mA requirement as well as about 39mA to cover the gate current of the three FETs and high side transformer. A 0.15Ω sense resistor is used to sense input current and servo to the command created by the outer voltage and multiplier. Thus the input current follows the input line voltage, and changes as necessary, in order to maintain constant bank voltage. The forward converter sees a voltage input of 382VDC unless the line voltage drops out, in which case the 470µF main capacitor discharges to 240VDC before the PWM stage is shut down. Compared to a typical off-line converter, the effective input voltage range of the forward converter is much smaller, simplifying the design. Additionally, the higher bus voltage provides greater hold-up times for given capacitor size.

Because the high side transformer effectively delays the turn-on reverse recovery spike past the end of the built-in blanking time, an external blanking transistor is needed. Controlling the output current during an output short circuit depends on the duty cycle reducing to a small fraction of steady state. An additional transistor disables blanking during turn-on and output short circuit.

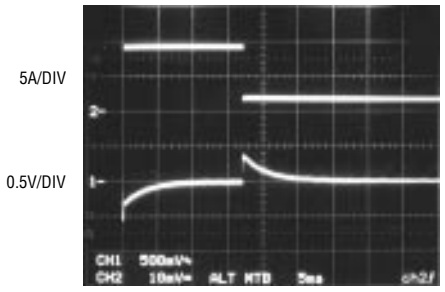


Figure 10

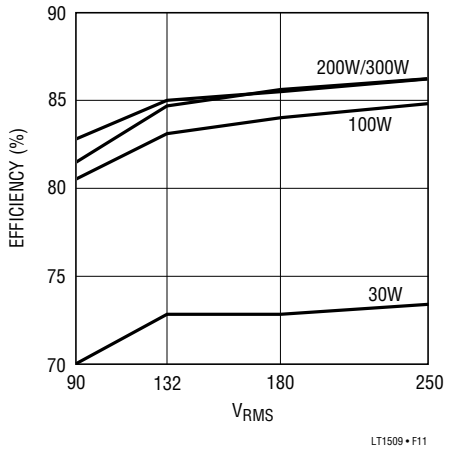
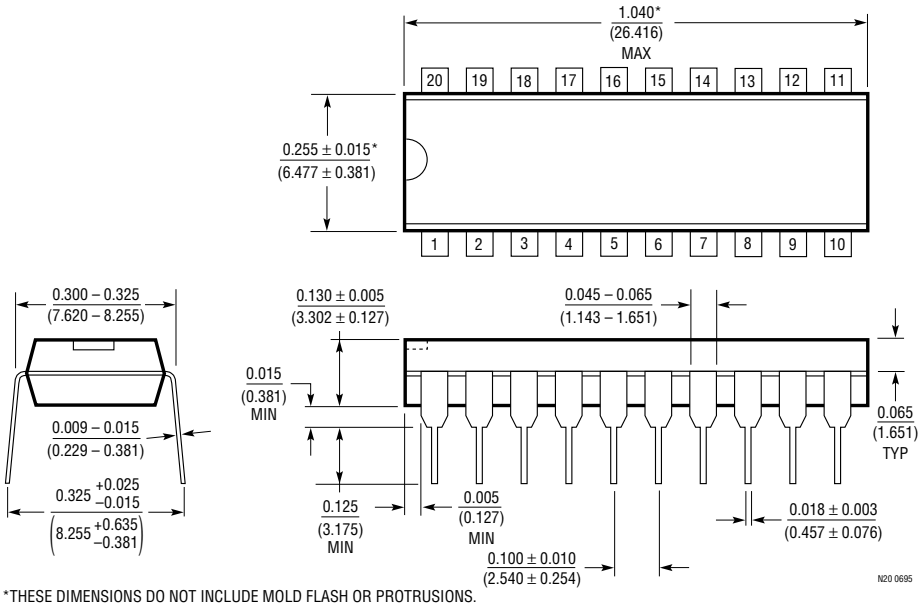


Figure 11

PACKAGE DESCRIPTION

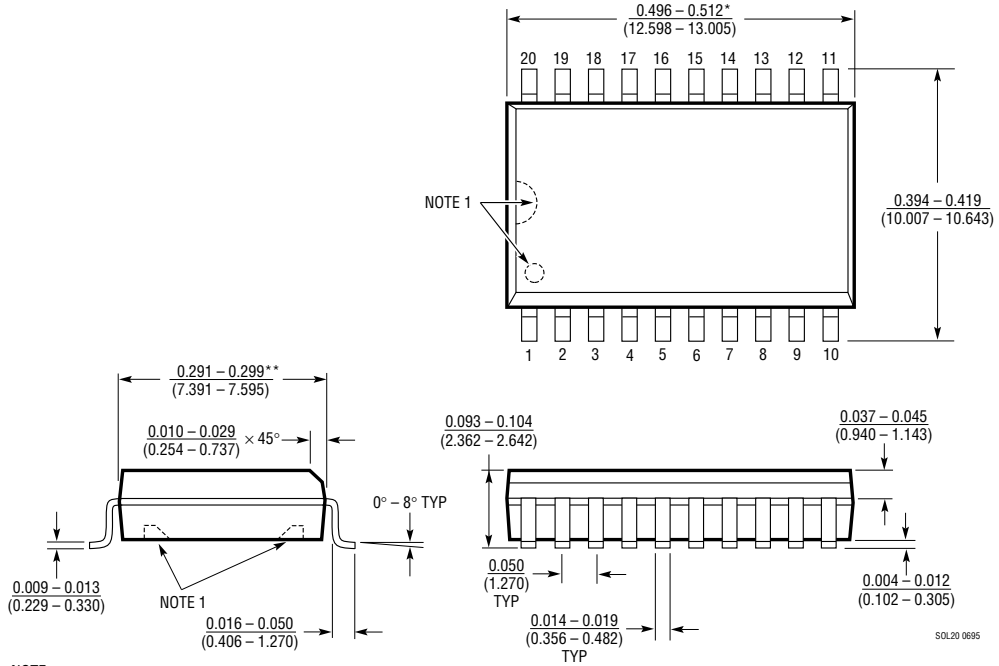
Dimension in inches (millimeters) unless otherwise noted.

N Package
20-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

SW Package
20-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE