SEPIC Constant-Current/ Constant-Voltage Battery Charger

FEATURES

- **Charger Input Voltage May Be Higher, Equal to or Lower Than Battery Voltage**
- **Charges Any Number of Cells Up to 30V***
- **1% Voltage Accuracy for Rechargeable Lithium Batteries**
- **500kHz Switching Frequency Minimizes Inductor Size**
- 100mV Current Sense Voltage for High Efficiency
- Battery Can Be Directly Grounded
- Charging Current Easily Programmable or Shut Down

APPLICATIONS

- Battery Charging of NiCd, NiMH, Lead-Acid or Lithium Rechargeable Cells
- Precision Current Limited Power Supply
- Constant-Voltage/Constant-Current Supply
- Transducer Excitation

*Maximum Input Voltage = 40V – V_{BAT}

DESCRIPTION

The LT®1512 is a 500kHz current mode switching regulator specially configured to create a constant-current/constant-voltage battery charger. In addition to the usual voltage feedback node, it has a current sense feedback circuit for accurately controlling output current of a flyback or SEPIC (Single-Ended Primary Inductance Converter) topology charger. These topologies allow the current sense circuit to be ground referred and completely separated from the battery itself, simplifying battery switching and system grounding problems. In addition, these topologies allow charging even when the input voltage is lower than the battery voltage.

Maximum switch current on the LT1512 is 1.5A. This allows battery charging currents up to 1A for a single lithium-ion cell. Accuracy of 1% in constant-voltage mode is perfect for lithium battery applications. Charging current can be easily programmed for all battery types.

TYPICAL APPLICATION

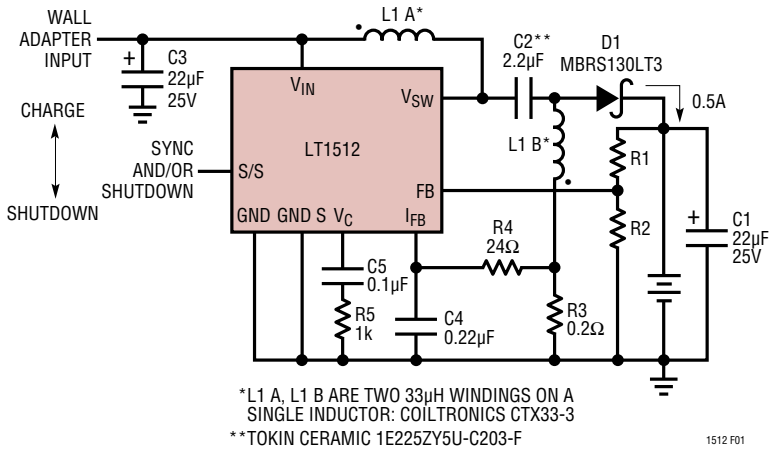
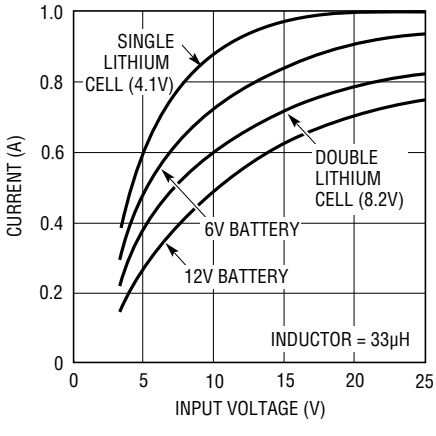


Figure 1. SEPIC Charger with 0.5A Output Current

Maximum Charging Current



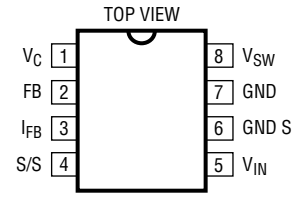
ACTUAL PROGRAMMED CHARGING CURRENT WILL BE INDEPENDENT OF INPUT VOLTAGE AND BATTERY VOLTAGE IF IT DOES NOT EXCEED THE VALUES SHOWN. THESE ARE ELECTRICAL LIMITATIONS BASED ON MAXIMUM SWITCH CURRENT. PACKAGE THERMAL LIMITATIONS MAY REDUCE MAXIMUM CHARGING CURRENT. SEE APPLICATIONS INFORMATION.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Voltage 30V
Switch Voltage 40V
S/S Pin Voltage 30V
FB Pin Voltage (Transient, 10ms) ..... ±10V
V_{FB} Pin Current 10mA
I_{FB} Pin Voltage (Transient, 10ms) ..... ±10V
Storage Temperature Range..... –65°C to 150°C
Ambient Temperature Range
LT1512C (Note 2)..... 0°C to 70°C
LT1512I..... –40°C to 85°C
Operating Junction Temperature Range
LT1512C (Note 2)..... –20°C to 125°C
LT1512I..... –40°C to 125°C
Short Circuit..... 0°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 130°C/W (S)

NOTE: CONTACT FACTORY CONCERNING 16-LEAD
FUSED-LEAD GN PACKAGE WITH LOWER THERMAL RESISTANCE

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1512CN8#PBF	LT1512CN8#TRPBF	1512	8-Lead PDIP	0°C to 70°C
LT1512CS8#PBF	LT1512CS8#TRPBF	1512	8-Lead Plastic SO	0°C to 70°C
LT1512IN8#PBF	LT1512IN8#TRPBF	1512I	8-Lead PDIP	–40°C to 85°C
LT1512IS8#PBF	LT1512IS8#TRPBF	1512I	8-Lead Plastic SO	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT1512CN8	LT1512CN8#TR	1512	8-Lead PDIP	0°C to 70°C
LT1512CS8	LT1512CS8#TR	1512	8-Lead Plastic SO	0°C to 70°C
LT1512IN8	LT1512IN8#TR	1512I	8-Lead PDIP	–40°C to 85°C
LT1512IS8	LT1512IS8#TR	1512I	8-Lead Plastic SO	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, V_C = 0.6V, V_{FB} = V_{REF}, I_{FB} = 0V, V_{SW} and S/S pins open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	V_{FB} Reference Voltage	Measured at FB Pin V_C = 0.8V	 ●	1.233 1.228	1.245 1.245	1.257 1.262	V V
	FB Input Current	V_{FB} = V_{REF}	 ●		300	550 600	nA nA
	FB Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 25V, V_C = 0.8V	●		0.01	0.03	%/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, V_C = 0.6V, V_{FB} = V_{REF}, I_{FB} = 0V, V_{SW} and S/S pins open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IREF}	I_{FB} Reference Voltage	Measured at I_{FB} Pin V_{FB} = 0V, V_C = 0.8V	 ●	–107 –110	–100 –100	–93 –90	mV mV
	I_{FB} Input Current	V_{IFB} = V_{IREF} (Note 3)	●	10	25	35	µA
	I_{FB} Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 25V, V_C = 0.8V	●		0.01	0.05	%/V
g_m	Error Amplifier Transconductance	ΔI_C = ±25µA	 ●	1100 700	1500	1900 2300	µmho µmho
	Error Amplifier Source Current	V_{FB} = V_{REF} – 150mV, V_C = 1.5V	●	120	200	350	µA
	Error Amplifier Sink Current	V_{FB} = V_{REF} + 150mV, V_C = 1.5V	●		1400	2400	µA
	Error Amplifier Clamp Voltage	High Clamp, V_{FB} = 1V Low Clamp, V_{FB} = 1.5V		1.70 0.25	1.95 0.40	2.30 0.52	V V
A_V	Error Amplifier Voltage Gain				500		V/V
	V_C Pin Threshold	Duty Cycle = 0%		0.8	1	1.25	V
f	Switching Frequency	2.7V ≤ V_{IN} ≤ 25V 0°C ≤ T_J ≤ 125°C –40°C ≤ T_J < 0°C (LT1512I)	 ● 	450 430 400	500 500	550 580 580	kHz kHz kHz
	Maximum Switch Duty Cycle		●	85	95		%
	Switch Current Limit Blanking Time				130	260	ns
BV	Output Switch Breakdown Voltage	0°C ≤ T_J ≤ 125°C –40°C ≤ T_J < 20°C (LT1512I)	● 	40 35	47		V V
V_{SAT}	Output Switch ON Resistance	I_{SW} = 2A	●		0.5	0.8	Ω
I_{LIM}	Switch Current Limit	Duty Cycle = 50% Duty Cycle = 80% (Note 4)	● ●	1.5 1.3	1.9 1.7	2.7 2.5	A A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch ON Time				15	25	mA/A
	Control Voltage to Switch Current Transconductance				2		A/V
	Minimum Input Voltage		●		2.4	2.7	V
I_Q	Supply Current	2.7V ≤ V_{IN} ≤ 25V	●		4	5.5	mA
	Shutdown Supply Current	2.7V ≤ V_{IN} ≤ 25V, $V_{S/S}$ ≤ 0.6V 0°C ≤ T_J ≤ 125°C –40°C ≤ T_J ≤ 0°C (LT1512I)	 ● 		12	30 50	µA µA
	Shutdown Threshold	2.7V ≤ V_{IN} ≤ 25V	●	0.6	1.3	2	V
	Shutdown Delay		●	5	12	25	µs
	S/S Pin Input Current	0V ≤ $V_{S/S}$ ≤ 5V	●	–10		15	µA
	Synchronization Frequency Range		●	600		800	kHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Commercial devices are guaranteed over 0°C to 125°C junction temperature range and 0°C to 70°C ambient temperature range. These parts are also designed, characterized and expected to operate over the –20°C to 85°C extended ambient temperature range, but are not tested at –20°C or 85°C. Devices with full guaranteed electrical specifications over the ambient temperature range –40°C to 85°C are available as industrial parts with an "I" suffix.

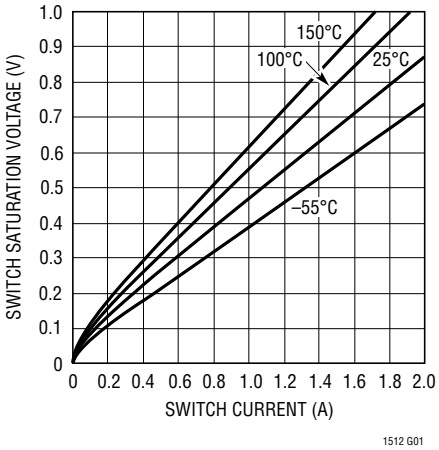
Maximum allowable ambient temperature may be limited by power dissipation. Parts may not necessarily be operated simultaneously at maximum power dissipation and maximum ambient temperature. Temperature rise calculations must be done as shown in the Applications Information section to ensure that maximum junction temperature does not exceed 125°C limit. With high power dissipation, maximum ambient temperature may be less than 70°C.

Note 3: The I_{FB} pin is servoed to its regulating state with V_C = 0.8V.

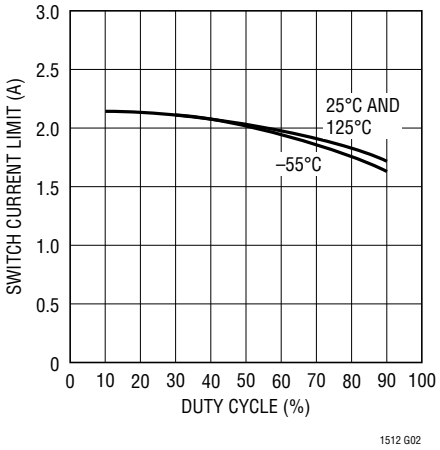
Note 4: For duty cycles (DC) between 50% and 85%, minimum guaranteed switch current is given by I_{LIM} = 0.667 (2.75 – DC).

TYPICAL PERFORMANCE CHARACTERISTICS

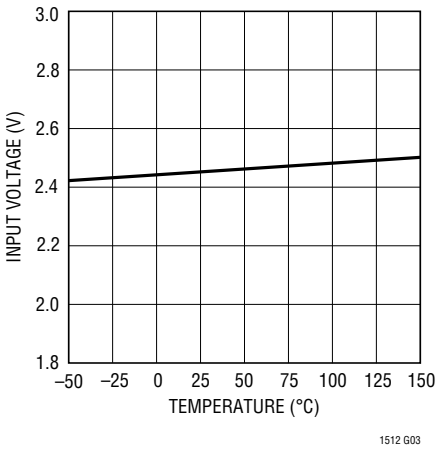
Switch Saturation Voltage vs Switch Current



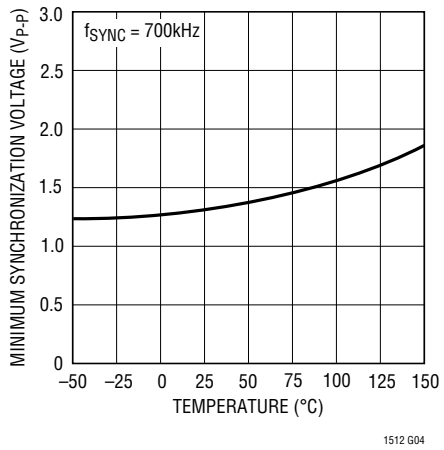
Switch Current Limit vs Duty Cycle



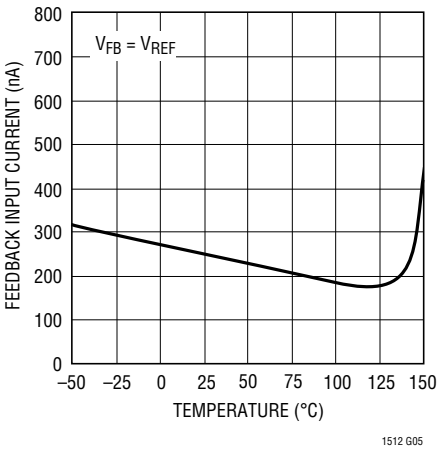
Minimum Input Voltage vs Temperature



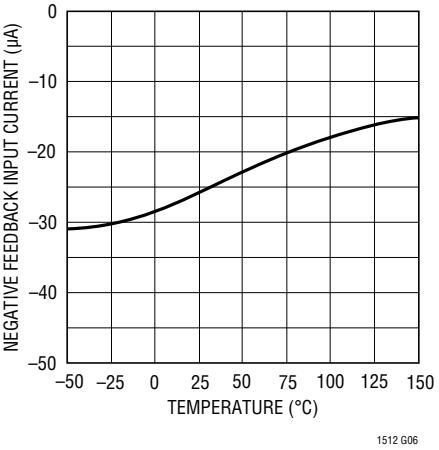
Minimum Peak-to-Peak Synchronization Voltage vs Temp



Feedback Input Current vs Temperature



Negative Feedback Input Current vs Temperature



PIN FUNCTIONS

V_C: The compensation pin is primarily used for frequency compensation, but it can also be used for soft starting and current limiting. It is the output of the error amplifier and the input of the current comparator. Peak switch current increases from 0A to 1.8A as the V_C voltage varies from 1V to 1.9V. Current out of the V_C pin is about 200µA when the pin is externally clamped below the internal 1.9V clamp level. Loop frequency compensation is performed with a capacitor or series RC network from the V_C pin *directly* to *the ground pin* (avoid ground loops).

FB: The feedback pin is used for positive output voltage sensing. This pin is the inverting input to the voltage error amplifier. The R1/R2 voltage divider connected to FB defines Li-Ion float voltage at full charge, or acts as a voltage limiter for NiCd or NiMH applications. Input bias current is typically 300nA, so divider current is normally set to 100µA to swamp out any output voltage errors due to bias current. The noninverting input of this amplifier is tied internally to a 1.245V reference. The grounded end of the output voltage divider should be connected directly to the LT1512 ground pin (avoid ground loops).

I_{FB}: The current feedback pin is used to sense charging current. It is the input to a current sense amplifier that controls charging current when the battery voltage is below the programmed voltage. During constant-current operation, the I_{FB} pin regulates at –100mV. Input resistance of this pin is 5kΩ, so filter resistance (R4, Figure 1) should be less than 50Ω. The 24Ω, 0.22µF filter shown in Figure 1 is used to convert the pulsating current in the sense resistor to a smooth DC current feedback signal.

S/S: This pin can be used for shutdown and/or synchronization. It is logic level compatible, but can be tied to V_{IN} if desired. It defaults to a high ON state when floated. A logic low state will shut down the charger to a micropower state. Driving the S/S pin with a continuous logic signal of 600kHz to 800kHz will synchronize switching frequency to the external signal. Shutdown is avoided in this mode with an internal timer.

V_{IN}: The input supply pin should be bypassed with a low ESR capacitor located right next to the IC chip. The grounded end of the capacitor must be connected directly to the ground plane to which the GND pin is connected.

GND S, GND: The LT1512 uses separate ground pins for switch current (GND) and the control circuitry (GND S). This isolates the control ground from any induced voltage created by fast switch currents. Both pins should be tied directly to the ground plane, but the external control circuit components such as the voltage divider, frequency compensation network and I_{FB} bypass capacitor should be connected directly to the GND S pin or to the ground plane close to the point where the GND S pin is connected.

V_{SW}: The switch pin is the collector of the power switch, carrying up to 1.5A of current with fast rise and fall times. Keep the traces on this pin as short as possible to minimize radiation and voltage spikes. In particular, the path in Figure 1 which includes SW to C2, D1, C1 and around to the LT1512 ground pin should be as short as possible to minimize voltage spikes at switch turn-off.

BLOCK DIAGRAM

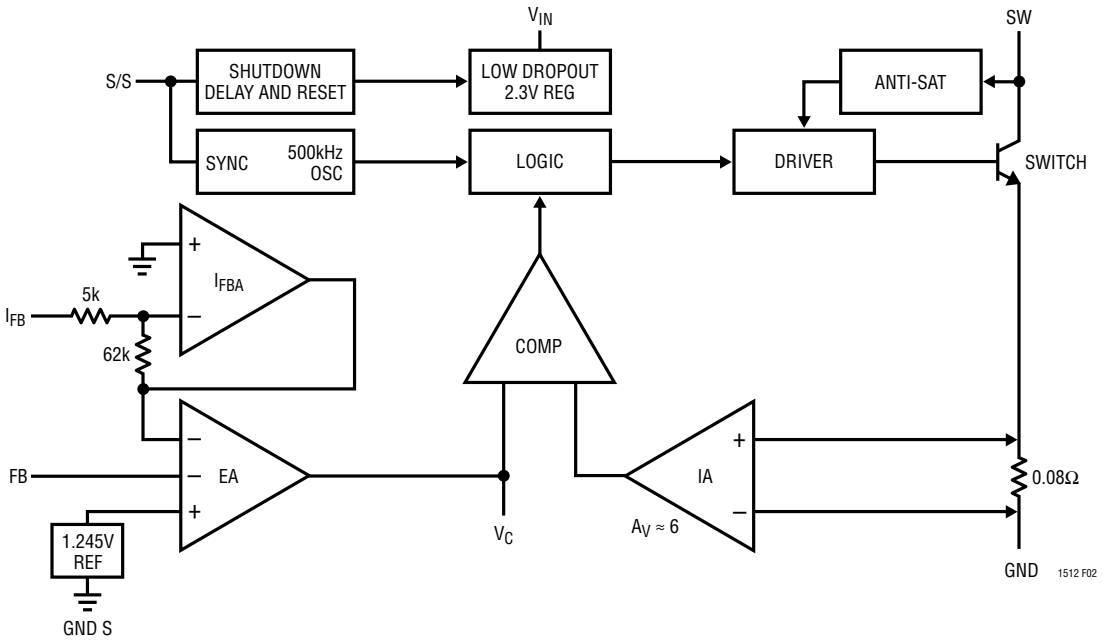


Figure 2

OPERATION

The LT1512 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage or current. Referring to the Block Diagram, the switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch current reaches a predetermined level. Control of output voltage and current is obtained by using the output of a dual feedback voltage sensing error amplifier to set switch current trip level. This technique has the advantage of simplified loop frequency compensation. A low dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1512. This low dropout design allows input voltage to vary from 2.7V to 25V. A 500kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Special adaptive antisat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A unique error amplifier design has two inverting inputs which allow for sensing both output voltage and current. A 1.245V bandgap reference biases the noninverting input. The first inverting input of the error amplifier is brought out for positive output voltage sensing. The second inverting input is driven by a "current" amplifier which is sensing output current via an external current sense resistor. The current amplifier is set to a fixed gain of –12.5 which provides a –100mV current limit sense voltage.

The error signal developed at the amplifier output is brought out externally and is used for frequency compensation. During normal regulator operation this pin sits at a voltage between 1V (low output current) and 1.9V (high output current). Switch duty cycle goes to zero if the V_C pin is pulled below the V_C pin threshold, placing the LT1512 in an idle mode.

APPLICATIONS INFORMATION

The LT1512 is an IC battery charger chip specifically optimized to use the SEPIC converter topology. The SEPIC topology has unique advantages for battery charging. It will operate with input voltages above, equal to or below the battery voltage, has no path for battery discharge when turned off and eliminates the snubber losses of flyback designs. It also has a current sense point that is ground referred and need not be connected directly to the battery. The two inductors shown are actually just two identical windings on one inductor core, although two separate inductors can be used.

A current sense voltage is generated with respect to ground across R3 in Figure 1. The average current through R3 is always identical to the current delivered to the battery. The LT1512 current limit loop will servo the voltage across R3 to –100mV when the battery voltage is below the voltage limit set by the output divider R1/R2. Constant current charging is therefore set at 100mV/R3. R4 and C4 filter the current signal to deliver a smooth feedback voltage to the I_{FB} pin. R1 and R2 form a divider for battery voltage sensing and set the battery float voltage. The suggested value for R2 is 12.4k. R1 is calculated from:

$$R1 = \frac{R2(V_{BAT} - 1.245)}{1.245 + R2(0.3\mu A)}$$

V_{BAT} = battery float voltage

0.3µA = typical FB pin bias current

A value of 12.4k for R2 sets divider current at 100µA. This is a constant drain on the battery when power to the charger is off. If this drain is too high, R2 can be increased to 41.2k, reducing divider current to 30µA. This introduces an additional uncorrectable error to the constant voltage float mode of about ±0.5% as calculated by:

$$V_{BAT}\ \text{Error} = \frac{\pm 0.15\mu A(R1)(R2)}{1.245(R1+R2)}$$

±0.15µA = expected variation in FB bias current around the nominal 0.3µA typical value.

With R2 = 41.2k and R1 = 228k, (V_{BAT} = 8.2V), the error due to variations in bias current would be ±0.42%.

A second option is to disconnect the voltage divider with a small NMOS transistor as shown in Figure 3. To ensure

APPLICATIONS INFORMATION

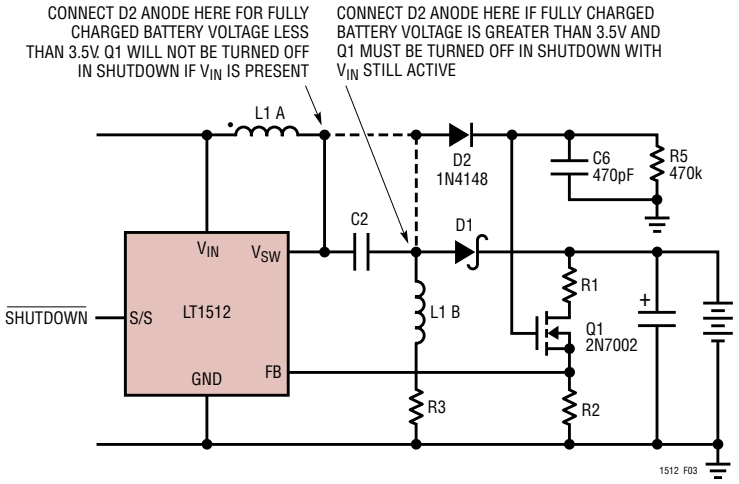


Figure 3. Eliminating Divider Current

adequate drive to the transistor (even when the V_{IN} voltage is at its lowest operating point of 2.4V), the FET gate is driven wth a peak detected voltage via D2. Note that there are two connections for D2. The L1 A connection must be used if the voltage divider is set for less than 3.5V (fully charged battery). Gate drive is equal to battery voltage *plus* input voltage. The disadvantage of this connection is that Q1 will still be "on" if the V_{IN} voltage is active and the charger is shut down via the S/S pin. The L1 B connection allows Q1 to turn off when V_{IN} is off or when shutdown is initiated, but the reduced gate drive (= V_{BAT}) is not adequate to ensure a Q1 on-state for fully charged battery voltages less than 3.5V. Do not substitute for Q1 unless the new device has adequate V_{GS} maximum rating, especially if D2 is connected to L1A. C6 filters the gate drive and R5 pulls the gate low when switching stops.

Disconnecting the divider leaves only D1 diode leakage as a battery drain. See Diode Selection for a discussion of diode leakage.

Maximum Input Voltage

Maximum input voltage for the circuit in Figure 1 is partly determined by battery voltage. A SEPIC converter has a maximum switch voltage equal to input voltage plus output voltage. The LT1512 has a maximum input voltage of 30V and a maximum switch voltage of 40V, so this limits maximum input voltage to 30V, or 40V – V_{BAT}, whichever is less. Maximum V_{BAT} = 40V – V_{IN}.

Shutdown and Synchronization

The dual function S/S pin provides easy shutdown and synchronization. It is logic level compatible and can be pulled high or left floating for normal operation. A logic low on the S/S pin activates shutdown, reducing input supply current to 12µA. To synchronize switching, drive the S/S pin between 600kHz and 800kHz.

Inductor Selection

L1A and L1B are normally just two identical windings on one core, although two separate inductors can be used. A typical value is 33µH, which gives about 0.25A peak-to-peak inductor current. Lower values will give higher ripple current, which reduces maximum charging current. 15µH can be used if charging currents are at least 20% lower than the values shown in the maximum charging current graph. Higher inductance values give slightly higher maximum charging current, but are larger and more expensive. A low loss toroid core such as KoolMµ, Molypermalloy or Metglas is recommended. Series resistance should be less than 0.1Ω for each winding. "Open core" inductors, such as rods or barrels are not recommended because they generate large magnetic fields which may interfere with other electronics close to the charger.

Input Capacitor

The SEPIC topology has relatively low input ripple current compared to other topologies and higher harmonics are

APPLICATIONS INFORMATION

especially low. RMS ripple current in the input capacitor is less than 0.1A with L = 33µH and less than 0.2A with L = 15µH. A low ESR 22µF, 25V solid tantalum capacitor (AVX type TPS or Sprague type 593D) is adequate for most applications with the following caveat. Solid tantalum capacitors can be destroyed with a very high turn-on surge current such as would be generated if a low impedance input source were "hot switched" to the charger input. If this condition can occur, the input capacitor should have the highest possible voltage rating, at least twice the surge input voltage if possible. Consult with the capacitor manufacturer before a final choice is made. A 2.2µF ceramic capacitor such as the one used for the coupling capacitor can also be used. These capacitors do not have a turn-on surge limitation. The input capacitor must be connected directly to the V_{IN} pin and the ground plane close to the LT1512.

Output Capacitor

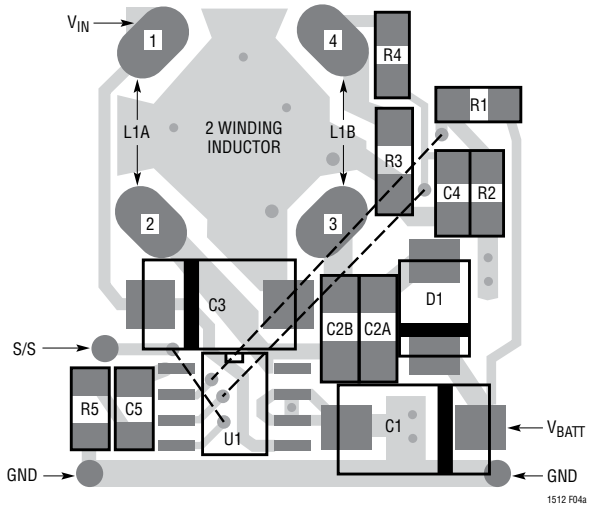
It is assumed as a worst case that all the switching output ripple current from the battery charger could flow in the output capacitor. This is a desirable situation if it is necessary to have very low switching ripple current in the battery itself. Ferrite beads or line chokes are often inserted in series with the battery leads to eliminate high frequency currents that could create EMI problems. This forces all the ripple current into the output capacitor. Total RMS current into the capacitor has a maximum value of about 0.5A, and this is handled with a 22µF, 25V capacitor shown in Figure 1. This is an AVX type TPS or Sprague type 593D surface mount solid tantalum unit intended for switching applications. Do not substitute other types without ensuring that they have adequate ripple current ratings. See Input Capacitor section for details of surge limitation on solid tantalum capacitors if the battery may be "hot switched" to the output of the charger.

Coupling Capacitor

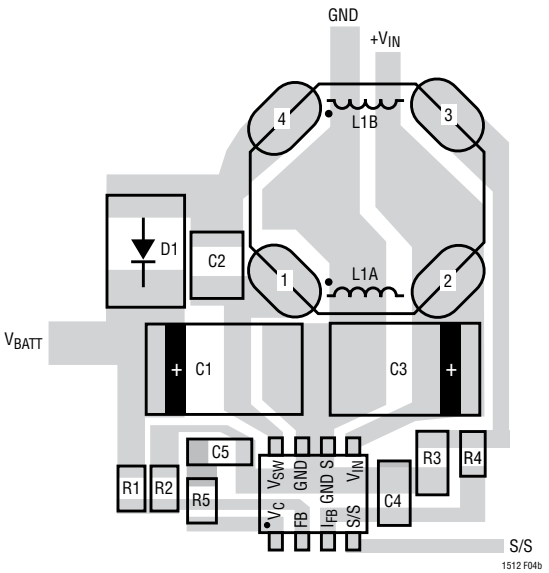
C2 in Figure 1 is the coupling capacitor that allows a SEPIC converter topology to work with input voltages either higher or lower than the battery voltage. DC bias on the capacitor is equal to input voltage. RMS ripple current in the coupling capacitor has a maximum value of about 0.5A at full charging current. A conservative formula to calculate this is:

$$I_{COUP(RMS)} = \frac{I_{CHRG}(V_{IN} + V_{BAT})(1.1)}{2(V_{IN})}$$

(1.1 is a fudge factor to account for inductor ripple current and other losses)



a. Double-Sided (Vias Connect to the Backside of Ground Plane. Dash Lines Indicate Interconnects on Backside. Demo Board Uses This Layout, Except that R5 Has Been Added to Increase Phase Margin)



b. Single-Sided Alternative Layout

Figure 4. LT1512 Suggested Layouts for Critical Thermal and Electrical Paths

APPLICATIONS INFORMATION

With I_{CHRG} = 0.5A, V_{IN} = 15V and V_{BAT} = 8.2V, I_{COUP} = 0.43A

The recommended capacitor is a 2.2µF ceramic type from Marcon or Tokin. These capacitors have extremely low ESR and high ripple current ratings in a small package. Solid tantalum units can be substituted if their ripple current rating is adequate, but typical values will increase to 22µF or more to meet the ripple current requirements.

Diode Selection

The switching diode should be a Schottky type to minimize both forward and reverse recovery losses. Average diode current is the same as output charging current , so this will be under 1A. A 1A diode is recommended for most applications, although smaller devices could be used at reduced charging current. *Maximum diode reverse voltage will be equal to input voltage plus battery voltage.*

Diode reverse leakage current will be of some concern during charger shutdown. This leakage current is a direct drain on the battery when the charger is not powered. High current Schottky diodes have relatively high leakage currents (2µA to 200µA) even at room temperature. The latest very-low-forward devices have especially high leakage currents. It has been noted that surface mount versions of some Schottky diodes have as much as ten times the leakage of their through-hole counterparts. This may be because a low forward voltage process is used to reduce power dissipation in the surface mount package. In any case, check leakage specifications carefully before making a final choice for the switching diode. Be aware that diode manufacturers want to specify a maximum leakage current that is ten times higher than the typical leakage. It is very difficult to get them to specify a low leakage current in high volume production. This is an on going problem for all battery charger circuits and most customers have to settle for a diode whose typical leakage is adequate, but theoretically has a worst-case condition of higher than desired battery drain.

Thermal Considerations

Care should be taken to ensure that worst-case conditions do not cause excessive die temperatures. Typical thermal resistance is 130°C/W for the S8 package but this number will vary depending on the mounting technique (copper area, air flow, etc).

Average supply current (including driver current) is:

$$I_{IN} = 4mA + \frac{(V_{BAT})(I_{CHRG})(0.024)}{V_{IN}}$$

Switch power dissipation is given by:

$$P_{SW} = \frac{(I_{CHRG})^2(R_{SW})(V_{BAT}+V_{IN})(V_{BAT})}{(V_{IN})^2}$$

R_{SW} = output switch ON resistance

Total power dissipation of the die is equal to supply current times supply voltage, plus switch power:

$P_{D(TOTAL)} = (I_{IN})(V_{IN}) + P_{SW}$

For V_{IN} = 10V, V_{BAT} = 8.2V, I_{CHRG} = 0.5A, R_{SW} = 0.65Ω

I_{IN} = 4mA + 10mA = 14mA

P_{SW} = 0.24W

P_D = (0.014)(10) + 0.24 = 0.38W

The S8 package has a thermal resistance of 130°C/W. (Contact factory concerning 16-lead fused-lead package with footprint approximately same as S8 package and with lower thermal resistance.) Die temperature rise will be (0.38W)(130°C/W) = 49°C. A maximum ambient temperature of 60°C will give a die temperature of 60°C + 49°C = 109°C. This is only slightly less than the maximum junction temperature of 125°C, illustrating the importance of doing these calculations!

Programmed Charging Current

LT1512 charging current can be programmed with a PWM signal from a processor as shown in Figure 5. C6 and D2 form a peak detector that converts a positive logic signal to a negative signal. The average negative signal at the

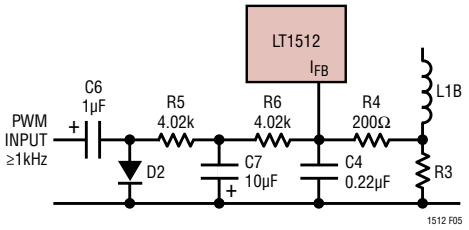


Figure 5. Programming Charge Current

APPLICATIONS INFORMATION

input to R5 is equal to the processor V_{CC} level multiplied by the inverse PWM ratio. This assumes that the PWM signal is a CMOS output that swings rail-to-rail with a source resistance less than a few hundred ohms. The negative voltage is converted to a current by R5 and R6 and filtered by C7. This current multiplied by R4 generates a voltage that subtracts from the 100mV sense voltage of the LT1512. This is not a high precision technique because of the errors in V_{CC} and the diode voltage, but it can typically be used to adjust charging current over a 20% to 100% range with good repeatability (full charging current accuracy is not affected). To reduce the load on the logic signal, R4 has been increased from 24Ω to 200Ω. This causes a known increase in full-scale charging current (PWM = 0) of 3% due to the 5k input resistance of the I_{FB} pin. Note that 100% duty cycle gives full charging current and that very low duty cycles (especially zero!) will not operate correctly. Very low duty cycle (<10%) is a problem because the peak detector requires a finite up-time to reset C6.

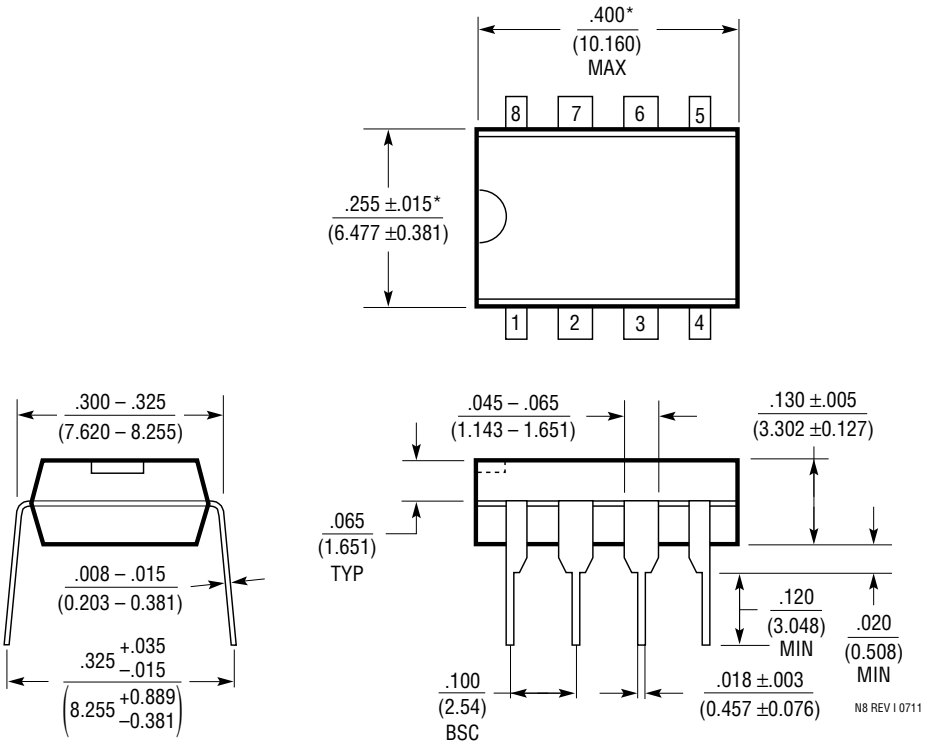
More Help

Linear Technology Field Application Engineers have a CAD spreadsheet program for detailed calculations of circuit operating conditions, and our Applications Department is always ready to lend a helping hand. For additional information refer to the LT1372 data sheet. This part is identical to the LT1512 except for the current amplifier circuitry.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510 Rev I)



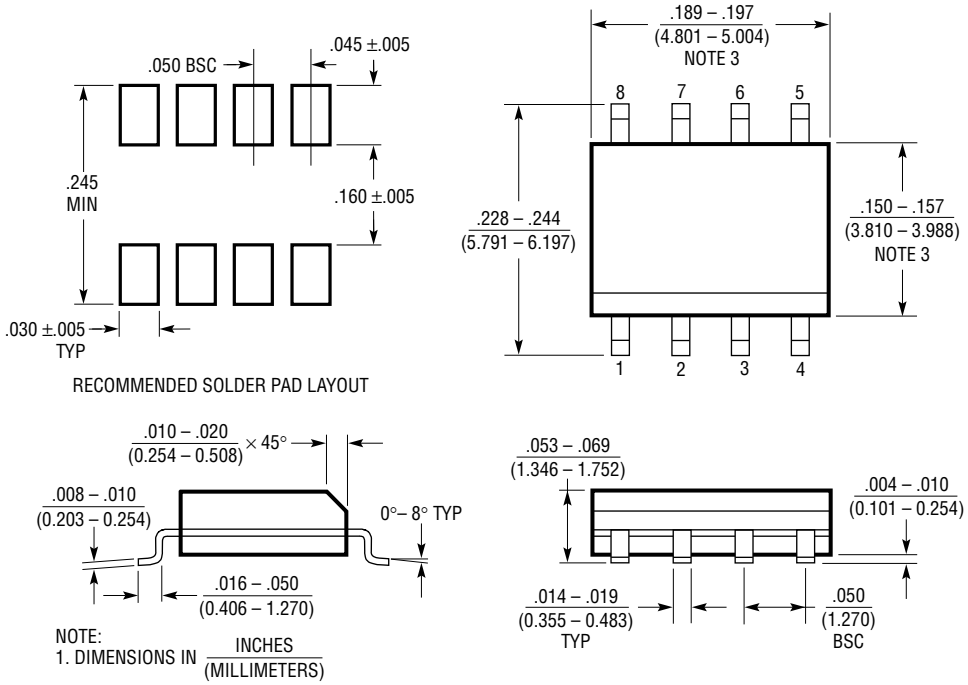
NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610 Rev G)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

SO8 REV G 0212

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	6/14	Reconfigured inputs to LM301	14
C	3/15	Changed inductor value units from “mH” to “µH”	1, 14