1.4nV/√Hz 180MHz Filter Building Block

FEATURES

- **Single-Ended to Differential Conversion**
- **Low Noise: 1.4nV/√Hz**
- **20μV_{RMS} Total Wideband Noise in Filter with 2MHz f_C**
- Dynamic Range: 104dB SNR at ±5V
- Total Supply Voltage: 2.7V to 12V
- Rail-to-Rail Outputs
- DC Accurate: Op Amp V_{OS} 0.5mV (Typ)
- Trimmed Bandwidth for Accurate Filters
- No External Clock Required
- MSOP-8 Surface Mount Package

APPLICATIONS

- Low Noise, High Speed Filters to 5MHz
- Low Noise Differential Circuits
- Communication Channel or Roofing Filters
- Antialias or Reconstruction Filtering
- Video Signal Processing
- Single-Ended to Differential Conversion

DESCRIPTION

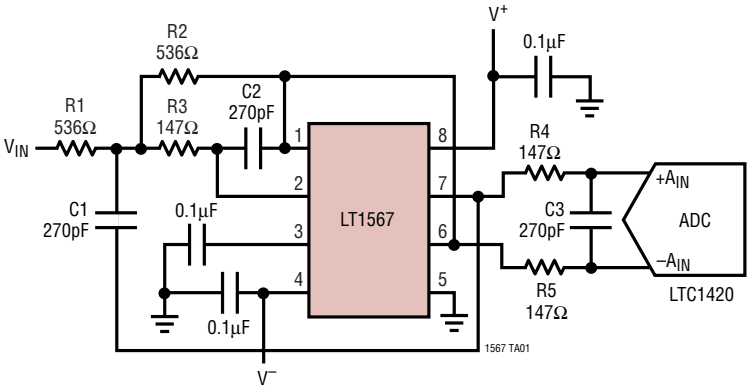
The LT®1567 is an analog building block optimized for very low noise high frequency filter applications. It contains two wideband rail-to-rail operational amplifiers, one of them internally configured as a unity-gain inverter. With the addition of a few passive components, the LT1567 becomes a flexible second order filter section with cutoff frequency (f_C) up to 5MHz, ideal for antialiasing or for channel filtering in high speed data communications systems. A spreadsheet-based design tool is available at www.linear.com for designing lowpass and bandpass filters using the LT1567.

In addition to low noise and high speed, the LT1567 features single-ended to differential conversion for direct driving of high speed differential input A/D converters. The LT1567 operates from a total power supply voltage of 2.7V to 12V and supports signal-to-noise ratios above 100dB.

The LT1567 is available in an 8-lead MSOP package.

TYPICAL APPLICATION

2MHz 3-Pole Antialias Filter with Single-Ended to Differential Conversion



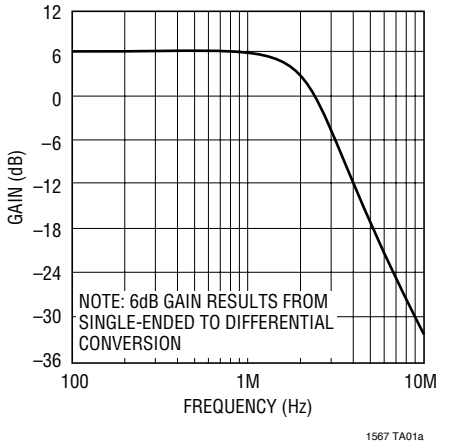
96dB DIFFERENTIAL SNR WITH 3V TOTAL SUPPLY

$$GAIN = \frac{R2}{R1} \leq \frac{2.5MHz}{f_{-3dB}}$$

R3 = R4 = R5, C1 = C2 = C3

$$f_{-3dB} = \frac{1.82}{2\pi R2C2} = \frac{1}{4\pi R3C3};\ f_{-3dB} \leq 2.5MHz$$

Frequency Response

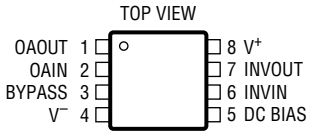


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 12.6V
Input Current (Note 2) ..... ±25mA
Operating Temperature Range (Note 3)
LT1567C ..... –40°C to 85°C
LT1567I ..... –40°C to 85°C
Specified Temperature Range (Note 4)
LT1567C ..... –40°C to 85°C
LT1567I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 200°C/W

ORDER PART NUMBER
LT1567CMS8 LT1567IMS8
MS8 PART MARKING
LTWH LTWJ

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range (Note 4), otherwise specifications and typical values are at T_A = 25°C. V_S = ±2.5V, R_L = 1K, V_{OUT} = 0 on both amplifiers unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Total Supply Voltage			2.7		12	V
Supply Current	V_S = ±1.5V	●		8.5	15	mA
	V_S = ±2.5V	●		9	16	mA
	V_S = ±5V	●		11	19	mA
OA Output Positive Voltage Swing	V_S = ±1.5V, R_L = 1k	●	1.30	1.45		V
	V_S = ±2.5V, R_L = 1k	●	2.20	2.45		V
	V_S = ±2.5V, R_L=100	●	1.90	2.25		V
	V_S = ±5V, R_L = 1k	●	4.70	4.90		V
OA Output Negative Voltage Swing	V_S = ±1.5V, R_L = 1k	●	–1.30	–1.45		V
	V_S = ±2.5V, R_L = 1k	●	–2.20	–2.45		V
	V_S = ±2.5V, R_L=100	●	–2.00	–2.30		V
	V_S = ±5V, R_L = 1k	●	–4.70	–4.90		V
INV Output Positive Voltage Swing	V_S = ±1.5V, R_L = 1k	●	1.30	1.40		V
	V_S = ±2.5V, R_L = 1k	●	2.20	2.50		V
	V_S = ±2.5V, R_L = 100 (LT1567I Only, Note 5)	●	1.80	2.00		V
	V_S = ±5V, R_L = 1k	●	4.60	4.80		V
INV Output Negative Voltage Swing	V_S = ±1.5V, R_L = 1k	●	–1.30	–1.40		V
	V_S = ±2.5V, R_L = 1k	●	–2.20	–2.40		V
	V_S = ±2.5V, R_L = 100 (LT1567I Only, Note 5)	●	–1.80	–2.00		V
	V_S = ±5V, R_L = 1k	●	–4.50	–4.80		V
Common Mode Input Voltage Range (DC BIAS, Pin 5) (See Pin Functions)	V_S = ±1.5V, CMRR ≥ 40dB (Note 6)	●	–0.5		0.5	V
	V_S = ±5V, CMRR ≥ 40dB (Note 6)	●	–3.8		3.5	V
DC Common Mode Rejection Ratio (CMRR)	V_S = ±1.5V, DC BIAS = –0.25V to 0.25V	●	80			dB
	V_S = ±5V, DC BIAS = –2.5V to 2.5V	●	65	90		dB
DC Power Supply Rejection Ratio (PSRR)	V_S = ±1.5V to ±5V, DC BIAS = 0V	●	80	100		dB
OA Input Offset Voltage		●		0.5	3	mV
INV Output Offset Voltage		●		5	9	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range (Note 4), otherwise specifications and typical values are at T_A = 25°C. V_S = ±2.5V, R_L = 1K, V_{OUT} = 0 on both amplifiers unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OA Input Bias Current		●		3	10	µA
DC BIAS Input Bias Current		●		6	15	µA
OA DC Open-Loop Gain	V_S = ±1.5V, R_L = 1k, V_O = –1V to 1V V_S = ±2.5V, R_L = 1k, V_O = –2V to 2V V_S = ±2.5V, R_L = 100, V_O = –1.5V to 1.5V V_S = ±5V, R_L = 1k, V_O = –4V to 4V	● ● ● ●	7.5 10 1.2 10	55 60 7.0 80		V/mV V/mV V/mV V/mV
INV DC Gain	V_S = ±1.5V, R_L = 1k, V_{IN} = –1V to 1V V_S = ±2.5V, R_L = 1k, V_{IN} = –2V to 2V V_S = ±2.5V, R_L = 100, V_{IN} = –1.5V to 1.5V V_S = ±5V, R_L = 1k, V_{IN} = –4V to 4V	● ● ● ●	0.97 0.97 0.97 0.97		1.04 1.04 1.04 1.04	V/V V/V V/V V/V
INV DC Input Resistance	V_S = ±2.5V, R_L = 1k, V_{IN} = –2V to 2V	●	450	600	750	Ω
OA Gain Bandwidth Product	Measured at 2MHz, V_S = ±1.5V Measured at 2MHz, V_S = ±2.5V Measured at 2MHz, V_S = ±5V	● ● ●	100 110 120	180 185 190		MHz MHz MHz
INV Bandwidth	–3dB			85		MHz
INV AC Gain	Measured at 2MHz	●	0.96	1.0	1.05	V/V
OA Slew Rate	V_S = ±5V			55		V/µs
INV Slew Rate	V_S = ±5V			90		V/µs
OA Input Voltage Noise Density (Note 7)	f = 100kHz			1.4		nV/√Hz
OA Input Current Noise Density	f = 100kHz			1.0		pA/√Hz
Wideband Output Noise for a Second Order Filter (Figure 1)	f_C = 2MHz, BW = 4MHz (Note 8) f_C = 5MHz, BW = 10MHz (Note 8)			20 30		μV_{RMS} μV_{RMS}
Total Harmonic Distortion (THD) for a Second Order Filter (Figure 1)	f = 1MHz, f_C = 2MHz, V_{OUT} = $1V_{RMS}$ f = 2.5MHz, f_C = 5MHz, V_{OUT} = $1V_{RMS}$			–88 –70		dB dB
Output Short-Circuit Current (Note 9)		●	8	50		mA
OA Output Impedance	f = 100kHz, OA Connected as Unity-Gain Inverter			0.03		Ω
INV Output Impedance	f = 100kHz			0.7		Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs of each op amp are protected by back-to-back diodes and diodes to each supply. If either input exceeds the supply or the differential input voltage exceeds 1.4V, the input current should be limited to less than 25mA.

Note 3: The LT1567C and LT1567I are guaranteed functional over the operating temperature range –40°C to 85°C.

Note 4: The LT1567C is guaranteed to meet specified performance from 0°C to 70°C. The LT1567C is designed, characterized and expected to meet specified performance from –40°C to 85°C but not tested or QA sampled at these temperatures. The LT1567I is guaranteed to meet specified performance from –40°C to 85°C.

Note 5: With INVIN pin driven to ±2V.

Note 6: This parameter is not 100% tested.

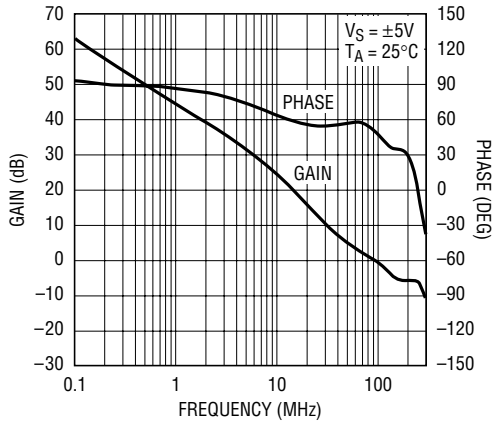
Note 7: The input referred voltage noise density of the unity gain inverter is 5.6nV/√Hz which includes the noise of the gain setting resistors.

Note 8: For f_C = 2MHz, C1 = C2 = 180pF, R1 = R2 = 604Ω, R3 = 316Ω and for f_C = 5MHz, C1 = C2 = 180pF, R1 = R2 = 232Ω, R1 = 130Ω. BW is the bandwidth of the noise measurement (Figure 1 circuit).

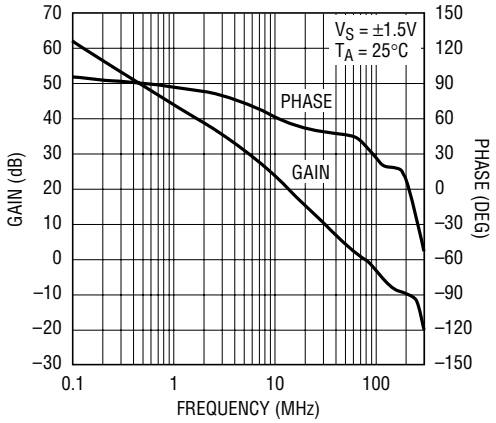
Note 9: Under direct short circuit conditions, with T_A < 25°C the output current is reduced.

TYPICAL PERFORMANCE CHARACTERISTICS

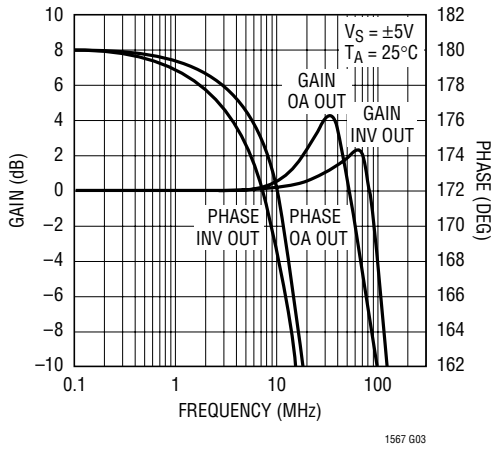
OA Open-Loop Gain and Phase vs Frequency



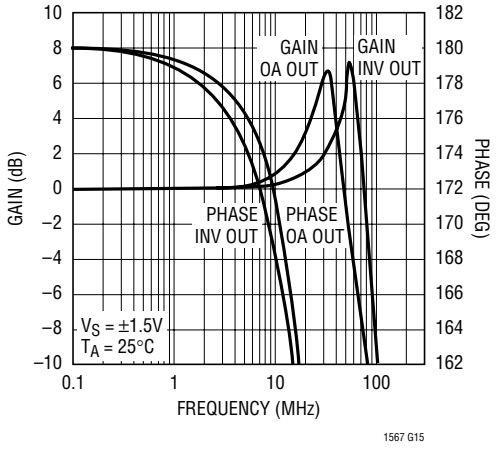
OA Open-Loop Gain and Phase vs Frequency



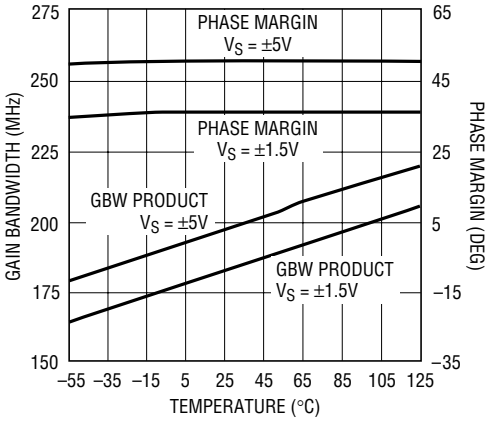
Closed-Loop Gain and Phase of OA and INV vs Frequency (A_V = –1)



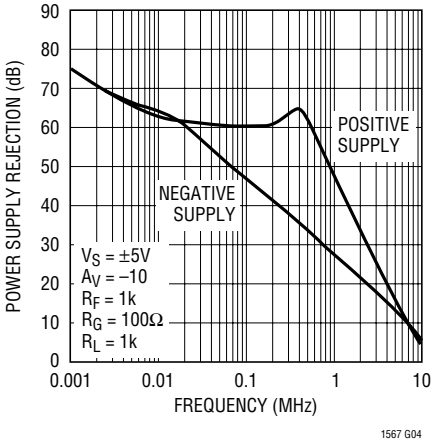
Closed-Loop Gain and Phase of OA and INV vs Frequency (A_V = –1)



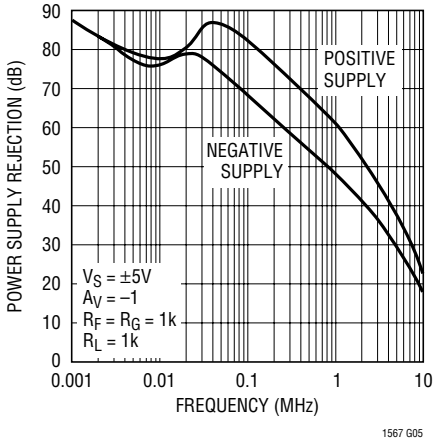
OA Gain Bandwidth Product and Phase Margin vs Temperature



PSRR of OA vs Frequency

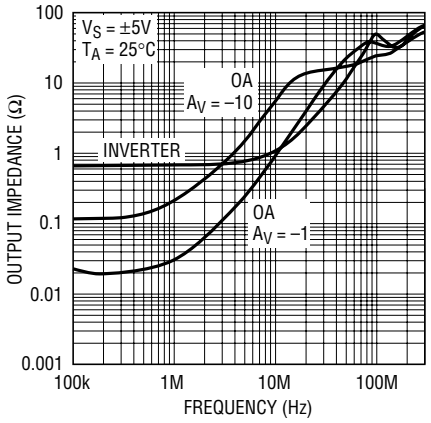


PSRR of OA or INV vs Frequency

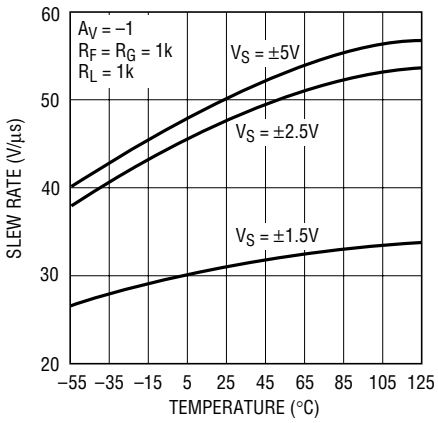


TYPICAL PERFORMANCE CHARACTERISTICS

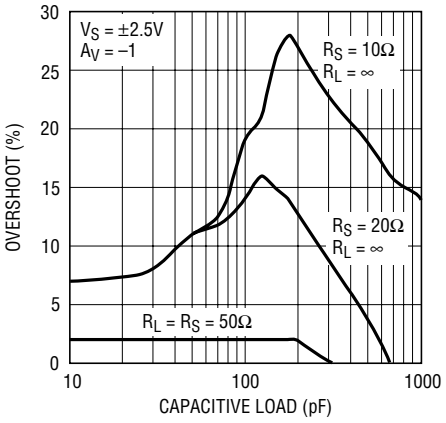
Output Impedance vs Frequency



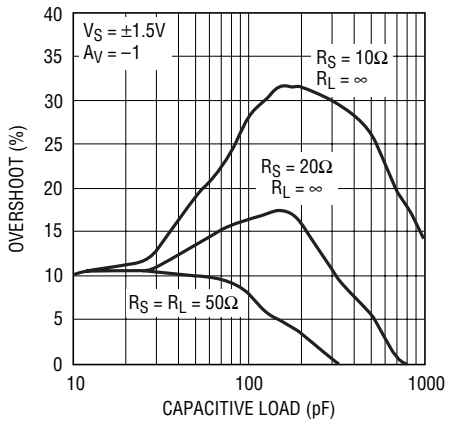
OA Rising Slew Rate vs Temperature



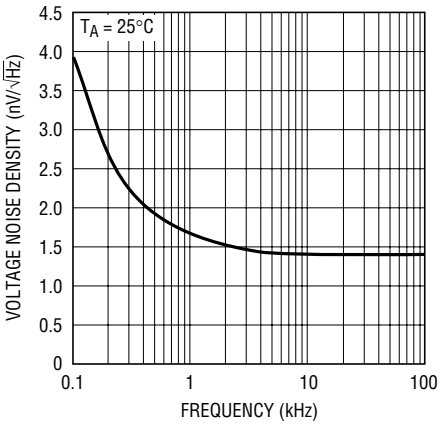
Output Overshoot vs Series Resistor and Capacitive Load



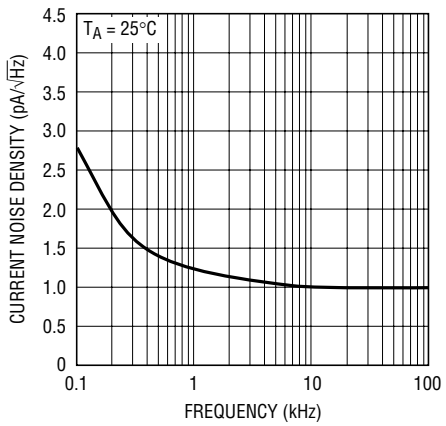
Output Overshoot vs Series Resistor and Capacitive Load



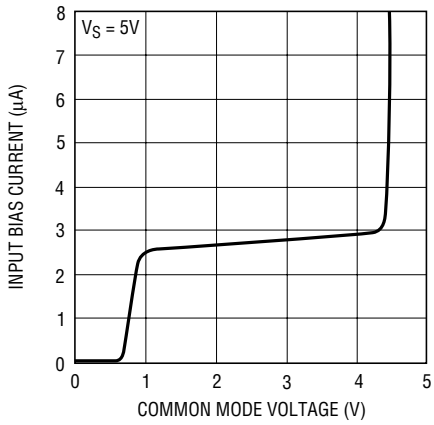
Input Voltage Noise Density of OA vs Frequency



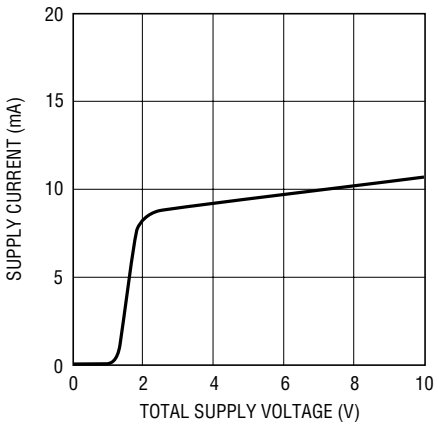
Input Current Noise Density of OA vs Frequency



Input Bias Current of OA vs Common Mode Voltage



Supply Current vs Supply Voltage



PIN FUNCTIONS

OAOUT (Pin 1): Output of the Uncommitted Op Amp (OA). As with most wideband op amps, it is important to avoid connecting heavy capacitive loads (above about 10pF) directly to this output. Such loads will impair AC stability and should be isolated from the output through series resistance.

OAIN (Pin 2): Inverting or "–" Input of the Uncommitted Op Amp (OA) in the LT1567. The noninverting or "+" input of this amplifier is shared with that of the INV amplifier and accessed via the DC BIAS and BYPASS pins. The OA amplifier is optimized for minimal wideband noise.

BYPASS (Pin 3): AC Ground Bypass. A decoupling capacitor, typically 0.1μF, from this pin to a printed circuit ground plane must be used. Use the shortest possible wiring.

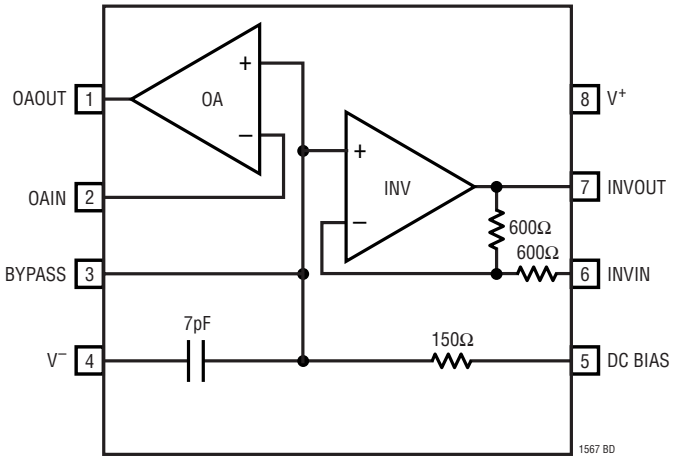
Power Supply Pins (Pins 4, 8): The V^- and V^+ pins should be bypassed with 0.1μF capacitors to an adequate analog ground plane using the shortest possible wiring. Electrically clean supplies and a low impedance ground are important to obtain the wide dynamic range and bandwidth available from the LT1567. Low noise linear power supplies are recommended. Switching supplies require special care because of the inevitable risk of their switching noise coupling into the signal path, reducing dynamic range.

DC BIAS (Pin 5): DC Biasing Input. Sets the DC voltage at the noninverting inputs of the two internal amplifiers; designed for use as a DC reference, not a signal input.The DC BIAS input includes a small series resistor, both to balance DC offsets in the presence of input bias currents and also to suppress the "Q" factor of possible parasitic high frequency resonant circuits introduced by wiring inductance. The reference voltage at the noninverting inputs of the two amplifiers is decoupled for very high frequencies with a small internal capacitor to the chip substrate, nominally 7pF. An external capacitor, typically 0.1μF, to a nearby ground plane must be added at Pin 3 (BYPASS) for a clean wideband DC reference biasing voltage.

INVIN (Pin 6): Unity-Gain Inverter Input. The "inverter" (INV) amplifier in the LT1567 is connected to internal resistors (nominally 600Ω each) to form a closed-loop amplifier with a wideband voltage gain of nominally –1. This amplifier is similar to the uncommitted op amp (OA) but is optimized for high frequency linearity.

INVOUT (Pin 7): Output of the INV or "Inverter" Amplifier, with a Nominal Gain of –1 from the INVIN Pin. As with most wideband op amps, it is important to avoid connecting heavy capacitive loads (above about 10pF) directly to this output. Such loads will impair AC stability and should be isolated from the output through series resistance.

BLOCK DIAGRAM



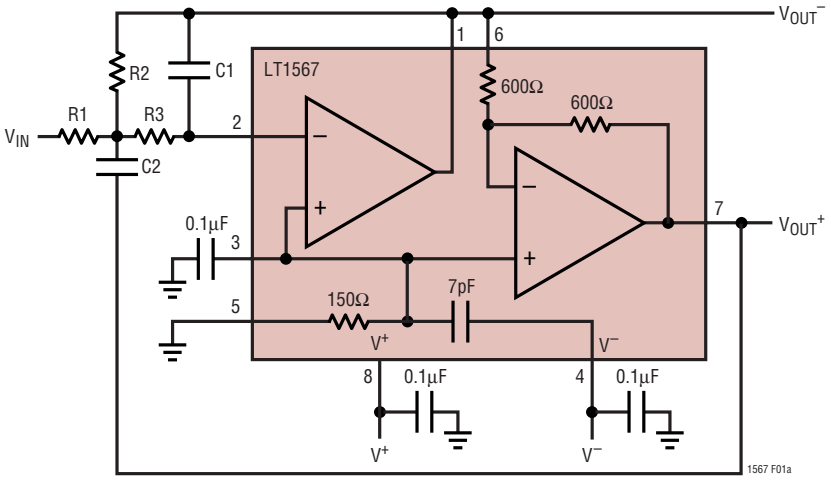
APPLICATIONS INFORMATION

Functional Description

The LT1567 contains two low noise rail-to-rail output, wideband operational amplifiers, one of them connected internally as a unity-gain inverter. These two amplifiers can form a second order multiple feedback filter configuration (Figure 1) for megahertz signal frequencies, with exceptionally low total noise. The amplifier in the dedicated inverter (INV) is optimized for better high frequency linearity while the uncommitted operational amplifier (OA) is optimized for lower input noise voltage, addressing the different sensitivities to these effects when used as a filter section. This combination produces a low noise filter with better distortion performance than would be possible with identical amplifiers.

LT1567 Free Design Software

A spreadsheet-based design tool is available at www.linear.com for designing lowpass and bandpass filters using the LT1567.



DESIGN EQUATIONS:

GAIN = 1 AND $f_C \leq 1MHz$ $\left(GAIN = \frac{R2}{R1}\right)$

f_C IS THE FILTER'S CUTOFF FREQUENCY

$R1 = R2,\ C1 = C2,\ C1 \leq \frac{1}{1000 \bullet f_C}$

BUTTERWORTH $R2 = \frac{1}{4.44 \bullet C1 \bullet f_C}$

$R3 = \frac{R2}{2}$

CHEBYSHEV 0.25dB RIPPLE $R2 = \frac{1}{5.65 \bullet C1 \bullet f_C}$

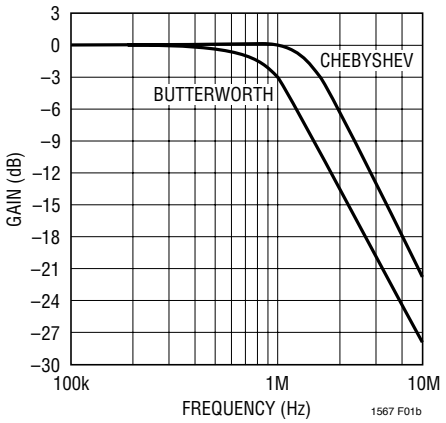
$R3 = \frac{R2}{2.62}$

$$f_O = \frac{1}{2\pi\sqrt{R2R3\ C2}}$$

$$Q = \frac{\sqrt{\frac{R2}{R3}}}{GAIN + 1}$$

$$\text{TRANSFER FUNCTION } H(s) = \frac{(2\pi f_O)^2}{s^2 + \frac{(2\pi f_O)}{Q}s + (2\pi f_O)^2}$$

Gain vs Frequency



GAIN IS MEASURED TO EITHER OUTPUT ALONE.
IF OUTPUT USED DIFFERENTIALLY, $V_{OUT}^+ - V_{OUT}^- = 2\times V_{IN}$

Figure 1. 2nd Order Lowpass Filter and Gain Response for f_C = 1MHz (Butterworth: C1 = C2 = 390pF, R1 = R2 = 576Ω, R3 = 280Ω Chebyshev: C1 = C2 = 390pF, R1 = R2 = 453Ω, R3 = 174Ω)

APPLICATIONS INFORMATION

The simple-to-use spreadsheet requires the user to define the desired corner (or center) frequency, the passband gain and a capacitor value for a choice of second or third order Chebyshev or Butterworth lowpass or second order bandpass filters.

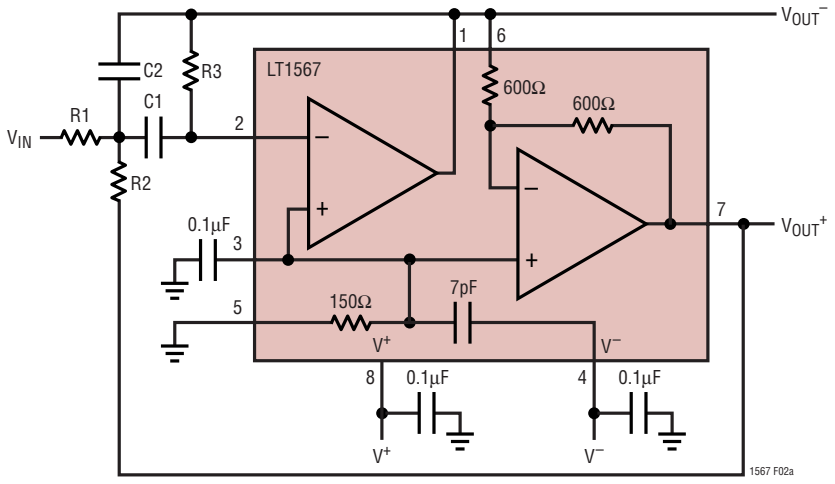
The spreadsheet outputs the required external standard component values and provides a circuit diagram.

Signal Ground

Both operational amplifiers within the LT1567 are designed for inverting operation (constant common mode input) and they share a single reference node on the chip. Two pins permit access to this node: DC BIAS and BYPASS. For a clean reference over a wide bandwidth, the normal procedure is to connect DC BIAS to a DC potential or ground and BYPASS to a decoupling capacitor that returns to a ground plane.

Differential Output Feature

The multiple feedback filter section of Figure 1 inherently includes two outputs of opposite signal polarity: a DC inverting output from the OA (Pin 1) and a DC noninverting



DESIGN EQUATIONS FOR $f_{CENTER} \leq 1MHz$

f_{CENTER} IS THE FILTER'S CENTER FREQUENCY

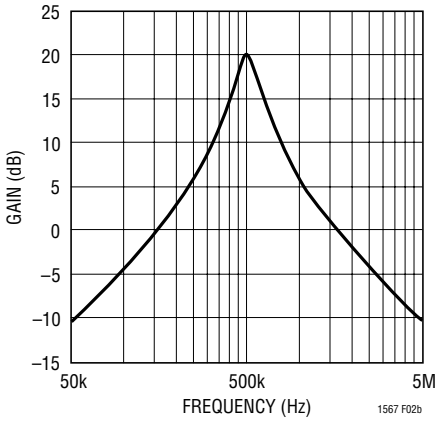
MAXIMUM $f_{CENTER} = 5MHz/GAIN$

GN IS GAIN AT f_{CENTER} = R3/R1, R2 = R3, C1 = C2

$$f_{CENTER} = \frac{\sqrt{GN+1}}{2 \bullet \pi \bullet R2 \bullet C1} \quad -3dB\ BANDWIDTH = \frac{f_{CENTER}}{\sqrt{GN+1}}$$

$$C1 \leq \frac{\sqrt{GN+1}}{2500 \bullet f_C} \quad R3 = \frac{\sqrt{GN+1}}{2\pi \bullet C1 \bullet f_{CENTER}}$$

Gain vs Frequency



GAIN IS MEASURED TO EITHER OUTPUT ALONE.
IF OUTPUT USED DIFFERENTIALLY, $V_{OUT}^+ - V_{OUT}^- = 2\times V_{IN}$

Figure 2. 2nd Order Bandpass Filter and Gain Response for f_C = 500kHz, Gain = 10 (C1 = C2 = 1000pF, R2 = R3 = 1.05k, R1 = 105Ω)

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output from the INV block (Pin 7). These two outputs maintain equal gain and 180° phase shift over a wide frequency range. This feature permits choosing the signal polarity in single ended applications, and also performs single ended to differential conversion. The latter property is useful as an antialiasing filter to drive standard monolithic A/D converters having differential inputs, as illustrated on the first page of this data sheet.

Dealing with High Source Impedances

The voltage V_{IN} in Figure 1, on the left side of R1, is the signal voltage that the filter sees. If a voltage source with significant internal impedance drives the V_{IN} node in Figure 1, then the filter input V_{IN} may differ from the source's open-circuit output, and the difference can be complex, because the filter presents a complex impedance to V_{IN}. A rule of thumb is that a source impedance is negligibly "low" if it is much smaller than R1 at frequencies of interest. Otherwise, the source impedance (resistive or reactive) effectively adds to R1 and may change the signal frequency response compared to that with a low source impedance. If the source is resistive and predictable, then it may be possible to design for it by reducing R1. Unpredictable or nonresistive source impedances that are not much less than R1 should be buffered.

Construction and Instrumentation Cautions

Electrically clean construction is important in applications seeking the full dynamic range and bandwidth of the LT1567. Using the shortest possible wiring or printed-circuit paths will minimize parasitic capacitance and inductance. High quality supply bypass capacitors of 0.1µF near the chip, connected to a ground plane, provide good decoupling from a clean, low inductance power source. But several inches of wire (i.e., a few microhenrys of inductance) from the power supplies, unless decoupled by substantial capacitance (≥10µF) near the chip, can cause a high Q LC resonance in the hundreds of kHz in the chip's supplies or ground reference. This may impair filter performance at those frequencies. In stringent filter applications, a compact, carefully laid out printed circuit board with good ground plane makes a difference in both stopband rejection and distortion. Finally, equipment to measure filter performance can itself introduce distortion or noise. Checking for these limits with a wire in place of the filter is a prudent routine procedure.

Low Noise Differential Circuits

The LT1567 is an optimum analog building for designing single supply differential circuits to process low level signals. Figure 3 shows a single ended to differential amplifier driving a 1st order differential RC filter. The differential output of Figure 3 is a function of input (V_{IN}) and the V_{REF} voltage on Pin 5. (The range of the V_{REF} voltage on Pin 5 in Figures 3, 4 and 5 is the common mode input voltage range parameter under Electrical Characteristics.)The graph of Figure 3 shows the differential signal-to-noise ratio for a gain of 2 and a gain of 10. Increasing the differential gain increases the differential signal-to-noise ratio. The equivalent input noise is equal to the output noise divided by the gain. For example, with a gain equal to 2 (R2 = R1 = 200Ω) and a gain equal to 10 (R2 = 1k, R1 = 200Ω), the equivalent input noise is 4.59nV/$\sqrt{Hz}$ and 2.04nV/$\sqrt{Hz}$ respectively. The V_{REF} voltage on Pin 5 can be set by a voltage divider or a reference voltage source. To maximize the unclipped LT1567 output swing, the DC output voltage should be set at $V^+/2$. However, if V_{INDC} (the input DC voltage) is within the range of V_{REF}, then V_{REF} can be equal to V_{INDC}. The input signal can also be AC coupled to the input resistor, R1, and V_{REF} set to the DC voltage of the circuit following the amplifier. For example, V_{REF} might be set to 1.2V to bias the input of an I and Q modulator used in broadband communication systems.

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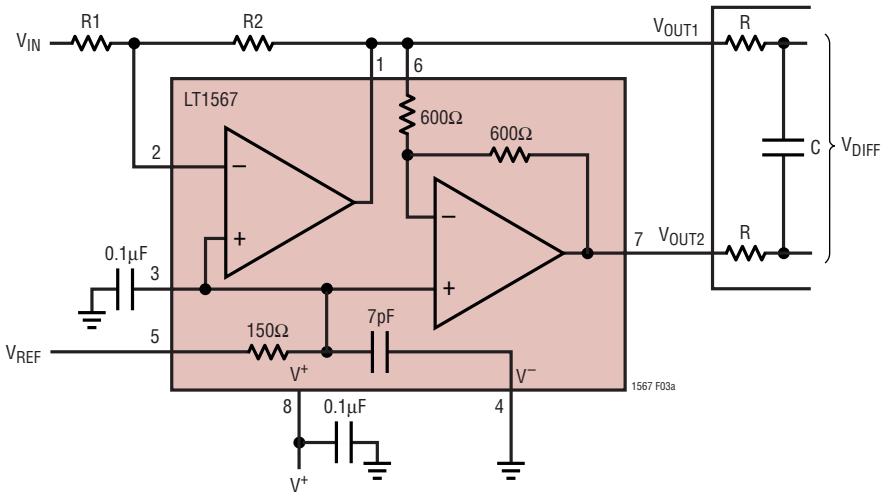

$$V_{OUT1} = -\frac{R2}{R1} \bullet V_{IN} + \left(\frac{R2}{R1} + 1\right) \bullet V_{REF} \qquad V_{OUT2} = -V_{OUT1} + 2\,V_{REF}$$

$$V_{DIFF} = V_{OUT2} - V_{OUT1} = 2 \bullet \frac{R2}{R1} \bullet (V_{IN} - V_{REF}) \qquad f_{-3dB} = \frac{1}{4\pi \bullet R \bullet C}$$

$f_{\eta BW}$ IS THE NOISE BANDWIDTH $\qquad f_{\eta BW} = \dfrac{1.57}{4\pi \bullet R \bullet C}$

Differential Output Signal-to-Noise Ratio (for a Sinewave Signal)

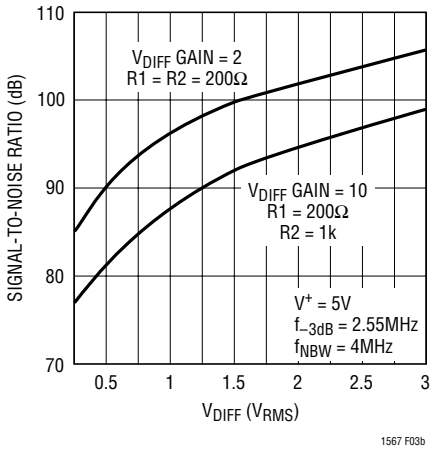

Figure 3. A Single Ended to Differential Amplifier

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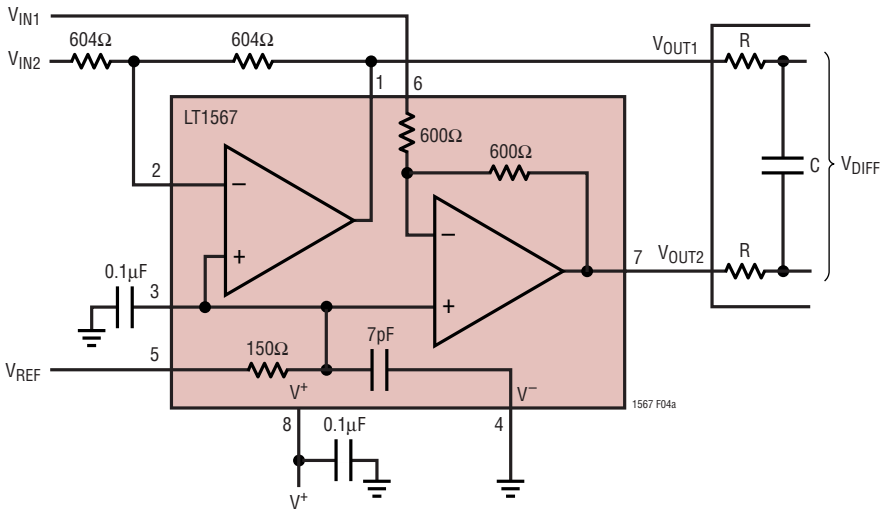
Figure 4 shows an LT1567 single supply differential buffer driving a differential 1st order RC filter. The V_{REF} voltage is subject to the common mode (DC BIAS) limits in the spec table. Within this constraint, V_{REF} can be used to adjust the output common mode level, as noted in Figure 4. For example, in a single 5V power supply circuit, if the input common mode DC voltage is 1.1V and V_{REF} is 1.8V, then the output common mode DC voltage is 2.5V.

Figure 5 shows a low noise differential to single ended amplifier and 1st order lowpass filter. The input common mode rejection depends on the matching of resistors R1 and R3 and the LT1567 inverter gain tolerance (common mode rejection is at least 38dB up to 1MHz with 1% resistors and 5% inverter gain tolerance). The DC voltage at the amplifier's output (V_{OUT}) is V_{REF}.

Output Drive

The output of the LT1567 op amp (Pin 1) can typically provide at least ±20mA. The minimum resistive load to ground that Pin 1 or Pin 7 can drive depends on the feedback resistor and the peak output voltage. For example, the differential driver circuit in Figure 4 is operating with a single 5V supply, V_{REF} and V_{INDC} are equal to 2.5V and the peak AC signal (V_{INAC}) is 1V. If the outputs provide 1.66mA to the feedback resistors (1V/604Ω), then 18.34mA is available to drive a resistive load. With the peak output voltage at 3.5V (2.5V DC plus 1V peak AC), the outputs can drive resistive loads of 191Ω or greater.



$V_{OUT1} = -V_{IN2} + 2V_{REF}$

$V_{OUT2} = -V_{IN1} + 2V_{REF}$

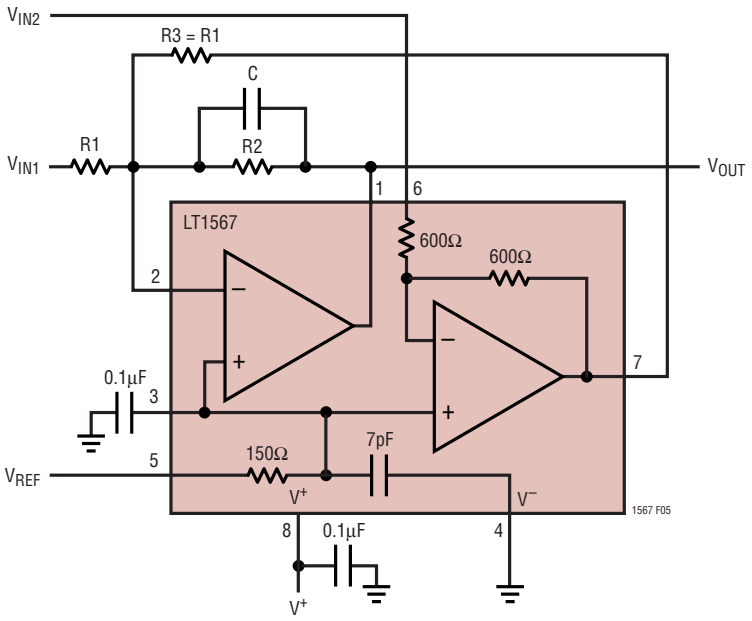
COMMON MODE V_{OUT} IS $2V_{REF} - (\text{COMMON MODE } V_{IN})$

$V_{DIFF} = V_{OUT2} - V_{OUT1} = V_{IN2} - V_{IN1}$ $\quad f_{-3dB} = \frac{1}{4\pi \bullet R \bullet C}$

$f_{\eta BW}$ IS THE NOISE BANDWIDTH $\quad f_{\eta BW} = \frac{1.57}{4\pi \bullet R \bullet C}$

Figure 4. A Differential Buffer/Driver

APPLICATIONS INFORMATION



WITH R3 AND R1 EQUAL, $V_{OUT} = V_{REF} + \left(\frac{R2}{R1}\right)(V_{IN2} - V_{IN1})$

GAIN FROM $(V_{IN2} - V_{IN1})$ TO V_{OUT} IS $\left(\frac{R2}{R1}\right)$ $f_{-3dB} = \frac{1}{2\pi \bullet R2 \bullet C}$

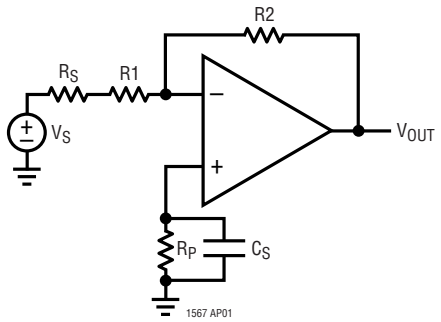
IF R1 = R3 = 604Ω, THEN

R2	GAIN	Vη, INPUT REFERRED NOISE (nV/√Hz)
604Ω	1	9.0
1.21k	2	8.4
2.43k	4	8.1

NOISE AT V_{OUT} = GAIN • Vη • $\sqrt{f_{\eta BW}}$; $f_{\eta BW} = 1.57 \bullet f_{-3dB}$

Figure 5. A Differential to Single Ended Amplifier/Filter

APPENDIX: OUTPUT NOISE OF AN OP AMP INVERTING AMPLIFIER



NOISE AT V_{OUT} IN V_{RMS} = V_{ON} IN $V/\sqrt{Hz} \bullet \sqrt{f_{NBW}}$

f_{NBW} = NOISE BANDWIDTH

$$V_{ON} = \sqrt{\left(\frac{R2}{R1 + R_S} + 1\right)^2 \bullet V_N^2 + \left(\frac{R2}{R1 + R_S}\right)^2 \bullet (V_{R1}^2 + V_{SN}^2) + V_{R2}^2 + (I_N \bullet R2)^2}$$

IF V_{SN} AND $R_S = 0$

THEN

$$V_{ON} = \sqrt{\left(\frac{R2}{R1} + 1\right)^2 \bullet V_N^2 + \left(\frac{R2}{R1}\right)^2 \bullet V_{R1}^2 + V_{R2}^2 + (I_N \bullet R2)^2}$$

V_{ON} is the voltage noise density in $V/\sqrt{Hz}$ at the inverter's output.

V_N is the op amp's voltage noise density in $V/\sqrt{Hz}$.

I_N is the op amp's current noise density in $A/\sqrt{Hz}$.

V_{SN} is the voltage noise density of the input voltage source V_S with source resistance R_S. (If V_{SN} is less than one-half the noise of resistor R1, then the calculation error when omitting V_{SN} is less than 4.3%.)

V_{R1} and V_{R2} is the voltage noise density of the thermal noise of resistors (R1 + R_S) and R2 respectively. Resistor R_S is typically smaller than R1 and is omitted from noise calculations. The voltage noise density of the thermal noise of a resistor R is approximately $0.128x\sqrt{RnV}/\sqrt{Hz}$ at 25°C.

The R_P resistor noise at the op amp's plus input is equal to $\sqrt{(kT/C_S)}$ and is omitted from noise calculations. (If $C_S = 0.1\mu F$, the R_P noise is $0.2\mu V_{RMS}$ at 25°C, k = $1.38x10^{-23}$ and T = 273°C + 25°C.)

The noise bandwidth (f_{NBW}) is greater than a circuit's –3dB bandwidth. (For a 1st, 2nd or 3rd order Butterworth filter, f_{NBW} is 1.57x, 1.22x and 1.15x respectively the –3dB bandwidth.)

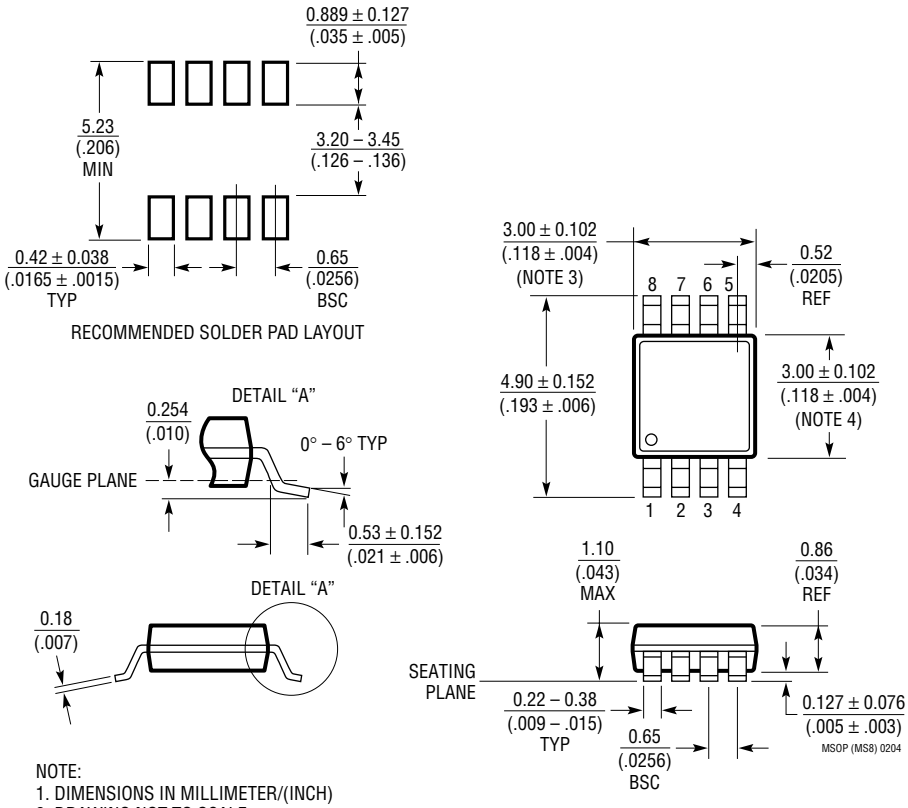
Example: Calculate V_{ON}, the voltage noise density of an LT1567 op amp inverter for R1 = R2 = 604Ω. With $V_N = 1.4nV/\sqrt{Hz}$ and $I_N = 1pA/\sqrt{Hz}$.

$$V_{ON} = \sqrt{\left(\frac{604}{604} + 1\right)^2 \bullet (1.4 \bullet 10^{-9})^2 + \left(\frac{604}{604}\right)^2 \bullet (0.128 \bullet 10^{-9} \bullet \sqrt{604})^2 + (0.128 \bullet 10^{-9} \bullet \sqrt{604})^2 + (10^{-12} \bullet 604)^2}$$

$V_{ON} = 5.29nV/\sqrt{Hz}$

PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX