

# 30MHz, 10V/ $\mu$ s, Dual/Quad Rail-to-Rail Input and Output Precision Op Amps

## FEATURES

- **Gain-Bandwidth Product: 30MHz**
- **Slew Rate: 10V/ $\mu$ s**
- **Low Supply Current per Amplifier: 3.5mA**
- Input Common Mode Range Includes Both Rails
- Output Swings Rail-to-Rail
- Input Offset Voltage, Rail-to-Rail: 525 $\mu$ V Max
- Input Offset Current: 150nA Max
- Input Bias Current: 1000nA Max
- Open-Loop Gain: 1000V/mV Min
- Low Input Noise Voltage: 6nV/ $\sqrt{\text{Hz}}$  Typ
- Low Distortion: -91dBc at 100kHz
- Wide Supply Range: 2.7V to  $\pm$ 15V
- Large Output Drive Current: 35mA Min
- Dual in 8-Pin PDIP and SO Packages
- Quad in Narrow 14-Pin SO Package

## APPLICATIONS

- Active Filters
- Rail-to-Rail Buffer Amplifiers
- Driving A/D Converters
- Low Voltage Signal Processing
- Battery-Powered Systems

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## DESCRIPTION

The LT<sup>®</sup>1630/LT1631 are dual/quad, rail-to-rail input and output op amps with a 30MHz gain-bandwidth product and a 10V/ $\mu$ s slew rate.

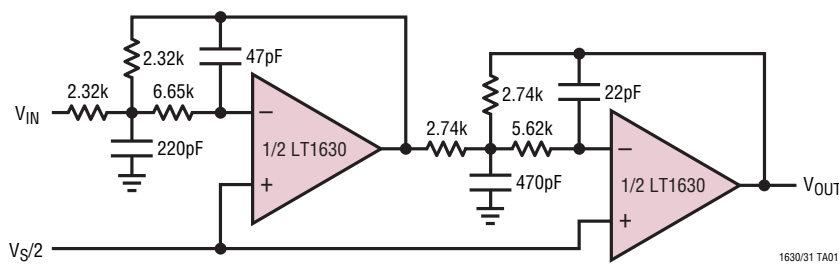
The LT1630/LT1631 have excellent DC precision over the full range of operation. Input offset voltage is typically less than 150 $\mu$ V and the minimum open-loop gain of one million into a 10k load virtually eliminates all gain error. To maximize common mode rejection, the LT1630/LT1631 employ a patented trim technique for both input stages, one at the negative supply and the other at the positive supply, that gives a typical CMRR of 106dB over the full input range.

The LT1630/LT1631 maintain their performance for supplies from 2.7V to 36V and are specified at 3V, 5V and  $\pm$ 15V supplies. The inputs can be driven beyond the supplies without damage or phase reversal of the output. The output delivers load currents in excess of 35mA.

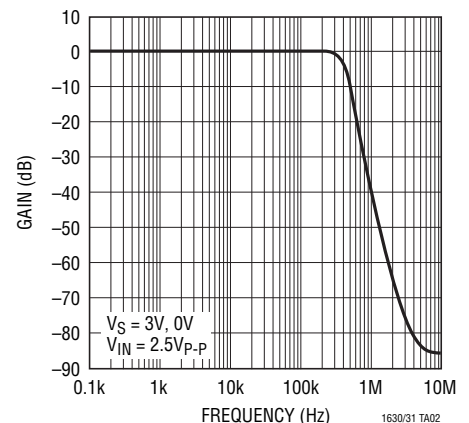
The LT1630 is available in 8-pin PDIP and SO packages with the standard dual op amp pinout. The LT1631 features the standard quad op amp configuration and is available in a 14-pin plastic SO package. These devices can be used as plug-in replacements for many standard op amps to improve input/output range and performance.

## TYPICAL APPLICATION

Single Supply, 400kHz, 4th Order Butterworth Filter



Frequency Response

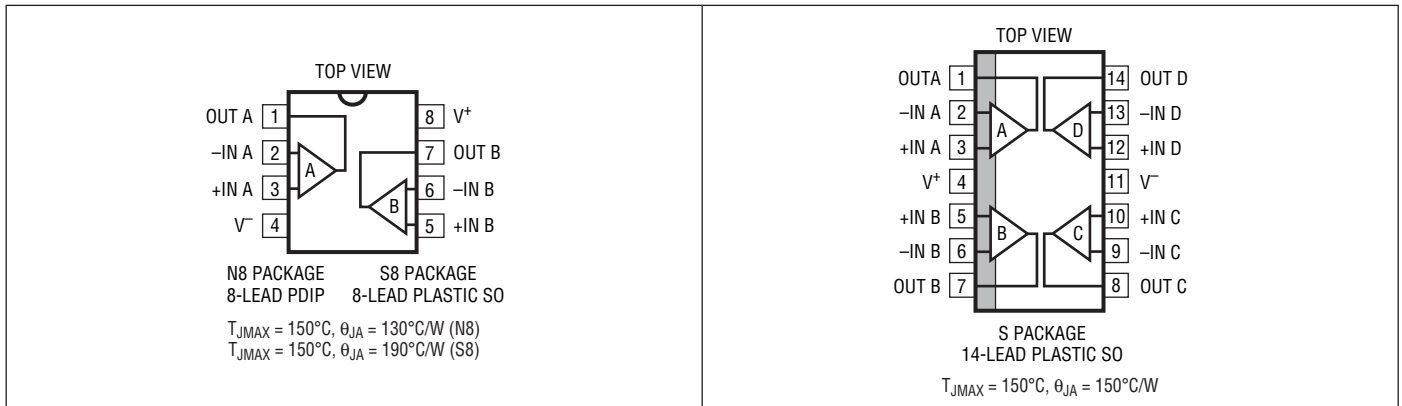


# LT1630/LT1631

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V+ to V-) .....	36V	Specified Temperature Range (Note 4) .....	
Input Current.....	±10mA	C-Grade/I-Grade .....	-40°C to 85°C
Output Short-Circuit Duration (Note 2).....	Continuous	H-Grade .....	-40°C to 125°C
Operating Temperature Range		Junction Temperature .....	150°C
C-Grade/I-Grade .....	-40°C to 85°C	Storage Temperature Range .....	-65°C to 150°C
H-Grade .....	-40°C to 125°C	Lead Temperature (Soldering, 10 sec).....	300°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1630CN8#PBF	LT1630CN8#TRPBF	LT1630CN8	8-Lead PDIP	-40°C to 85°C
LT1630CS8#PBF	LT1630CS8#TRPBF	1630	8-Lead Plastic SO	-40°C to 85°C
LT1630IN8#PBF	LT1630IN8#TRPBF	LT1630IN8	8-Lead PDIP	-40°C to 85°C
LT1630IS8#PBF	LT1630IS8#TRPBF	1630I	8-Lead Plastic SO	-40°C to 85°C
LT1630HS8#PBF	LT1630HS8#TRPBF	1630H	8-Lead Plastic SO	-40°C to 125°C
LT1631CS#PBF	LT1631CS#TRPBF	LT1631CS	14-Lead Plastic SO	-40°C to 85°C
LT1631IS#PBF	LT1631IS#TRPBF	LT1631IS	14-Lead Plastic SO	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

**ELECTRICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{V}, 0\text{V}$ ;  $V_S = 3\text{V}, 0\text{V}$ ;  $V_{CM} = V_{OUT} = \text{half supply}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{OS}$	Input Offset Voltage	$V_{CM} = V^+$		150	525	$\mu\text{V}$
		$V_{CM} = V^-$		150	525	$\mu\text{V}$
$\Delta V_{OS}$	Input Offset Shift	$V_{CM} = V^- \text{ to } V^+$		150	525	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^-, V^+$ (Note 5)		200	950	$\mu\text{V}$
$I_B$	Input Bias Current	$V_{CM} = V^+$	0	540	1000	nA
		$V_{CM} = V^-$	-1000	-540	0	nA
$\Delta I_B$	Input Bias Current Shift	$V_{CM} = V^- \text{ to } V^+$		1080	2000	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+$ (Note 5) $V_{CM} = V^-$ (Note 5)		25	300	nA nA
$I_{OS}$	Input Offset Current	$V_{CM} = V^+$		20	150	nA
		$V_{CM} = V^-$		20	150	nA
$\Delta I_{OS}$	Input Offset Current Shift	$V_{CM} = V^- \text{ to } V^+$		40	300	nA
	Input Noise Voltage	0.1Hz to 10Hz		300		nV <sub>p-p</sub>
$e_n$	Input Noise Voltage Density	$f = 1\text{kHz}$		6		nV/ $\sqrt{\text{Hz}}$
$i_n$	Input Noise Current Density	$f = 1\text{kHz}$		0.9		pA/ $\sqrt{\text{Hz}}$
$C_{IN}$	Input Capacitance			5		pF
$A_{VOL}$	Large-Signal Voltage Gain	$V_S = 5\text{V}, V_O = 300\text{mV to } 4.7\text{V}, R_L = 10\text{k}$	500	3500		V/mV
		$V_S = 3\text{V}, V_O = 300\text{mV to } 2.7\text{V}, R_L = 10\text{k}$	400	2000		V/mV
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}, V_{CM} = V^- \text{ to } V^+$	79	90		dB
		$V_S = 3\text{V}, V_{CM} = V^- \text{ to } V^+$	75	86		dB
	CMRR Match (Channel-to-Channel) (Note 5)	$V_S = 5\text{V}, V_{CM} = V^- \text{ to } V^+$ $V_S = 3\text{V}, V_{CM} = V^- \text{ to } V^+$	72	96		dB dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.7\text{V to } 12\text{V}, V_{CM} = V_O = 0.5\text{V}$	87	105		dB
	PSRR Match (Channel-to-Channel) (Note 5)	$V_S = 2.7\text{V to } 12\text{V}, V_{CM} = V_O = 0.5\text{V}$	80	107		dB
	Minimum Supply Voltage (Note 9)	$V_{CM} = V_O = 0.5\text{V}$		2.6	2.7	V
$V_{OL}$	Output Voltage Swing Low (Note 6)	No Load		14	30	mV
		$I_{SINK} = 0.5\text{mA}$		31	60	mV
		$I_{SINK} = 25\text{mA}, V_S = 5\text{V}$		600	1200	mV
		$I_{SINK} = 20\text{mA}, V_S = 3\text{V}$		500	1000	mV
$V_{OH}$	Output Voltage Swing High (Note 6)	No Load		15	40	mV
		$I_{SOURCE} = 0.5\text{mA}$		42	80	mV
		$I_{SOURCE} = 20\text{mA}, V_S = 5\text{V}$		900	1800	mV
		$I_{SOURCE} = 15\text{mA}, V_S = 3\text{V}$		680	1400	mV
$I_{SC}$	Short-Circuit Current	$V_S = 5\text{V}$	$\pm 20$	$\pm 41$		mA
		$V_S = 3\text{V}$	$\pm 15$	$\pm 30$		mA
$I_S$	Supply Current per Amplifier			3.5	4.4	mA
GBW	Gain-Bandwidth Product (Note 7)	$f = 100\text{kHz}$	15	30		MHz
SR	Slew Rate (Note 8)	$V_S = 5\text{V}, A_V = -1, R_L = \text{Open}, V_O = 4\text{V}$	4.6	9.2		V/ $\mu\text{s}$
		$V_S = 3\text{V}, A_V = -1, R_L = \text{Open}$	4.2	8.5		V/ $\mu\text{s}$
$t_S$	Settling Time	$V_S = 5\text{V}, A_V = 1, R_L = 1\text{k}, 0.01\%, V_{STEP} = 2\text{V}$		520		ns

# LT1630/LT1631

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range of  $0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$ .  $V_S = 5\text{V}, 0\text{V}$ ;  $V_S = 3\text{V}, 0\text{V}$ ;  $V_{CM} = V_{OUT} = \text{half supply}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{OS}$	Input Offset Voltage	$V_{CM} = V^+ - 0.1\text{V}$	●		175	700	$\mu\text{V}$
		$V_{CM} = V^- + 0.2\text{V}$	●		175	700	$\mu\text{V}$
$V_{OS\ TC}$	Input Offset Voltage Drift (Note 3)	$V_{CM} = V^+ - 0.1\text{V}$	●		2.5	5.5	$\mu\text{V}/^{\circ}\text{C}$
			●		1	3.5	$\mu\text{V}/^{\circ}\text{C}$
$\Delta V_{OS}$	Input Offset Voltage Shift	$V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●		175	750	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^- + 0.2\text{V}, V^+ - 0.1\text{V}$ (Note 5)	●		200	1200	$\mu\text{V}$
$I_B$	Input Bias Current	$V_{CM} = V^+ - 0.1\text{V}$	●	0	585	1100	nA
		$V_{CM} = V^- + 0.2\text{V}$	●	-1100	-585	0	nA
$\Delta I_B$	Input Bias Current Shift	$V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●		1170	2200	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+ - 0.1\text{V}$ (Note 5) $V_{CM} = V^- + 0.2\text{V}$ (Note 5)	● ●		25 25	340 340	nA nA
$I_{OS}$	Input Offset Current	$V_{CM} = V^+ - 0.1\text{V}$	●		20	170	nA
		$V_{CM} = V^- + 0.2\text{V}$	●		20	170	nA
$\Delta I_{OS}$	Input Offset Current Shift	$V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●		40	340	nA
$A_{VOL}$	Large-Signal Voltage Gain	$V_S = 5\text{V}, V_O = 300\text{mV}$ to $4.7\text{V}, R_L = 10\text{k}$	●	450	3500		V/mV
		$V_S = 3\text{V}, V_O = 300\text{mV}$ to $2.7\text{V}, R_L = 10\text{k}$	●	350	2000		V/mV
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}, V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●	75	89		dB
		$V_S = 3\text{V}, V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●	71	83		dB
	CMRR Match (Channel-to-Channel) (Note 5)	$V_S = 5\text{V}, V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$ $V_S = 3\text{V}, V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	● ●	70 65	90 85		dB dB
PSRR	Power Supply Rejection Ratio	$V_S = 3\text{V}$ to $12\text{V}, V_{CM} = V_O = 0.5\text{V}$	●	82	101		dB
	PSRR Match (Channel-to-Channel) (Note 5)	$V_S = 3\text{V}$ to $12\text{V}, V_{CM} = V_O = 0.5\text{V}$	●	78	102		dB
	Minimum Supply Voltage (Note 9)	$V_{CM} = V_O = 0.5\text{V}$	●		2.6	2.7	V
$V_{OL}$	Output Voltage Swing Low (Note 6)	No Load	●		17	40	mV
		$I_{SINK} = 0.5\text{mA}$	●		36	80	mV
		$I_{SINK} = 25\text{mA}, V_S = 5\text{V}$	●		700	1400	mV
		$I_{SINK} = 20\text{mA}, V_S = 3\text{V}$	●		560	1200	mV
$V_{OH}$	Output Voltage Swing High (Note 6)	No Load	●		16	40	mV
		$I_{SOURCE} = 0.5\text{mA}$	●		50	100	mV
		$I_{SOURCE} = 15\text{mA}, V_S = 5\text{V}$	●		820	1600	mV
		$I_{SOURCE} = 10\text{mA}, V_S = 3\text{V}$	●		550	1100	mV
$I_{SC}$	Short-Circuit Current	$V_S = 5\text{V}$	●	$\pm 18$	$\pm 36$		mA
		$V_S = 3\text{V}$	●	$\pm 13$	$\pm 25$		mA
$I_S$	Supply Current per Amplifier		●		4.0	5.1	mA
GBW	Gain-Bandwidth Product (Note 7)	$f = 100\text{kHz}$	●	14	28		MHz
SR	Slew Rate (Note 8)	$V_S = 5\text{V}, A_V = -1, R_L = \text{Open}, V_O = 4\text{V}$	●	4.2	8.3		V/ $\mu\text{s}$
		$V_S = 3\text{V}, A_V = -1, R_L = \text{Open}$	●	3.9	7.7		V/ $\mu\text{s}$

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range of  $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ .  $V_S = 5\text{V}, 0\text{V}$ ;  $V_S = 3\text{V}, 0\text{V}$ ;  $V_{CM} = V_{OUT} = \text{half supply}$ , unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{OS}$	Input Offset Voltage	$V_{CM} = V^+ - 0.1\text{V}$	●	250	775	$\mu\text{V}$
		$V_{CM} = V^- + 0.2\text{V}$	●	250	775	$\mu\text{V}$
$V_{OS\ TC}$	Input Offset Voltage Drift (Note 3)	$V_{CM} = V^+ - 0.1\text{V}$	●	2.5	5.5	$\mu\text{V}/^{\circ}\text{C}$
			●	1	3.5	$\mu\text{V}/^{\circ}\text{C}$
$\Delta V_{OS}$	Input Offset Voltage Shift	$V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●	200	750	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^- + 0.2\text{V}, V^+$ (Note 5)	●	210	1500	$\mu\text{V}$
$I_B$	Input Bias Current	$V_{CM} = V^+ - 0.1\text{V}$	●	0	650	nA
		$V_{CM} = V^- + 0.2\text{V}$	●	-1300	-650	0
$\Delta I_B$	Input Bias Current Shift	$V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●	1300	2600	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+ - 0.1\text{V}$ (Note 5) $V_{CM} = V^- + 0.2\text{V}$ (Note 5)	● ●	25 25	390 390	nA nA
$I_{OS}$	Input Offset Current	$V_{CM} = V^+ - 0.1\text{V}$	●	25	195	nA
		$V_{CM} = V^- + 0.2\text{V}$	●	25	195	nA
$\Delta I_{OS}$	Input Offset Current Shift	$V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●	50	390	nA
$A_{VOL}$	Large-Signal Voltage Gain	$V_S = 5\text{V}, V_O = 300\text{mV}$ to $4.7\text{V}, R_L = 10\text{k}$	●	400	3500	V/mV
		$V_S = 3\text{V}, V_O = 300\text{mV}$ to $2.7\text{V}, R_L = 10\text{k}$	●	300	1800	V/mV
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}, V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$ $V_S = 3\text{V}, V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	● ●	75 71	87 83	dB dB
	CMRR Match (Channel-to-Channel) (Note 5)	$V_S = 5\text{V}, V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$ $V_S = 3\text{V}, V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	● ●	69 65	89 85	dB dB
	PSRR	$V_S = 3\text{V}$ to $12\text{V}, V_{CM} = V_O = 0.5\text{V}$	●	82	98	dB
PSRR	PSRR Match (Channel-to-Channel) (Note 5)	$V_S = 3\text{V}$ to $12\text{V}, V_{CM} = V_O = 0.5\text{V}$	●	78	102	dB
	Minimum Supply Voltage (Note 9)	$V_{CM} = V_O = 0.5\text{V}$	●	2.6	2.7	V
$V_{OL}$	Output Voltage Swing Low (Note 6)	No Load	●	18	40	mV
		$I_{SINK} = 0.5\text{mA}$	●	38	80	mV
		$I_{SINK} = 25\text{mA}, V_S = 5\text{V}$	●	730	1500	mV
		$I_{SINK} = 20\text{mA}, V_S = 3\text{V}$	●	580	1200	mV
$V_{OH}$	Output Voltage Swing High (Note 6)	No Load	●	15	40	mV
		$I_{SOURCE} = 0.5\text{mA}$	●	55	110	mV
		$I_{SOURCE} = 15\text{mA}, V_S = 5\text{V}$	●	860	1700	mV
		$I_{SOURCE} = 10\text{mA}, V_S = 3\text{V}$	●	580	1200	mV
$I_{SC}$	Short-Circuit Current	$V_S = 5\text{V}$	●	$\pm 17$	$\pm 34$	mA
		$V_S = 3\text{V}$	●	$\pm 12$	$\pm 24$	mA
$I_S$	Supply Current per Amplifier		●	4.1	5.2	mA
GBW	Gain-Bandwidth Product (Note 7)	$f = 100\text{kHz}$	●	14	28	MHz
SR	Slew Rate (Note 8)	$V_S = 5\text{V}, A_V = -1, R_L = \text{Open}, V_O = 4\text{V}$	●	3.5	7	V/ $\mu\text{s}$
		$V_S = 3\text{V}, A_V = -1, R_L = \text{Open}$	●	3.3	6.5	V/ $\mu\text{s}$

# LT1630/LT1631

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range of  $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$ .  $V_S = 5\text{V}, 0\text{V}$ ;  $V_S = 3\text{V}, 0\text{V}$ ;  $V_{\text{CM}} = V_{\text{OUT}} = \text{half supply}$ , unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{\text{OS}}$	Input Offset Voltage	$V_{\text{CM}} = V^+ - 0.1\text{V}$	●	345	950	$\mu\text{V}$
		$V_{\text{CM}} = V^- + 0.2\text{V}$	●	345	950	$\mu\text{V}$
$V_{\text{OS TC}}$	Input Offset Voltage Drift (Note 3)	$V_{\text{CM}} = V^+ - 0.1\text{V}$	●	2.5	5.5	$\mu\text{V}/^{\circ}\text{C}$
			●	1	3.5	$\mu\text{V}/^{\circ}\text{C}$
$\Delta V_{\text{OS}}$	Input Offset Voltage Shift	$V_{\text{CM}} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●	200	750	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel)	$V_{\text{CM}} = V^- + 0.2\text{V}, V^+$ (Note 5)	●	210	1500	$\mu\text{V}$
$I_{\text{B}}$	Input Bias Current	$V_{\text{CM}} = V^+ - 0.1\text{V}$	●	0	650	nA
		$V_{\text{CM}} = V^- + 0.2\text{V}$	●	-1300	-650	0
$\Delta I_{\text{B}}$	Input Bias Current Shift	$V_{\text{CM}} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●	1300	2600	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{\text{CM}} = V^+ - 0.1\text{V}$ (Note 5) $V_{\text{CM}} = V^- + 0.2\text{V}$ (Note 5)	● ●	25 25	390 390	nA nA
$I_{\text{OS}}$	Input Offset Current	$V_{\text{CM}} = V^+ - 0.1\text{V}$	●	25	195	nA
		$V_{\text{CM}} = V^- + 0.2\text{V}$	●	25	195	nA
$\Delta I_{\text{OS}}$	Input Offset Current Shift	$V_{\text{CM}} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●	50	390	nA
$A_{\text{VOL}}$	Large-Signal Voltage Gain	$V_S = 5\text{V}, V_O = 300\text{mV}$ to $4.7\text{V}, R_L = 10\text{k}$	●	200	3100	V/mV
		$V_S = 3\text{V}, V_O = 300\text{mV}$ to $2.7\text{V}, R_L = 10\text{k}$	●	150	1625	V/mV
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}, V_{\text{CM}} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●	72	87	dB
		$V_S = 3\text{V}, V_{\text{CM}} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●	69	83	dB
	CMRR Match (Channel-to-Channel) (Note 5)	$V_S = 5\text{V}, V_{\text{CM}} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$ $V_S = 3\text{V}, V_{\text{CM}} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	● ●	67 63	89 85	dB dB
PSRR	Power Supply Rejection Ratio	$V_S = 3\text{V}$ to $12\text{V}, V_{\text{CM}} = V_O = 0.5\text{V}$	●	82	98	dB
	PSRR Match (Channel-to-Channel) (Note 5)	$V_S = 3\text{V}$ to $12\text{V}, V_{\text{CM}} = V_O = 0.5\text{V}$	●	78	102	dB
	Minimum Supply Voltage (Note 9)	$V_{\text{CM}} = V_O = 0.5\text{V}$	●	2.6	2.7	V
$V_{\text{OL}}$	Output Voltage Swing Low (Note 6)	No Load	●	18	40	mV
		$I_{\text{SINK}} = 0.5\text{mA}$	●	38	100	mV
		$I_{\text{SINK}} = 25\text{mA}, V_S = 5\text{V}$	●	730	1600	mV
		$I_{\text{SINK}} = 20\text{mA}, V_S = 3\text{V}$	●	580	1300	mV
$V_{\text{OH}}$	Output Voltage Swing High (Note 6)	No Load	●	15	40	mV
		$I_{\text{SOURCE}} = 0.5\text{mA}$	●	55	120	mV
		$I_{\text{SOURCE}} = 15\text{mA}, V_S = 5\text{V}$	●	860	1800	mV
		$I_{\text{SOURCE}} = 10\text{mA}, V_S = 3\text{V}$	●	580	1300	mV
$I_{\text{SC}}$	Short-Circuit Current	$V_S = 5\text{V}$	●	$\pm 17$	$\pm 34$	mA
		$V_S = 3\text{V}$	●	$\pm 12$	$\pm 24$	mA
$I_{\text{S}}$	Supply Current per Amplifier		●	4.1	5.6	mA
GBW	Gain-Bandwidth Product (Note 7)	$f = 100\text{kHz}$	●	13	28	MHz
SR	Slew Rate (Note 8)	$V_S = 5\text{V}, A_V = -1, R_L = \text{Open}, V_O = 4\text{V}$	●	3.5	7	V/ $\mu\text{s}$
		$V_S = 3\text{V}, A_V = -1, R_L = \text{Open}$	●	3.3	6.5	V/ $\mu\text{s}$

**ELECTRICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $V_{CM} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{OS}$	Input Offset Voltage	$V_{CM} = V^+$		220	1000	$\mu\text{V}$
		$V_{CM} = V^-$		220	1000	$\mu\text{V}$
$\Delta V_{OS}$	Input Offset Voltage Shift	$V_{CM} = V^-$ to $V^+$		150	1000	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^-, V^+$ (Note 5)		200	1500	$\mu\text{V}$
$I_B$	Input Bias Current	$V_{CM} = V^+$	0	550	1100	nA
		$V_{CM} = V^-$	-1100	-550	0	nA
$\Delta I_B$	Input Bias Current Shift	$V_{CM} = V^-$ to $V^+$		1100	2200	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+$ (Note 5) $V_{CM} = V^-$ (Note 5)		20 20	300 300	nA nA
$I_{OS}$	Input Offset Current	$V_{CM} = V^+$		20	150	nA
		$V_{CM} = V^-$		20	150	nA
$\Delta I_{OS}$	Input Offset Current Shift	$V_{CM} = V^-$ to $V^+$		40	300	nA
	Input Noise Voltage	0.1Hz to 10Hz		300		nV <sub>P-P</sub>
$e_n$	Input Noise Voltage Density	$f = 1\text{kHz}$		6		nV/ $\sqrt{\text{Hz}}$
$i_n$	Input Noise Current Density	$f = 1\text{kHz}$		0.9		pA/ $\sqrt{\text{Hz}}$
$C_{IN}$	Input Capacitance	$f = 100\text{kHz}$		3		pF
$A_{VOL}$	Large-Signal Voltage Gain	$V_O = -14.5\text{V}$ to $14.5\text{V}$ , $R_L = 10\text{k}$ $V_O = -10\text{V}$ to $10\text{V}$ , $R_L = 2\text{k}$	1000 650	5000 3500		V/mV V/mV
	Channel Separation	$V_O = -10\text{V}$ to $10\text{V}$ , $R_L = 2\text{k}$	112	134		dB
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to $V^+$	89	106		dB
	CMRR Match (Channel-to-Channel) (Note 5)	$V_{CM} = V^-$ to $V^+$	86	110		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$	87	105		dB
	PSRR Match (Channel-to-Channel) (Note 5)	$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$	82	107		dB
$V_{OL}$	Output Voltage Swing Low (Note 6)	No Load		16	35	mV
		$I_{SINK} = 5\text{mA}$		150	300	mV
		$I_{SINK} = 25\text{mA}$		600	1200	mV
$V_{OH}$	Output Voltage Swing High (Note 6)	No Load		15	40	mV
		$I_{SINK} = 5\text{mA}$		250	500	mV
		$I_{SINK} = 25\text{mA}$		1200	2400	mV
$I_{SC}$	Short-Circuit Current		$\pm 35$	$\pm 70$		mA
$I_S$	Supply Current per Amplifier			4.1	5.0	mA
GBW	Gain-Bandwidth Product (Note 7)	$f = 100\text{kHz}$	15	30		MHz
SR	Slew Rate	$A_V = -1$ , $R_L = \text{Open}$ , $V_O = \pm 10\text{V}$ , Measure at $V_O = \pm 5\text{V}$	5	10		V/ $\mu\text{s}$
$t_S$	Settling Time	0.01%, $V_{STEP} = 10\text{V}$ , $A_V = 1$ , $R_L = 1\text{k}$		1.2		$\mu\text{s}$

# LT1630/LT1631

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range of  $0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$ .  $V_S = \pm 15\text{V}$ ,  $V_{\text{CM}} = 0\text{V}$ ,  $V_{\text{OUT}} = 0\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{\text{OS}}$	Input Offset Voltage	$V_{\text{CM}} = V^+ - 0.1\text{V}$	●		300	1250	$\mu\text{V}$
		$V_{\text{CM}} = V^- + 0.2\text{V}$	●		300	1250	$\mu\text{V}$
$V_{\text{OS TC}}$	Input Offset Voltage Drift (Note 3)		●		4.5	7	$\mu\text{V}/^{\circ}\text{C}$
		$V_{\text{CM}} = V^+ - 0.1\text{V}$	●		1.5	4	$\mu\text{V}/^{\circ}\text{C}$
$\Delta V_{\text{OS}}$	Input Offset Voltage Shift	$V_{\text{CM}} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●		180	1100	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel)	$V_{\text{CM}} = V^- + 0.2\text{V}$ , $V^+ - 0.1\text{V}$ (Note 5)	●		300	2000	$\mu\text{V}$
$I_{\text{B}}$	Input Bias Current	$V_{\text{CM}} = V^+ - 0.1\text{V}$	●	0	600	1200	nA
		$V_{\text{CM}} = V^- + 0.2\text{V}$	●	-1200	-600	0	nA
$\Delta I_{\text{B}}$	Input Bias Current Shift	$V_{\text{CM}} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●		1200	2400	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{\text{CM}} = V^+ - 0.1\text{V}$ (Note 5) $V_{\text{CM}} = V^- + 0.2\text{V}$ (Note 5)	● ●		30 30	350 350	nA nA
$I_{\text{OS}}$	Input Offset Current	$V_{\text{CM}} = V^+ - 0.1\text{V}$	●		25	175	nA
		$V_{\text{CM}} = V^- + 0.2\text{V}$	●		25	175	nA
$\Delta I_{\text{OS}}$	Input Offset Current Shift	$V_{\text{CM}} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●		50	350	nA
$A_{\text{VOL}}$	Large-Signal Voltage Gain	$V_0 = -14.5\text{V}$ to $14.5\text{V}$ , $R_L = 10\text{k}$ $V_0 = -10\text{V}$ to $10\text{V}$ , $R_L = 2\text{k}$	● ●	900 600	6000 4000		V/mV V/mV
	Channel Separation	$V_0 = -10\text{V}$ to $10\text{V}$ , $R_L = 2\text{k}$	●	112	132		dB
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●	88	104		dB
	CMRR Match (Channel-to-Channel) (Note 5)	$V_{\text{CM}} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●	84	104		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$	●	86	100		dB
	PSRR Match (Channel-to-Channel) (Note 5)	$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$	●	80	104		dB
$V_{\text{OL}}$	Output Voltage Swing Low (Note 6)	No Load	●		19	45	mV
		$I_{\text{SINK}} = 5\text{mA}$	●		175	350	mV
		$I_{\text{SINK}} = 25\text{mA}$	●		670	1400	mV
$V_{\text{OH}}$	Output Voltage Swing High (Note 6)	No Load	●		15	40	mV
		$I_{\text{SOURCE}} = 5\text{mA}$	●		300	600	mV
		$I_{\text{SOURCE}} = 25\text{mA}$	●		1400	2800	mV
$I_{\text{SC}}$	Short-Circuit Current		●	$\pm 28$	$\pm 57$		mA
$I_{\text{S}}$	Supply Current per Amplifier		●		4.6	5.6	mA
GBW	Gain-Bandwidth Product (Note 7)	$f = 100\text{kHz}$	●	14	28		MHz
SR	Slew Rate	$A_V = -1$ , $R_L = \text{Open}$ , $V_0 = \pm 10\text{V}$ , Measured at $V_0 = \pm 5\text{V}$	●	4.5	9		V/ $\mu\text{s}$



**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range of  $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ .  $V_S = \pm 15\text{V}$ ,  $V_{CM} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$ , unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{OS}$	Input Offset Voltage	$V_{CM} = V^+ - 0.1\text{V}$	●		350	1400	$\mu\text{V}$
		$V_{CM} = V^- + 0.2\text{V}$	●		350	1400	$\mu\text{V}$
$V_{OS\ TC}$	Input Offset Voltage Drift (Note 3)		●		4.5	7	$\mu\text{V}/^{\circ}\text{C}$
		$V_{CM} = V^+ - 0.1\text{V}$	●		1.5	4	$\mu\text{V}/^{\circ}\text{C}$
$\Delta V_{OS}$	Input Offset Voltage Shift	$V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●		180	1200	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^- + 0.2\text{V}$ , $V^+ - 0.1\text{V}$ (Note 5)	●		350	2200	$\mu\text{V}$
$I_B$	Input Bias Current	$V_{CM} = V^+ - 0.1\text{V}$	●	0	690	1400	nA
		$V_{CM} = V^- + 0.2\text{V}$	●	-1400	-690	0	nA
$\Delta I_B$	Input Bias Current Shift	$V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●		1380	2800	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+ - 0.1\text{V}$ (Note 5) $V_{CM} = V^- + 0.2\text{V}$ (Note 5)	● ●		30 30	420 420	nA nA
$I_{OS}$	Input Offset Current	$V_{CM} = V^+ - 0.1\text{V}$	●		30	210	nA
		$V_{CM} = V^- + 0.2\text{V}$	●		30	210	nA
$\Delta I_{OS}$	Input Offset Current Shift	$V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●		60	420	nA
$A_{VOL}$	Large-Signal Voltage Gain	$V_O = -14.5\text{V}$ to $14.5\text{V}$ , $R_L = 10\text{k}$ $V_O = -10\text{V}$ to $10\text{V}$ , $R_L = 2\text{k}$	● ●	700 400	6000 4000		V/mV V/mV
	Channel Separation	$V_O = -10\text{V}$ to $10\text{V}$ , $R_L = 2\text{k}$	●	112	132		dB
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●	87	104		dB
	CMRR Match (Channel-to-Channel) (Note 5)	$V_{CM} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●	84	104		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$	●	84	100		dB
	PSRR Match (Channel-to-Channel) (Note 5)	$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$	●	80	100		dB
$V_{OL}$	Output Voltage Swing Low (Note 6)	No Load	●		22	50	mV
		$I_{SINK} = 5\text{mA}$	●		180	350	mV
		$I_{SINK} = 25\text{mA}$	●		700	1400	mV
$V_{OH}$	Output Voltage Swing High (Note 6)	No Load	●		15	40	mV
		$I_{SOURCE} = 5\text{mA}$	●		300	600	mV
		$I_{SOURCE} = 25\text{mA}$	●		1500	3000	mV
$I_{SC}$	Short-Circuit Current		●	$\pm 27$	$\pm 54$		mA
$I_S$	Supply Current per Amplifier		●		4.8	5.9	mA
GBW	Gain-Bandwidth Product (Note 7)	$f = 100\text{kHz}$	●	14	27		MHz
SR	Slew Rate	$A_V = -1$ , $R_L = \text{Open}$ , $V_O = \pm 10\text{V}$ , Measured at $V_O = \pm 5\text{V}$	●	4.2	8.5		V/ $\mu\text{s}$

# LT1630/LT1631

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range of  $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$ .  $V_S = \pm 15\text{V}$ ,  $V_{\text{CM}} = 0\text{V}$ ,  $V_{\text{OUT}} = 0\text{V}$ , unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{\text{OS}}$	Input Offset Voltage	$V_{\text{CM}} = V^+ - 0.1\text{V}$	●		525	1600	$\mu\text{V}$
		$V_{\text{CM}} = V^- + 0.2\text{V}$	●		525	1600	$\mu\text{V}$
$V_{\text{OS TC}}$	Input Offset Voltage Drift (Note 3)		●		4.5	7	$\mu\text{V}/^{\circ}\text{C}$
		$V_{\text{CM}} = V^- - 0.1\text{V}$	●		1.5	4	$\mu\text{V}/^{\circ}\text{C}$
$\Delta V_{\text{OS}}$	Input Offset Voltage Shift	$V_{\text{CM}} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●		220	1300	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel)	$V_{\text{CM}} = V^- + 0.2\text{V}$ , $V^+ - 0.1\text{V}$ (Note 5)	●		350	2200	$\mu\text{V}$
$I_{\text{B}}$	Input Bias Current	$V_{\text{CM}} = V^+ - 0.1\text{V}$	●	0	750	1500	nA
		$V_{\text{CM}} = V^- + 0.2\text{V}$	●	-1500	-750	0	nA
$\Delta I_{\text{B}}$	Input Bias Current Shift	$V_{\text{CM}} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●		1380	2800	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{\text{CM}} = V^+ - 0.1\text{V}$ (Note 5) $V_{\text{CM}} = V^- + 0.2\text{V}$ (Note 5)	● ●		42	460	nA nA
$I_{\text{OS}}$	Input Offset Current	$V_{\text{CM}} = V^+ - 0.1\text{V}$	●		30	210	nA
		$V_{\text{CM}} = V^- + 0.2\text{V}$	●		30	210	nA
$\Delta I_{\text{OS}}$	Input Offset Current Shift	$V_{\text{CM}} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●		60	420	nA
$A_{\text{VOL}}$	Large-Signal Voltage Gain	$V_{\text{O}} = -14.5\text{V}$ to $14.5\text{V}$ , $R_{\text{L}} = 10\text{k}$ $V_{\text{O}} = -10\text{V}$ to $10\text{V}$ , $R_{\text{L}} = 2\text{k}$	● ●	700 400	6000 4000		V/mV V/mV
	Channel Separation	$V_{\text{O}} = -10\text{V}$ to $10\text{V}$ , $R_{\text{L}} = 2\text{k}$	●	112	132		dB
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●	87	104		dB
	CMRR Match (Channel-to-Channel) (Note 5)	$V_{\text{CM}} = V^- + 0.2\text{V}$ to $V^+ - 0.1\text{V}$	●	84	104		dB
PSRR	Power Supply Rejection Ratio	$V_{\text{S}} = \pm 5\text{V}$ to $\pm 15\text{V}$	●	84	100		dB
	PSRR Match (Channel-to-Channel) (Note 5)	$V_{\text{S}} = \pm 5\text{V}$ to $\pm 15\text{V}$	●	80	100		dB
$V_{\text{OL}}$	Output Voltage Swing Low (Note 6)	No Load	●		22	60	mV
		$I_{\text{SINK}} = 5\text{mA}$	●		180	400	mV
		$I_{\text{SINK}} = 25\text{mA}$	●		700	1500	mV
$V_{\text{OH}}$	Output Voltage Swing High (Note 6)	No Load	●		15	50	mV
		$I_{\text{SOURCE}} = 5\text{mA}$	●		300	675	mV
		$I_{\text{SOURCE}} = 25\text{mA}$	●		1500	3300	mV
$I_{\text{SC}}$	Short-Circuit Current		●	$\pm 27$	$\pm 54$		mA
$I_{\text{S}}$	Supply Current per Amplifier		●		4.8	6.4	mA
GBW	Gain-Bandwidth Product (Note 7)	$f = 100\text{kHz}$	●	13	27		MHz
SR	Slew Rate	$A_{\text{V}} = -1$ , $R_{\text{L}} = \text{Open}$ , $V_{\text{O}} = \pm 10\text{V}$ , Measured at $V_{\text{O}} = \pm 5\text{V}$	●	4.2	8.5		V/ $\mu\text{s}$

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

**Note 3:** This parameter is not 100% tested.

**Note 4:** The LT1630C/LT1631C are guaranteed to meet specified performance from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ . The LT1630C/LT1631C and are designed, characterized and expected to meet specified performance from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  but are not tested or QA sampled at these temperatures. The LT1630I/LT1631I are guaranteed to meet specified performance from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The LT1630H is guaranteed to meet specified performance from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

**Note 5:** Matching parameters are the difference between amplifiers A and D and between B and C on the LT1631; between the two amplifiers on the LT1630.

**Note 6:** Output voltage swings are measured between the output and power supply rails.

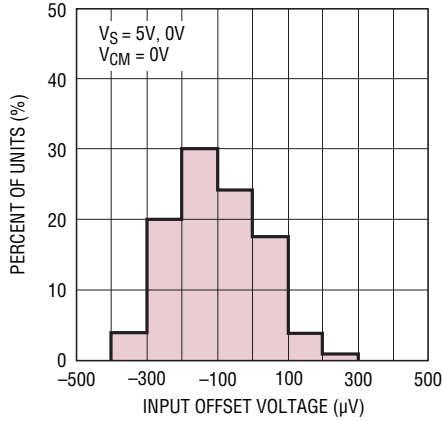
**Note 7:**  $V_{\text{S}} = 3\text{V}$ ,  $V_{\text{S}} = \pm 15\text{V}$  GBW limit guaranteed by correlation to 5V tests.

**Note 8:**  $V_{\text{S}} = 3\text{V}$ ,  $V_{\text{S}} = 5\text{V}$  slew rate limit guaranteed by correlation to  $\pm 15\text{V}$  tests.

**Note 9:** Minimum supply voltage is guaranteed by testing the change of  $V_{\text{OS}}$  to be less than  $250\mu\text{V}$  when the supply voltage is varied from 3V to 2.7V.

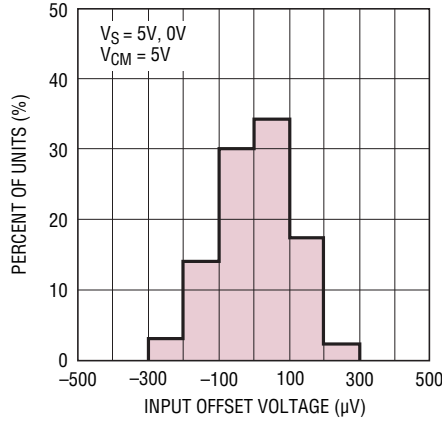
# TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{OS}$  Distribution,  $V_{CM} = 0V$  (PNP Stage)**



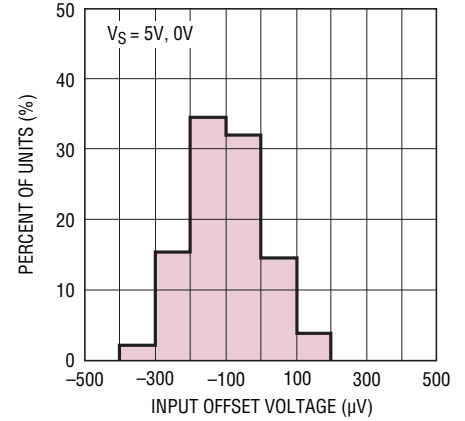
1630/31 G32

**$V_{OS}$  Distribution,  $V_{CM} = 5V$  (NPN Stage)**



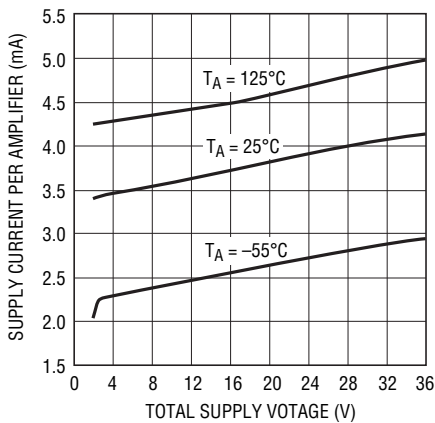
1630/31 G33

**$\Delta V_{OS}$  Shift for  $V_{CM} = 0V$  to  $5V$**



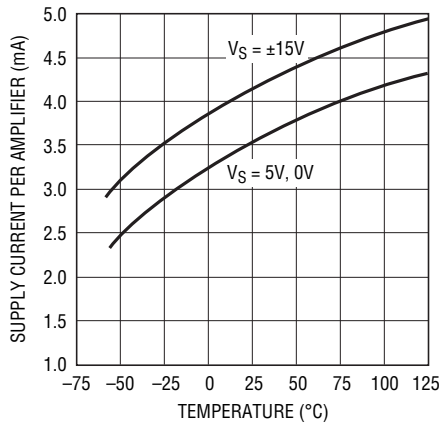
1630/31 G34

**Supply Current vs Supply Voltage**



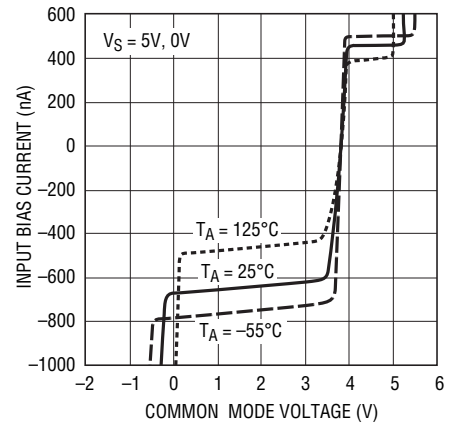
1630/31 G01

**Supply Current vs Temperature**



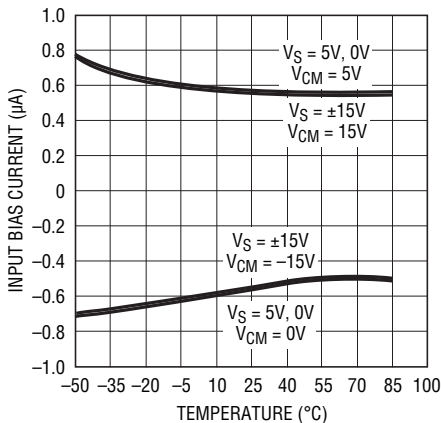
1630/31 G02

**Input Bias Current vs Common Mode Voltage**



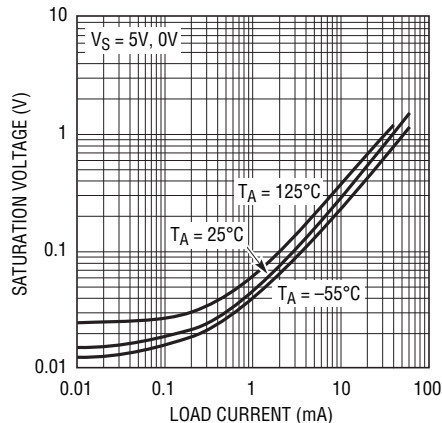
1630/31 G03

**Input Bias Current vs Temperature**



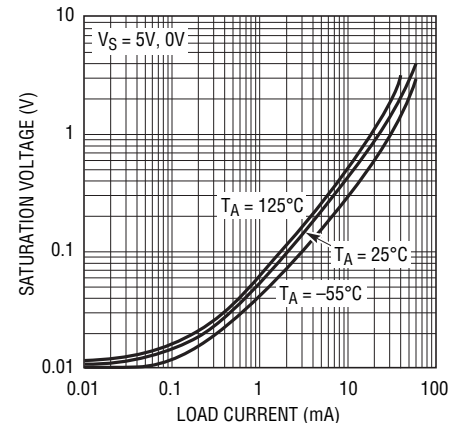
1630/31 G04

**Output Saturation Voltage vs Load Current (Output Low)**



1630/31 G05

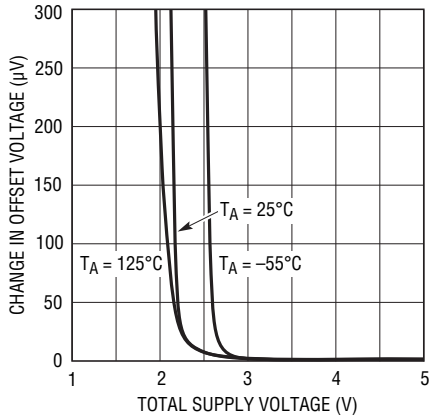
**Output Saturation Voltage vs Load Current (Output High)**



1630/31 G06

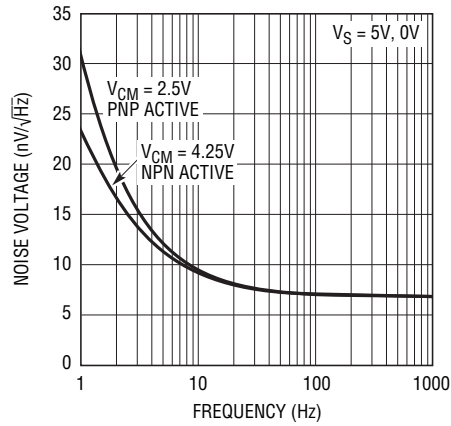
## TYPICAL PERFORMANCE CHARACTERISTICS

### Minimum Supply Voltage



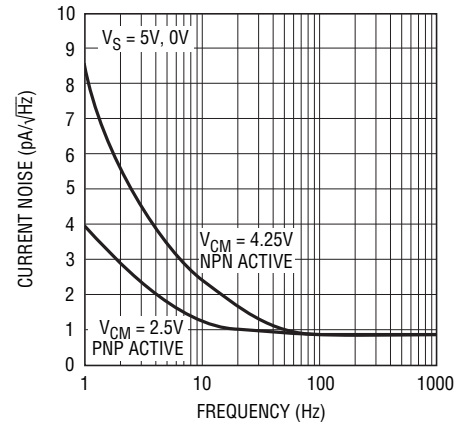
1630/31 G07

### Noise Voltage Spectrum



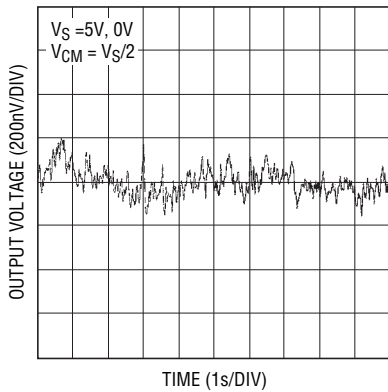
11630/31 G09

### Current Noise Spectrum



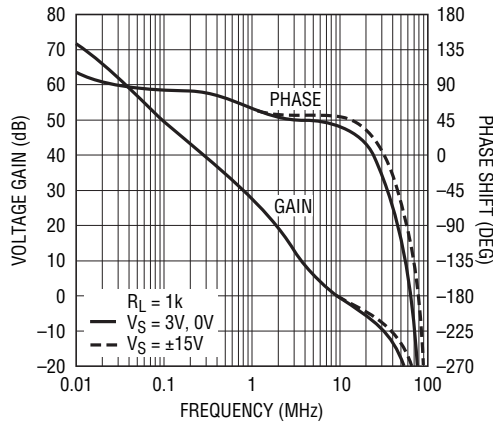
1630/31 G10

### 0.1Hz to 10Hz Output Voltage Noise



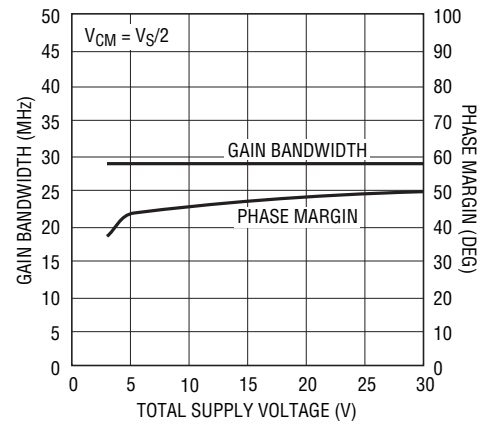
1630/31 G25

### Gain and Phase vs Frequency



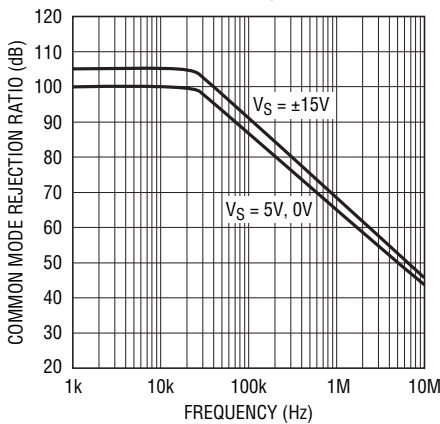
1630/31 G11

### Gain Bandwidth and Phase Margin vs Supply Voltage



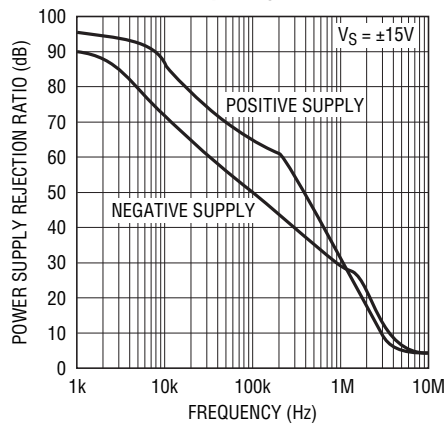
1630/31 G14

### CMRR vs Frequency



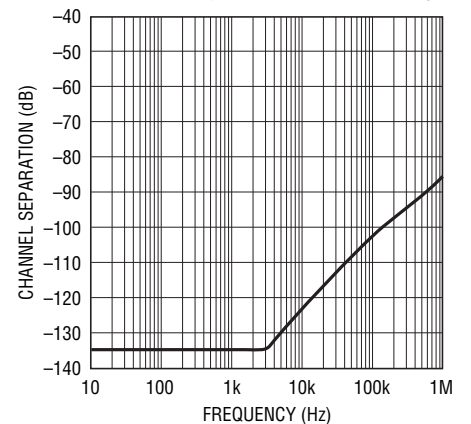
1630/31 G12

### PSRR vs Frequency



1630/31 G13

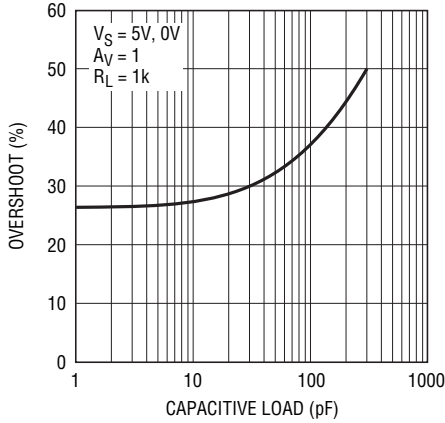
### Channel Separation vs Frequency



1630/31 G15

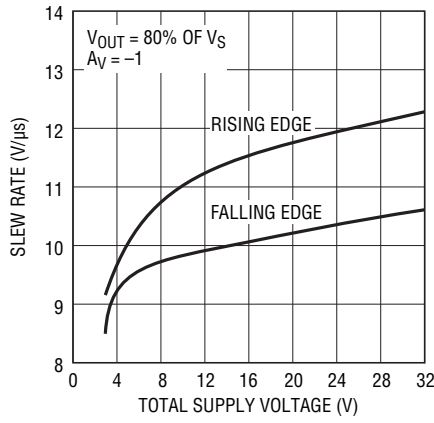
# TYPICAL PERFORMANCE CHARACTERISTICS

**Capacitive Load Handling**



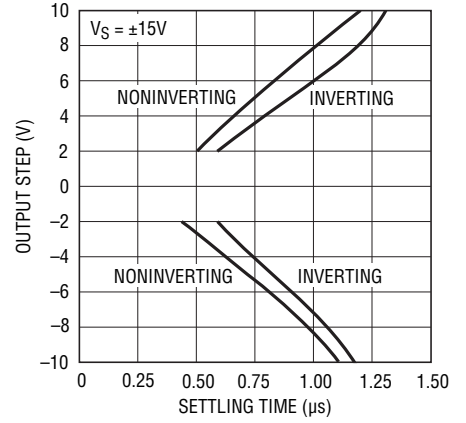
1630/31 G16

**Slew Rate vs Supply Voltage**



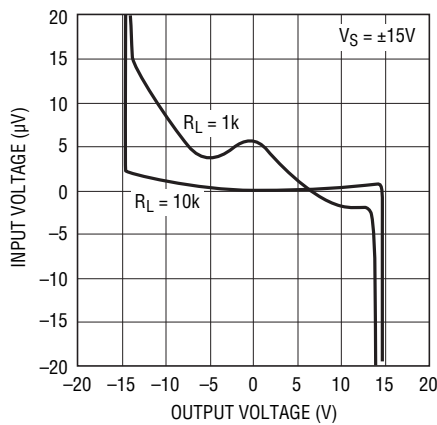
1630/31 G17

**Output Step vs Settling Time to 0.01%**



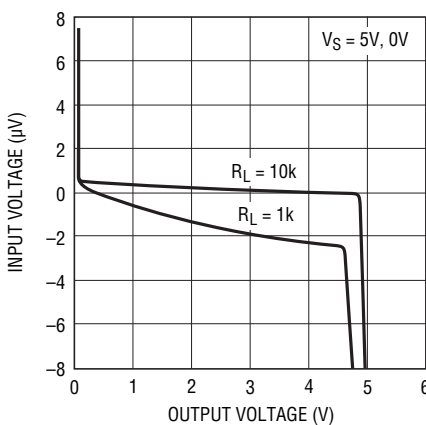
1630/31 G18

**Open-Loop Gain**



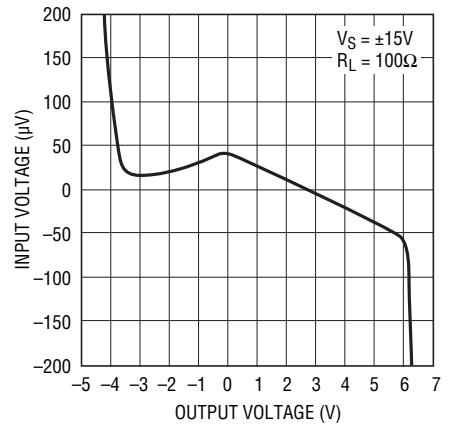
1630/31 G19

**Open-Loop Gain**



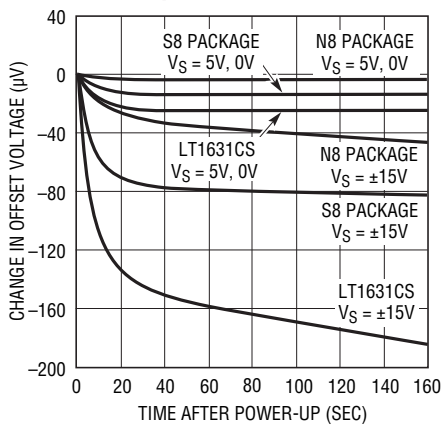
1630/31 G20

**Open-Loop Gain**



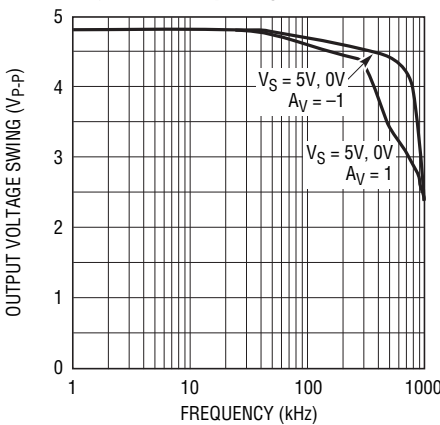
1630/31 G21

**Warm-Up Drift vs Time**



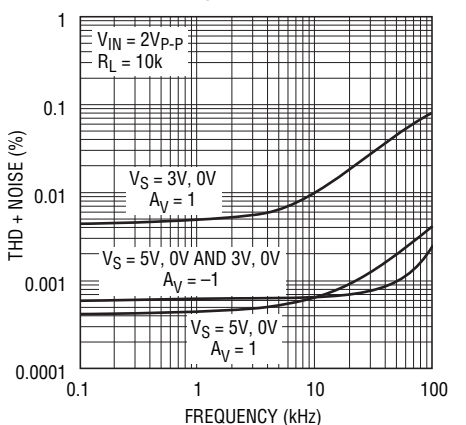
1630/31 G22

**Maximum Undistorted Output Signal vs Frequency**



1630/31 G24

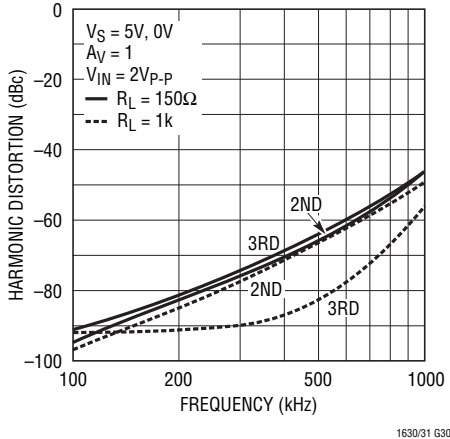
**Total Harmonic Distortion + Noise vs Frequency**



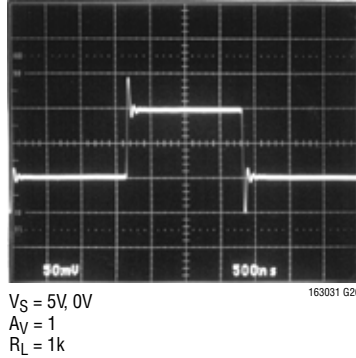
1630/31 G23

TYPICAL PERFORMANCE CHARACTERISTICS

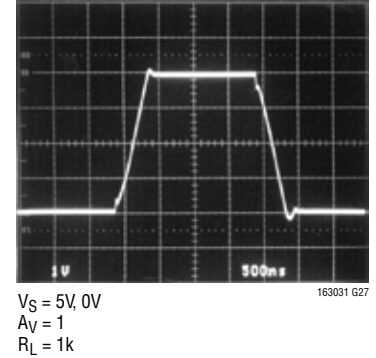
Harmonic Distortion vs Frequency



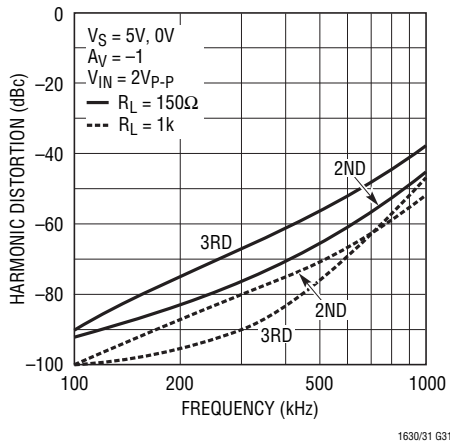
5V Small-Signal Response



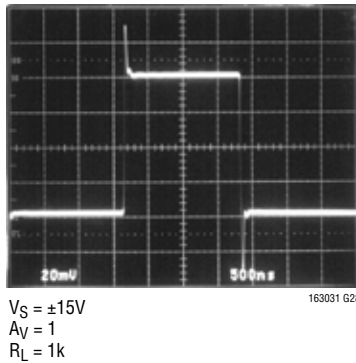
5V Large-Signal Response



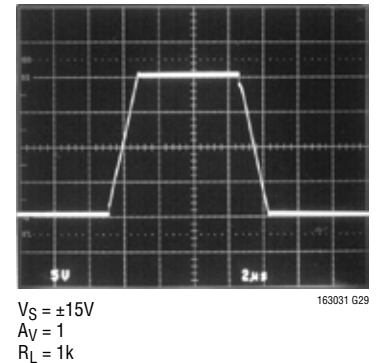
Harmonic Distortion vs Frequency



±15V Small-Signal Response



±15V Large-Signal Response



APPLICATIONS INFORMATION

Rail-to-Rail Input and Output

The LT1630/LT1631 are fully functional for an input and output signal range from the negative supply to the positive supply. Figure 1 shows a simplified schematic of the amplifier. The input stage consists of two differential amplifiers, a PNP stage Q1/Q2 and an NPN stage Q3/Q4 that are active over different ranges of input common mode voltage. The PNP differential input pair is active for input common mode voltages  $V_{CM}$  between the negative supply to approximately 1.4V below the positive supply. As  $V_{CM}$  moves closer toward the positive supply, the transis-

tor Q5 will steer the tail current  $I_1$  to the current mirror Q6/Q7, activating the NPN differential pair and the PNP pair becomes inactive for the rest of the input common mode range up to the positive supply.

The output is configured with a pair of complementary common emitter stages Q14/Q15 that enables the output to swing from rail to rail. These devices are fabricated on Linear Technology's proprietary complementary bipolar process to ensure similar DC and AC characteristics. Capacitors C1 and C2 form local feedback loops that lower the output impedance at high frequencies.

## APPLICATIONS INFORMATION

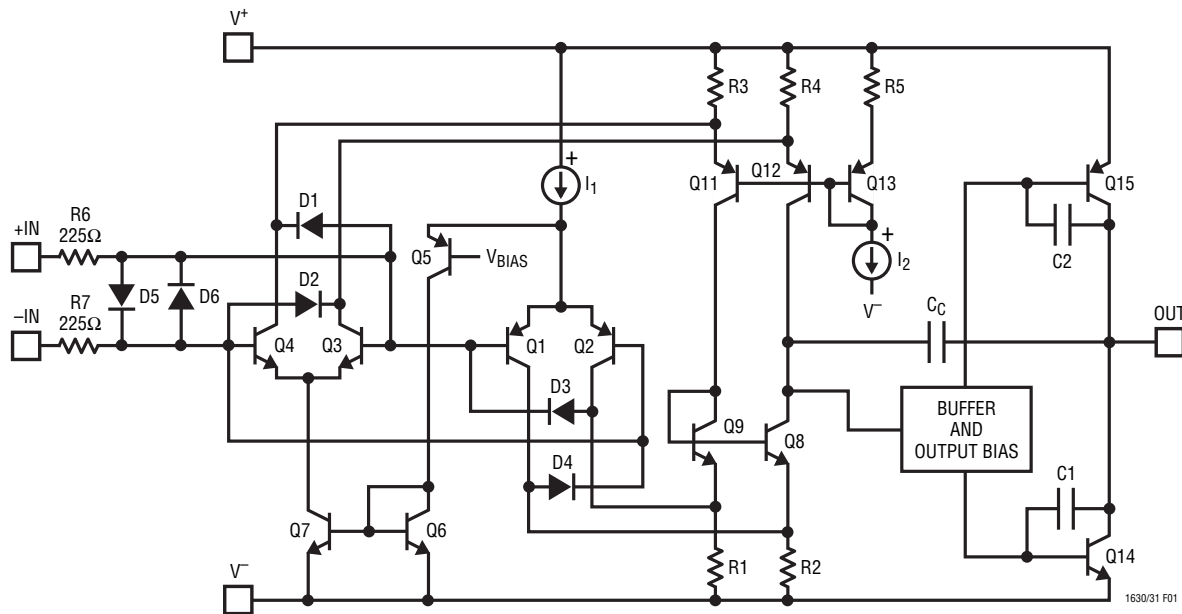


Figure 1. LT1630 Simplified Schematic Diagram

### Power Dissipation

The LT1630/LT1631 amplifiers combine high speed and large output current drive in a small package. Because the amplifiers operate over a very wide supply range, it is possible to exceed the maximum junction temperature of 150°C in plastic packages under certain conditions. Junction temperature,  $T_J$ , is calculated from the ambient temperature,  $T_A$ , and power dissipation,  $P_D$ , as follows:

$$\text{LT1630CN8: } T_J = T_A + (P_D \cdot 130^\circ\text{C/W})$$

$$\text{LT1630CS8: } T_J = T_A + (P_D \cdot 190^\circ\text{C/W})$$

$$\text{LT1631CS: } T_J = T_A + (P_D \cdot 150^\circ\text{C/W})$$

The power dissipation in the IC is the function of the supply voltage, output voltage and load resistance. For a given supply voltage, the worst-case power dissipation  $P_{D\text{MAX}}$  occurs at the maximum supply current and when the output voltage is at half of either supply voltage (or the maximum swing if less than 1/2 supply voltage). Therefore  $P_{D\text{MAX}}$  is given by:

$$P_{D\text{MAX}} = (V_S \cdot I_{S\text{MAX}}) + (V_S/2)^2/R_L$$

To ensure that the LT1630/LT1631 are used properly, calculate the worst-case power dissipation, get the thermal resistance for a chosen package and its maximum junction temperature to derive the maximum ambient temperature.

Example: An LT1630CS8 operating on  $\pm 15\text{V}$  supplies and driving a  $500\Omega$ , the worst-case power dissipation per amplifier is given by:

$$P_{D\text{MAX}} = (30\text{V} \cdot 4.75\text{mA}) + (15\text{V} - 7.5\text{V})(7.5/500) \\ = 0.143 + 0.113 = 0.256\text{W}$$

If both amplifiers are loaded simultaneously, then the total power dissipation is 0.512W. The SO-8 package has a junction-to-ambient thermal resistance of  $190^\circ\text{C/W}$  in still air. Therefore, the maximum ambient temperature that the part is allowed to operate is:

$$T_A = T_J - (P_{D\text{MAX}} \cdot 190^\circ\text{C/W}) \\ T_A = 150^\circ\text{C} - (0.512\text{W} \cdot 190^\circ\text{C/W}) = 53^\circ\text{C}$$

For a higher operating temperature, lower the supply voltage or use the DIP package part.



## APPLICATIONS INFORMATION

### Input Offset Voltage

The offset voltage changes depending upon which input stage is active, and the maximum offset voltages are trimmed to less than  $525\mu\text{V}$ . To maintain the precision characteristics of the amplifier, the change of  $V_{OS}$  over the entire input common mode range (CMRR) is guaranteed to be less than  $525\mu\text{V}$  on a single 5V supply.

### Input Bias Current

The input bias current polarity depends on the input common mode voltage. When the PNP differential pair is active, the input bias currents flow out of the input pins. They flow in the opposite direction when the NPN input stage is active. The offset voltage error due to input bias currents can be minimized by equalizing the noninverting and inverting input source impedance.

### Output

The outputs of the LT1630/LT1631 can deliver large load currents; the short-circuit current limit is 70mA. Take care to keep the junction temperature of the IC below the absolute maximum rating of  $150^{\circ}\text{C}$  (refer to the Power Dissipation section). The output of these amplifiers have reverse-biased diodes to each supply. If the output is forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to several hundred mA, no damage to the part will occur.

### Overdrive Protection

To prevent the output from reversing polarity when the input voltage exceeds the power supplies, two pairs of crossing diodes D1 to D4 are employed. When the input voltage exceeds either power supply by approximately 700mV, D1/D2 or D3/D4 will turn on, forcing the output to the proper polarity. For this phase reversal protection to work properly, the input current must be limited to less than 5mA. If the amplifier is to be severely overdriven, an external resistor should be used to limit the overdrive current.

The LT1630/LT1631's input stages are protected against large differential input voltages by a pair of back-to-back diodes D5/D6. When a differential voltage of more than 0.7V is applied to the inputs, these diodes will turn on, preventing the emitter-base breakdown of the input transistors. The current in D5/D6 should be limited to less than 10mA. Internal  $225\Omega$  resistors R6 and R7 will limit the input current for differential input signals of 4.5V or less. For larger input levels, a resistor in series with either or both inputs should be used to limit the current. Worst-case differential input voltage usually occurs when the output is shorted to ground. In addition, the amplifier is protected against ESD strikes up to 3kV on all pins.

### Capacitive Load

The LT1630/LT1631 are wideband amplifiers that can drive capacitive loads up to 200pF on  $\pm 15\text{V}$  supplies in a unity-gain configuration. On a 3V supply, the capacitive load should be kept to less than 100pF. When there is a need to drive larger capacitive loads, a resistor of  $20\Omega$  to  $50\Omega$  should be connected between the output and the capacitive load. The feedback should still be taken from the output so that the resistor isolates the capacitive load to ensure stability.

### Feedback Components

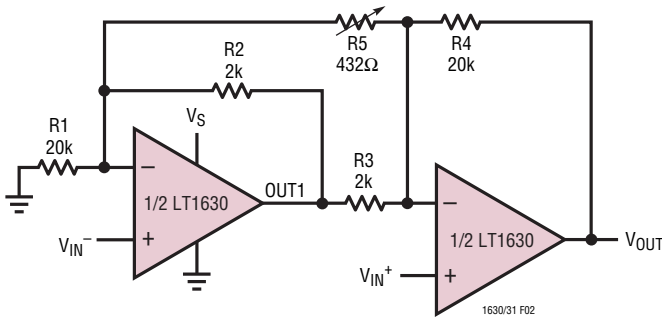
The low input bias currents of the LT1630/LT1631 make it possible to use the high value feedback resistors to set the gain. However, care must be taken to ensure that the pole formed by the feedback resistors and the total capacitance at the inverting input does not degrade stability. For instance, the LT1630/LT1631 in a noninverting gain of 2, set with two 20k resistors, will probably oscillate with 10pF total input capacitance (5pF input capacitance and 5pF board capacitance). The amplifier has a 5MHz crossing frequency and a  $52^{\circ}$  phase margin at 6dB of gain. The feedback resistors and the total input capacitance form a pole at 1.6MHz that induces a phase shift of  $72^{\circ}$  at 5MHz! The solution is simple: either lower the value of the resistors or add a feedback capacitor of 10pF or more.



## TYPICAL APPLICATIONS

### Single Supply, 40dB Gain, 350kHz Instrumentation Amplifier

An instrumentation amplifier with a rail-to-rail output swing, operating from a 3V supply can be constructed with the LT1630 as shown in Figure 2. The amplifier has a nominal gain of 100, which can be adjusted with resistor R5. The DC output level is set by the difference of the two inputs multiplied by the gain of 100. Common mode range can be calculated by the equations shown with Figure 2. For example, the common mode range is from 0.15V to 2.65V if the output is set at one half of the 3V supply. The common mode rejection is greater than 110dB at 100Hz when trimmed with resistor R1. The amplifier has a bandwidth of 355kHz as shown in Figure 3.



BW = 355kHz

$$A_V = \frac{R4}{R3} \left( 1 + \frac{R2}{R1} + \frac{R3+R2}{R5} \right) = 100$$

$$V_{OUT} = (V_{IN+} - V_{IN-}) \cdot A_V$$

LOWER LIMIT COMMON MODE INPUT VOLTAGE

$$V_{CML} = \left[ \left( \frac{V_{OUT}}{A_V} \right) \frac{R2}{R5} + 0.1V \right] \frac{1.0}{1.1}$$

UPPER LIMIT COMMON MODE INPUT VOLTAGE

$$V_{CMH} = \left[ \left( \frac{V_{OUT}}{A_V} \right) \frac{R2}{R5} + (V_S - 0.15V) \right] \frac{1.0}{1.1}$$

WHERE  $V_S$  IS THE SUPPLY CURRENT

Figure 2. Single Supply, 40dB Gain Instrumentation Amplifier

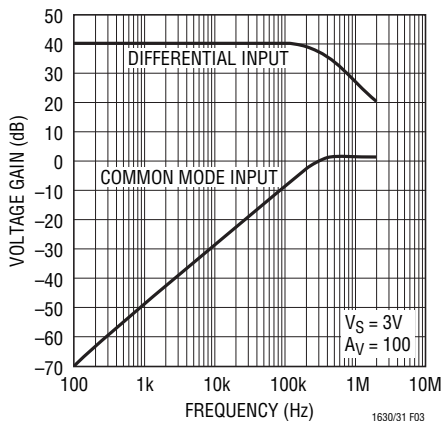


Figure 3. Frequency Response

### Tunable Q Notch Filter

A single supply, tunable Q notch filter as shown in Figure 4 is built with LT1630 to maximize the output swing. The filter has a gain of 2, and the notch frequency ( $f_0$ ) is set by the values of R and C. The resistors R10 and R11 set up the DC level at the output. The Q factor can be adjusted by varying the value of R8. The higher value of R8 will decrease Q as depicted in Figure 5, because the output induces less of feedback to amplifier A2. The value of R7 should be equal or greater than R9 to prevent oscillation. If R8 is a short and R9 is larger than R7, then the positive feedback from the output will create phase inversion at the output of amplifier A2, which will lead to oscillation.

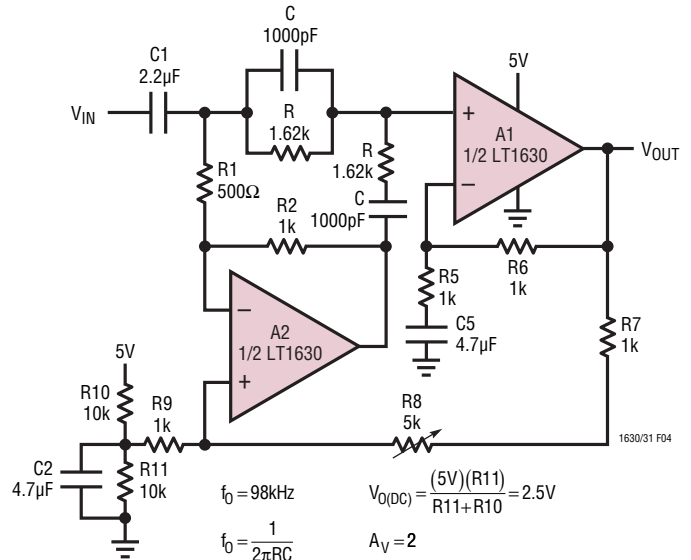


Figure 4. Tunable Q Notch Filter

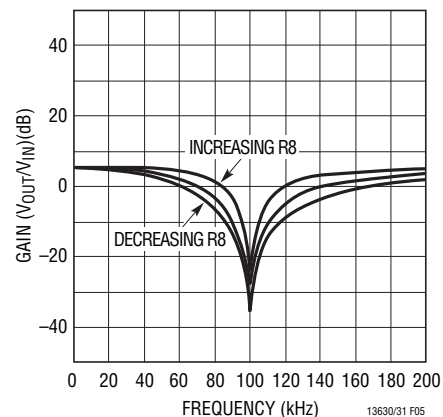
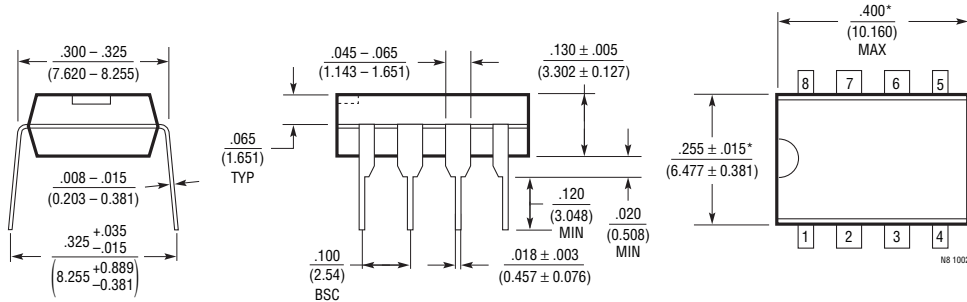


Figure 5. Frequency Response

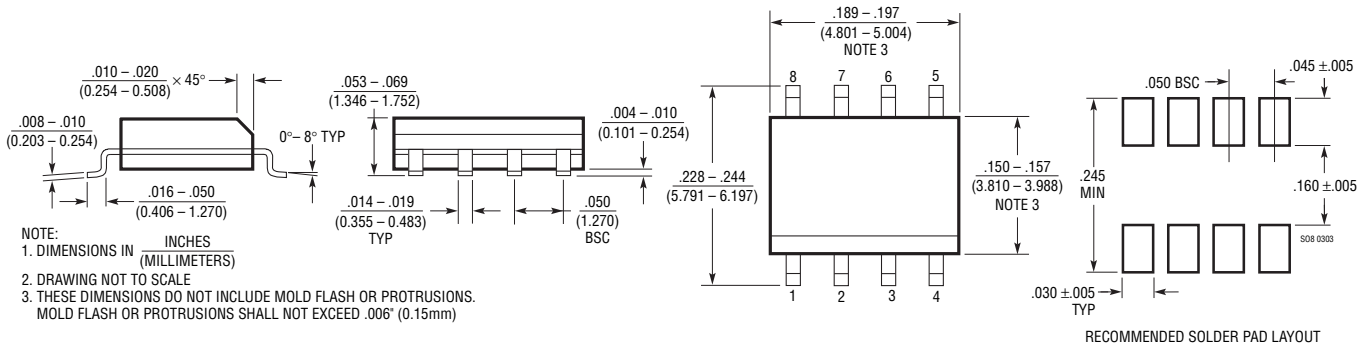
## PACKAGE DESCRIPTION

### N8 Package 8-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)



NOTE:  
1. DIMENSIONS ARE IN INCHES  
MILLIMETERS  
\*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

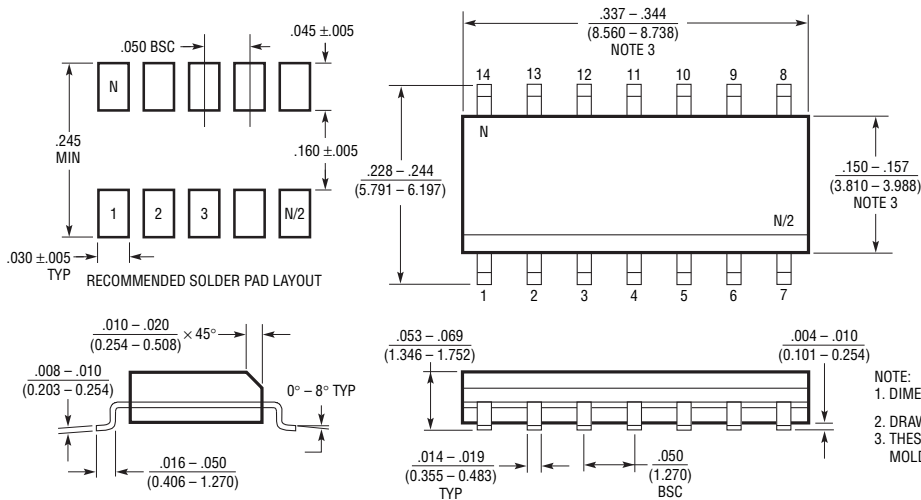
### S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



NOTE:  
1. DIMENSIONS IN INCHES  
(MILLIMETERS)  
2. DRAWING NOT TO SCALE  
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

RECOMMENDED SOLDER PAD LAYOUT

### S Package 14-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



NOTE:  
1. DIMENSIONS IN INCHES  
(MILLIMETERS)  
2. DRAWING NOT TO SCALE  
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

## REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	2/2010	Changes to Absolute Maximum Ratings	2
		Updated Order Information Section	2
		Added H Grade Part	2
		Added H Grade Electrical Characteristics Tables	6, 10