

Over-The-Top Micropower Rail-to-Rail Input and Output Op Amp

FEATURES

- Rail-to-Rail Input and Output
- Micropower: 50 μ A I_Q , 44V Supply
- Operating Temperature Range: -40°C to 125°C
- Over-The-Top[®]: Input Common Mode Range Extends 44V Above V_{EE} , Independent of V_{CC}
- Low Input Offset Voltage: 225 μ V Max
- Specified on 3V, 5V and \pm 15V Supplies
- High Output Current: 18mA
- Output Shutdown
- Output Drives 10,000pF with Output Compensation
- Reverse Battery Protection to 27V
- High Voltage Gain: 2000V/mV
- High CMRR: 110dB
- 220kHz Gain-Bandwidth Product
- 8-Lead DFN, MSOP, PDIP and SO Packages

APPLICATIONS

- Battery- or Solar-Powered Systems
 - Portable Instrumentation
 - Sensor Conditioning
- Supply Current Sensing
- Battery Monitoring
- MUX Amplifiers
- 4mA to 20mA Transmitters

DESCRIPTION

The LT[®]1636 op amp operates on all single and split supplies with a total voltage of 2.7V to 44V drawing less than 50 μ A of quiescent current. The LT1636 can be shut down, making the output high impedance and reducing the quiescent current to 4 μ A. The LT1636 has a unique input stage that operates and remains high impedance when above the positive supply. The inputs take 44V both differential and common mode, even when operating on a 3V supply. The output swings to both supplies. Unlike most micropower op amps, the LT1636 can drive heavy loads; its rail-to-rail output drives 18mA. The LT1636 is unity-gain stable into all capacitive loads up to 10,000pF when a 0.22 μ F and 150 Ω compensation network is used.

The LT1636 is reverse supply protected: it draws no current for reverse supply up to 27V. Built-in resistors protect the inputs for faults below the negative supply up to 22V. There is no phase reversal of the output for inputs 5V below V_{EE} or 44V above V_{EE} , independent of V_{CC} .

The LT1636 op amp is available in the 8-pin MSOP, PDIP and SO packages. For space limited applications the LT1636 is available in a 3mm \times 3mm \times 0.8mm dual fine pitch leadless package (DFN).

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TYPICAL APPLICATION

Over-The-Top Current Source with Shutdown



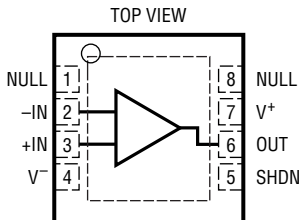
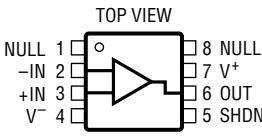
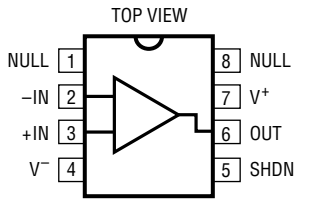
Input Bias Current vs Common Mode Voltage



ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-)	44V	Specified Temperature Range (Note 4)	
Input Differential Voltage	44V	LT1636C/LT1636I	-40°C to 85°C
Input Current	±25mA	LT1636H	-40°C to 125°C
Shutdown Pin Voltage Above V^-	32V	Junction Temperature	150°C
Shutdown Pin Current	±10mA	Junction Temperature (DD Package)	125°C
Output Short-Circuit Duration (Note 2)	Continuous	Storage Temperature Range	-65°C to 150°C
Operating Temperature Range (Note 3)		Storage Temperature Range	
LT1636C/LT1636I	-40°C to 85°C	(DD Package)	-65°C to 125°C
LT1636H	-40°C to 125°C	Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

 <p>DD PACKAGE 8-LEAD (3mm × 3mm) PLASTIC DFN $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 160^{\circ}\text{C/W}$ (NOTE 2) UNDERSIDE METAL CONNECTED TO V^-</p>		 <p>MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 250^{\circ}\text{C/W}$</p>		 <p>N8 PACKAGE 8-LEAD PDIP S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 150^{\circ}\text{C/W}$ (N8) $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 190^{\circ}\text{C/W}$ (S8)</p>	
ORDER PART NUMBER	DD PART* MARKING	ORDER PART NUMBER	MS8 PART* MARKING	ORDER PART NUMBER	S8 PART* MARKING
LT1636CDD LT1636IDD	LAAJ	LT1636CMS8 LT1636IMS8	LTCL	LT1636CN8 LT1636CS8 LT1636IN8 LT1636IS8 LT1636HS8	1636 1636I 1636H

*The temperature grades are identified by a label on the shipping container. Consult factory for parts specified with wider operating temperature ranges.

3V AND 5V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range of $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$.
 $V_S = 3\text{V}$, 0V ; $V_S = 5\text{V}$, 0V ; $V_{CM} = V_{OUT} = \text{half supply unless otherwise specified. (Note 4)}$

SYMBOL	PARAMETER	CONDITIONS	LT1636C/LT1636I			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	N8 Package $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$		50	225	μV
			●		400	μV
			●		550	μV
		S8 Package $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$		50	225	μV
			●		600	μV
			●		750	μV
MS8 Package $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$		50	225	μV		
	●		700	μV		
	●		1050	μV		

3V AND 5V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range of $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$.
 $V_S = 3\text{V}, 0\text{V}$; $V_S = 5\text{V}, 0\text{V}$; $V_{CM} = V_{OUT} = \text{half supply unless otherwise specified. (Note 4)}$

SYMBOL	PARAMETER	CONDITIONS	LT1636C/LT1636I			UNITS
			MIN	TYP	MAX	
		DD Package $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●	75	425	μV
			●		900	μV
			●		1050	μV
	Input Offset Voltage Drift (Note 9)	N8 Package, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ S8 Package, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ MS8 Package, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ DD Package, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●	1	5	$\mu\text{V}/^{\circ}\text{C}$
			●	2	8	$\mu\text{V}/^{\circ}\text{C}$
			●	2	10	$\mu\text{V}/^{\circ}\text{C}$
			●	2	10	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current	$V_{CM} = 44\text{V}$ (Note 5)	●	0.1	0.8	nA
			●		0.6	μA
I_B	Input Bias Current	$V_{CM} = 44\text{V}$ (Note 5) $V_S = 0\text{V}$	●	5	8	nA
			●	3	6	μA
				0.1		nA
	Input Noise Voltage	0.1Hz to 10Hz		0.7		μV_{P-P}
e_n	Input Noise Voltage Density	$f = 1\text{kHz}$		52		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 1\text{kHz}$		0.035		$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	Differential Common Mode, $V_{CM} = 0\text{V}$ to 44V		6	10	M Ω
				7	15	M Ω
C_{IN}	Input Capacitance			4		pF
	Input Voltage Range		●	0	44	V
CMRR	Common Mode Rejection Ratio (Note 5)	$V_{CM} = 0\text{V}$ to $V_{CC} - 1\text{V}$ $V_{CM} = 0\text{V}$ to 44V (Note 8)	●	84	110	dB
			●	86	98	dB
A_{VOL}	Large-Signal Voltage Gain	$V_S = 3\text{V}, V_O = 500\text{mV}$ to 2.5V, $R_L = 10\text{k}$ $V_S = 3\text{V}, 0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ $V_S = 3\text{V}, -40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●	200	1300	V/mV
			●	133		V/mV
			●	100		V/mV
		$V_S = 5\text{V}, V_O = 500\text{mV}$ to 4.5V, $R_L = 10\text{k}$ $V_S = 5\text{V}, 0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ $V_S = 5\text{V}, -40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●	400	2000	V/mV
			●	250		V/mV
			●	200		V/mV
V_{OL}	Output Voltage Swing LOW	No Load $I_{SINK} = 5\text{mA}$ $V_S = 5\text{V}, I_{SINK} = 10\text{mA}$	●		2	mV
			●		480	mV
			●		875	mV
			●		860	1600
V_{OH}	Output Voltage Swing HIGH	$V_S = 3\text{V}$, No Load $V_S = 3\text{V}, I_{SOURCE} = 5\text{mA}$	●	2.95	2.985	V
			●	2.55	2.8	V
		$V_S = 5\text{V}$, No Load $V_S = 5\text{V}, I_{SOURCE} = 10\text{mA}$	●	4.95	4.985	V
			●	4.30	4.75	V
I_{SC}	Short-Circuit Current (Note 2)	$V_S = 3\text{V}$, Short to GND $V_S = 3\text{V}$, Short to V_{CC}		7	15	mA
				20	42	mA
		$V_S = 5\text{V}$, Short to GND $V_S = 5\text{V}$, Short to V_{CC}		12	25	mA
				25	50	mA
PSRR	Power Supply Rejection Ratio	$V_S = 2.7\text{V}$ to 12.5V, $V_{CM} = V_O = 1\text{V}$	●	90	103	dB
	Reverse Supply Voltage	$I_S = -100\mu\text{A}$	●	27	40	V
I_S	Supply Current	(Note 6)	●	42	55	μA
			●		60	μA
	Supply Current, SHDN	$V_{PIN5} = 2\text{V}$, No Load (Note 6)	●	4	12	μA
I_{SD}	Shutdown Pin Current	$V_{PIN5} = 0.3\text{V}$, No Load (Note 6) $V_{PIN5} = 2\text{V}$, No Load (Note 5)	●	0.5	15	nA
			●	1.1	5	μA
	Output Leakage Current, SHDN	$V_{PIN5} = 2\text{V}$, No Load (Note 6)	●	0.05	1	μA
	Maximum Shutdown Pin Current	$V_{PIN5} = 32\text{V}$, No Load (Note 5)	●	27	150	μA
t_{ON}	Turn-On Time	$V_{PIN5} = 5\text{V}$ to 0V, $R_L = 10\text{k}$		120		μs
t_{OFF}	Turn-Off Time	$V_{PIN5} = 0\text{V}$ to 5V, $R_L = 10\text{k}$		2.5		μs

3V AND 5V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range of $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$.
 $V_S = 3\text{V}, 0\text{V}; V_S = 5\text{V}, 0\text{V}; V_{CM} = V_{OUT} = \text{half supply unless otherwise specified. (Note 4)}$

SYMBOL	PARAMETER	CONDITIONS	LT1636C/LT1636I			UNITS
			MIN	TYP	MAX	
GBW	Gain Bandwidth Product (Note 5)	$f = 1\text{kHz}$	110	200		kHz
		$0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$	● 100			kHz
		$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	● 90			kHz
SR	Slew Rate (Note 7)	$A_V = -1, R_L = \infty$	0.035	0.07		V/ μs
		$0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$	● 0.031			V/ μs
		$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	● 0.030			V/ μs

±15V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range of $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$.
 $V_S = \pm 15\text{V}, V_{CM} = 0\text{V}, V_{OUT} = 0\text{V}, V_{SHDN} = V^- \text{ unless otherwise specified. (Note 4)}$

SYMBOL	PARAMETER	CONDITIONS	LT1636C/LT1636I			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	N8 Package		100	450	μV
		$0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$	●		550	μV
		$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●		700	μV
		S8 Package		100	450	μV
		$0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$	●		750	μV
		$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●		900	μV
		MS8 Package		100	450	μV
		$0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$	●		850	μV
		$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●		1200	μV
		DD Package		125	650	μV
		$0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$	●		1050	μV
		$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●		1200	μV
	Input Offset Voltage Drift (Note 9)	N8 Package, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●	1	4	$\mu\text{V}/^{\circ}\text{C}$
		S8 Package, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●	2	8	$\mu\text{V}/^{\circ}\text{C}$
		MS8 Package, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●	2	10	$\mu\text{V}/^{\circ}\text{C}$
		DD Package, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●	2	10	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		●	0.2	1.0	nA
I_B	Input Bias Current		●	4	10	nA
	Input Noise Voltage	0.1Hz to 10Hz		1		μV_{p-p}
e_n	Input Noise Voltage Density	$f = 1\text{kHz}$		52		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 1\text{kHz}$		0.035		$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	Differential	5.2	13		$\text{M}\Omega$
		Common Mode, $V_{CM} = -15\text{V to } 14\text{V}$		12000		$\text{M}\Omega$
C_{IN}	Input Capacitance			4		pF
	Input Voltage Range		●	-15	29	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -15\text{V to } 29\text{V}$	●	86	103	dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 14\text{V}, R_L = 10\text{k}$		100	500	V/mV
		$0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$	●	75		V/mV
		$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●	50		V/mV
V_{OL}	Output Voltage Swing LOW	No Load	●	-14.997	-14.95	V
		$I_{SINK} = 5\text{mA}$	●	-14.500	-14.07	V
		$I_{SINK} = 10\text{mA}$	●	-14.125	-13.35	V
V_{OH}	Output Voltage Swing HIGH	No Load	●	14.9	14.975	V
		$I_{SOURCE} = 5\text{mA}$	●	14.5	14.750	V
		$I_{SOURCE} = 10\text{mA}$	●	14.3	14.650	V

±15V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range of $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, $V_{OUT} = 0\text{V}$, $V_{SHDN} = V^-$ unless otherwise specified. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LT1636C/LT1636I			UNITS	
			MIN	TYP	MAX		
I_{SC}	Short-Circuit Current (Note 2)	Short to GND $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●	±18	±30	mA	
			●	±15		mA	
			●	±10		mA	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.35\text{V to } \pm 22\text{V}$	●	90	114	dB	
I_S	Supply Current		●		50	70	μA
			●			85	μA
I_{SHDN}	Shutdown Pin Current	$V_{PIN5} = -20\text{V}$, $V_S = \pm 22\text{V}$, No Load $V_{PIN5} = -20\text{V}$, $V_S = \pm 22\text{V}$, No Load	●		12	30	μA
			●		0.7	15	nA
I_{SHDN}	Maximum Shutdown Pin Current	$V_{PIN5} = 32\text{V}$, $V_S = \pm 22\text{V}$	●		1.2	8	μA
			●		27	150	μA
GBW	Gain Bandwidth Product	$f = 1\text{kHz}$ $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●	125	220	kHz	
			●	110		kHz	
SR	Slew Rate	$A_V = -1$, $R_L = \infty$, $V_O = \pm 10\text{V}$ Measured at $\pm 5\text{V}$ $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	●	100		kHz	
			●	0.0375	0.075	V/μs	
			●	0.033		V/μs	
			●	0.030		V/μs	

3V AND 5V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range of $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$. $V_S = 3\text{V}$, 0V ; $V_S = 5\text{V}$, 0V ; $V_{CM} = V_{OUT} = \text{half supply}$ unless otherwise specified. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LT1636H			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	50	325	μV
			●		3	mV
	Input Offset Voltage Drift (Note 9)		●	3	10	μV/°C
I_{OS}	Input Offset Current	$V_{CM} = 44\text{V}$ (Note 5)	●		3	nA
			●		1	μA
I_B	Input Bias Current	$V_{CM} = 44\text{V}$ (Note 5)	●		30	nA
			●		10	μA
	Input Voltage Range		●	0.3	44	V
CMRR	Common Mode Rejection Ratio (Note 5)	$V_{CM} = 0.3\text{V to } V_{CC} - 1\text{V}$ $V_{CM} = 0.3\text{V to } 44\text{V}$	●	72		dB
			●	74		dB
A_{VOL}	Large-Signal Voltage Gain	$V_S = 3\text{V}$, $V_O = 500\text{mV to } 2.5\text{V}$, $R_L = 10\text{k}$	●	200	1300	V/mV
		$V_S = 5\text{V}$, $V_O = 500\text{mV to } 4.5\text{V}$, $R_L = 10\text{k}$	●	20		V/mV
V_{OL}	Output Voltage Swing LOW	No Load $I_{SINK} = 2.5\text{mA}$	●		15	mV
			●		875	mV
V_{OH}	Output Voltage Swing HIGH	$V_S = 3\text{V}$, No Load $V_S = 3\text{V}$, $I_{SOURCE} = 5\text{mA}$	●	2.925		V
			●	2.35		V
			●	4.925		V
			●	4.10		V
PSRR	Power Supply Rejection Ratio	$V_S = 2.7\text{V to } 12.5\text{V}$, $V_{CM} = V_O = 1\text{V}$	●	80		dB
	Minimum Supply Voltage		●	2.7		V

3V AND 5V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range of $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$.
 $V_S = 3\text{V}, 0\text{V}; V_S = 5\text{V}, 0\text{V}; V_{\text{CM}} = V_{\text{OUT}} = \text{half supply unless otherwise specified. (Note 4)}$

SYMBOL	PARAMETER	CONDITIONS	LT1636H			UNITS
			MIN	TYP	MAX	
I_S	Reverse Supply Voltage	$I_S = -100\mu\text{A}$	●	25		V
	Supply Current	(Note 6)	●	42	55 75	μA μA
I_{SD}	Supply Current, SHDN	$V_{\text{PIN5}} = 2\text{V}$, No Load (Note 6)	●		15	μA
	Shutdown Pin Current	$V_{\text{PIN5}} = 0.3\text{V}$, No Load (Note 6)	●		200	nA
		$V_{\text{PIN5}} = 2\text{V}$, No Load (Note 5)	●		7	μA
	Output Leakage Current, SHDN	$V_{\text{PIN5}} = 2\text{V}$, No Load (Note 6)	●		5	μA
GBW	Maximum Shutdown Pin Current	$V_{\text{PIN5}} = 32\text{V}$, No Load (Note 5)	●		200	μA
	Gain Bandwidth Product	$f = 1\text{kHz}$ (Note 5)	●	110 60	200	kHz kHz
SR	Slew Rate	$A_V = -1, R_L = \infty$ (Note 7)	●	0.035 0.015	0.07	$\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$

$\pm 15\text{V}$ ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range of $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$.
 $V_S = \pm 15\text{V}, V_{\text{CM}} = 0\text{V}, V_{\text{OUT}} = 0\text{V}, V_{\text{SHDN}} = V^-$ unless otherwise specified. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LT1636H			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	100	550 3.4	μV mV
	Input Offset Voltage Drift (Note 9)		●	3	11	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		●		5	nA
I_B	Input Bias Current		●		50	nA
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = -14.7\text{V}$ to 29V	●	72		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 14\text{V}, R_L = 10\text{k}$	●	100 4	500	V/mV V/mV
	Output Voltage Swing	No Load $I_{\text{OUT}} = \pm 2.5\text{mA}$	● ●		± 14.8 ± 14.3	V V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.35\text{V}$ to $\pm 22\text{V}$	●	84		dB
	Minimum Supply Voltage		●	± 1.35		V
I_S	Supply Current		●	50	70 100	μA μA
	Positive Supply Current, SHDN	$V_{\text{PIN5}} = -20\text{V}, V_S = \pm 22\text{V}$, No Load	●		40	μA
I_{SHDN}	Shutdown Pin Current	$V_{\text{PIN5}} = -21.7\text{V}, V_S = \pm 22\text{V}$, No Load	●		200	nA
		$V_{\text{PIN5}} = -20\text{V}, V_S = \pm 22\text{V}$, No Load	●		10	μA
	Maximum Shutdown Pin Current	$V_{\text{PIN5}} = 32\text{V}, V_S = \pm 22\text{V}$	●		200	μA
V_L	Output Leakage Current, SHDN	$V_{\text{PIN5}} = -20\text{V}, V_S = \pm 22\text{V}$, No Load	●		100	μA
	Shutdown Pin Input Low Voltage	$V_S = \pm 22\text{V}$	●		-21.7	V
V_H	Shutdown Pin Input High Voltage	$V_S = \pm 22\text{V}$	●	-20		V
GBW	Gain Bandwidth Product	$f = 1\text{kHz}$	●	125 75	220	kHz kHz
	Slew Rate	$A_V = -1, R_L = \infty, V_O = \pm 10\text{V}$ Measured at $V_O = \pm 5\text{V}$	●	0.0375 0.02	0.075	$\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: A heat sink may be required to keep the junction temperature below absolute maximum. The θ_{JA} specified for the DD package is with minimal PCB heat spreading metal. A significant reduction in θ_{JA} can be obtained with expanded PCB metal area on all layers of a board.

Note 3: The LT1636C and LT1636I are guaranteed functional over the operating temperature range of -40°C to 85°C . The LT1636H is guaranteed functional over the operating temperature range of -40°C to 125°C .

Note 4: The LT1636C is guaranteed to meet specified performance from 0°C to 70°C . The LT1636C is designed, characterized and expected to meet specified performance from -40°C to 85°C but is not tested or QA

sampled at these temperatures. The LT1636I is guaranteed to meet specified performance from -40°C to 85°C . The LT1636H is guaranteed to meet specified performance from -40°C to 125°C .

Note 5: $V_S = 5\text{V}$ limits are guaranteed by correlation to $V_S = 3\text{V}$ and $V_S = \pm 15\text{V}$ or $V_S = \pm 22\text{V}$ tests.

Note 6: $V_S = 3\text{V}$ limits are guaranteed by correlation to $V_S = 5\text{V}$ and $V_S = \pm 15\text{V}$ or $V_S = \pm 22\text{V}$ tests.

Note 7: Guaranteed by correlation to slew rate at $V_S = \pm 15\text{V}$ and GBW at $V_S = 3\text{V}$ and $V_S = \pm 15\text{V}$ tests.

Note 8: This specification implies a typical input offset voltage of $600\mu\text{V}$ at $V_{CM} = 44\text{V}$ and a maximum input offset voltage of 3mV at $V_{CM} = 44\text{V}$.

Note 9: This parameter is not 100% tested.

TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



1636 G01

Minimum Supply Voltage



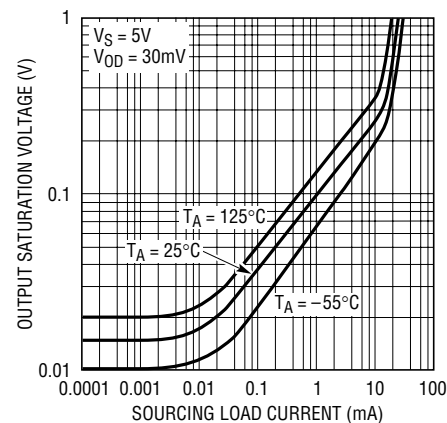
1636 G02

Input Bias Current vs Common Mode Voltage



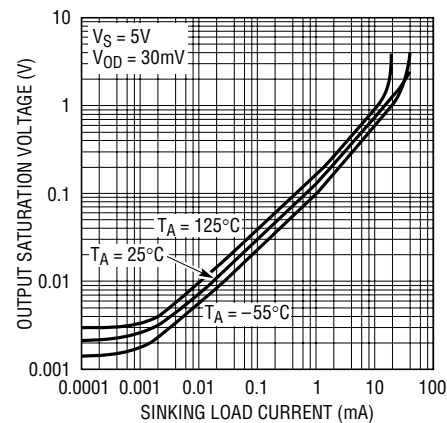
1636 G03

Output Saturation Voltage vs Load Current (Output High)



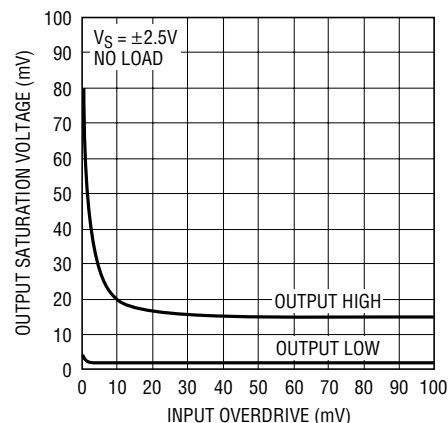
1636 G04

Output Saturation Voltage vs Load Current (Output Low)



1636 G05

Output Saturation Voltage vs Input Overdrive



1636 G06

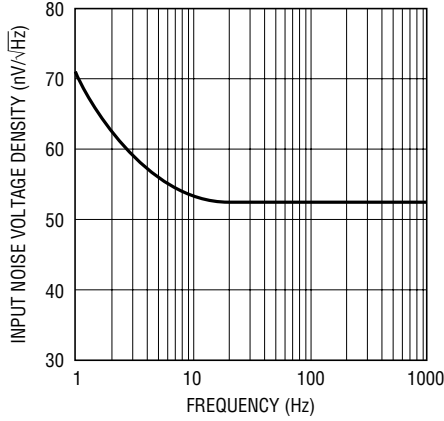
TYPICAL PERFORMANCE CHARACTERISTICS

0.1Hz to 10Hz Noise Voltage



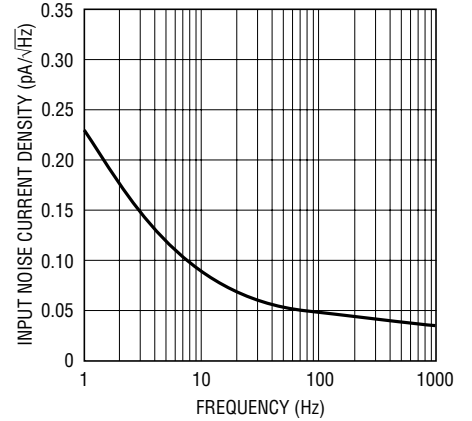
1636 G07

Noise Voltage Density vs Frequency



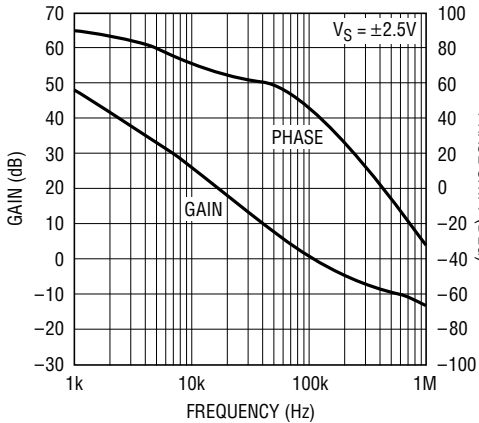
1636 G08

Input Noise Current vs Frequency



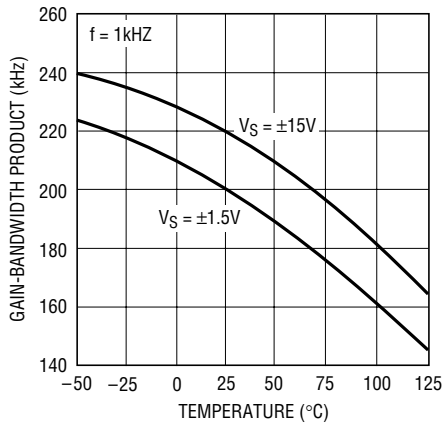
1636 G09

Open-Loop Gain and Phase Shift vs Frequency



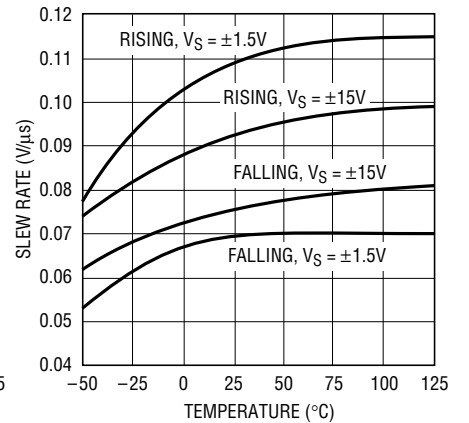
1636 G10

Gain-Bandwidth Product vs Temperature



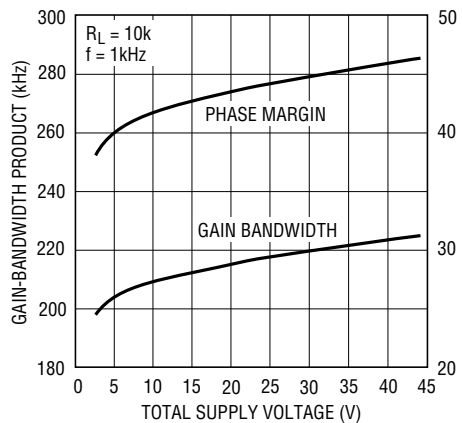
1636 G11

Slew Rate vs Temperature



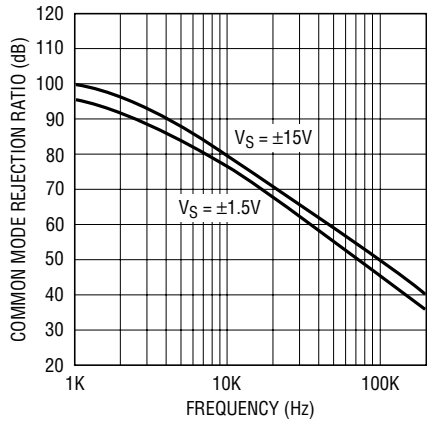
1636 G12

Gain-Bandwidth Product and Phase Margin vs Supply Voltage



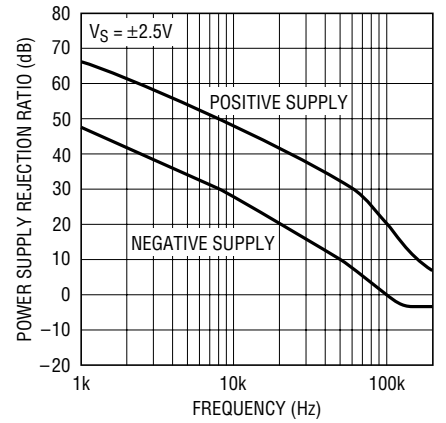
1636 G13

CMRR vs Frequency



1636 G14

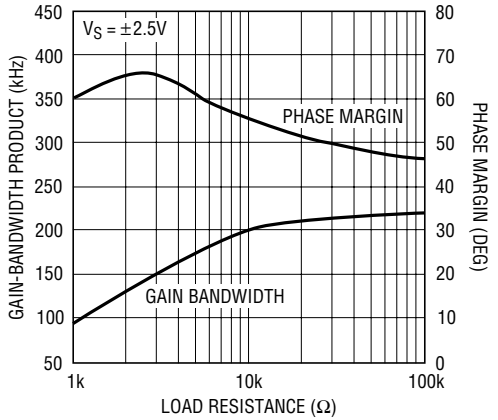
PSRR vs Frequency



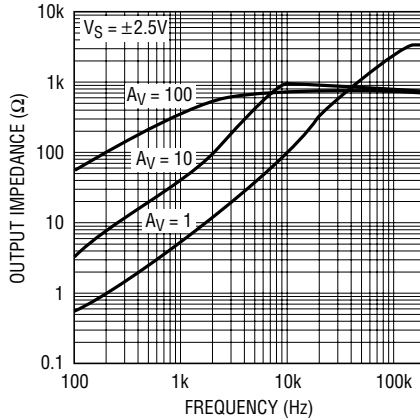
1636 G15

TYPICAL PERFORMANCE CHARACTERISTICS

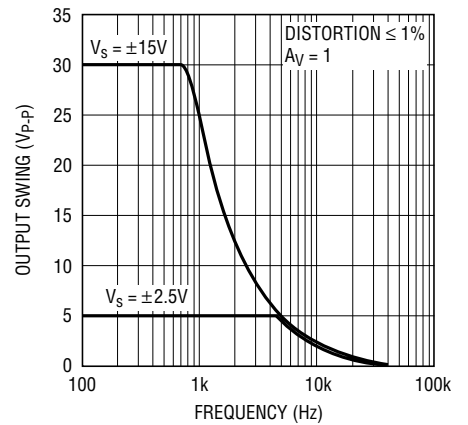
Gain-Bandwidth Product and Phase Margin vs Load Resistance



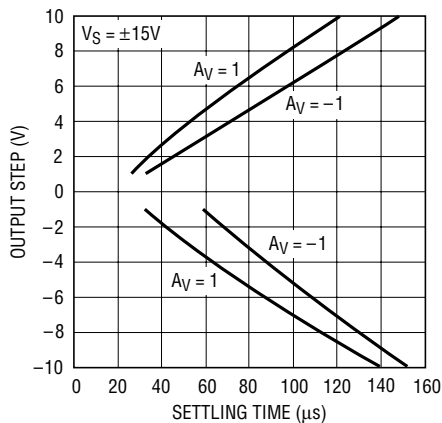
Output Impedance vs Frequency



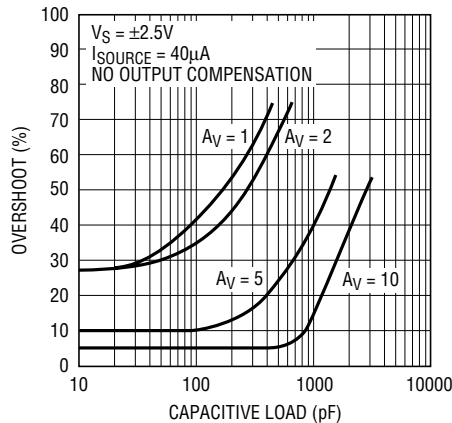
Undistorted Output Swing vs Frequency



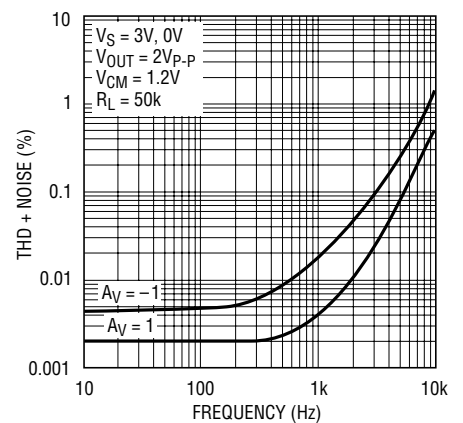
Settling Time to 0.1% vs Output Step



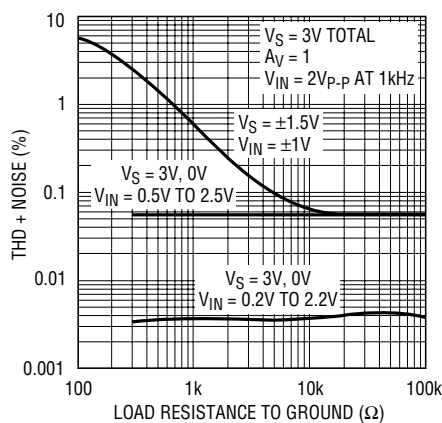
Capacitive Load Handling, Overshoot vs Capacitive Load



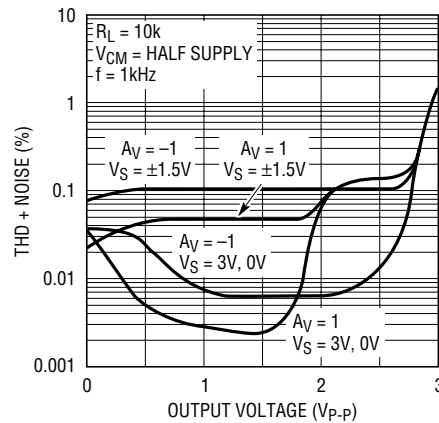
Total Harmonic Distortion + Noise vs Frequency



Total Harmonic Distortion + Noise vs Load Resistance

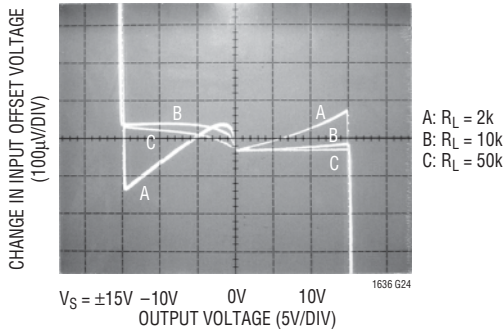


Total Harmonic Distortion + Noise vs Output Voltage

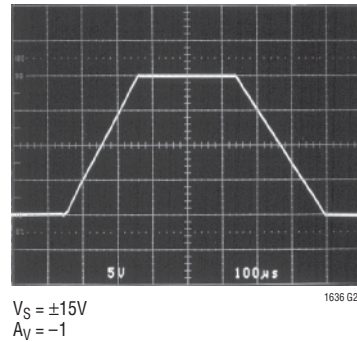


TYPICAL PERFORMANCE CHARACTERISTICS

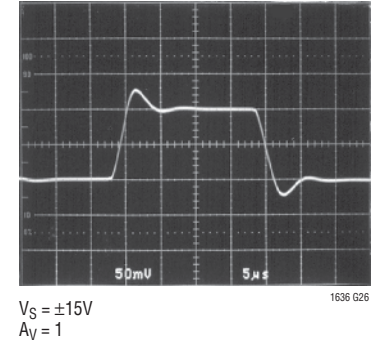
Open-Loop Gain



Large-Signal Response



Small-Signal Response



APPLICATIONS INFORMATION

Supply Voltage

The positive supply pin of the LT1636 should be bypassed with a small capacitor (about $0.01\mu F$) within an inch of the pin. When driving heavy loads an additional $4.7\mu F$ electrolytic capacitor should be used. When using split supplies, the same is true for the negative supply pin.

The LT1636 is protected against reverse battery voltages up to 27V. In the event a reverse battery condition occurs, the supply current is less than 1nA.

When operating the LT1636 on total supplies of 20V or more, the supply must not be brought up faster than $1\mu s$. This is especially true if low ESR bypass capacitors are used. A series RLC circuit is formed from the supply lead inductance and the bypass capacitor. 5Ω of resistance in the supply or the bypass capacitor will dampen the tuned circuit enough to limit the rise time.

Inputs

The LT1636 has two input stages, NPN and PNP (see Simplified Schematic), resulting in three distinct operating regions as shown in the Input Bias Current vs Common Mode typical performance curve.

For input voltages about 0.8V or more below V^+ , the PNP input stage is active and the input bias current is typically $-4nA$. When the input voltage is about 0.5V or less from V^+ , the NPN input stage is operating and the input bias current is typically 10nA. Increases in temperature will

cause the voltage at which operation switches from the PNP stage to the NPN stage to move towards V^+ . The input offset voltage of the NPN stage is untrimmed and is typically $600\mu V$.

A Schottky diode in the collector of each NPN transistor of the NPN input stage allows the LT1636 to operate with either or both of its inputs above V^+ . At about 0.3V above V^+ the NPN input transistor is fully saturated and the input bias current is typically $3\mu A$ at room temperature. The input offset voltage is typically $600\mu V$ when operating above V^+ . The LT1636 will operate with its input 44V above V^- regardless of V^+ .

The inputs are protected against excursions as much as 22V below V^- by an internal 1k resistor in series with each input and a diode from the input to the negative supply. There is no output phase reversal for inputs up to 5V below V^- . There are no clamping diodes between the inputs and the maximum differential input voltage is 44V.

Output

The output voltage swing of the LT1636 is affected by input overdrive as shown in the typical performance curves. When monitoring voltages within 100mV of V^+ , gain should be taken to keep the output from clipping.

The output of the LT1636 can be pulled up to 27V beyond V^+ with less than 1nA of leakage current, provided that V^+ is less than 0.5V.

APPLICATIONS INFORMATION

The normally reverse biased substrate diode from the output to V^- will cause unlimited currents to flow when the output is forced below V^- . If the current is transient and limited to 100mA, no damage will occur.

The LT1636 is internally compensated to drive at least 200pF of capacitance under any output loading conditions. A 0.22 μ F capacitor in series with a 150 Ω resistor between the output and ground will compensate these amplifiers for larger capacitive loads, up to 10,000pF, at all output currents.

Distortion

There are two main contributors of distortion in op amps: output crossover distortion as the output transitions from sourcing to sinking current and distortion caused by nonlinear common mode rejection. Of course, if the op amp is operating inverting there is no common mode induced distortion. When the LT1636 switches between input stages there is significant nonlinearity in the CMRR. Lower load resistance increases the output crossover distortion, but has no effect on the input stage transition distortion. For lowest distortion the LT1636 should be operated single supply, with the output always sourcing current and with the input voltage swing between ground and ($V^+ - 0.8V$). See the Typical Performance Characteristics curves.

Gain

The open-loop gain is less sensitive to load resistance when the output is sourcing current. This optimizes performance in single supply applications where the load is

returned to ground. The typical performance photo of Open-Loop Gain for various loads shows the details.

Shutdown

The LT1636 can be shut down two ways: using the shutdown pin or bringing V^+ to within 0.5V of V^- . When V^+ is brought to within 0.5V of V^- both the supply current and output leakage current drop to less than 1nA. When the shutdown pin is brought 1.2V above V^- , the supply current drops to about 4 μ A and the output leakage current is less than 1 μ A, independent of V^+ . In either case the input bias current is less than 0.1nA (even if the inputs are 44V above the negative supply).

The shutdown pin can be taken up to 32V above V^- . The shutdown pin can be driven below V^- , however the pin current through the substrate diode should be limited with an external resistor to less than 10mA.

Input Offset Nulling

The input offset voltage can be nulled by placing a 10k potentiometer between Pins 1 and 8 with its wiper to V^- (see Figure 1). The null range will be at least $\pm 1mV$.



Figure 1. Input Offset Nulling

TYPICAL APPLICATIONS

MUX Amplifier



MUX Amplifier Waveforms



$V_S = 5V$
 $V_{IN1} = 1.2kHz$ AT $4V_{p-p}$, $V_{IN2} = 2.4kHz$ AT $2V_{p-p}$
 INPUT SELECT = $120Hz$ AT $5V_{p-p}$

Optional Output Compensation for Capacitive Loads Greater Than 200pF



SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
 (Reference LTC DWG # 05-08-1698)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. EXPOSED PAD SHALL BE SOLDER PLATED

MS8 Package
8-Lead Plastic MSOP
 (Reference LTC DWG # 05-08-1660)



NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

N8 Package 8-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)