

## FEATURES

- Allows Safe Board Insertion and Removal from a Live  $-48\text{V}$  Backplane
- Operates from  $-10\text{V}$  to  $-80\text{V}$
- Programmable Inrush Current
- Allows  $50\text{mA}$  of Reverse Drain Pin Current
- Programmable Electronic Circuit Breaker
- Programmable Overvoltage Protection
- Programmable Undervoltage Lockout
- Power Good Control Output

## APPLICATIONS

- Central Office Switching
- $-48\text{V}$  Distributed Power Systems
- Negative Power Supply Control

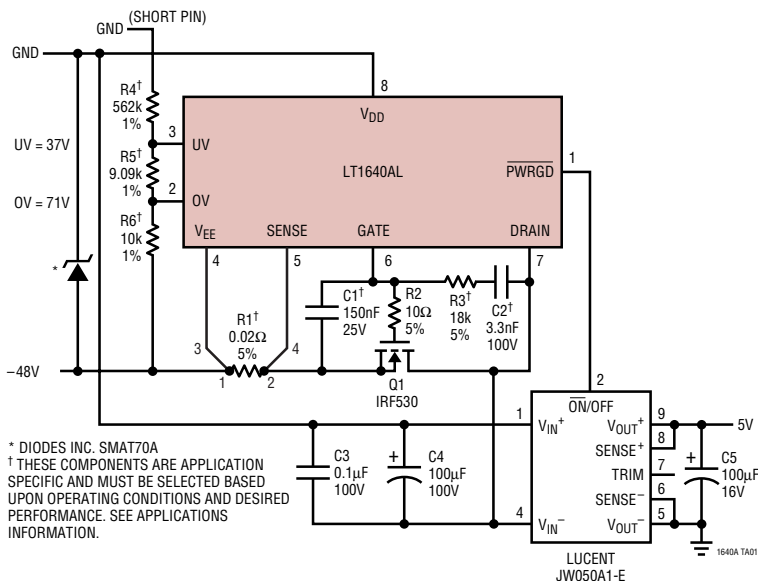
## DESCRIPTION

The LT<sup>®</sup>1640AL/LT1640AH are 8-pin, negative voltage Hot Swap<sup>™</sup> controllers that allow a board to be safely inserted and removed from a live backplane. Inrush current is limited to a programmable value by controlling the gate voltage of an external N-channel pass transistor. The pass transistor is turned off if the input voltage is less than the programmable undervoltage threshold or greater than the overvoltage threshold. A programmable electronic circuit breaker protects the system against shorts. The PWRGD (LT1640AL) or PWRGD (LT1640AH) signal can be used to directly enable a power module. The LT1640AL is designed for modules with a low enable input and the LT1640AH for modules with a high enable input.

The LT1640AL/LT1640AH are available in 8-pin PDIP and SO packages.

LT, LTC and LT are registered trademarks of Linear Technology Corporation. Hot Swap is a trademark of Linear Technology Corporation.

## TYPICAL APPLICATION



### Input Inrush Current



# LT1640AL/LT1640AH

## ABSOLUTE MAXIMUM RATINGS (Note 1), All Voltages Referred to V<sub>EE</sub>

Supply Voltage (V <sub>DD</sub> – V <sub>EE</sub> ) .....	–0.3V to 100V	Operating Temperature Range	
PWRGD, PWRGD Pins .....	–0.3V to 100V	LT1640ALC/LT1640AHC .....	0°C to 70°C
DRAIN Pin .....	–2V to 100V	LT1640ALI/LT1640AHI .....	–40°C to 85°C
SENSE, GATE Pins .....	–0.3V to 20V	Storage Temperature Range .....	–65°C to 150°C
UV, OV Pins .....	–0.3V to 60V	Lead Temperature (Soldering, 10 sec) .....	300°C
Maximum Junction Temperature .....	125°C		

## PACKAGE/ORDER INFORMATION

TOP VIEW	ORDER PART NUMBER	TOP VIEW	ORDER PART NUMBER
<p>N8 PACKAGE 8-LEAD PDIP</p> <p>S8 PACKAGE 8-LEAD PLASTIC SO</p> <p>T<sub>JMAX</sub> = 125°C, θ<sub>JA</sub> = 120°C/W (N8) T<sub>JMAX</sub> = 125°C, θ<sub>JA</sub> = 150°C/W (S8)</p>	LT1640ALCN8 LT1640ALCS8 LT1640ALIN8 LT1640ALIS8	<p>N8 PACKAGE 8-LEAD PDIP</p> <p>S8 PACKAGE 8-LEAD PLASTIC SO</p> <p>T<sub>JMAX</sub> = 125°C, θ<sub>JA</sub> = 120°C/W (N8) T<sub>JMAX</sub> = 125°C, θ<sub>JA</sub> = 150°C/W (S8)</p>	LT1640AHCN8 LT1640AHCS8 LT1640AHIN8 LT1640AHIS8
S8 PART MARKING		S8 PART MARKING	
1640AL 640ALI		1640AH 640AHI	

Consult factory for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T<sub>A</sub> = 25°C. (Note 2), V<sub>DD</sub> = 48V, V<sub>EE</sub> = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>DC</b>							
V <sub>DD</sub>	Supply Operating Range		●	10	80	V	
I <sub>DD</sub>	Supply Current	UV = 3V, OV = V <sub>EE</sub> , SENSE = V <sub>EE</sub>	●	1.3	5	mA	
V <sub>CB</sub>	Circuit Breaker Trip Voltage	V <sub>CB</sub> = (V <sub>SENSE</sub> – V <sub>EE</sub> )	●	40	50	60	mV
I <sub>PU</sub>	GATE Pin Pull-Up Current	Gate Drive On, V <sub>GATE</sub> = V <sub>EE</sub>	●	–30	–45	–60	μA
I <sub>PD</sub>	GATE Pin Pull-Down Current	Any Fault Condition		24	50	70	mA
I <sub>SENSE</sub>	SENSE Pin Current	V <sub>SENSE</sub> = 50mV		–20		μA	
ΔV <sub>GATE</sub>	External Gate Drive	(V <sub>GATE</sub> – V <sub>EE</sub> ), 15V ≤ V <sub>DD</sub> ≤ 80V	●	10	13.5	18	V
		(V <sub>GATE</sub> – V <sub>EE</sub> ), 10V ≤ V <sub>DD</sub> < 15V	●	6	8	15	V
V <sub>UVH</sub>	UV Pin High Threshold Voltage	UV Low to High Transition	●	1.213	1.243	1.272	V
V <sub>UVL</sub>	UV Pin Low Threshold Voltage	UV High to Low Transition	●	1.198	1.223	1.247	V
V <sub>UVHY</sub>	UV Pin Hysteresis			20		mV	
I <sub>INUV</sub>	UV Pin Input Current	V <sub>UV</sub> = V <sub>EE</sub>	●	–0.02	–0.5	μA	
V <sub>OVH</sub>	OV Pin High Threshold Voltage	OV Low to High Transition	●	1.198	1.223	1.247	V
V <sub>OVL</sub>	OV Pin Low Threshold Voltage	OV High to Low Transition	●	1.165	1.203	1.232	V
V <sub>OVHY</sub>	OV Pin Hysteresis			20		mV	
I <sub>INOV</sub>	OV Pin Input Current	V <sub>OV</sub> = V <sub>EE</sub>	●	–0.03	–0.5	μA	

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 2),  $V_{DD} = 48\text{V}$ ,  $V_{EE} = 0\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{PG}$	Power Good Threshold	$V_{DRAIN} - V_{EE}$ , High to Low Transition	1.1	1.4	2.0	V
$V_{PGHY}$	Power Good Threshold Hysteresis			0.4		V
$I_{DRAIN}$	Drain Input Bias Current	$V_{DRAIN} = 48\text{V}$	● 10	50	500	$\mu\text{A}$
$V_{OL}$	PWRGD Output Low Voltage	PWRGD (LT1640AL), ( $V_{DRAIN} - V_{EE}$ ) < $V_{PG}$ $I_{OUT} = 1\text{mA}$ $I_{OUT} = 5\text{mA}$	●	0.48 1.50	0.8 3.0	V V
	PWRGD Output Low Voltage (PWRGD – DRAIN)	PWRGD (LT1640AH), $V_{DRAIN} = 5\text{V}$ $I_{OUT} = 1\text{mA}$	●	0.75	1.0	V
$I_{OH}$	Output Leakage	PWRGD (LT1640AL), $V_{DRAIN} = 48\text{V}$ , $V_{PWRGD} = 80\text{V}$	●	0.05	10	$\mu\text{A}$
$R_{OUT}$	Power Good Output Impedance (PWRGD to DRAIN)	PWRGD (LT1640AH), ( $V_{DRAIN} - V_{EE}$ ) < $V_{PG}$	● 2	6.5		$\text{k}\Omega$

**AC**

$t_{PHLOV}$	OV High to GATE Low	Figures 1, 2		1.7		$\mu\text{s}$
$t_{PHLUV}$	UV Low to GATE Low	Figures 1, 3		1.5		$\mu\text{s}$
$t_{PLHOV}$	OV Low to GATE High	Figures 1, 2		5.5		$\mu\text{s}$
$t_{PLHUV}$	UV High to GATE High	Figures 1, 3		6.5		$\mu\text{s}$
$t_{PHLSENSE}$	SENSE High to Gate Low	Figures 1, 4	2	3	4	$\mu\text{s}$
$t_{PHLPG}$	DRAIN Low to PWRGD Low	(LT1640AL) Figures 1, 5		0.5		$\mu\text{s}$
	DRAIN Low to (PWRGD – DRAIN) High	(LT1640AH) Figures 1, 5		0.5		$\mu\text{s}$
$t_{PLHPG}$	DRAIN High to PWRGD High	(LT1640AL) Figures 1, 5		0.5		$\mu\text{s}$
	DRAIN High to (PWRGD – DRAIN) Low	(LT1640AH) Figures 1, 5		0.5		$\mu\text{s}$

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to  $V_{EE}$  unless otherwise specified.

**TYPICAL PERFORMANCE CHARACTERISTICS**

Supply Current vs Supply Voltage



1640A G01

Supply Current vs Temperature



1640A G02

Gate Voltage vs Supply Voltage



1640A G03

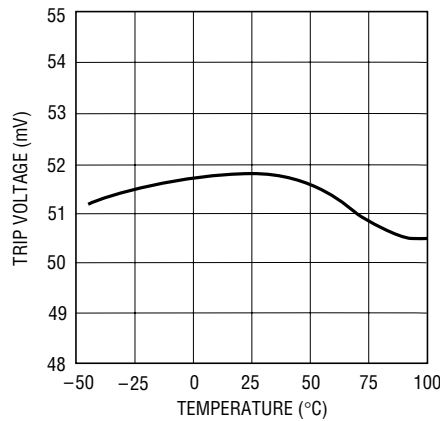
## TYPICAL PERFORMANCE CHARACTERISTICS

Gate Voltage vs Temperature



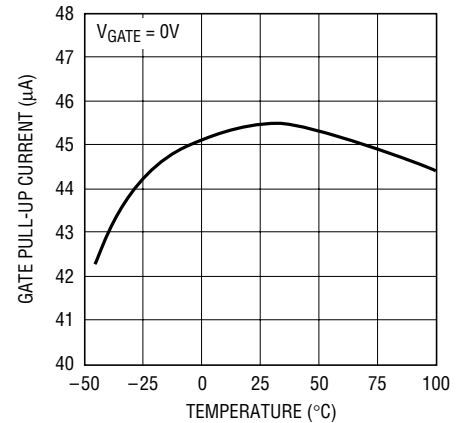
1640A G04

Circuit Breaker Trip Voltage vs Temperature



1640A G05

Gate Pull-Up Current vs Temperature



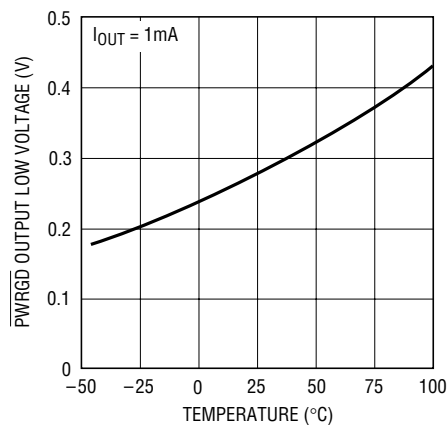
1640A G06

Gate Pull-Down Current vs Temperature



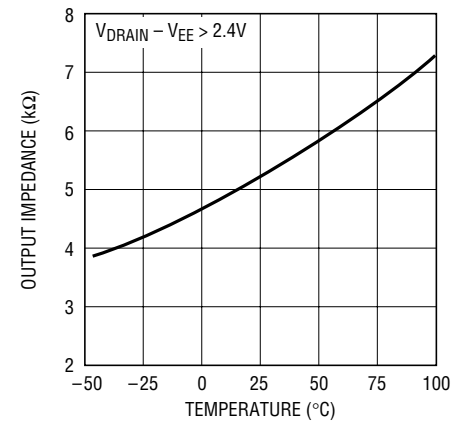
1640A G07

PWRGD Output Low Voltage vs Temperature (LT1640AL)



1640A G08

PWRGD Output Impedance vs Temperature (LT1640AH)



1640A G09

## PIN FUNCTIONS

**PWRGD/PWRGD (Pin 1):** Power Good Output Pin. This pin will toggle when  $V_{DRAIN}$  is within  $V_{PG}$  of  $V_{EE}$ . This pin can be connected directly to the enable pin of a power module.

When the DRAIN pin of the LT1640AL is above  $V_{EE}$  by more than  $V_{PG}$ , the PWRGD pin will be high impedance, allowing the pull-up current of the module's enable pin to pull the pin high and turn the module off. When  $V_{DRAIN}$  drops below  $V_{PG}$ , the PWRGD pin sinks current to  $V_{EE}$ , pulling the enable pin low and turning on the module.

When the DRAIN pin of the LT1640AH is above  $V_{EE}$  by more than  $V_{PG}$ , the PWRGD pin will sink current to the DRAIN pin which pulls the module's enable pin low, forcing it off. When  $V_{DRAIN}$  drops below  $V_{PG}$ , the PWRGD sink current is turned off and a 6.5k resistor is connected between PWRGD and DRAIN, allowing the module's pull-up current to pull the enable pin high and turn on the module.

## PIN FUNCTIONS

**OV (Pin 2):** Analog Overvoltage Input. When OV is pulled above the 1.223V low-to-high threshold, an overvoltage condition is detected and the GATE pin will be immediately pulled low. The GATE pin will remain low until OV drops below the 1.203V high-to-low threshold.

**UV (Pin 3):** Analog Undervoltage Input. When UV is pulled below the 1.223V high to low threshold, an undervoltage condition is detected and the GATE pin will be immediately pulled low. The GATE pin will remain low until UV rises above the 1.243 low-to-high threshold.

The UV pin is also used to reset the electronic circuit breaker. If the UV pin is cycled low and high following the trip of the circuit breaker, the circuit breaker is reset and a normal power-up sequence will occur.

**V<sub>EE</sub> (Pin 4):** Negative Supply Voltage Input. Connect to the lower potential of the power supply.

**SENSE (Pin 5):** Circuit Breaker Sense Pin. With a sense resistor placed in the supply path between V<sub>EE</sub> and SENSE, the circuit breaker will trip when the voltage across the resistor exceeds 50mV. Noise spikes of less than 2μs are filtered out and will not trip the circuit breaker.

If the circuit breaker trip current is set to twice the normal operating current, only 25mV is dropped across the sense resistor during normal operation. To disable the circuit breaker, V<sub>EE</sub> and SENSE can be shorted together.

**GATE (Pin 6):** Gate Drive Output for the External N-Channel. The GATE pin will go high when the following start-up conditions are met: the UV pin is high, the OV pin is low and  $(V_{SENSE} - V_{EE}) < 50mV$ . The GATE pin is pulled high by a 45μA current source and pulled low with a 50mA current source.

**DRAIN (Pin 7):** Analog Drain Sense Input. Connect this pin to the drain of the external N-channel and the V<sup>-</sup> pin of the power module. When the DRAIN pin is below V<sub>PG</sub>, the PWRGD or PWRGD pin will toggle. In some conditions, the DRAIN pin is pulled below V<sub>EE</sub>. The part is not damaged if the reverse DRAIN pin current is limited to 50mA.

**V<sub>DD</sub> (Pin 8):** Positive Supply Voltage Input. Connect this pin to the higher potential of the power supply inputs and the V<sup>+</sup> pin of the power module. The input supply voltage ranges from 10V to 80V.

## BLOCK DIAGRAM



## TEST CIRCUIT



Figure 1. Test Circuit

## TIMING DIAGRAMS



Figure 2. OV to GATE Timing



Figure 3. UV to GATE Timing



Figure 4. SENSE to GATE Timing



Figure 5. DRAIN to PWRGD/PWRGD Timing

## APPLICATIONS INFORMATION

### Hot Circuit Insertion

When circuit boards are inserted into a live –48V backplane, the bypass capacitors at the input of the board’s power module or switching power supply can draw huge transient currents as they charge up. The transient currents can cause permanent damage to the board’s components and cause glitches on the system power supply.

The LT1640A is designed to turn on a board’s supply voltage in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. The chip also provides undervoltage, overvoltage and overcurrent protection while keeping the power module off until its input voltage is stable and within tolerance.

### Power Supply Ramping

The input to the power module on a board is controlled by placing an external N-channel pass transistor (Q1) in the power path (Figure 6a, all waveforms are with respect to the V<sub>EE</sub> pin of the LT1640A). R1 provides current fault detection and R2 prevents high frequency oscillations. Resistors R4, R5 and R6 provide undervoltage and overvoltage sensing. By ramping the gate of Q1 up at a slow rate, the surge current charging load capacitors C3 and C4 can be limited to a safe value when the board makes connection.

Resistor R3 and capacitor C2 act as a feedback network to accurately control the inrush current. The inrush current can be calculated with the following equation:

$$I_{INRUSH} = (45\mu A \cdot C_L) / C2$$

where C<sub>L</sub> is the total load capacitance equal to C3 + C4 + module input capacitance.

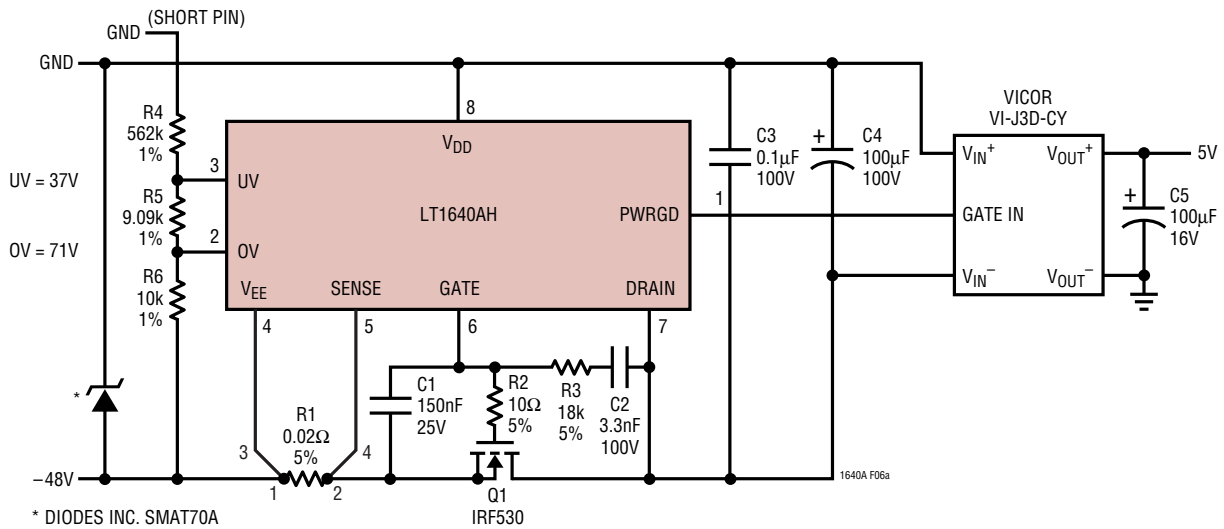


Figure 6a. Inrush Control Circuitry

## APPLICATIONS INFORMATION

Capacitor C1 and resistor R3 prevent Q1 from momentarily turning on when the power pins first make contact. Without C1 and R3, capacitor C2 would pull the gate of Q1 up to a voltage roughly equal to  $V_{EE} \cdot C2/C_{GS}(Q1)$  before the LT1640A could power up and actively pull the gate low. By placing capacitor C1 in parallel with the gate capacitance of Q1 and isolating them from C2 using resistor R3, the problem is solved. The value of C1 should be:

$$\left( \frac{V_{INMAX} - V_{TH}}{V_{TH}} \right) \cdot (C2 + C_{GD})$$

where  $V_{TH}$  is the MOSFET's minimum gate threshold and  $V_{INMAX}$  is the maximum operating input voltage.

R3's value is not critical and is given by  $(V_{INMAX} + \Delta V_{GATE}) / 5mA$ .

The waveforms are shown in Figure 6b. When the power pins make contact, they bounce several times. While the contacts are bouncing, the LT1640A senses an undervoltage condition and the GATE is immediately pulled low when the power pins are disconnected.

Once the power pins stop bouncing, the GATE pin starts to ramp up. When Q1 turns on, the GATE voltage is held constant by the feedback network of R3 and C2. When the DRAIN voltage has finished ramping, the GATE pin then ramps to its final value.



Figure 6b. Inrush Control Waveforms



## APPLICATIONS INFORMATION

### Electronic Circuit Breaker

The LT1640A features an electronic circuit breaker function that protects against short circuits or excessive supply currents. By placing a sense resistor between the  $V_{EE}$  and SENSE pin, the circuit breaker will be tripped whenever the voltage across the sense resistor is greater than 50mV for more than  $3\mu\text{s}$  as shown in Figure 7.

Note that the circuit breaker threshold should be set sufficiently high to account for the sum of the load current and the inrush current. If the load current can be controlled by the  $\overline{\text{PWRGD}}$ /PWRGD pin (as in Figure 6a), the threshold can be set lower, since it will never need to accommodate inrush current and load current simultaneously.

When the circuit breaker trips, the GATE pin is immediately pulled to  $V_{EE}$  and the external N-channel turns off. The GATE pin will remain low until the circuit breaker is reset by pulling UV low, then high or cycling power to the part.

If more than  $3\mu\text{s}$  deglitching time is needed to reject current noise, an external resistor and capacitor can be added to the sense circuit as shown in Figure 8. R7 and C3 act as a lowpass filter that will slow down the SENSE pin voltage from rising too fast. Since the SENSE pin will source current, typically  $20\mu\text{A}$ , there will be a voltage drop

on R7. This voltage will be counted into the circuit breaker trip voltage just as the voltage across the sense resistor. A small resistor is recommended for R7. A  $100\Omega$  for R7 will cause a 2mV error. The following equation can be used to estimate the delay time at the SENSE pin:

$$t = -R \cdot C \cdot \ln \left( 1 - \frac{V(t) - V(t_0)}{V_i - V(t_0)} \right)$$

Where  $V(t)$  is the circuit breaker trip voltage, typically 50mV.  $V(t_0)$  is the voltage drop across the sense resistor before the short or overcurrent condition occurs.  $V_i$  is the voltage across the sense resistor when the short current or overcurrent is applied on it.

Example: A system has a 1A current load and a  $0.02\Omega$  sense resistor is used. An extended delay circuit needs to be designed for a  $50\mu\text{s}$  delay time after the load jumps to 5A. In this case:

$$V(t) = 50\text{mV}$$

$$V(t_0) = 20\text{mV}$$

$$V_i = 5\text{A} \cdot 0.02\Omega = 100\text{mV}$$

If we choose  $R = 100\Omega$ , we will get  $C = 1\mu\text{F}$ .



Figure 7. Short-Circuit Protection Waveforms

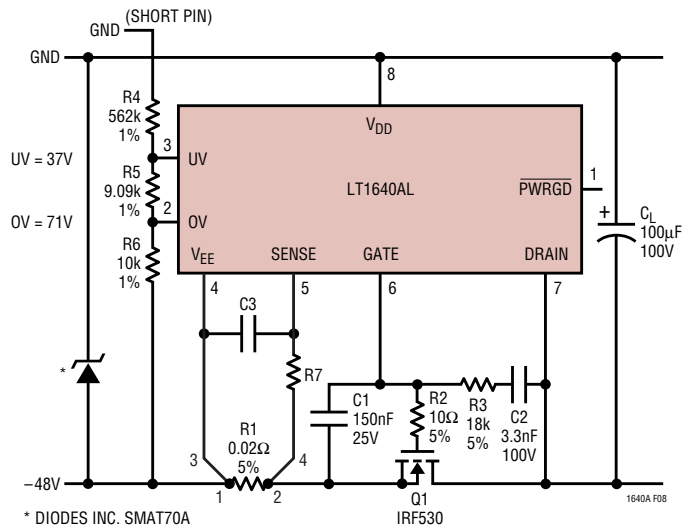


Figure 8. Extending the Short-Circuit Protection Delay

## APPLICATIONS INFORMATION

Under some conditions, a short circuit at the output can cause the input supply to dip below the UV threshold, resetting the circuit breaker immediately.

The LT1640A then cycles on and off repeatedly until the short is removed. This can be minimized by adding a deglitching delay to the UV pin with a capacitor from UV to  $V_{EE}$ . This capacitor forms an RC time constant with the resistors at UV, allowing the input supply to recover before the UV pin resets the circuit breaker.

A circuit that automatically resets the circuit breaker after a current fault is shown in Figure 9.

Transistors Q2 and Q3 along with R7, R8, C4 and D1 form a programmable one-shot circuit. Before a short occurs, the GATE pin is pulled high and Q3 is turned on, pulling node 2 to  $V_{EE}$ . Resistor R8 turns off Q2. When a short occurs, the GATE pin is pulled low and Q3 turns off. Node 2 starts to charge C4 and Q2 turns on, pulling the UV pin low and resetting the circuit breaker. As soon as C4 is fully charged, R8 turns off Q2, UV goes high and the GATE starts to ramp up. Q3 turns back on and quickly pulls node 2 back to  $V_{EE}$ . Diode D1 clamps node 3 one diode drop below  $V_{EE}$ . The duty cycle is set to 10% to prevent Q1 from overheating.



Figure 9. Automatic Restart After Current Fault

**APPLICATIONS INFORMATION**

**Undervoltage and Overvoltage Detection**

The UV (Pin 3) and OV (Pin 2) pins can be used to detect undervoltage and overvoltage conditions at the power supply input. The UV and OV pins are internally connected to analog comparators with 20mV of hysteresis. When the UV pin falls below its threshold or the OV pin rises above its threshold, the GATE pin is immediately pulled low. The GATE pin will be held low until UV is high and OV is low.

The undervoltage and overvoltage trip voltages can be programmed using a three resistor divider as shown in

Figure 10a. With R4 = 562k, R5 = 9.09k and R6 = 10k, the undervoltage threshold is set to 37V and the overvoltage threshold is set to 71V. The resistor divider will also amplify the 20mV hysteresis at the UV pin and OV pin to 0.6V and 1.2V at the input, respectively.

More hysteresis can be added to the UV threshold by connecting resistor R3 between the UV pin and the GATE pin as shown in Figure 10b.



Figure 10a. Undervoltage and Overvoltage Sensing



Figure 10b. Programmable Hysteresis for Undervoltage Detection

## APPLICATIONS INFORMATION

The new threshold voltage when the input moves from low to high is:

$$V_{UV,LH} = V_{UVH} \left( \frac{R2 \cdot R3 + R1 \cdot R3 + R1 \cdot R2}{R2 \cdot R3} \right)$$

where  $V_{UVH}$  is typically 1.243V.

The new threshold voltage when the input moves from high to low is:

$$V_{UV,HL} = V_{UVL} \left( \frac{R2 \cdot R3 + R1 \cdot R3 + R1 \cdot R2}{R2 \cdot R3} \right) - \left( V_{GATE} \cdot \frac{R1}{R3} \right)$$

where  $V_{UVL}$  is typically 1.223V.

The new hysteresis value will be:

$$V_{HYS} = V_{UVHY} \left( \frac{R2 \cdot R3 + R1 \cdot R3 + R1 \cdot R2}{R2 \cdot R3} \right) + \left( V_{GATE} \cdot \frac{R1}{R3} \right)$$

With  $R1 = 562k$ ,  $R2 = 16.9k$  and  $R3 = 1.62M$ ,  $V_{GATE} = 13.5V$  and  $V_{UVHY} = 20mV$ , the undervoltage threshold will be 43V (from low to high) and 37.6V (from high to low). The hysteresis is 5.4V. A separate resistor divider should be used to set the overvoltage threshold given by:

$$V_{OV} = V_{OVH} \left( \frac{R4 + R5}{R5} \right)$$

With  $R4 = 506k$ ,  $R5 = 8.87k$  and  $V_{OVH} = 1.223V$ , the overvoltage threshold will be 71V.

### $\overline{PWRGD}$ /PWRGD Output

The  $\overline{PWRGD}$ /PWRGD output can be used to directly enable a power module when the input voltage to the module is within tolerance. The LT1640AL has a  $\overline{PWRGD}$  output for modules with an active low enable input, and the LT1640AH has a PWRGD output for modules with an active high enable input.

When the DRAIN voltage of the LT1640AH is high with respect to  $V_{EE}$  (Figure 11), the internal transistor Q3 is turned off and R7 and Q2 clamp the PWRGD pin one diode drop ( $\approx 0.7V$ ) above the DRAIN pin. Transistor Q2 sinks the module's pull-up current and the module turns off.

When the DRAIN voltage drops below  $V_{PG}$ , Q3 will turn on, shorting the bottom of R7 to DRAIN and turning Q2 off. The pull-up current in the module then flows through R7, pulling the PWRGD pin high and enabling the module.

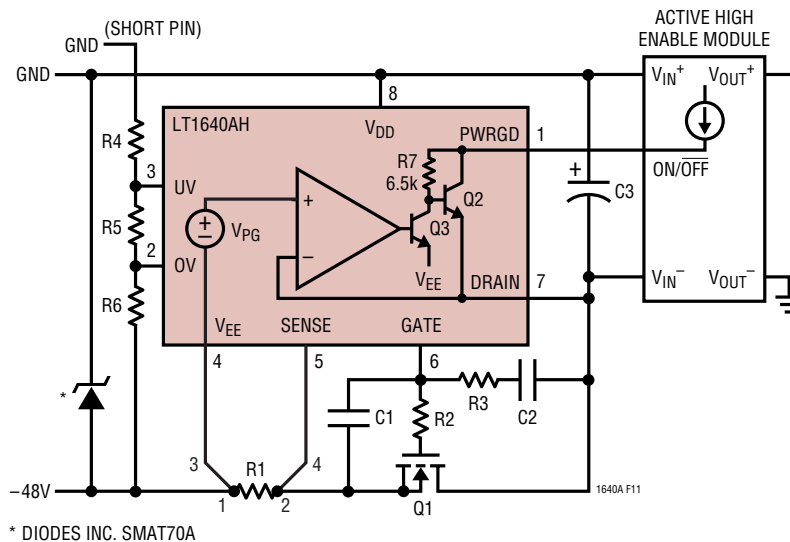


Figure 11. Active High Enable Module

## APPLICATIONS INFORMATION

When the DRAIN voltage of the LT1640AL is high with respect to  $V_{EE}$ , the internal pull-down transistor Q2 is off and the  $\overline{\text{PWRGD}}$  pin is in a high impedance state (Figure 12). The  $\overline{\text{PWRGD}}$  pin will be pulled high by the module's internal pull-up current source, turning the module off. When the DRAIN voltage drops below  $V_{PG}$ , Q2 will turn on and the  $\overline{\text{PWRGD}}$  pin will pull low, enabling the module.

The  $\overline{\text{PWRGD}}$  signal can also be used to turn on an LED or optoisolator to indicate that the power is good as shown in Figure 13.

### Gate Pin Voltage Regulation

When the supply voltage to the chip is more than 15.5V, the GATE pin voltage is regulated at 13.5V above  $V_{EE}$ . If the supply voltage is less than 15.5V, the GATE voltage will be about 2V below the supply voltage. At the minimum 10V supply voltage, the gate voltage is guaranteed to be greater

than 6V. The gate voltage will be no greater than 18V for supply voltages up to 80V.

### Drain Pin Protection

A unique feature of the LT1640A is the ruggedness of the DRAIN pin. The DRAIN is designed to withstand negative voltages (with respect to  $V_{EE}$ ) without requiring an external diode. A short circuit on the  $-48\text{V}$  backplane pulls up the  $V_{EE}$  pin, but due to the storage capacitor C3 (Figure 12), the DRAIN pin is held more negative than the  $V_{EE}$  pin. The body diode of Q1, plus the  $I \cdot R$  drop across R1 (if R1 is small), holds the DRAIN pin to less than 1.5V below  $V_{EE}$ . A 1.5V reverse voltage gives rise to a 50mA reverse drain current, which is within the design capability of the LT1640A. A design with R1 larger than  $0.1\Omega$  may require a resistor in series with the DRAIN pin to not exceed the 50mA drain current maximum.



Figure 12. Active Low Enable Module

**APPLICATIONS INFORMATION**

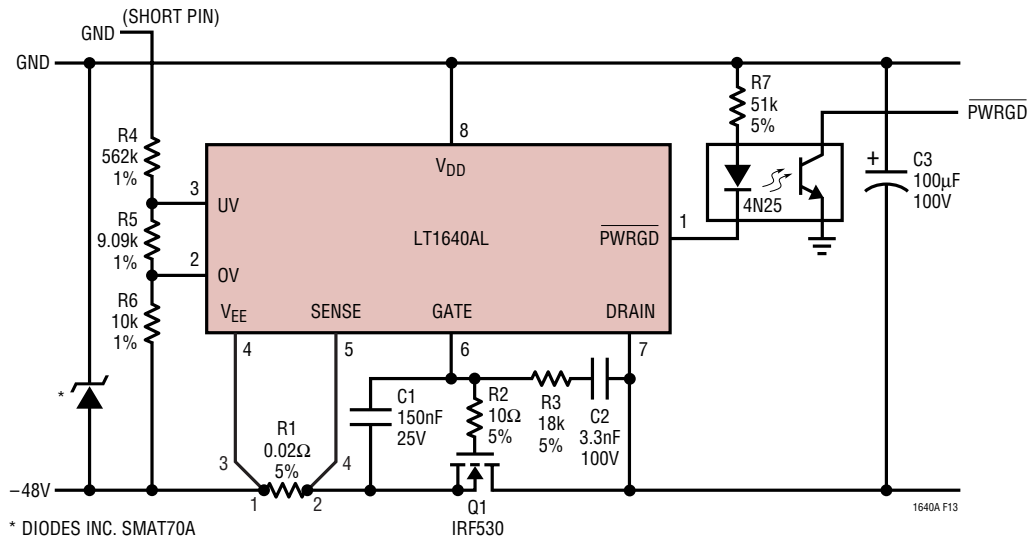
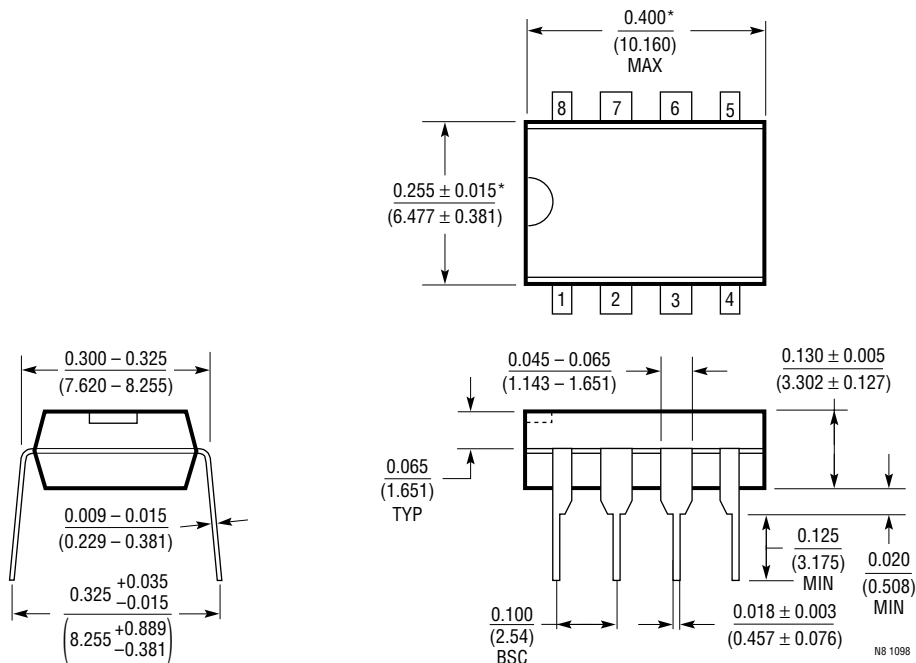


Figure 13. Using PWRGD to Drive an Optoisolator

**PACKAGE DESCRIPTION**

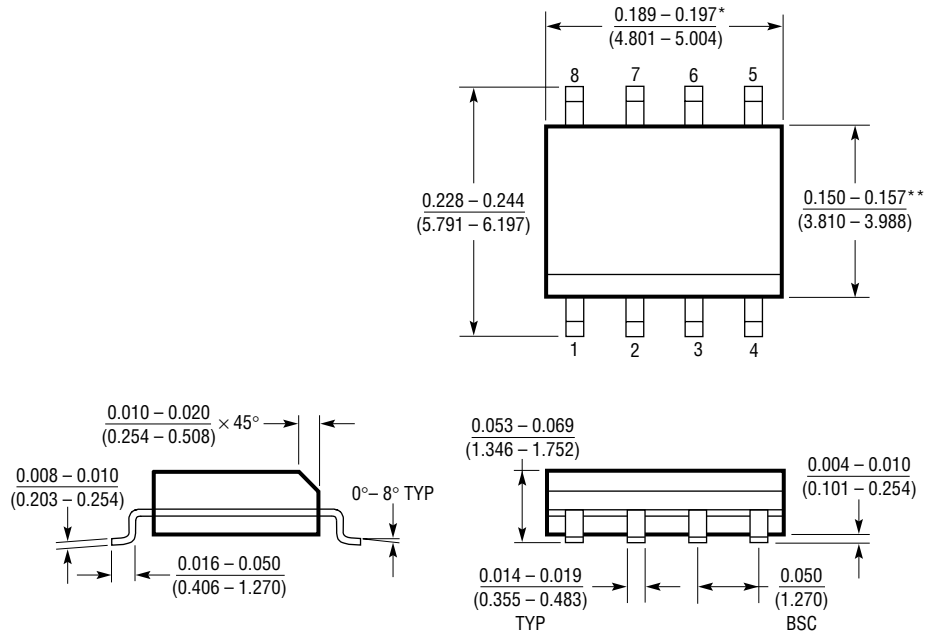
Dimensions in inches (millimeters) unless otherwise noted.

**N8 Package**  
**8-Lead PDIP (Narrow 0.300)**  
 (LTC DWG # 05-08-1510)



**PACKAGE DESCRIPTION** Dimensions in inches (millimeters) unless otherwise noted.

**S8 Package**  
**8-Lead Plastic Small Outline (Narrow 0.150)**  
 (LTC DWG # 05-08-1610)



\*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

\*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 1298