Positive High Voltage Hot Swap Controllers

FEATURES

- **Allows Safe Board Insertion and Removal from a Live Backplane**
- **Controls Supply Voltage from 9V to 80V**
- **Programmable Analog Foldback Current Limiting**
- High Side Drive for an External N-Channel
- Latched Operation Mode (LT1641-1)
- Automatic Retry (LT1641-2)
- User Programmable Supply Voltage Power-Up Rate
- Undervoltage Lockout
- Overvoltage Protection
- Both are available in 8-Lead SO Package

APPLICATIONS

- Hot Board Insertion
- Electronic Circuit Breaker
- Industrial High Side Switch/Circuit Breaker
- 24V/48V Industrial/Alarm Systems

DESCRIPTION

The LT®1641-1/LT1641-2 are 8-pin Hot Swap™ controllers that allow a board to be safely inserted and removed from a live backplane. Using an external N-channel pass transistor, the board supply voltage can be ramped up at a programmable rate. A high side switch driver controls an N-channel gate for supply voltages ranging from 9V to 80V.

The chips feature a programmable analog foldback current limit circuit. If the chips remain in current limit for more than a programmable time, the N-channel pass transistor is either latched off (LT1641-1) or is set to automatically restart after a time-out delay (LT1641-2).

The PWRGD output indicates when the output voltage, sensed by the FB pin, is within tolerance. The ON pin provides programmable undervoltage lockout.

The LT1641-1/LT1641-2 are available in the 8-lead SO package.

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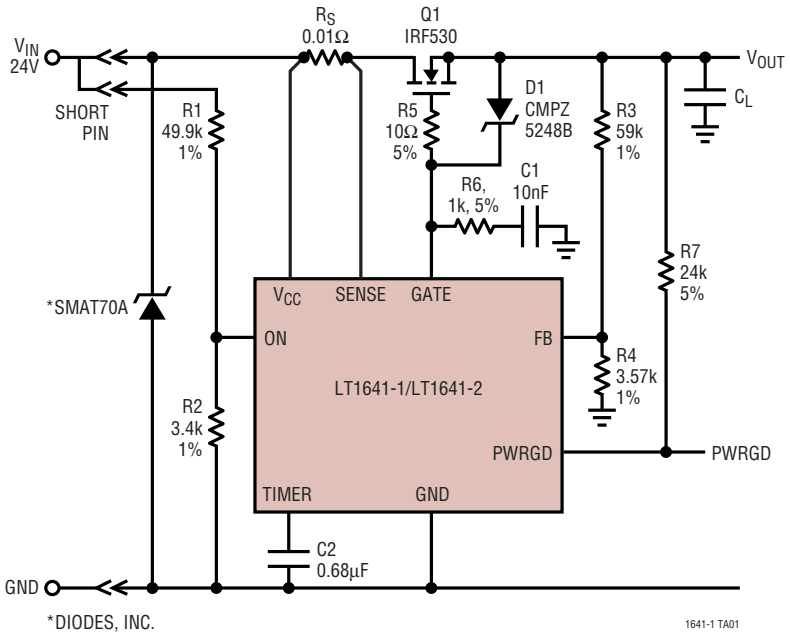
All other trademarks are the property of their respective owners.

TYPICAL APPLICATION

24V Input Voltage Application

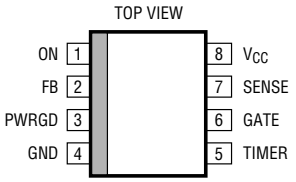


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) .....–0.3V to 100V
Input Voltage (SENSE).....–0.3V to 100V
Input Voltage (TIMER) .....–0.3V to 44V
Input Voltage (FB, ON).....–0.3V to 60V
Output Voltage (PWRGD) .....–0.3V to 100V
Output Voltage (GATE) .....–0.3V to 100V
Operating Temperature Range
LT1641-1C, LT1641-2C ..... 0°C to 70°C
LT1641-1I, LT1641-2I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER	S8 PART MARKING
LT1641-1CS8	16411
LT1641-1IS8	16411I
LT1641-2CS8	16412
LT1641-2IS8	16412I

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 24V

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	V_{CC} Operating Range		●	9		80	V
I_{CC}	V_{CC} Supply Current	ON = 3V	●		2	5.5	mA
V_{LKO}	V_{CC} Undervoltage Lockout		●	7.5	8.3	8.8	V
V_{FBH}	FB Pin High Voltage Threshold	FB Low to High Transition	●	1.280	1.313	1.345	V
V_{FBL}	FB Pin Low Voltage Threshold	FB High to Low Transition	●	1.221	1.233	1.245	V
V_{FBHST}	FB Pin Hysteresis Voltage				80		mV
I_{INFB}	FB Pin Input Current	V_{FB} = GND				–1	µA
ΔV_{FB}	FB Pin Threshold Line Regulation	9V ≤ V_{CC} ≤ 80V	●			0.05	mV/V
$V_{SENSETRIP}$	SENSE Pin Trip Voltage (V_{CC} – V_{SENSE})	V_{FB} = 0V V_{FB} = 1V	● ●	8 39	12 47	17 55	mV mV
I_{GATEUP}	GATE Pin Pull-Up Current	Charge Pump On, V_{GATE} = 7V	●	–5	–10	–20	µA
I_{GATEDN}	GATE Pin Pull-Down Current	Any Fault Condition, V_{GATE} = 2V	●	35	70	100	mA
ΔV_{GATE}	External N-Channel Gate Drive	V_{GATE} – V_{CC}, V_{CC} = 10.8V to 20V V_{CC} = 20V to 80V	● ●	4.5 10		18 18	V V
$I_{TIMERUP}$	TIMER Pin Pull-Up Current	V_{TIMER} = 0V	●	–24	–80	–132	µA
$I_{TIMERON}$	TIMER Pin Pull-Down Current	V_{TIMER} = 1V	●	1.5	3	5	µA
V_{ONH}	ON Pin High Threshold	ON Low to High Transition	●	1.280	1.313	1.345	V
V_{ONL}	ON Pin Low Threshold	ON High to Low Transition	●	1.221	1.233	1.245	V
V_{ONHYST}	ON Pin Hysteresis				80		mV
I_{INON}	ON Pin Input Current	V_{ON} = GND				–1	µA
V_{OL}	PWRGD Output Low Voltage	I_O = 2mA I_O = 4mA	● ●			0.4 2.5	V V
I_{OH}	PWRGD Pin Leakage Current	V_{PWRGD} = 80V	●			10	µA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 24V

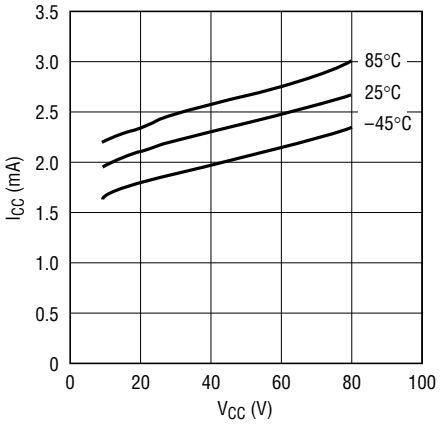
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHLON}	ON Low to GATE Low	Figures 1, 2		6		µs
t_{PLHON}	ON High to GATE High	Figures 1, 2		1.7		µs
t_{PHLFB}	FB Low to PWRGD Low	Figures 1, 3		3.2		µs
t_{PLHFB}	FB High to PWRGD High	Figures 1, 3		1.5		µs
$t_{PHLSENSE}$	(V_{CC} – SENSE) High to GATE Low	Figures 1, 4	0.5	1	2	µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

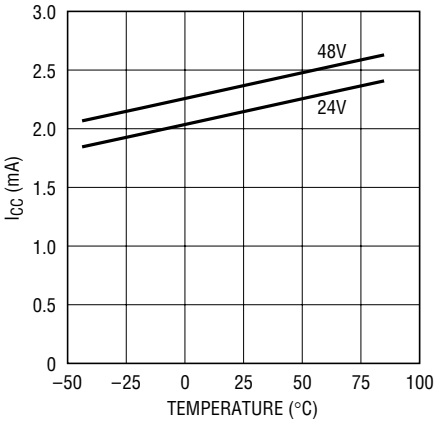
Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

TYPICAL PERFORMANCE CHARACTERISTICS

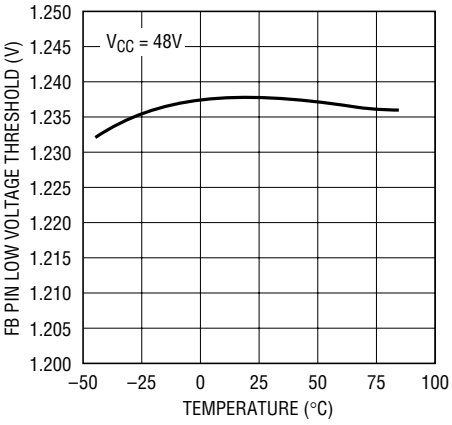
I_{CC} vs V_{CC}



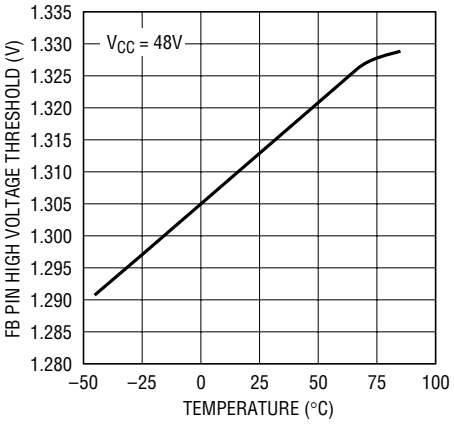
I_{CC} vs Temperature



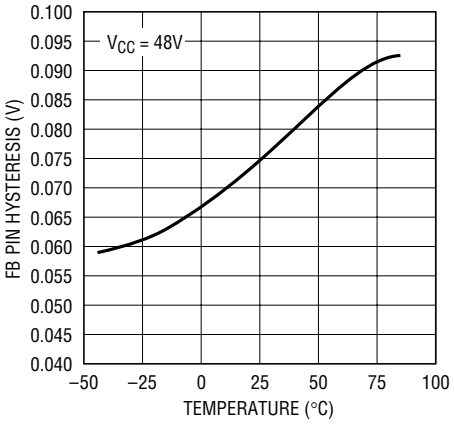
FB Pin Low Voltage Threshold vs Temperature



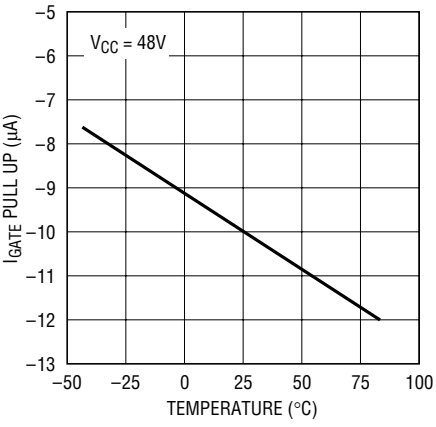
FB Pin High Voltage Threshold vs Temperature



FB Pin Hysteresis vs Temperature

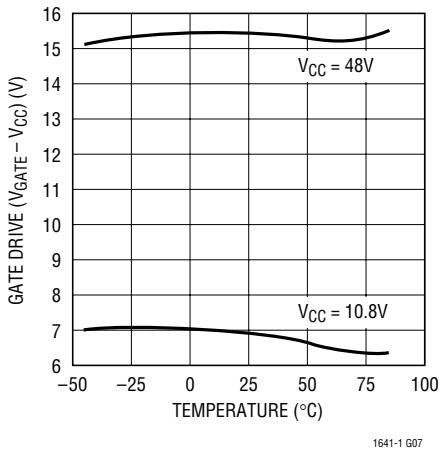


I_{GATE} Pull Up vs Temperature

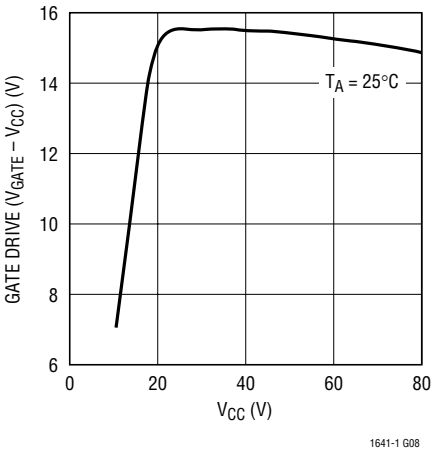


TYPICAL PERFORMANCE CHARACTERISTICS

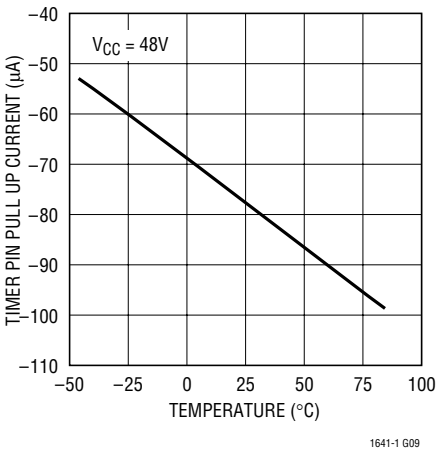
Gate Drive vs Temperature



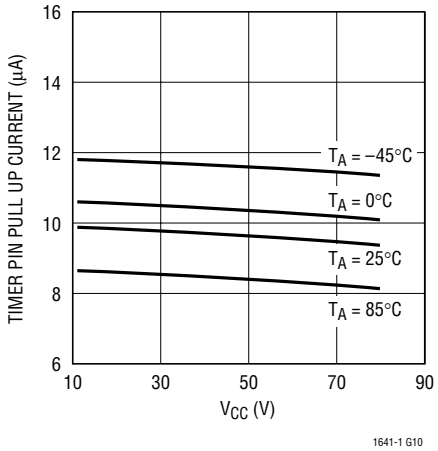
Gate Drive vs V_{CC}



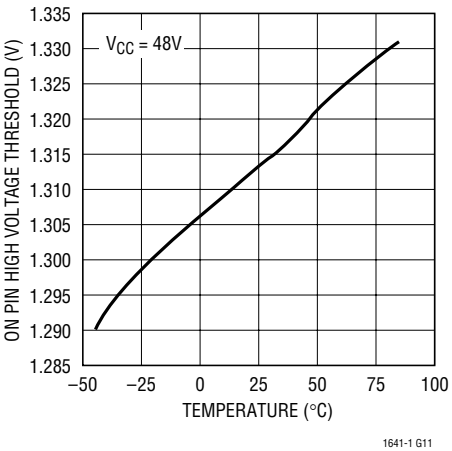
TIMER Pin Pull Up Current vs Temperature



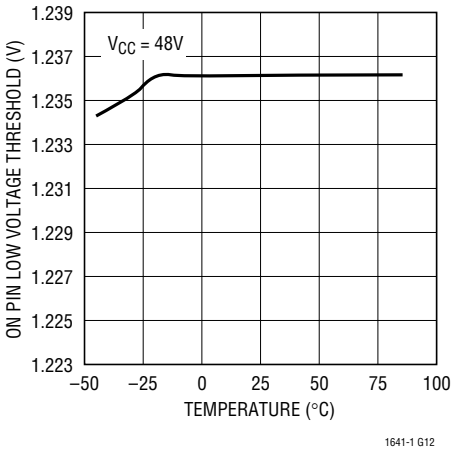
TIMER Pin Pull Up Current vs V_{CC}



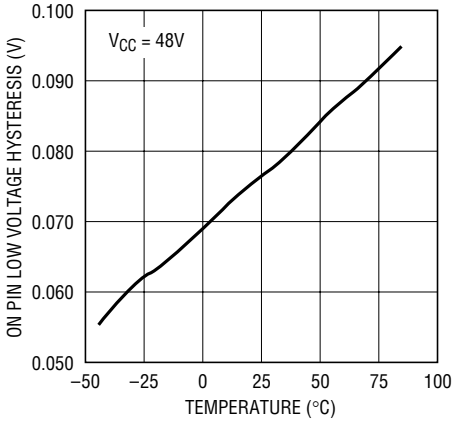
ON Pin High Voltage Threshold vs Temperature



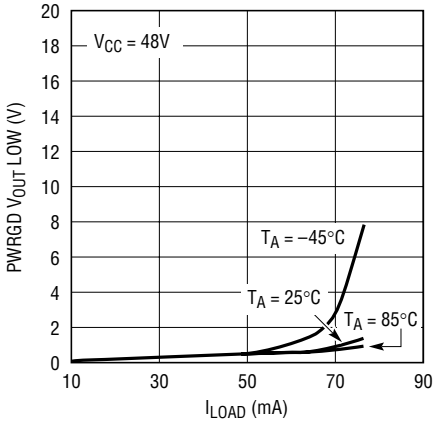
ON Pin Low Voltage Threshold vs Temperature



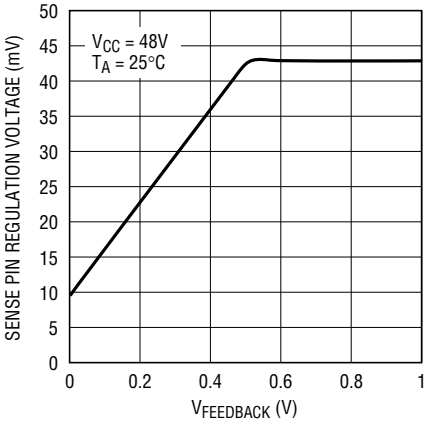
ON Pin Voltage Hysteresis vs Temperature



PWRGD V_{OUT} Low vs I_{LOAD}



SENSE Pin Regulation Voltage vs $V_{FEEDBACK}$



PIN FUNCTIONS

ON (Pin 1): The ON pin is used to implement undervoltage lockout. When the ON pin is pulled below the 1.233V High-to-Low threshold voltage, an undervoltage condition is detected and the GATE pin is pulled low to turn the MOSFET off. When the ON pin rises above the 1.313V Low-to-High threshold voltage, the MOSFET is turned on again.

Pulsing the ON pin low after a current limit fault will reset the fault latch and allow the part to turn back on.

FB (Pin 2): Power Good Comparator Input. It monitors the output voltage with an external resistive divider. When the voltage on the FB pin is lower than the High-to-Low threshold of 1.233V, the PWRGD pin is pulled low and released when the FB pin is pulled above the 1.313V Low-to-High threshold.

The FB pin also effects foldback current limit (see Figure 7 and related discussion).

PWRGD (Pin 3): Open Collector Output to GND. The PWRGD pin is pulled low whenever the voltage at the FB pin falls below the High-to-Low threshold voltage. It goes into a high impedance state when the voltage on the FB pin exceeds the Low-to-High threshold voltage. An external pull-up resistor can pull the pin to a voltage higher or lower than V_{CC}.

GND (Pin 4): Chip Ground.

TIMER (Pin 5): Timing Input. An external timing capacitor at this pin programs the maximum time the part is allowed to remain in current limit.

When the part goes into current limit, an 77µA pull-up current source starts to charge the timing capacitor. When the voltage on the TIMER pin reaches 1.233V, the GATE pin is pulled low; the pull-up current will be turned off and the capacitor is discharged by a 3µA pull-down current. When the TIMER pin falls below 0.5V, the GATE pin either turns on automatically (LT1641-2) or turns on once the ON pin is pulsed low to reset the internal fault latch (LT1641-1). If the ON pin is not cycled low, the GATE pin remains latched off. Use no less than 1.5nF for the timing capacitor, C2.

GATE (Pin 6): The High Side Gate Drive for the External N-Channel. An internal charge pump guarantees at least 10V of gate drive for supply voltages above 20V and 4.5V gate drive for supply voltages between 10.8V and 20V. The rising slope of the voltage at the GATE is set by an external capacitor connected from the GATE pin to GND and an internal 10µA pull-up current source from the charge pump output.

When the current limit is reached, the GATE pin voltage will be adjusted to maintain a constant voltage across the sense resistor while the timer capacitor starts to charge. If the TIMER pin voltage exceeds 1.233V, the GATE pin will be pulled low.

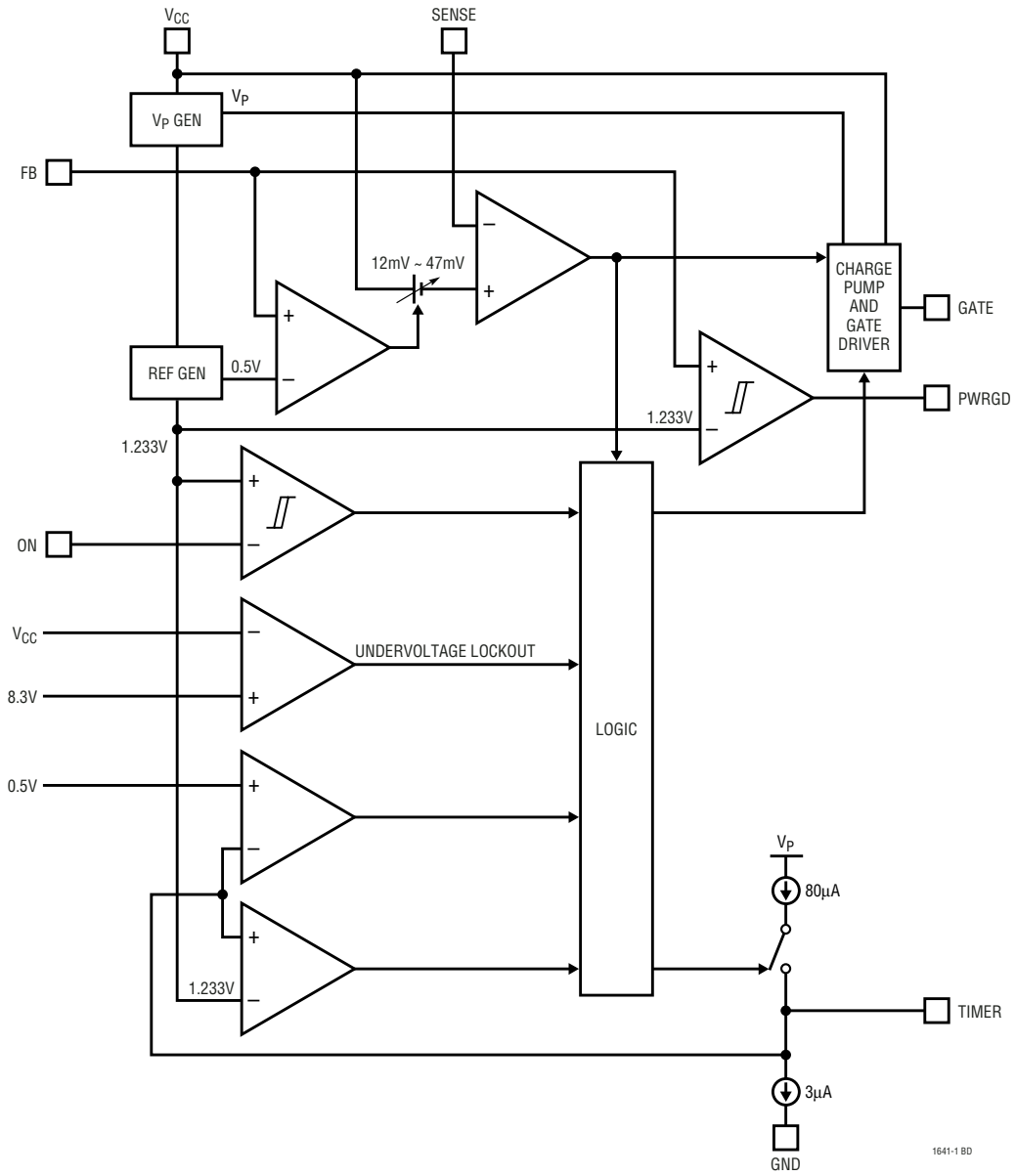
The GATE pin is pulled to GND whenever the ON pin is pulled low, the V_{CC} supply voltage drops below the 8.3V undervoltage lockout threshold or the TIMER pin rises above 1.233V.

SENSE (Pin 7): The Current Limit Sense Pin. A sense resistor must be placed in the supply path between V_{CC} and SENSE. The current limit circuit will regulate the voltage across the sense resistor ($V_{CC} – V_{SENSE}$) to 47mV when V_{FB} is 0.5V or higher. If V_{FB} drops below 0.5V, the voltage across the sense resistor decreases linearly and stops at 12mV when V_{FB} is 0V.

To defeat current limit, short the SENSE pin to the V_{CC} pin.

V_{CC} (Pin 8): The Positive Supply Input ranges from 9V to 80V for normal operation. I_{CC} is typically 2mA. An internal undervoltage lockout circuit disables the chip for inputs less than 8.3V.

BLOCK DIAGRAM



TEST CIRCUIT

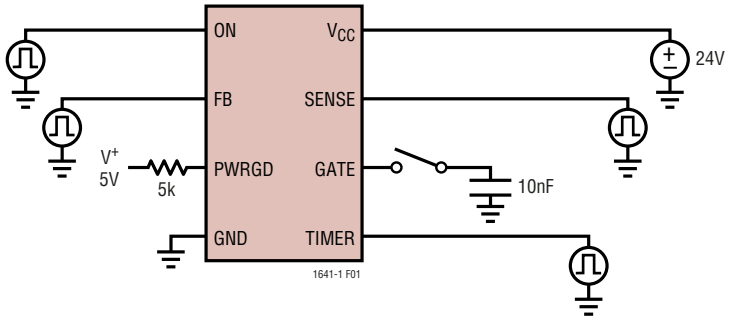


Figure 1

TIMING DIAGRAMS

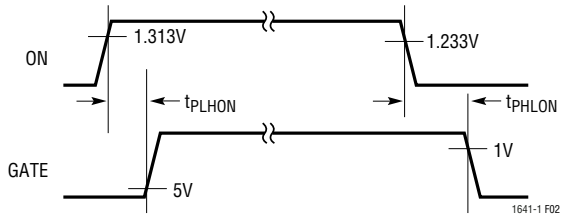


Figure 2. ON to GATE Timing

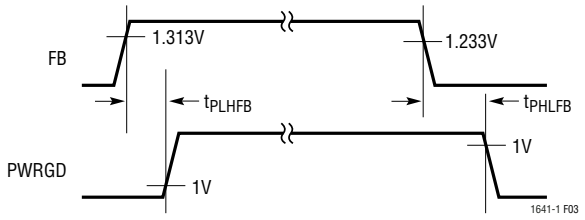


Figure 3. FB to PWRGD Timing

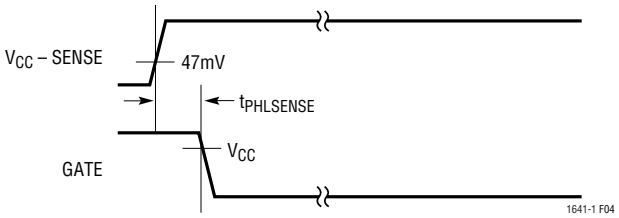


Figure 4. SENSE to GATE Timing

APPLICATIONS INFORMATION

Hot Circuit Insertion

When circuit boards are inserted into a live backplane, the supply bypass capacitors on the boards draw high peak currents from the backplane power bus as they charge up. The transient currents can permanently damage the connector pins and glitch the system supply, causing other boards in the system to reset.

The chip is designed to turn on a board's supply voltage in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. The chip also provides undervoltage and overcurrent protection while a power good output signal indicates when the output supply voltage is ready.

Power-Up Sequence

The power supply on a board is controlled by placing an external N-channel pass transistor (Q1) in the power path (Figure 5). Resistor R_S provides current detection and capacitor C1 provides control of the GATE slew rate. Resistor R6 provides current control loop compensation while R5 prevents high frequency oscillations in Q1. Resistors R1 and R2 provide undervoltage sensing.

After the power pins first make contact, transistor Q1 is turned off. If the voltage at the ON pin exceeds the turn-on threshold voltage, the voltage on the V_{CC} pin exceeds the undervoltage lockout threshold, and the voltage on the TIMER pin is less than 1.233V, transistor Q1 will be turned on (Figure 6). The voltage at the GATE pin rises with a slope equal to 10µA/C1 and the supply inrush current is set at $I_{INRUSH} = C_L \bullet 10\mu A/C1$. If the voltage across the current sense resistor R_S gets too high, the inrush current will then be limited by the internal current limit circuitry which adjusts the voltage on the GATE pin to maintain a constant voltage across the sense resistor.

Once the voltage at the output has reached its final value, as sensed by resistors R3 and R4, the PWRGD pin goes high.

APPLICATIONS INFORMATION

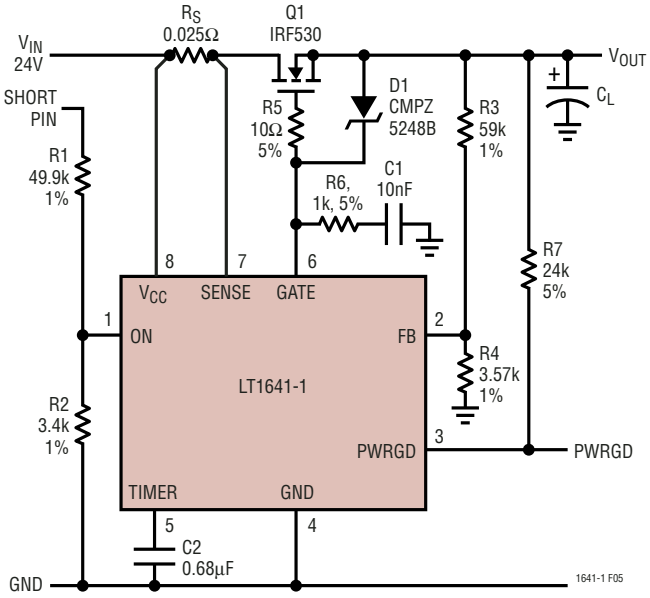


Figure 5. Typical Application

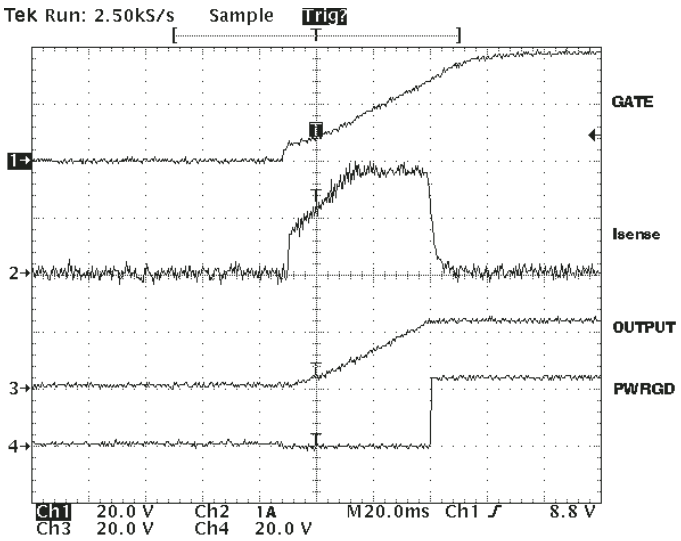


Figure 6. Power-Up Waveforms

Short-Circuit Protection

The chip features a programmable foldback current limit with an electronic circuit breaker that protects against short-circuits or excessive supply currents. The current limit is set by placing a sense resistor between V_{CC} (Pin 8) and SENSE (Pin 7).

To prevent excessive power dissipation in the pass transistor and to prevent voltage spikes on the input supply during short-circuit conditions at the output, the current folds back as a function of the output voltage, which is sensed at the FB pin (Figure 7).

When the voltage at the FB pin is 0V, the current limit circuit drives the GATE pin to force a constant 12mV drop across the sense resistor. As the output voltage at the FB pin increases, the voltage across the sense resistor increases until the FB pin reaches 0.5V, at which point the voltage across the sense resistor is held constant at 47mV.

The maximum current limit is calculated as:

$$I_{LIMIT} = 47mV/R_{SENSE}$$

For a 0.025Ω sense resistor, the current limit is set at 1.88A and folds back to 480mA when the output is shorted to ground.

The IC also features a variable overcurrent response time. The time required to regulate Q1's drain current depends on: Q1's input capacitance; gate capacitor C1 and compensation resistor R6; and the internal delay from the SENSE to the GATE pin. Figure 8 shows the delay from a voltage step at the SENSE pin until the GATE voltage starts falling, as a function of overdrive.

TIMER

The TIMER pin (Pin 5) provides a method for programming the maximum time the chip is allowed to operate in current limit. When the current limit circuitry is not active, the TIMER pin is pulled to GND by a 3µA current source. After the current limit circuit becomes active, an 80µA pull-up current source is connected to the TIMER pin and the voltage will rise with a slope equal to $77\mu A/C_{TIMER}$ as long as the current limit circuit remains active. Once the desired maximum current limit time is set, the capacitor value is: C(nF) = 62 • t(ms).

If the current limit circuit turns off, the TIMER pin will be discharged to GND by the 3µA current source.

Whenever the TIMER pin reaches 1.233V, either the internal fault latch is set (LT1641-1) or the autorestart latch is set (LT1641-2). The GATE pin is immediately pulled to GND and the TIMER pin is pulled back to GND by the 3µA

APPLICATIONS INFORMATION

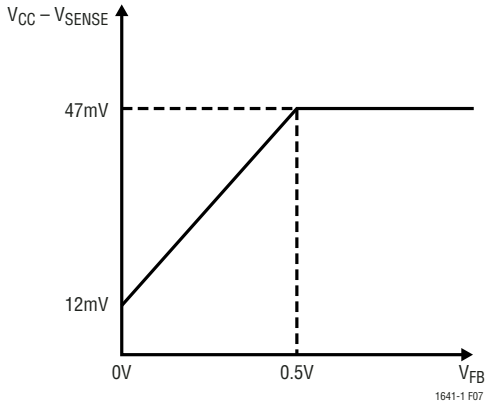


Figure 7. Current Limit Sense Voltage vs Feedback Pin Voltage

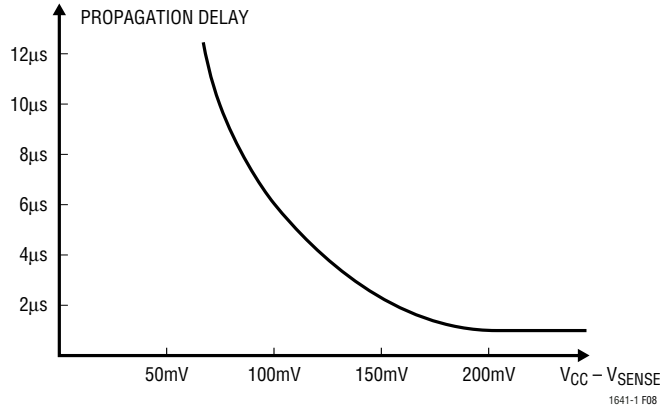


Figure 8. Response Time to Overcurrent

current source. When the TIMER pin falls below 0.5V, the GATE pin either turns on automatically (LT1641-2) or once the ON pin is pulsed low to reset the internal fault latch (LT1641-1).

The waveform in Figure 9 shows how the output latches off following a short-circuit. The drop across the sense resistor is held at 12mV as the timer ramps up. Since the output did not rise bringing FB above 0.5V, the circuit latches off. For Figure 9, C_T = 100nF.

Undervoltage and Overvoltage Detection

The ON pin can be used to detect an undervoltage condition at the power supply input. The ON pin is internally connected to an analog comparator with 80mV of hysteresis. If the ON pin falls below its threshold voltage (1.233V), the GATE pin is pulled low and is held low until ON is high again.

Figure 10 shows an overvoltage detection circuit. When the input voltage exceeds the Zener diode's breakdown voltage, D2 turns on and starts to pull the TIMER pin high. After the TIMER pin is pulled higher than 1.233V, the fault latch is set and the GATE pin is pulled to GND immediately, turning off transistor Q1. The waveforms are shown in Figure 11. Operation is restored either by interrupting power or by pulsing ON low.

Power Good Detection

The chip includes a comparator for monitoring the output voltage. The noninverting input (FB pin) is compared against an internal 1.233V precision reference and exhibits 80mV hysteresis. The comparator's output (PWRGD pin) is an open collector capable of operating from a pull-up as high as 100V.

The PWRGD pin can be used to directly enable/disable a power module with an active high enable input. Figure 12 shows how to use the PWRGD pin to control an active low enable input power module. Signal inversion is accomplished by transistor Q2 and R7.

Supply Transient Protection

The IC is 100% tested and guaranteed to be safe from damage with supply voltages up to 100V. However, spikes above 100V may damage the part. During a short-circuit condition, the large change in currents flowing through the power supply traces can cause inductive voltage spikes which could exceed 100V. To minimize the spikes, the power trace parasitic inductance should be minimized by using wider traces or heavier trace plating and a 0.1µF bypass capacitor placed between V_{CC} and GND. A surge suppressor at the input can also prevent damage from voltage surges.

APPLICATIONS INFORMATION

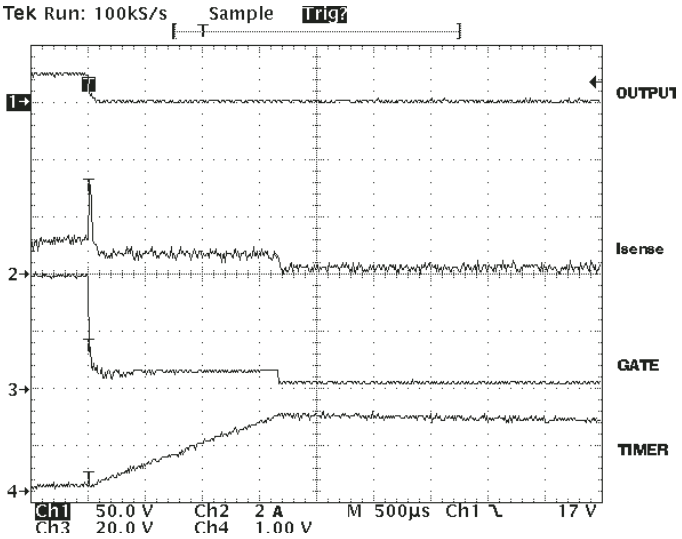


Figure 9. Short-Circuit Waveforms

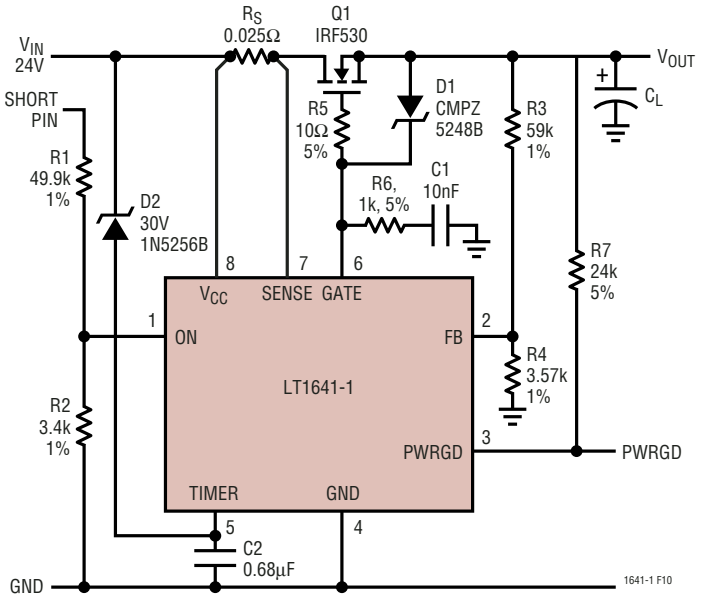


Figure 10. Overvoltage Detection

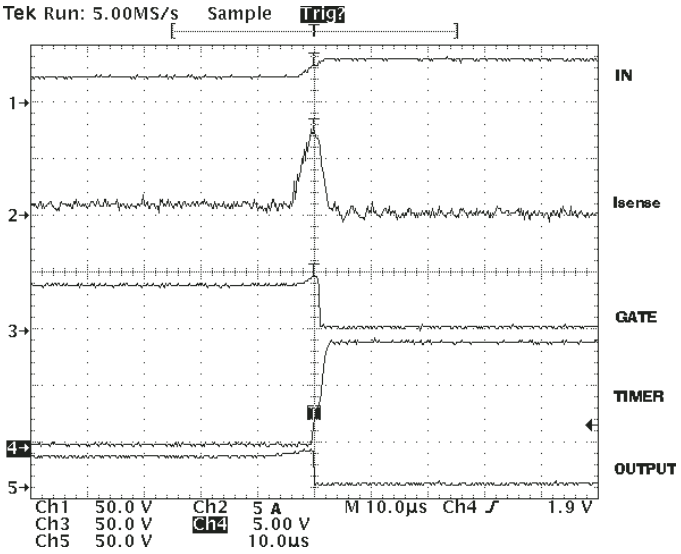


Figure 11. Overvoltage Waveforms

GATE Pin Voltage

A curve of gate drive vs V_{CC} is shown in Figure 13. The GATE pin is clamped to a maximum voltage of 18V above the input voltage. At minimum input supply voltage of 9V, the minimum gate drive voltage is 4.5V. When the input supply voltage is higher than 20V, the gate drive voltage is at least 10V and a regular N-FET can be used. In applications over a 9V to 24V range, a logic level N-FET must be used with a proper protection Zener diode between its gate and source (as D1 shown is Figure 5).

APPLICATIONS INFORMATION

Layout Considerations

To achieve accurate current sensing, a Kelvin connection is recommended. The minimum trace width for 1oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 530µΩ/□. Small resistances add up quickly in high current applications. To improve noise immunity, put the resistor divider to the ON pin close to the chip and keep traces to V_{CC} and GND short. A 0.1µF capacitor from the ON pin to GND also helps reject induced noise. Figure 14 shows a layout that addresses these issues.

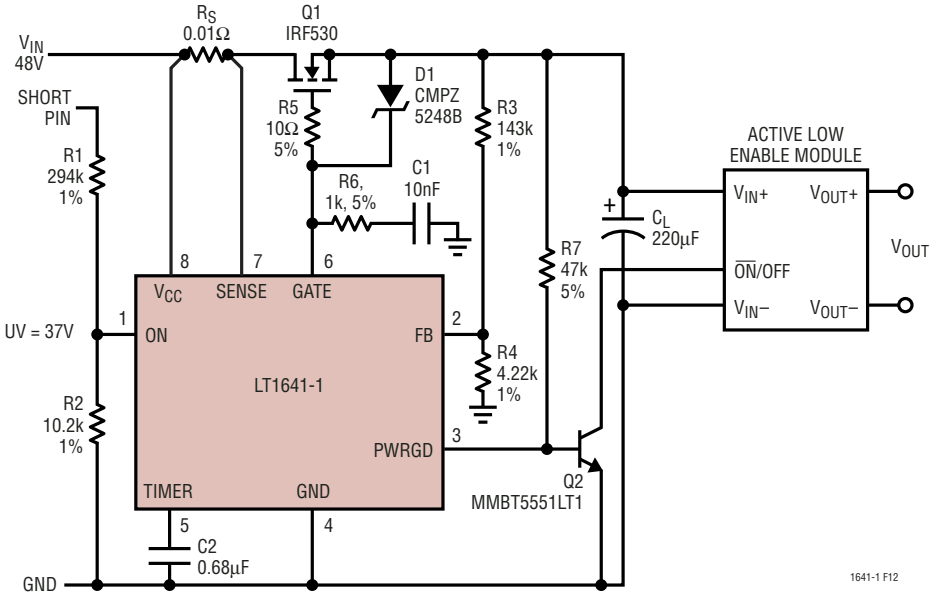


Figure 12. Active Low Enable Module

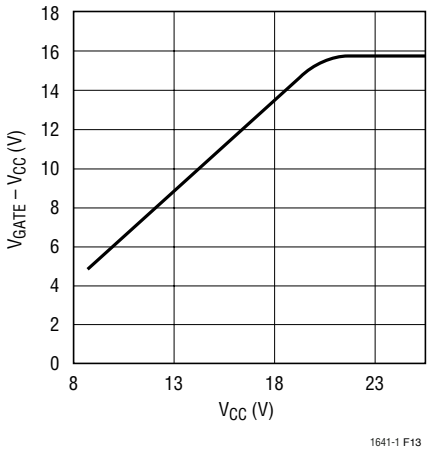


Figure 13. Gate Drive vs Supply Voltage

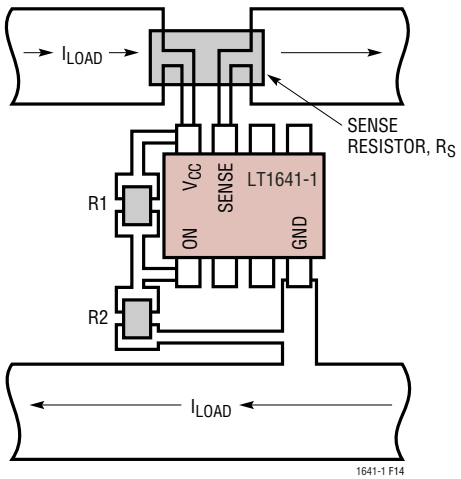


Figure 14. Recommended Layout for R1, R2 and R_S

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