

60ns, Low Power, Single Supply, Ground-Sensing Comparator

FEATURES

- **Low Power: 450 μ A**
- **Fast: 60ns at 20mV Overdrive**
85ns at 5mV Overdrive
- **Low Offset Voltage: 0.8mV**
- Operates Off Single 5V or Dual \pm 5V Supplies
- Input Common Mode Extends to Negative Supply
- No Minimum Input Slew Rate Requirement
- Complementary TTL Outputs
- Inputs Can Exceed Supplies without Phase Reversal
- Pin Compatible with LT1394, LT1016 and LT1116
- Output Latch Capability
- Available in 8-Lead MSOP and SO Packages

APPLICATIONS


- High Speed A/D Converters
- Zero-Crossing Detectors
- Current Sense for Switching Regulators
- Extended Range V/F Converters
- Fast Pulse Height/Width Discriminators
- High Speed Triggers
- Line Receivers
- High Speed Sampling Circuits

DESCRIPTION

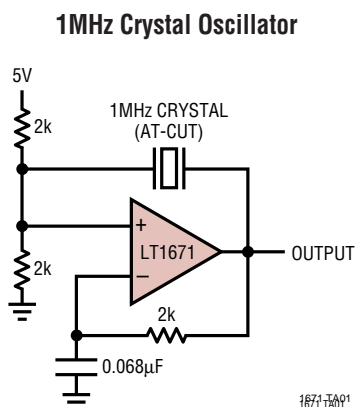
The LT[®]1671 is a low power 60ns comparator with complementary outputs and latch. The input common mode range extends from 1.5V below the positive supply down to the negative supply rail. Like the LT1394, LT1016 and LT1116, this comparator has complementary outputs designed to interface directly to TTL or CMOS logic. The LT1671 may operate from either a single 5V supply or dual \pm 5V supplies. Low offset voltage specifications and high gain allow the LT1671 to be used in precision applications.

The LT1671 is designed for improved speed and stability for a wide range of operating conditions. The output stage provides active drive in both directions for maximum speed into TTL, CMOS or passive loads with minimal cross-conduction current. Unlike other fast comparators, the LT1671 remains stable even for slow transitions through the active region, which eliminates the need to specify a minimum input slew rate.

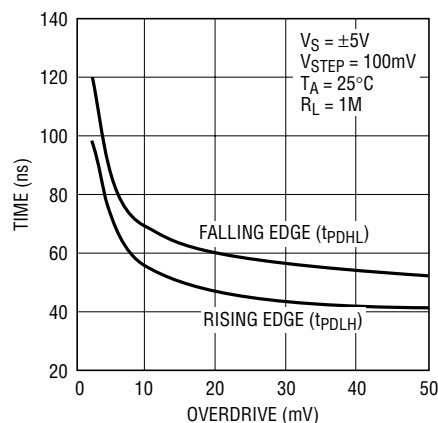
The LT1671 has an internal, TTL/CMOS compatible latch for retaining data at the outputs. The latch holds data as long as the LATCH pin is held high. Device parameters such as gain, offset and negative power supply current are not significantly affected by variations in negative supply voltage.

 LTC and LT are registered trademarks of Linear Technology Corporation.

TYPICAL APPLICATION



Propagation Delay vs Overdrive



ABSOLUTE MAXIMUM RATINGS (Note 1)

| | | | |
|---|-------|---|----------------|
| Total Supply Voltage (V^+ to V^-) | 12V | Operating Temperature Range | -40°C to 85°C |
| Positive Supply Voltage | 7V | Specified Temperature Range (Note 3) ... | -40°C to 85°C |
| Negative Supply Voltage | -7V | Junction Temperature | 150°C |
| Differential Input Voltage | ±12V | Storage Temperature Range | -65°C to 150°C |
| Input and Latch Current (Note 2) | ±10mA | Lead Temperature (Soldering, 10 sec.) | 300°C |
| Output Current (Continuous)(Note 2) | ±20mA | | |

PACKAGE/ORDER INFORMATION

| | | | |
|--|-------------------|---|------------------------|
| <p>MS8 PACKAGE 8-LEAD PLASTIC MSOP</p> <p>$T_{JMAX} = 150^{\circ}C, \theta_{JA} = 250^{\circ}C/W$</p> | ORDER PART NUMBER | <p>S8 PACKAGE 8-LEAD PLASTIC SO</p> <p>$T_{JMAX} = 150^{\circ}C, \theta_{JA} = 190^{\circ}C/W$</p> | ORDER PART NUMBER |
| | LT1671CMS8 | | LT1671CS8 LT1671IS8 |
| | MS8 PART MARKING | | S8 PART MARKING |
| | LTCT | | 1671 1671I |

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^{\circ}C$. $V^+ = 5V, V^- = -5V, V_{OUT}(Q) = 1.4V, V_{LATCH} = V_{CM} = 0V$ unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------------|------------------------------|--|--------|---------|------------|-------------------|
| V_{OS} | Input Offset Voltage | $R_S \leq 100\Omega$ (Note 4) | ● | 0.8 | 2.5 4.0 | mV mV |
| $\frac{\Delta V_{OS}}{\Delta T}$ | Input Offset Voltage Drift | | ● | 4 | | $\mu V/^{\circ}C$ |
| I_{OS} | Input Offset Current | | ● | 10 | 100 150 | nA nA |
| I_B | Input Bias Current | (Note 5) | ● | 120 | 280 350 | nA nA |
| V_{CMR} | Input Voltage Range (Note 6) | Single 5V Supply | ● ● | -5 0 | 3.5 3.5 | V V |
| CMRR | Common Mode Rejection Ratio | $-5V \leq V_{CM} \leq 3.5V, T_A > 0^{\circ}C$ | | 55 | 100 | dB |
| | | $-5V \leq V_{CM} \leq 3.3V, T_A \leq 0^{\circ}C$ | | 55 | | dB |
| PSRR | Power Supply Rejection Ratio | Single 5V Supply $0V \leq V_{CM} \leq 3.5V, T_A > 0^{\circ}C$ | | 55 | 100 | dB |
| | | $0V \leq V_{CM} \leq 3.3V, T_A \leq 0^{\circ}C$ | | 55 | | dB |
| A_V | Small Signal Voltage Gain | $4.6V \leq V^+ \leq 5.4V$ | ● | 50 | 85 | dB |
| | | $-7V \leq V^- \leq -2V$ | ● | 60 | 90 | dB |
| A_V | Small Signal Voltage Gain | $1V \leq V_{OUT} \leq 2V$ | | 2500 | 5000 | V/V |

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^\circ\text{C}$. $V^+ = 5\text{V}$, $V^- = -5\text{V}$, $V_{\text{OUT(Q)}} = 1.4\text{V}$, $V_{\text{LATCH}} = V_{\text{CM}} = 0\text{V}$ unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|---|---|-----|-------|-------------|--------------------------------|
| V_{OH} | Output Voltage Swing High | $V^+ \geq 4.6\text{V}$, $I_{\text{OUT}} = 400\mu\text{A}$ | ● | 2.7 | 3.1 | V |
| | | $V^+ \geq 4.6\text{V}$, $I_{\text{OUT}} = 4\text{mA}$ | ● | 2.4 | 3.0 | V |
| V_{OL} | Output Voltage Swing Low | $I_{\text{OUT}} = -400\mu\text{A}$ | ● | 0.3 | 0.5 | V |
| | | $I_{\text{OUT}} = -4\text{mA}$ | | 0.4 | | V |
| I^+ | Positive Supply Current | | | 450 | 800 1000 | μA μA |
| I^- | Negative Supply Current | | | 75 | 200 250 | μA μA |
| V_{IH} | LATCH Pin High Input Voltage | | ● | 2 | | V |
| V_{IL} | LATCH Pin Low Input Voltage | | ● | | 0.8 | V |
| I_{IL} | LATCH Pin Current | $V_{\text{LATCH}} = 0\text{V}$ | ● | -1000 | -250 | nA |
| t_{PD1} | Propagation Delay | $\Delta V_{\text{IN}} = 100\text{mV}$, $V_{\text{OD}} = 20\text{mV}$ | | 60 | 80 | ns |
| | | | ● | | 110 | ns |
| t_{PD2} | Propagation Delay (Note 7) | $\Delta V_{\text{IN}} = 100\text{mV}$, $V_{\text{OD}} = 5\text{mV}$ | | 85 | 100 | ns |
| | | | ● | | 130 | ns |
| Δt_{PD} | Differential Propagation Delay (Note 7) | $\Delta V_{\text{IN}} = 100\text{mV}$, $V_{\text{OD}} = 5\text{mV}$ | | 15 | 30 | ns |
| t_{LPD} | Latch Propagation Delay (Note 8) | | | 60 | | ns |
| t_{SU} | Latch Setup Time (Note 8) | | | -15 | | ns |
| t_{H} | Latch Hold Time (Note 8) | | | 35 | | ns |
| $t_{\text{PW(D)}}$ | Minimum Disable Pulse Width | | | 30 | | ns |

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: This parameter is guaranteed to meet specified performance through design and characterization. It has not been tested.

Note 3: The LT1671CS8 and LT1671CMS8 are guaranteed to meet specified performance from 0°C to 70°C and are designed, characterized and expected to meet these extended temperature limits, but are not tested at -40°C and 85°C . The LT1671IS8 is guaranteed to meet the extended temperature limits.

Note 4: Input offset voltage (V_{OS}) is defined as the average of the two voltages measured by forcing first one output, then the other to 1.4V.

Note 5: Input bias current (I_{B}) is defined as the average of the two input currents.

Note 6: Input voltage range is guaranteed in part by CMRR testing and in part by design and characterization.

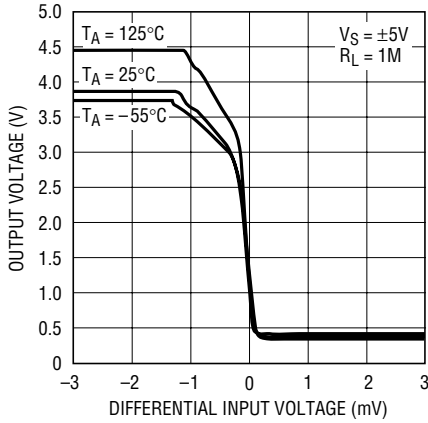
Note 7: t_{PD} and Δt_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The LT1671 is 100% tested with a 100mV step and 20mV overdrive. Correlation tests have shown that t_{PD} and Δt_{PD} limits can be guaranteed with this test, if additional DC tests are performed to guarantee that all internal bias conditions are correct. Propagation delay (t_{PD}) is measured with the overdrive added to the actual V_{OS} . Differential propagation delay is defined as:

$$\Delta t_{\text{PD}} = t_{\text{PDLH}} - t_{\text{PDHL}}$$

Note 8: Latch propagation delay (t_{LPD}) is the delay time for the output to respond when the LATCH pin is deasserted. Latch setup time (t_{SU}) is the interval in which the input signal must remain stable prior to asserting the latch signal. Latch hold time (t_{H}) is the interval after the latch is asserted in which the input signal must remain stable.

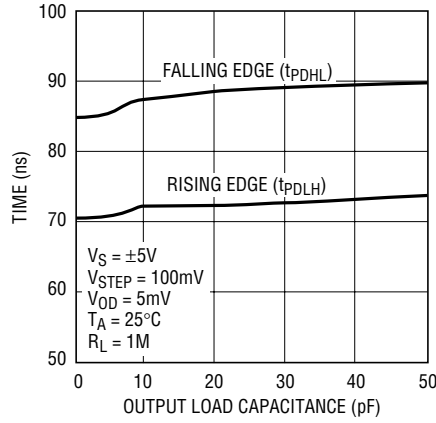
TYPICAL PERFORMANCE CHARACTERISTICS

Gain Characteristics



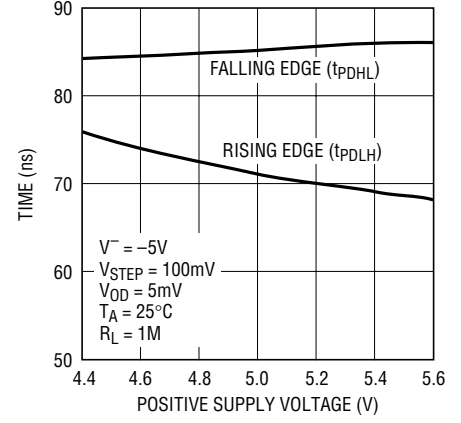
1671 G01

Propagation Delay vs Load Capacitance



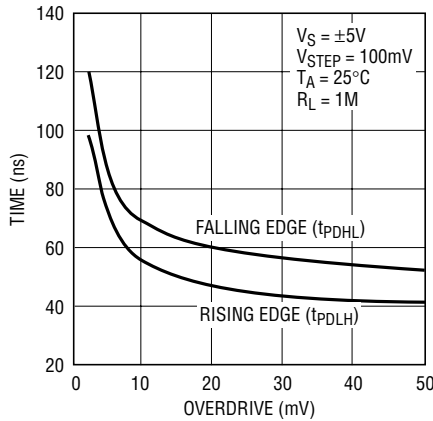
1671 G02

Propagation Delay vs Positive Supply Voltage



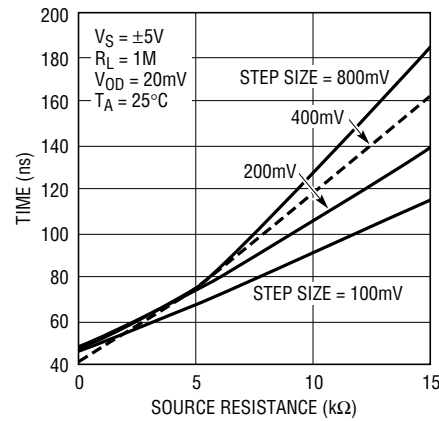
1671 G03

Propagation Delay vs Input Overdrive



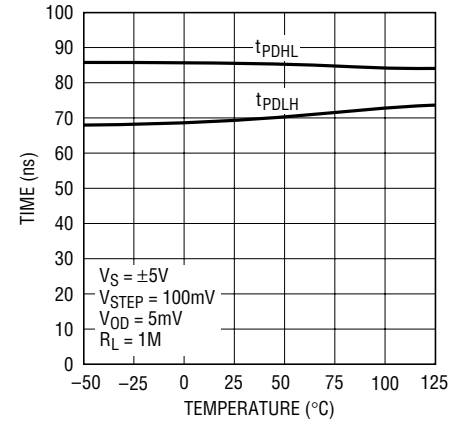
1671 TA02

Propagation Delay vs Source Resistance



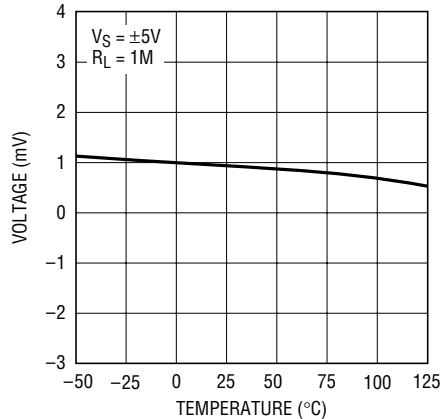
1671 G05

Propagation Delay vs Temperature



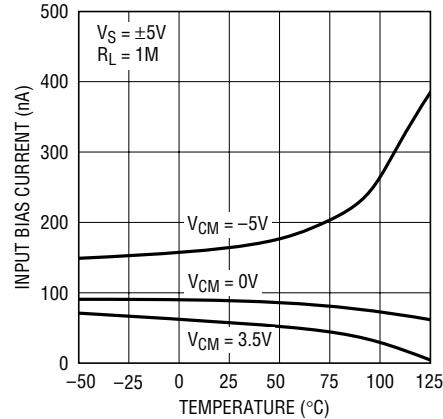
1671 G06

Input Offset Voltage vs Temperature



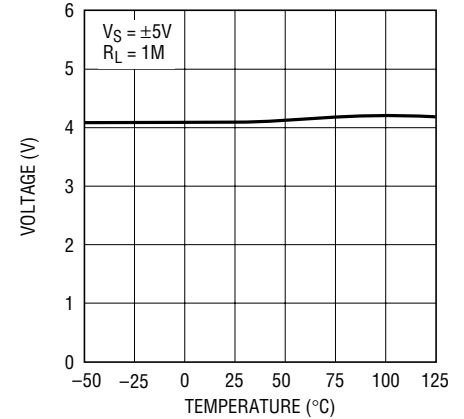
1671 G07

Input Bias Current vs Temperature



1671 G08

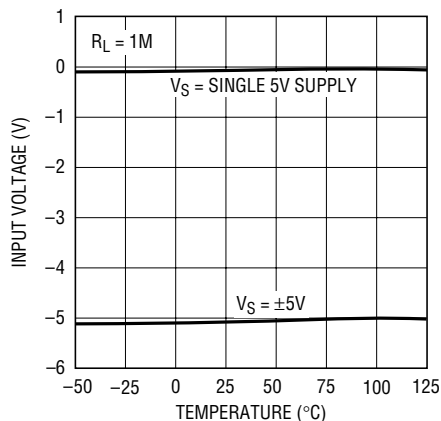
Positive Common Mode Limit vs Temperature



1671 G09

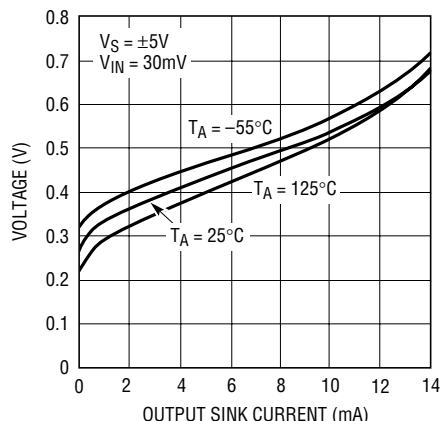
TYPICAL PERFORMANCE CHARACTERISTICS

Negative Common Mode Limit vs Temperature



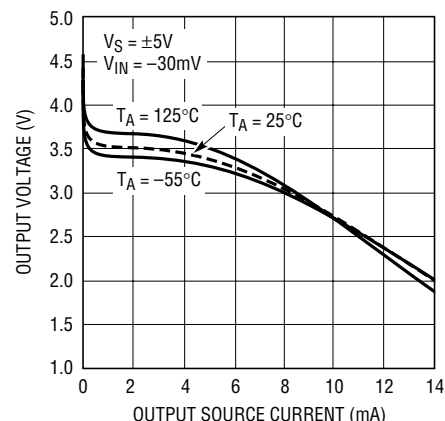
1671 G10

Output Low Voltage (V_{OL}) vs Output Sink Current



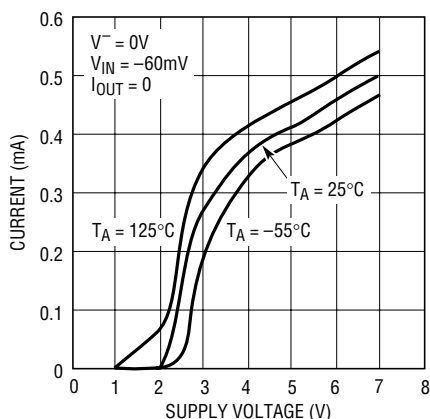
1671 G11

Output High Voltage (V_{OH}) vs Output Source Current



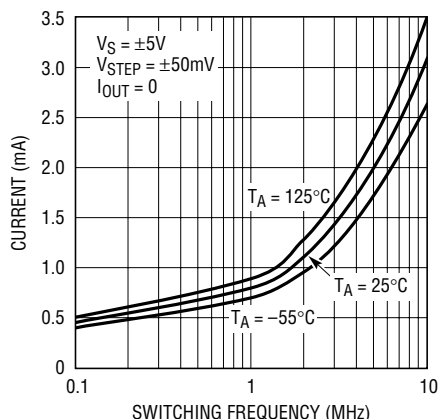
1671 G12

Positive Supply Current vs V^+ Supply Voltage



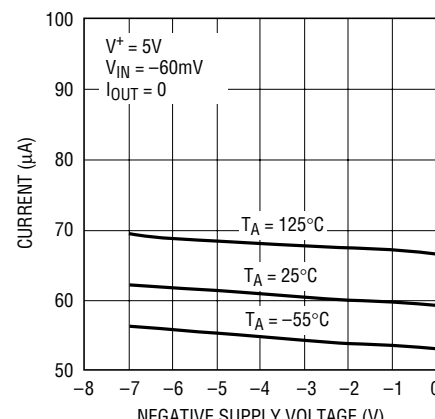
1671 G13

Positive Supply Current vs Switching Frequency



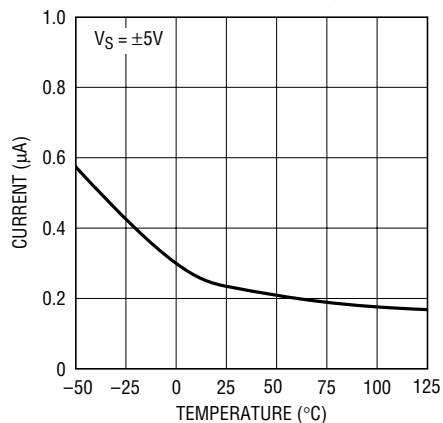
1671 G14

Negative Supply Current vs V^- Supply Voltage



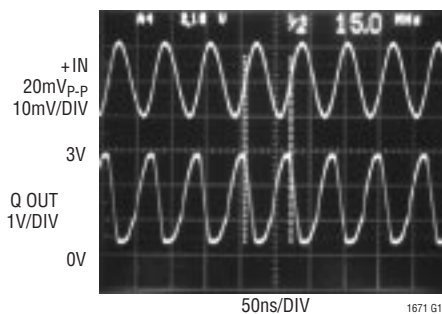
1671 G15

Latch Pin Current vs Temperature



1671 G16

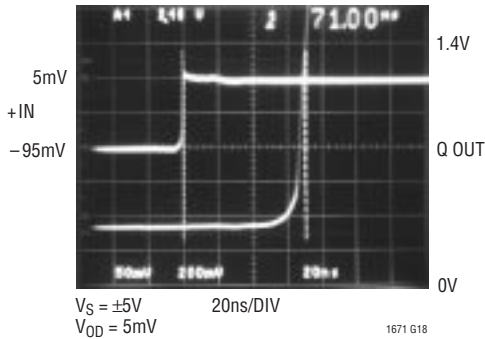
Response to 15MHz $\pm 10mV$ Sine Wave



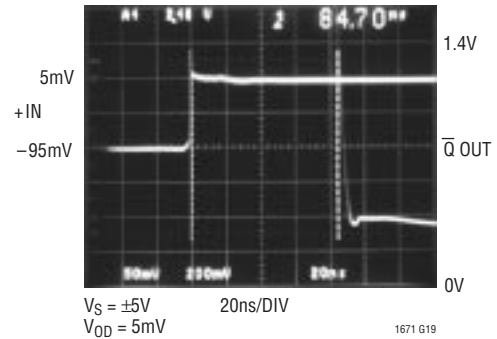
1671 G17

TYPICAL PERFORMANCE CHARACTERISTICS

t_{PD}^+ Response Time to 5mV Overdrive



t_{PD}^- Response Time to 5mV Overdrive



PIN FUNCTIONS

V⁺ (Pin 1): Positive Supply Voltage. Normally 5V.

+IN (Pin 2): Noninverting Input.

-IN (Pin 3): Inverting Input.

V⁻ (Pin 4): Negative Supply Voltage. Normally either 0V or -5V.

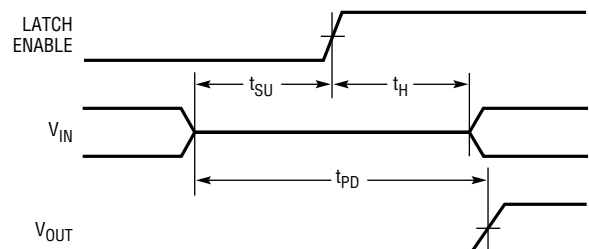
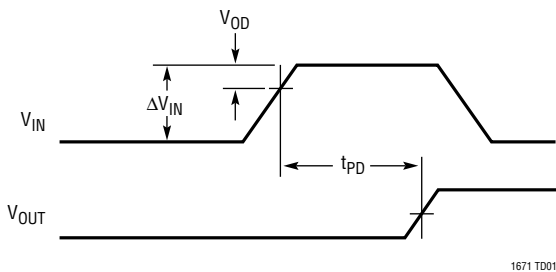
LATCH ENABLE (Pin 5): Latch Control Pin. When high, the outputs remain in a latched condition, independent of the current state of the inputs.

GND (Pin 6): Ground.

Q OUT (Pin 7): Noninverting Logic Output. This pin is high when +IN is above -IN and LATCH ENABLE is low.

Q-bar OUT (Pin 8): Inverting Logic Output. This pin is low when +IN is above -IN and LATCH ENABLE is low.

TIMING DIAGRAMS



APPLICATIONS INFORMATION

Common Mode Considerations

The LT1671 is specified for a common mode range of $-5V$ to $3.5V$ on a $\pm 5V$ supply or a common mode range of $0V$ to $3.5V$ on a single $5V$ supply. A more general consideration is that the common mode range is $0V$ below the negative supply and $1.5V$ below the positive supply, independent of the actual supply voltage. The criterion for common mode limit is that the output still responds correctly to a small differential input signal.

When either input signal falls below the negative common mode limit, the internal PN diode formed with the substrate can turn on, resulting in significant current flow through the die. An external Schottky clamp diode between the input and the negative rail can speed up recovery from negative overdrive by preventing the substrate diode from turning on.

The zero crossing detector in Figure 1 demonstrates the use of a fast clamp diode. The zero crossing detector terminates the transmission line at its 50Ω characteristic impedance. Negative inputs should not fall below $-2V$ to keep the signal current within the clamp diode's maximum forward rating. Positive inputs should not exceed the device's absolute maximum ratings nor the power rating on the terminating resistor.

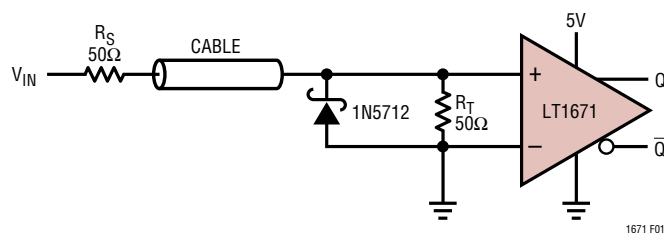


Figure 1. Fast Zero Crossing Detector

Either input may go above the positive common mode limit without damaging the comparator. The upper voltage limit is determined by an internal diode from each input to the positive supply. The input may go above the positive supply as long as it does not go far enough above it to conduct more than $10mA$. Functionality will continue if the remaining input stays within the allowed common mode range. There will, however, be an increase in propagation delay as the input signal switches back into the common mode range.

Input Bias Current

Input bias current is measured with the output held at $1.4V$. As with any PNP differential input stage, the LT1671 bias current flows out of the device. It will go to zero on an input which is high and double on an input which is low.

LATCH Pin Dynamics

The LATCH pin is intended to retain input data (output latched) when the LATCH pin goes high. The pin will float to a high state when disconnected, so a flow-through condition requires that the LATCH pin be grounded. The LATCH pin is designed to be driven with either a TTL or CMOS output. It has no built-in hysteresis.

To guarantee data retention, the input signal must remain valid at least $35ns$ after the latch goes high (hold time), and must be valid at least $-15ns$ before the latch goes high (setup time). The negative setup time simply means that the data arriving $15ns$ after (rather than before) the latch signal is valid. When the latch signal goes low, new data will appear at the output in approximately $60ns$ (latch propagation delay).

Measuring Response Time

To properly measure the response of the LT1671 requires an input signal source with very fast rise times and exceptionally clean settling characteristics. The last requirement comes about because the standard comparator test calls for an input step size that is large compared to the overdrive amplitude. Typical test conditions are $100mV$ step size with $5mV$ overdrive. This requires an input signal that settles to within $1%$ ($1mV$) of final value in only a few nanoseconds with no ringing or settling tail. Ordinary high speed pulse generators are not capable of generating such a signal, and in any case, no ordinary oscilloscope is capable of displaying the waveform to check its fidelity. Some means must be used to inherently generate a fast, clean edge with known final value. The circuit shown in Figure 2 is the best electronic means of generating a fast, clean step to test comparators. It uses a very fast transistor in a common base configuration. The transistor is switched off with a fast edge from the generator and the collector voltage settles to exactly $0V$ in just a few nanoseconds. The most important feature of this

APPLICATIONS INFORMATION

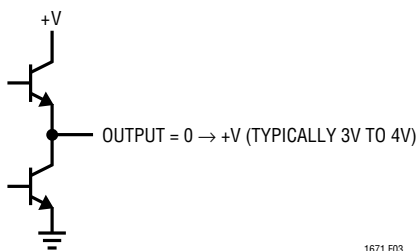


Figure 3. Simplified LT1671 Output Stage

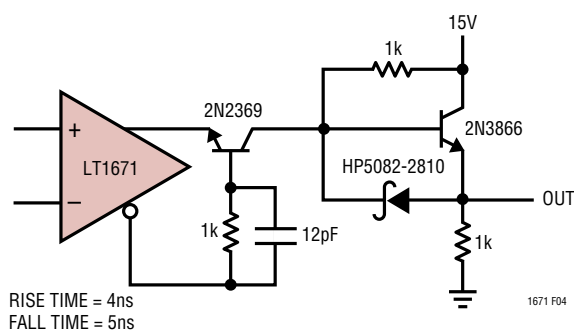


Figure 4. Level Shift Has Noninverting Voltage Gain

Figure 5 is a very versatile stage. It features a bipolar swing that is set by the output transistor's supplies. This 3ns delay stage is ideal for driving FET switch gates. Q1, a gated current source, switches the Baker-clamped output transistor, Q2. The heavy feedforward capacitor from the

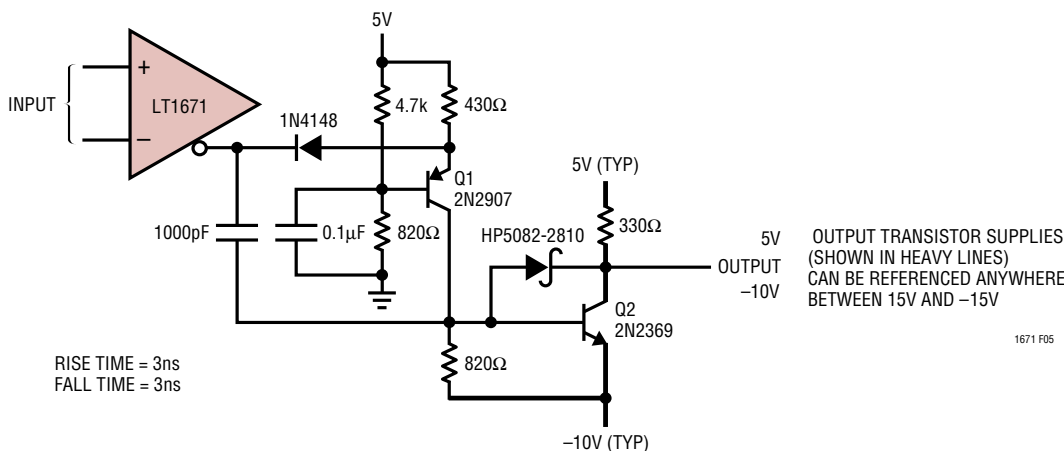


Figure 5. Level Shift with Inverting Voltage Gain—Bipolar Swing

LT1671 is the key to low delay, providing Q2's base with nearly ideal drive. This capacitor loads the LT1671's output transition, but Q2's switching is clean with 3ns delay on the rise and fall of the pulse. Figure 6 is similar to Figure 4 except that a sink transistor has replaced the Schottky diode. The two emitter-followers drive a power MOSFET that switches 1A at 15V. Most of the 7ns to 9ns delay in this stage occurs in the MOSFET and the 2N2369.

When designing level shifters, remember to use transistors with fast switching times and high f_T . To get the kind of results shown, switching times in the nanosecond range and an f_T approaching 1GHz are required.

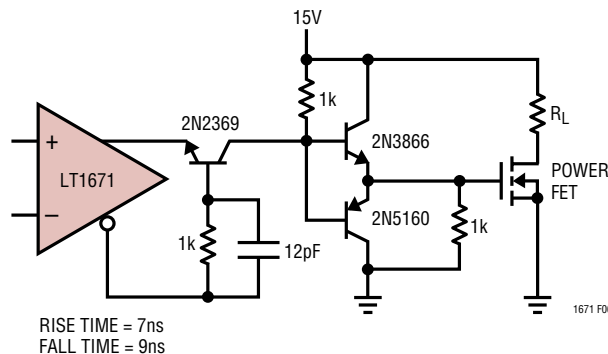


Figure 6. Noninverting Voltage Gain Level Shift

APPLICATIONS INFORMATION

Crystal Oscillators

Figure 7 shows a crystal oscillator circuit. In the circuit, the resistors at the LT1671's positive input set a DC bias point. The 2k-0.068 μ F path sets up phase shifted feedback and the circuit looks like a wideband unity-gain follower at DC. The crystal's path provides resonant positive feedback and stable oscillation occurs.

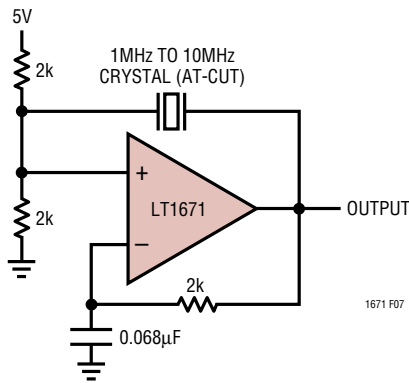


Figure 7. 1MHz to 10MHz Crystal Oscillator

Switchable Output Crystal Oscillator

Figure 8 permits crystals to be electronically switched by logic commands. This circuit is similar to the previous examples, except that oscillation is only possible when one of the logic inputs is biased high.

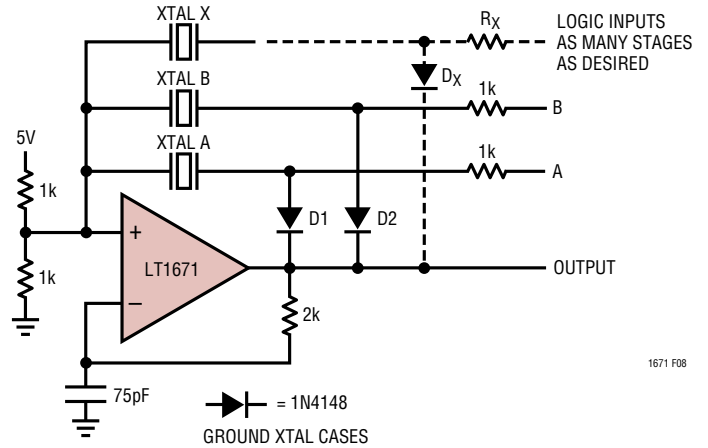
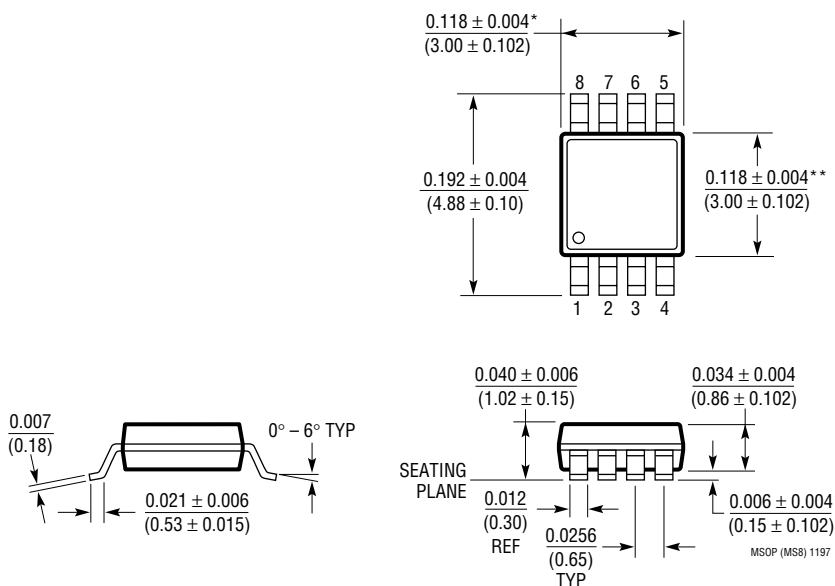


Figure 8. Switchable Output Crystal Oscillator. Biasing A or B High Places Associated Crystal in Feedback Path. Additional Crystal Branches Are Permissible

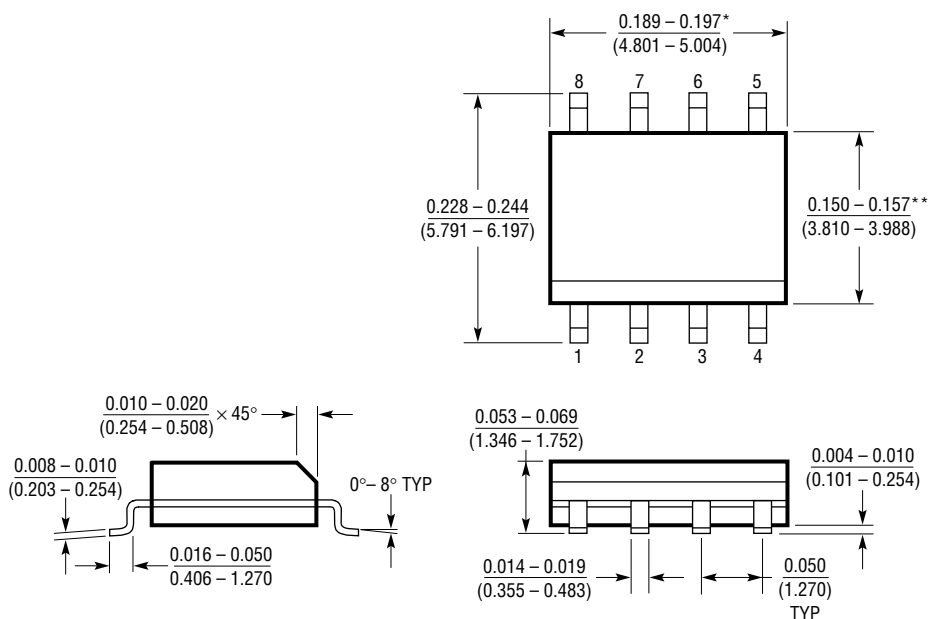
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

MS8 Package
8-Lead Plastic MSOP
 (LTC DWG # 05-08-1660)



- * DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006* (0.152mm) PER SIDE
- ** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006* (0.152mm) PER SIDE

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
 (LTC DWG # 05-08-1610)



- * DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006* (0.152mm) PER SIDE
- ** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010* (0.254mm) PER SIDE