

FEATURES

- Rail-to-Rail Input and Output
- 100% Tested Low Voltage Noise:
 $3.9\text{nV}/\sqrt{\text{Hz}}$ Typ at 1kHz
 $5.5\text{nV}/\sqrt{\text{Hz}}$ Max at 1kHz
- Single Supply Operation from 2.7V to 36V
- Offset Voltage: $100\mu\text{V}$ Max
- Low Input Bias Current: 20nA Max
- High A_{VOL} : $3\text{V}/\mu\text{V}$ Min, $R_L = 10\text{k}$
- High CMRR: 100dB Min
- High PSRR: 106dB Min
- Gain Bandwidth Product: 20MHz
- Operating Temperature Range: -40°C to 85°C
- Matching Specifications
- No Phase Inversion
- 8-Lead SO and 14-Lead SO Packages


APPLICATIONS

- Strain Gauge Amplifiers
- Portable Microphones
- Battery-Powered Rail-to-Rail Instrumentation
- Low Noise Signal Processing
- Microvolt Accuracy Threshold Detection
- Infrared Detectors

DESCRIPTION

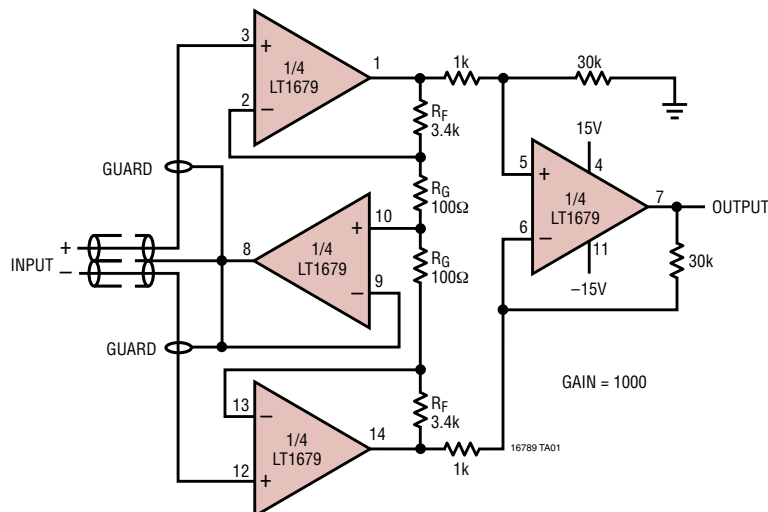
The LT[®]1678/LT1679 are dual/quad rail-to-rail op amps offering both low noise and precision: $3.9\text{nV}/\sqrt{\text{Hz}}$ wideband noise, 1/f corner frequency of 4Hz and 90nV peak-to-peak 0.1Hz to 10Hz noise are combined with outstanding precision: $100\mu\text{V}$ maximum offset voltage, greater than 100dB common mode and power supply rejection and 20MHz gain bandwidth product. The LT1678/LT1679 bring precision as well as low noise to single supply applications as low as 3V. The input range exceeds the power supply by 100mV with no phase inversion while the output can swing to within 170mV of either rail.

The LT1678/LT1679 are offered in the SO-8 and SO-14 packages. A full set of matching specifications are also provided, facilitating their use in matching dependent applications such as a two op amp instrumentation amplifier design. The LT1678/LT1679 are specified for supply voltages of $\pm 15\text{V}$, single 5V as well as single 3V. For a single amplifier with similar performance, see the LT1677 data sheet.

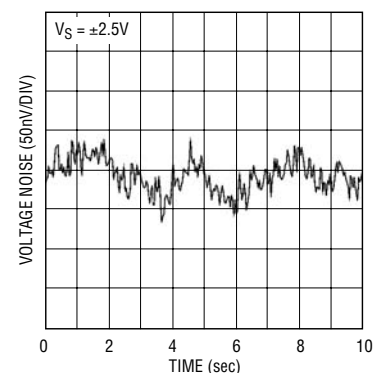
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TYPICAL APPLICATION

Instrumentation Amplifier with Shield Driver



0.1Hz to 10Hz Voltage Noise



16789 TA01b

sn16789 16789fs

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage	±18V	Lead Temperature (Soldering, 10 sec.)	300°C
Input Voltages (Note 2)	0.3V Beyond Either Rail	Operating Temperature Range	
Differential Input Current (Note 2)	±25mA	(Note 4)	-40°C to 85°C
Output Short-Circuit Duration (Note 3)	Indefinite	Specified Temperature Range	
Storage Temperature Range	-65°C to 150°C	(Note 5)	-40°C to 85°C

PACKAGE/ORDER INFORMATION

<p>S8 PACKAGE 8-LEAD PLASTIC SO T_{JMAX} = 150°C, θ_{JA} = 190°C/W</p>	ORDER PART NUMBER	<p>S PACKAGE 14-LEAD PLASTIC SO T_{JMAX} = 150°C, θ_{JA} = 160°C/W</p>	ORDER PART NUMBER
	LT1678CS8 LT1678IS8		LT1679CS LT1679IS
	S8 PART MARKING		
	1678 1678I		

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 3V, V_{CM} = V_O = 1.7V; V_S = 5V, V_{CM} = V_O = 2.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)	MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	(Note 11)		35	100	μV
		0°C ≤ T _A ≤ 70°C	●	55	270	μV
		-40°C ≤ T _A ≤ 85°C	●	75	350	μV
		V _S = 5V, V _{CM} = V _S + 0.1V		150	550	μV
		V _S = 5V, V _{CM} = V _S - 0.3V, 0°C ≤ T _A ≤ 70°C	●	180	750	μV
V _S = 5V, V _{CM} = V _S - 0.3V, -40°C ≤ T _A ≤ 85°C	●	200	1000	μV		
	Average Input Offset Drift (Note 10)	V _S = 5V, V _{CM} = -0.1V		1.5	30	mV
		V _S = 5V, V _{CM} = 0V, 0°C ≤ T _A ≤ 70°C	●	1.8	45	mV
		V _S = 5V, V _{CM} = 0V, -40°C ≤ T _A ≤ 85°C	●	2.0	50	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift (Note 10)		●	0.40	3	μV/°C
I _B	Input Bias Current	(Note 11)		±2	±20	nA
		0°C ≤ T _A ≤ 70°C	●	±3	±35	nA
		-40°C ≤ T _A ≤ 85°C	●	±7	±50	nA
		V _S = 5V, V _{CM} = V _S + 0.1V		0.19	0.40	μA
		V _S = 5V, V _{CM} = V _S - 0.3V, 0°C ≤ T _A ≤ 70°C	●	0.19	0.60	μA
V _S = 5V, V _{CM} = V _S - 0.3V, -40°C ≤ T _A ≤ 85°C	●	0.25	0.75	μA		
	Average Input Bias Current	V _S = 5V, V _{CM} = -0.1V		-5	-0.41	μA
		V _S = 5V, V _{CM} = 0V, 0°C ≤ T _A ≤ 70°C	●	-8.4	-0.45	μA
		V _S = 5V, V _{CM} = 0V, -40°C ≤ T _A ≤ 85°C	●	-10	-0.47	μA

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = 3\text{V}$, $V_{CM} = V_O = 1.7\text{V}$; $V_S = 5\text{V}$, $V_{CM} = V_O = 2.5\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)	MIN	TYP	MAX	UNITS
I_{OS}	Input Offset Current	(Note 11)		4	25	nA
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	5	35	nA
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	8	55	nA
		$V_S = 5\text{V}$, $V_{CM} = V_S + 0.1\text{V}$		6	30	nA
		$V_S = 5\text{V}$, $V_{CM} = V_S - 0.3\text{V}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	10	40	nA
	$V_S = 5\text{V}$, $V_{CM} = V_S - 0.3\text{V}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	15	65	nA	
		$V_S = 5\text{V}$, $V_{CM} = -0.1\text{V}$		0.1	1.6	μA
		$V_S = 5\text{V}$, $V_{CM} = 0\text{V}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	0.1	2.0	μA
		$V_S = 5\text{V}$, $V_{CM} = 0\text{V}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	0.15	2.4	μA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 7)		90		nV _{p-p}
		$V_{CM} = V_S$ $V_{CM} = 0\text{V}$		180 1600		nV _{p-p} nV _{p-p}
	Input Noise Voltage Density (Note 8)	$f_0 = 10\text{Hz}$		4.4		nV/ $\sqrt{\text{Hz}}$
		$V_{CM} = V_S$, $f_0 = 10\text{Hz}$		6.6		nV/ $\sqrt{\text{Hz}}$
		$V_{CM} = 0\text{V}$, $f_0 = 10\text{Hz}$		19		nV/ $\sqrt{\text{Hz}}$
		$f_0 = 1\text{kHz}$		3.9	5.5	nV/ $\sqrt{\text{Hz}}$
		$V_{CM} = V_S$, $f_0 = 1\text{kHz}$		5.3		nV/ $\sqrt{\text{Hz}}$
		$V_{CM} = 0\text{V}$, $f_0 = 1\text{kHz}$		9		nV/ $\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f_0 = 10\text{Hz}$		1.2		pA/ $\sqrt{\text{Hz}}$
		$f_0 = 1\text{kHz}$		0.3		pA/ $\sqrt{\text{Hz}}$
V_{CM}	Input Voltage Range		-0.1		$V_S + 0.1\text{V}$	V
			0		$V_S - 0.3\text{V}$	V
R_{IN}	Input Resistance	Common Mode		2		G Ω
C_{IN}	Input Capacitance			4.2		pF
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}$, $V_{CM} = 1.9\text{V}$ to 3.9V		98	120	dB
		$V_S = 5\text{V}$, $V_{CM} = 1.9\text{V}$ to 3.9V	●	92	120	dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.7\text{V}$ to 36V , $V_{CM} = V_O = 1.7\text{V}$		100	125	dB
		$V_S = 3.1\text{V}$ to 36V , $V_{CM} = V_O = 1.7\text{V}$	●	98	120	dB
A_{VOL}	Large-Signal Voltage Gain	$V_S = 3\text{V}$, $R_L = 10\text{k}$, $V_O = 2.5\text{V}$ to 0.7V		0.6	3	V/ μV
			●	0.3	2	V/ μV
		$V_S = 3\text{V}$, $R_L = 2\text{k}$, $V_O = 2.2\text{V}$ to 0.7V		0.5	3	V/ μV
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	0.4	0.9	V/ μV
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	0.4	0.8	V/ μV
		$V_S = 3\text{V}$, $R_L = 600\Omega$, $V_O = 2.2\text{V}$ to 0.7V		0.20	0.43	V/ μV
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	0.15	0.40	V/ μV
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	0.10	0.35	V/ μV
		$V_S = 5\text{V}$, $R_L = 10\text{k}$, $V_O = 4.5\text{V}$ to 0.7V		1	3.8	V/ μV
		$0^\circ\text{C} < T_A < 70^\circ\text{C}$	●	0.6	2	V/ μV
		$-40 < T_A < 85^\circ\text{C}$	●	0.3	2	V/ μV
		$V_S = 5\text{V}$, $R_L = 2\text{k}$, $V_O = 4.2\text{V}$ to 0.7V		0.7	3.5	V/ μV
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	0.6	3.2	V/ μV
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	0.5	3.0	V/ μV
		$V_S = 5\text{V}$, $R_L = 600\Omega$, $V_O = 4.2\text{V}$ to 0.7V		0.6	3.0	V/ μV
	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	0.5	2.8	V/ μV	
	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	0.4	2.5	V/ μV	
V_{OL}	Output Voltage Swing Low (Note 11)	Above GND				
		$I_{SINK} = 0.1\text{mA}$		80	170	mV
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	125	200	mV
	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	130	250	mV	

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = 3\text{V}$, $V_{CM} = V_O = 1.7\text{V}$; $V_S = 5\text{V}$, $V_{CM} = V_O = 2.5\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)	MIN	TYP	MAX	UNITS
V_{OL}	Output Voltage Swing Low (Note 11)	Above GND $I_{SINK} = 2.5\text{mA}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	170	250	mV
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	195	320	mV
		Above GND $I_{SINK} = 10\text{mA}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	205	350	mV
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	370	600	mV
V_{OH}	Output Voltage Swing High (Note 11)	Below V_S $I_{SOURCE} = 0.1\text{mA}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	75	150	mV
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	85	200	mV
		Below V_S $I_{SOURCE} = 2.5\text{mA}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	93	250	mV
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	110	250	mV
		Below V_S $I_{SOURCE} = 10\text{mA}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	195	350	mV
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	205	375	mV
I_{SC}	Output Short-Circuit Current (Note 3)	$V_S = 3\text{V}$	●	15	22	mA
				13	19	mA
		$V_S = 5\text{V}$	●	18	29	mA
			14	25	mA	
SR	Slew Rate (Note 13)	$A_V = -1$, $R_L = 10\text{k}$	●	4	6	V/ μs
		$R_L = 10\text{k}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	3.5	5.8	V/ μs
		$R_L = 10\text{k}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	3	5.5	V/ μs
GBW	Gain Bandwidth Product (Note 11)	$f_0 = 100\text{kHz}$	●	13	20	MHz
		$f_0 = 100\text{kHz}$	●	12.5	19	MHz
t_S	Settling Time	2V Step 0.1%, $A_V = +1$		1.4		μs
		2V Step 0.01%, $A_V = +1$		2.4		μs
R_O	Open-Loop Output Resistance Closed-Loop Output Resistance	$I_{OUT} = 0$		100		Ω
		$A_V = 100$, $f = 10\text{kHz}$		1		Ω
I_S	Supply Current per Amplifier (Note 12)		●	2	3.4	mA
				2.5	3.8	mA
ΔV_{OS}	Offset Voltage Match (Notes 11, 15)	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	35	150	μV
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	55	400	μV
			●	75	525	μV
ΔI_{B+}	Noninverting Bias Current Match (Notes 11, 15)	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	± 2	± 30	nA
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	± 3	± 55	nA
			●	± 7	± 75	nA
ΔCMRR	Common Mode Rejection Match (Notes 11, 14, 15)	$V_S = 5\text{V}$, $V_{CM} = 1.9\text{V}$ to 3.9V	●	94	110	dB
				88	110	dB
ΔPSRR	Power Supply Rejection Match (Notes 11, 14, 15)	$V_S = 2.7\text{V}$ to 36V , $V_{CM} = V_O = 1.7\text{V}$	●	96	120	dB
		$V_S = 3.1\text{V}$ to 36V , $V_{CM} = V_O = 1.7\text{V}$	●	94	120	dB

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = V_O = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	20	150	μV
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	30	350	μV
				45	420	μV
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Input Offset Drift (Note 10)		●	0.40	3	$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	± 2	± 20	nA
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	± 3	± 35	nA
				± 7	± 50	nA
I_{OS}	Input Offset Current	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	3	25	nA
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	5	35	nA
				8	55	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 7)		90		nV _{p-p}
		$V_{CM} = 15\text{V}$		180		nV _{p-p}
		$V_{CM} = -15\text{V}$		1600		nV _{p-p}
	Input Noise Voltage Density	$f_0 = 10\text{Hz}$		4.4		nV $\sqrt{\text{Hz}}$
		$V_{CM} = 15\text{V}, f_0 = 10\text{Hz}$		6.6		nV $\sqrt{\text{Hz}}$
		$V_{CM} = -15\text{V}, f_0 = 10\text{Hz}$		19		nV $\sqrt{\text{Hz}}$
		$f_0 = 1\text{kHz}$		3.9	5.5	nV $\sqrt{\text{Hz}}$
		$V_{CM} = 15\text{V}, f_0 = 1\text{kHz}$		5.3		nV $\sqrt{\text{Hz}}$
		$V_{CM} = -15\text{V}, f_0 = 1\text{kHz}$		9		nV $\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f_0 = 10\text{Hz}$		1.2		pA $\sqrt{\text{Hz}}$
		$f_0 = 1\text{kHz}$		0.3		pA $\sqrt{\text{Hz}}$
V_{CM}	Input Voltage Range (Note 16)		●	-13.3	14	V
R_{IN}	Input Resistance	Common Mode		2		G Ω
C_{IN}	Input Capacitance			4.2		pF
CMRR	Common Mode Rejection Ratio	$V_{CM} = -13.3\text{V}$ to 14V	●	100	130	dB
				96	124	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.7\text{V}$ to $\pm 18\text{V}$	●	106	130	dB
				100	125	dB
A_{VOL}	Large-Signal Voltage Gain	$R_L = 10\text{k}, V_O = \pm 14\text{V}$		3	7	V/ μV
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	2	6	V/ μV
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	1	4	V/ μV
		$R_L = 2\text{k}, V_O = \pm 13.5\text{V}$		0.8	1.7	V/ μV
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	0.5	1.4	V/ μV
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	0.4	1.1	V/ μV

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = V_O = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)	MIN	TYP	MAX	UNITS
V_{OL}	Output Voltage Swing Low	Above $-V_S$ $I_{SINK} = 0.1\text{mA}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	110	200	mV
			●	125	230	mV
			●	130	260	mV
		Above $-V_S$ $I_{SINK} = 2.5\text{mA}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	170	280	mV
			●	195	350	mV
			●	205	380	mV
		Above $-V_S$ $I_{SINK} = 10\text{mA}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	370	600	mV
			●	440	700	mV
			●	450	750	mV
V_{OH}	Output Voltage Swing High	Below $+V_S$ $I_{SOURCE} = 0.1\text{mA}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	80	150	mV
			●	90	200	mV
			●	100	250	mV
		Below $+V_S$ $I_{SOURCE} = 2.5\text{mA}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	110	200	mV
			●	120	300	mV
			●	120	350	mV
		Below $+V_S$ $I_{SOURCE} = 10\text{mA}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	200	450	mV
			●	250	500	mV
			●	250	550	mV
I_{SC}	Output Short-Circuit Current (Note 3)		●	20	35	mA
			●	15	28	mA
SR	Slew Rate	$R_L = 10\text{k}$ (Note 9)	●	4	6	V/ μs
		$R_L = 10\text{k}$ (Note 9) $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	3.5	5.8	V/ μs
		$R_L = 10\text{k}$ (Note 9) $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	3	5.5	V/ μs
GBW	Gain Bandwidth Product	$f_0 = 100\text{kHz}$	●	13	20	MHz
		$f_0 = 100\text{kHz}$	●	12.5	19	MHz
THD	Total Harmonic Distortion	$R_L = 2\text{k}$, $A_V = 1$, $f_0 = 1\text{kHz}$, $V_O = 20\text{V}_{P-P}$		0.00025		%
t_S	Settling Time	10V Step 0.1%, $A_V = +1$		2.7		μs
		10V Step 0.01%, $A_V = +1$		3.9		μs
R_O	Open-Loop Output Resistance	$I_{OUT} = 0$		100		Ω
	Closed-Loop Output Resistance	$A_V = 100$, $f = 10\text{kHz}$		1		Ω
I_S	Supply Current per Amplifier		●	2.5	3.5	mA
			●	3	4.5	mA
	Channel Separation	$f = 10\text{Hz}$, $V_O = \pm 10\text{V}$, $R_L = 10\text{k}$		132		dB
ΔV_{OS}	Offset Voltage Match (Note 15)	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	5	225	μV
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	30	525	μV
			●	45	630	μV
ΔI_{B+}	Noninverting Bias Current Match (Note 15)	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	± 2	± 30	nA
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	± 3	± 55	nA
			●	± 7	± 75	nA
ΔCMRR	Common Mode Rejection Match (Notes 14, 15)	$V_{CM} = -13.3\text{V}$ to 14V	●	96	120	dB
			●	92	115	dB
ΔPSRR	Power Supply Rejection Match (Notes 14, 15)	$V_S = \pm 1.7\text{V}$ to $\pm 18\text{V}$	●	100	123	dB
			●	96	120	dB

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds $\pm 1.4V$, the input current should be limited to 25mA. If the common mode range exceeds either rail, the input current should be limited to 10mA.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum.

Note 4: The LT1678C/LT1679C and LT1678I/LT1679I are guaranteed functional over the Operating Temperature Range of $-40^{\circ}C$ to $85^{\circ}C$.

Note 5: The LT1678C/LT1679C are guaranteed to meet specified performance from $0^{\circ}C$ to $70^{\circ}C$. The LT1678C/LT1679C are designed, characterized and expected to meet specified performance from $-40^{\circ}C$ to $85^{\circ}C$ but is not tested or QA sampled at these temperatures. The LT1678I/LT1679I are guaranteed to meet specified performance from $-40^{\circ}C$ to $85^{\circ}C$.

Note 6: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifier; i.e., out of 100 LT1678/LT1679s, typically 60 op amps will be better than the indicated specification.

Note 7: See the test circuit and frequency response curve for 0.1Hz to 10Hz tester in the Applications Information section.

Note 8: Noise is 100% tested at $\pm 15V$ supplies.

Note 9: Slew rate is measured in $A_V = -1$; input signal is $\pm 10V$, output measured at $\pm 5V$.

Note 10: This parameter is not 100% tested.

Note 11: $V_S = 5V$ limits are guaranteed by correlation to $V_S = 3V$ and $V_S = \pm 15V$ tests.

Note 12: $V_S = 3V$ limits are guaranteed by correlation to $V_S = 5V$ and $V_S = \pm 15V$ tests.

Note 13: Guaranteed by correlation to slew rate at $V_S = \pm 15V$ and GBW at $V_S = 3V$ and $V_S = \pm 15V$ tests.

Note 14: $\Delta CMRR$ and $\Delta PSRR$ are defined as follows:

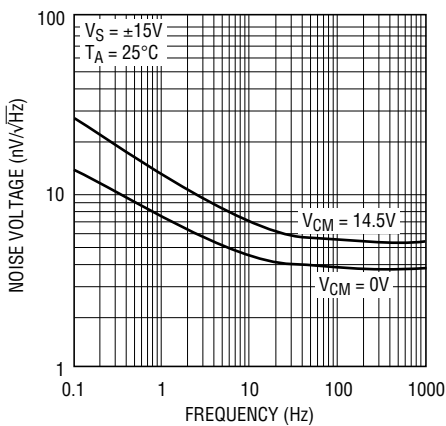
1. CMRR and PSRR are measured in $\mu V/V$ on the individual amplifiers.
2. The difference is calculated between the matching sides in $\mu V/V$.
3. The result is converted to dB.

Note 15: Matching parameters are the difference between amplifiers A and B on the LT1678 and between amplifiers A and D and B and C in the LT1679.

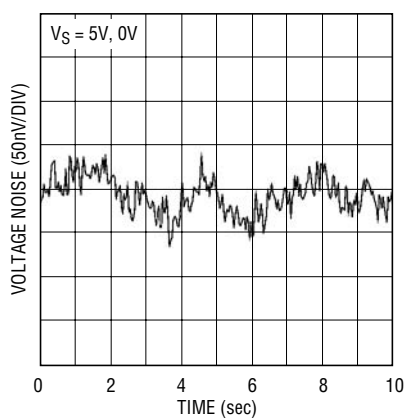
Note 16: Input range guaranteed by the common mode rejection ratio test.

TYPICAL PERFORMANCE CHARACTERISTICS

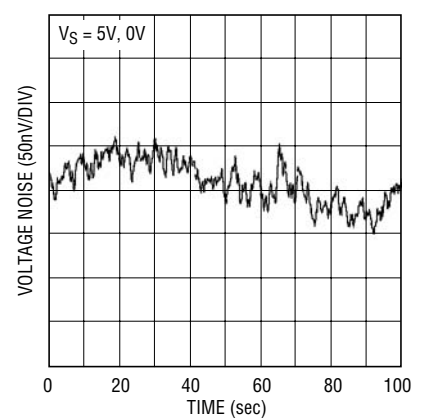
Voltage Noise vs Frequency



0.1Hz to 10Hz Voltage Noise

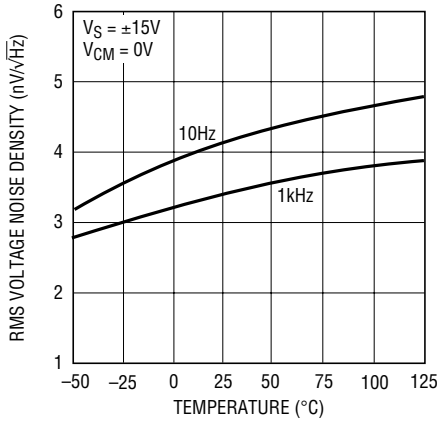


0.01Hz to 1Hz Voltage Noise

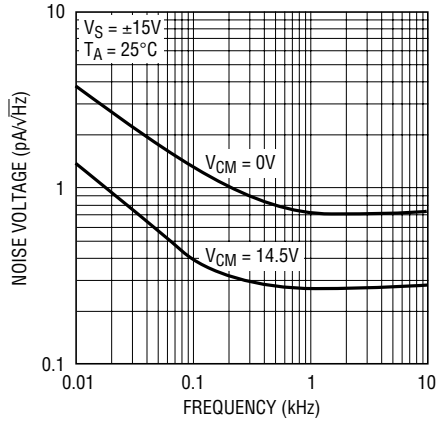


TYPICAL PERFORMANCE CHARACTERISTICS

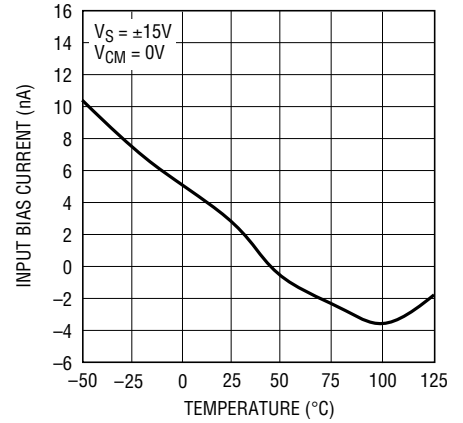
Voltage Noise vs Temperature



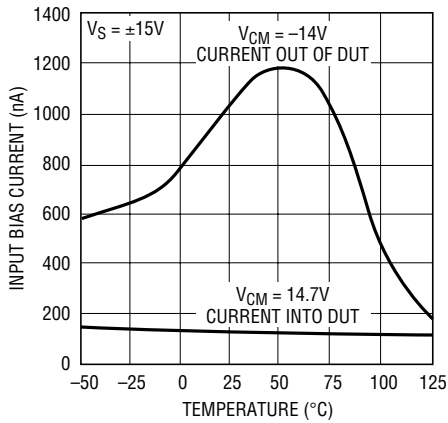
Current Noise vs Frequency



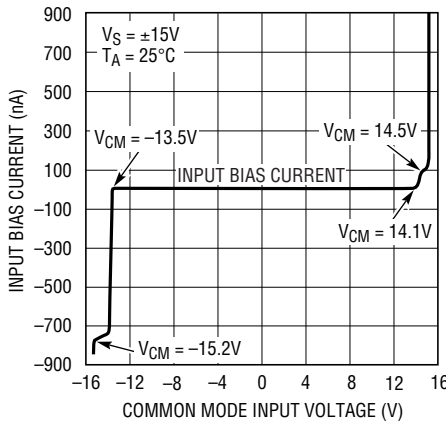
Input Bias Current vs Temperature



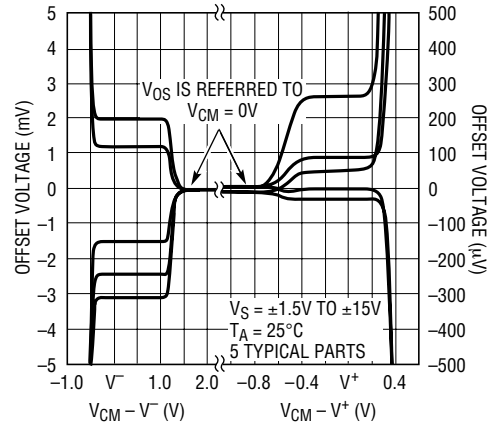
Input Bias Current vs Temperature



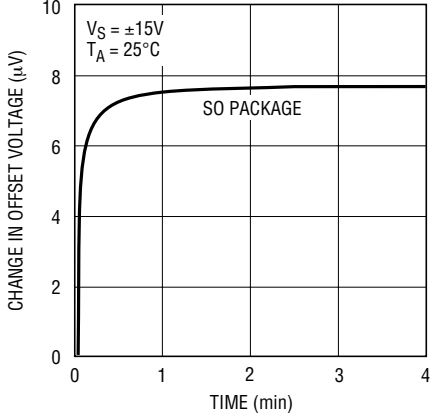
Input Bias Current Over the Common Mode Range



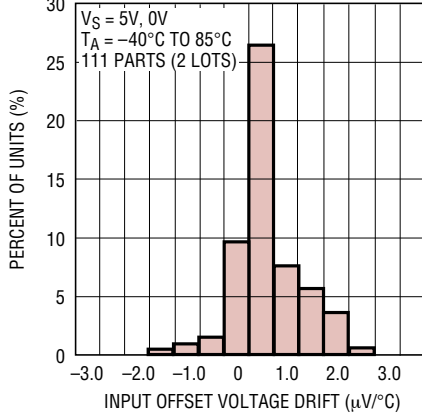
Offset Voltage Shift vs Common Mode



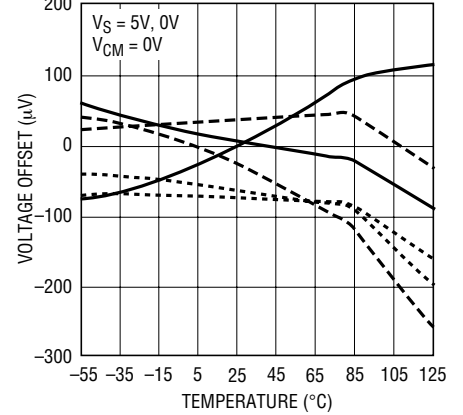
Warm-Up Drift vs Time



Distribution of Input Offset Voltage Drift (SO-8)

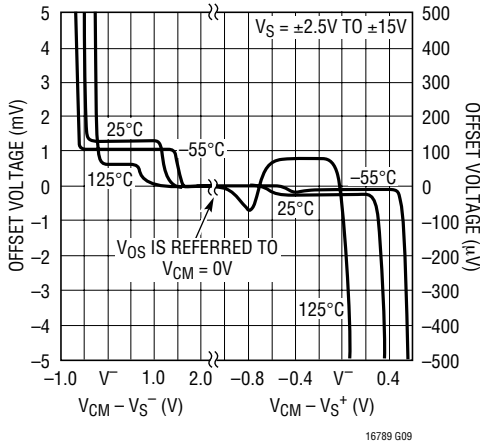


VS vs Temperature of Representative Units

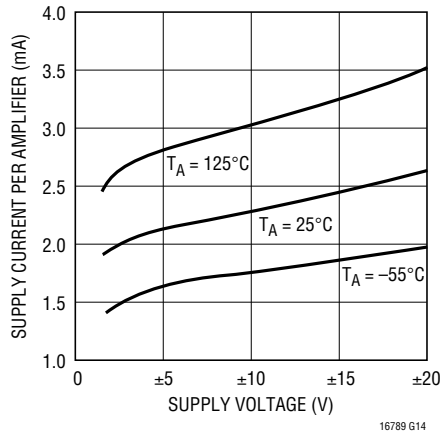


TYPICAL PERFORMANCE CHARACTERISTICS

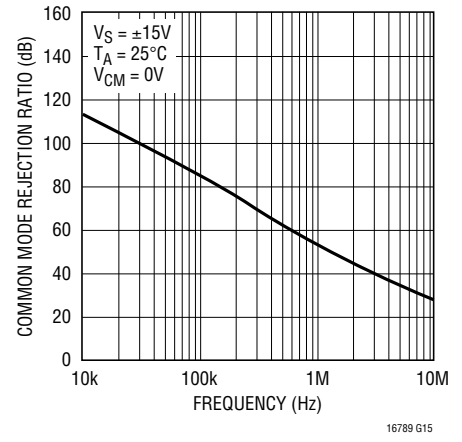
Common Mode Range vs Temperature



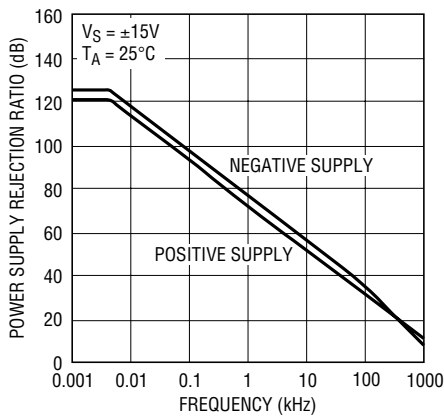
Supply Current vs Supply Voltage



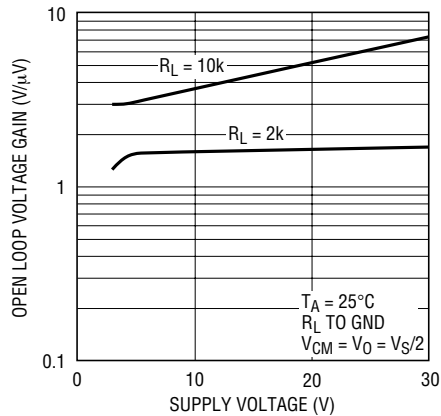
Common Mode Rejection Ratio vs Frequency



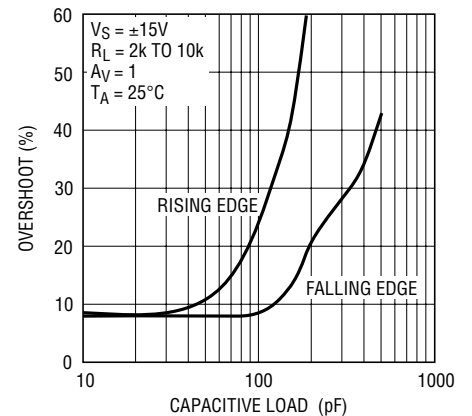
Power Supply Rejection Ratio vs Frequency



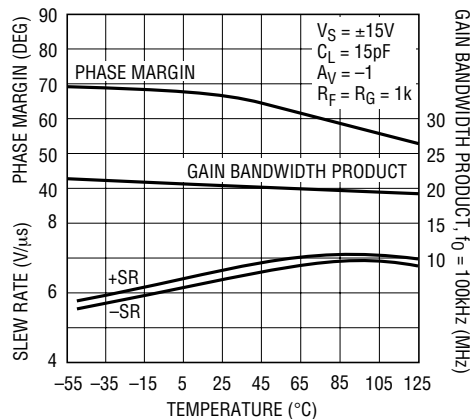
Voltage Gain vs Supply Voltage



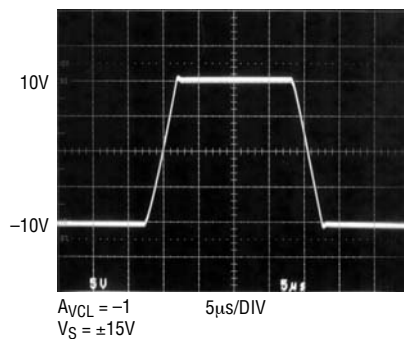
% Overshoot vs Capacitive Load



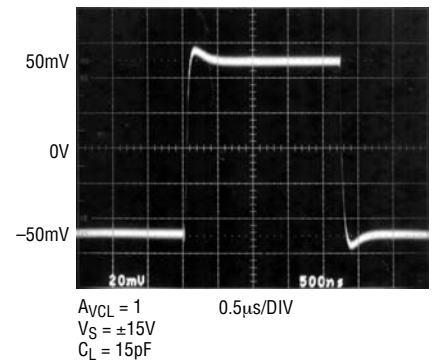
Phase Margin, Gain Bandwidth Product and Slew Rate vs Temperature



Large Signal Transient Response

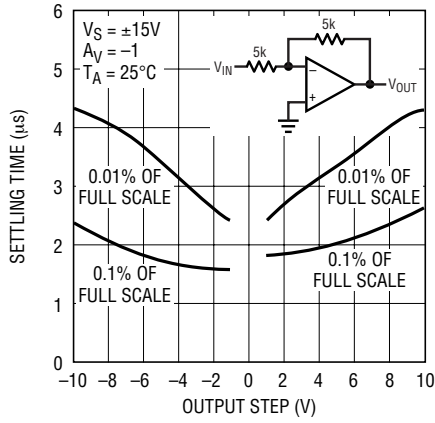


Small Signal Transient Response



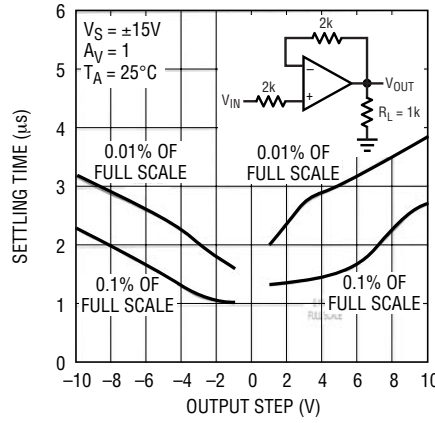
TYPICAL PERFORMANCE CHARACTERISTICS

Settling Time vs Output Step (Inverting)



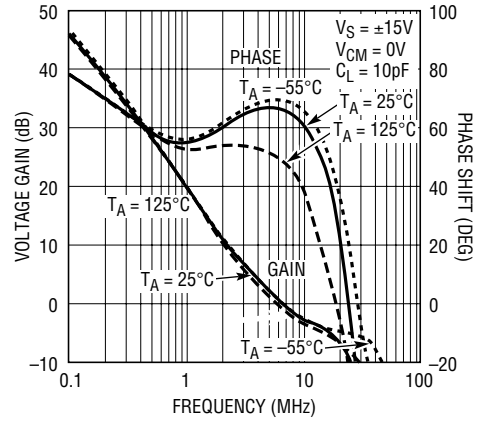
16789 G22

Settling Time vs Output Step (Noninverting)



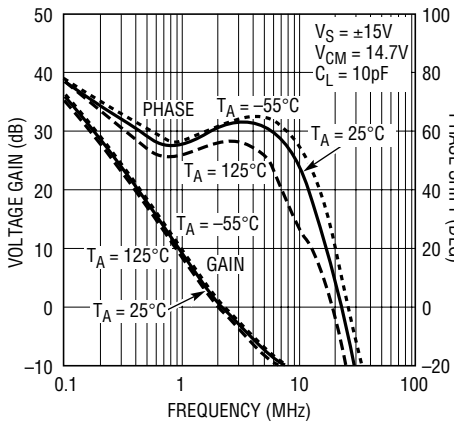
16789 G23

Gain, Phase Shift vs Frequency



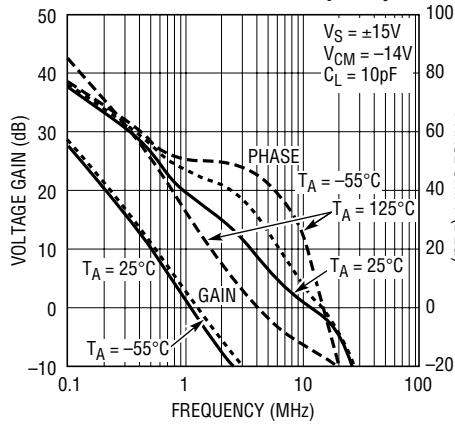
16789 G24

Gain, Phase Shift vs Frequency



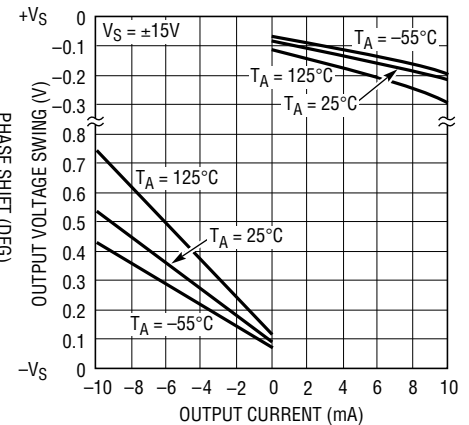
16789 G25

Gain, Phase Shift vs Frequency



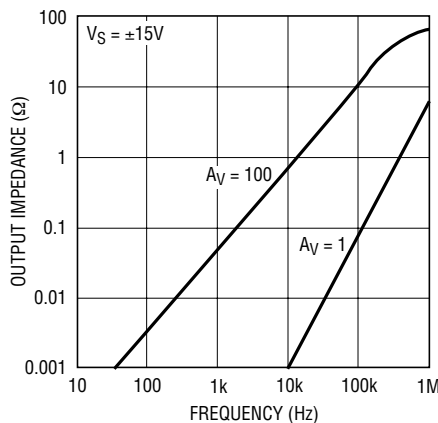
16789 G26

Output Voltage Swing vs Load Current



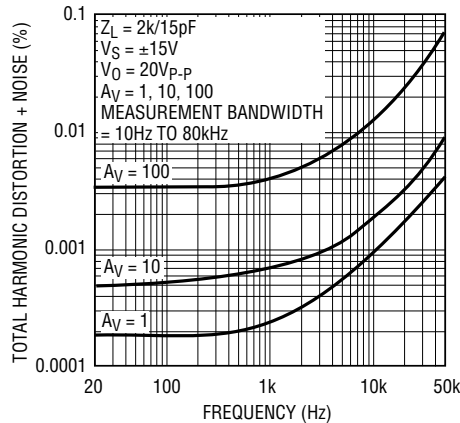
16789 G27

Closed-Loop Output Impedance vs Frequency



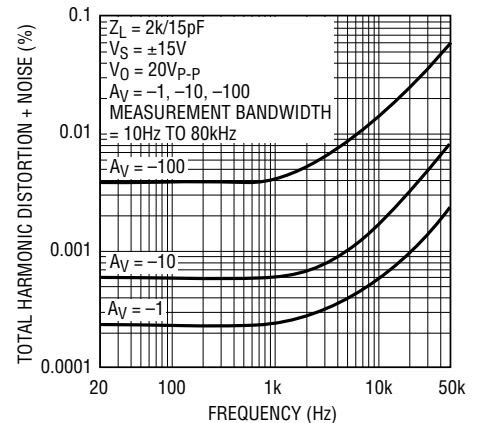
16789 G28

Total Harmonic Distortion and Noise vs Frequency for Noninverting Gain



16789 G29

Total Harmonic Distortion and Noise vs Frequency for Inverting Gain



16789 G30

APPLICATIONS INFORMATION

Rail-to-Rail Operation

To take full advantage of an input range that can exceed the supply, the LT1678/LT1679 are designed to eliminate phase reversal. Referring to the photographs shown in Figure 1, the LT1678/LT1679 are operating in the follower mode ($A_V = +1$) at a single 3V supply. The output of the LT1678/LT1679 clips cleanly and recovers with no phase reversal. This has the benefit of preventing lock-up in servo systems and minimizing distortion components.

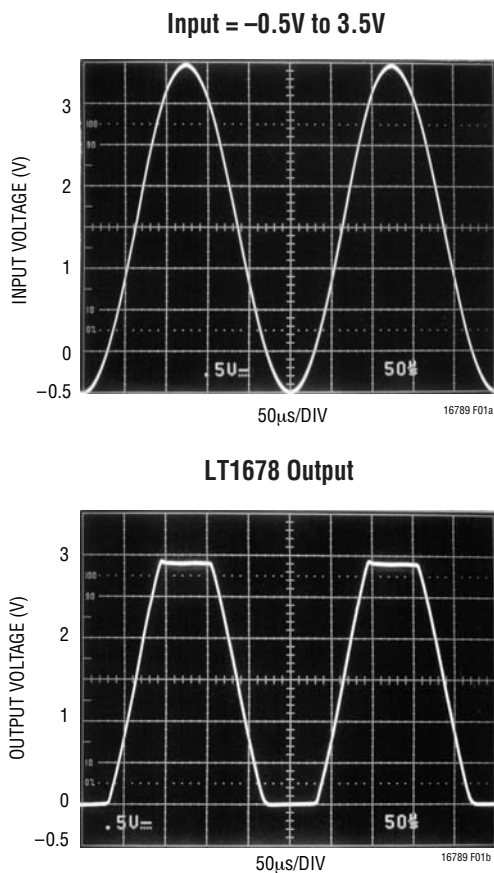


Figure 1. Voltage Follower with Input Exceeding the Supply Voltage ($V_S = 3V$)

Unity-Gain Buffer Application

When $R_F \leq 100\Omega$ and the input is driven with a fast, large-signal pulse ($>1V$), the output waveform will look as shown in the pulsed operation diagram (Figure 2).

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the

input and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_F \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V) and the amplifier stays in its active mode and a smooth transition will occur.

As with all operational amplifiers when $R_F > 2k$, a pole will be created with R_F and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20pF to 50pF) in parallel with R_F will eliminate this problem.

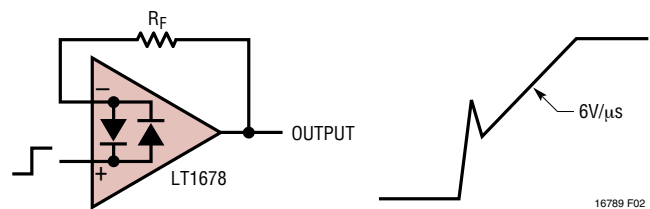


Figure 2. Pulsed Operation

Noise Testing

The 0.1Hz to 10Hz peak-to-peak noise of the LT1678/LT1679 are measured in the test circuit shown (Figure 3). The frequency response of this noise tester (Figure 4) indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed ten seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 90nV peak-to-peak noise performance of the LT1678/LT1679 requires special test precautions:

1. The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically $3\mu V$ due to its chip temperature increasing $10^\circ C$ to $20^\circ C$ from the moment the power supplies are turned on. In the ten-second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.
2. For similar reasons, the device must be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.

APPLICATIONS INFORMATION

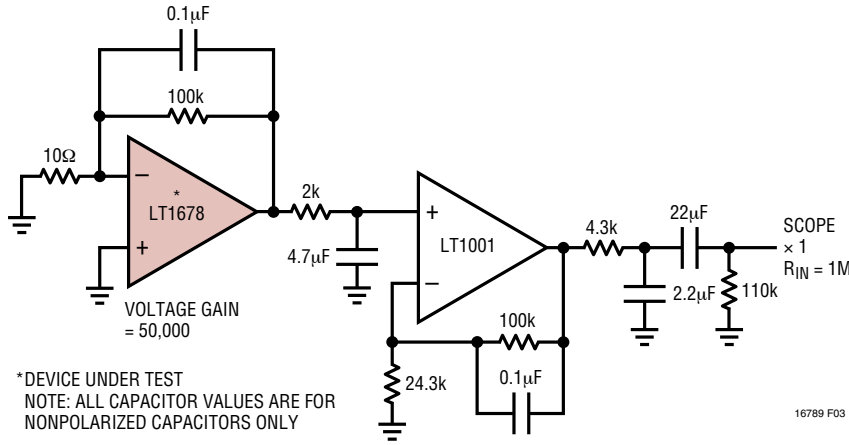


Figure 3. 0.1Hz to 10Hz Noise Test Circuit

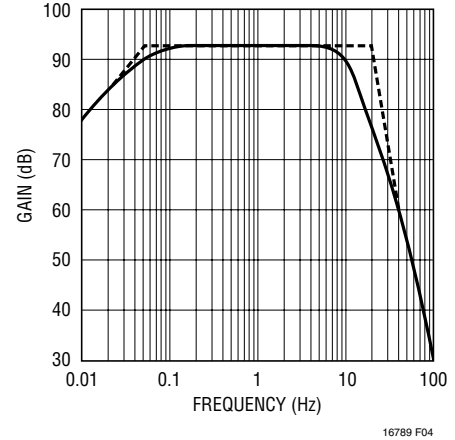


Figure 4. 0.1Hz to 10Hz Peak-to-Peak Noise Tester Frequency Response

3. Sudden motion in the vicinity of the device can also “feedthrough” to increase the observed noise.

Current noise is measured in the circuit shown in Figure 5 and calculated by the following formula:

$$i_n = \frac{\left[(e_{no})^2 - (130\text{nV} \cdot 101)^2 \right]^{1/2}}{(1\text{M}\Omega)(101)}$$

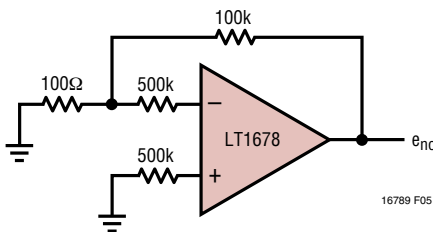


Figure 5.

The LT1678/LT1679 achieve their low noise, in part, by operating the input stage at 100μA versus the typical 10μA of most other op amps. Voltage noise is inversely proportional while current noise is directly proportional to the square root of the input stage current. Therefore, the LT1678/LT1679’s current noise will be relatively high. At low frequencies, the low 1/f current noise corner frequency (≈ 200Hz) minimizes current noise to some extent.

In most practical applications, however, current noise will not limit system performance. This is illustrated in the Total Noise vs Source Resistance plot (Figure 6) where:

$$\text{Total Noise} = \left[(\text{op amp voltage noise})^2 + (\text{resistor noise})^2 + (\text{current noise } R_S)^2 \right]^{1/2}$$

Three regions can be identified as a function of source resistance:

- (i) $R_S \leq 400\Omega$. Voltage noise dominates
- (ii) $400\Omega \leq R_S \leq 50\text{k}$ at 1kHz } Resistor Noise Dominates
- $400\Omega \leq R_S \leq 8\text{k}$ at 10Hz } Dominates
- (iii) $R_S > 50\text{k}$ at 1kHz } Current Noise Dominates
- $R_S > 8\text{k}$ at 10Hz } Dominates

Clearly the LT1678/LT1679 should not be used in region (iii), where total system noise is at least six times higher than the voltage noise of the op amp, i.e., the low voltage noise specification is completely wasted. In this region the LT1113 or LT1169 are better choices.

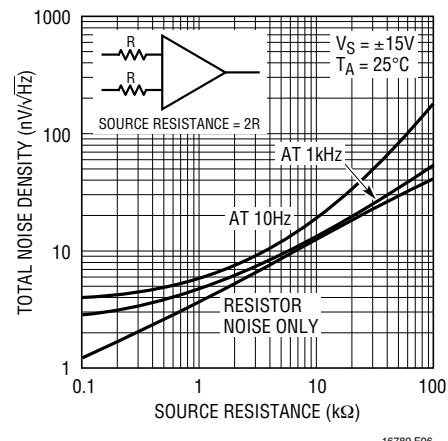


Figure 6. Total Noise vs Source Resistance

APPLICATIONS INFORMATION

Rail-to-Rail Input

The input common mode range for the LT1678/LT1679 can exceed the supplies by at least 100mV. As the common mode voltage approaches the positive rail ($+V_S - 0.7V$), the tail current for the input pair (Q1, Q2) is reduced, which prevents the input pair from saturating (refer to the Simplified Schematic). The voltage drop across the load resistors R_{C1} , R_{C2} is reduced to less than 200mV, degrading the slew rate, bandwidth, voltage noise, offset voltage and input bias current (the cancellation is shut off).

When the input common mode range goes below 1.5V above the negative rail, the NPN input pair (Q1, Q2) shuts off and the PNP input pair (Q8, Q9) turns on. The offset voltage, input bias current, voltage noise and bandwidth are also degraded. The graph of Offset Voltage Shift vs Common Mode shows where the knees occur by displaying the change in offset voltage. The change-over points are temperature dependent; see the graph Common Mode Range vs Temperature.

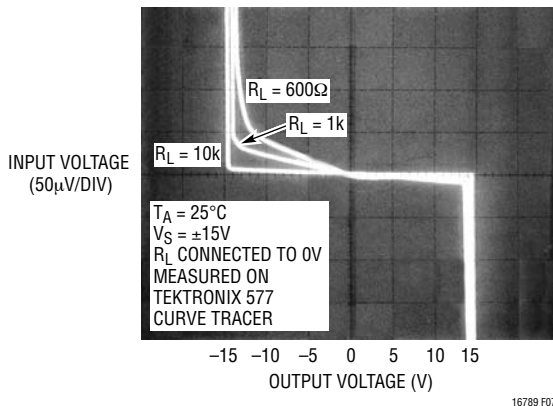


Figure 7. Voltage Gain Split Supply

Rail-to-Rail Output

The rail-to-rail output swing is achieved by using transistor collectors (Q28, Q29 referring to the Simplified Schematic) instead of customary class A-B emitter followers for the output stage. The output NPN transistor (Q29) sinks the current necessary to move the output in the negative direction. The change in Q29's base emitter voltage is reflected directly to the gain node (collectors of Q20 and Q16). For large sinking currents, the delta V_{BE} of Q29 can dominate the gain. Figure 7 shows the change in input voltage for a change in output voltage for different load resistors connected between the supplies. The gain is much higher for output voltages above ground (Q28 sources current) since the change in base emitter voltage of Q28 is attenuated by the gain in the PNP portion of the output stage. Therefore, for positive output swings (output sourcing current) there is hardly any change in input voltage for any load resistance. Highest gain and best linearity are achieved when the output is sourcing current, which is the case in single supply operation when the load is ground referenced. Figure 8 shows gains for both sinking and sourcing load currents for a worst-case load of 600Ω.

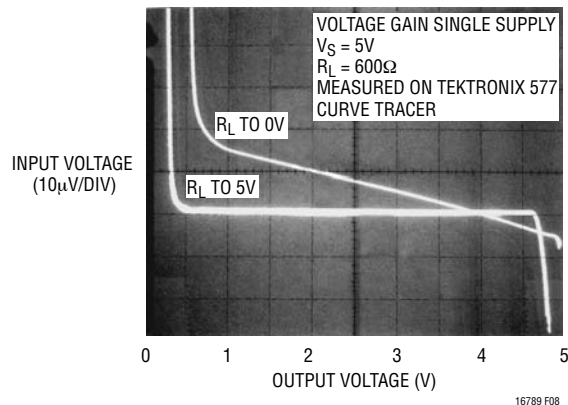
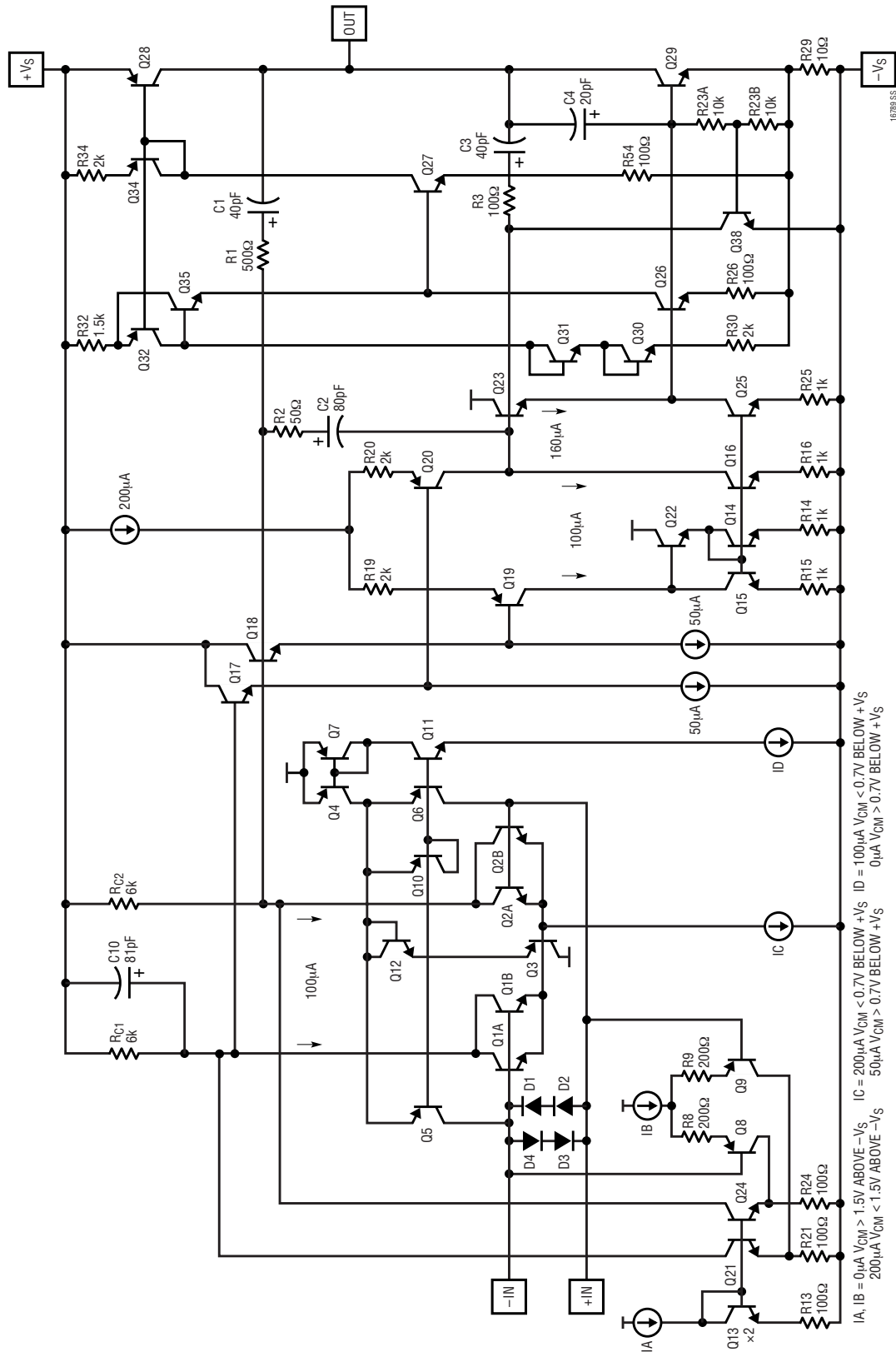


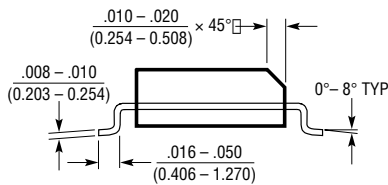
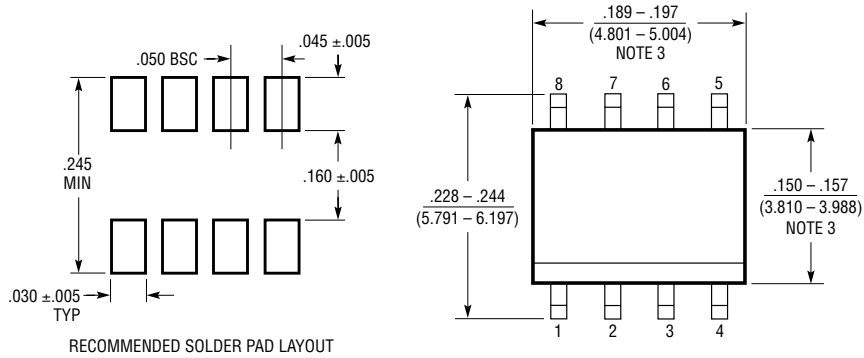
Figure 8. Voltage Gain Single Supply

SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

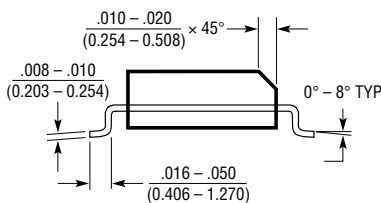
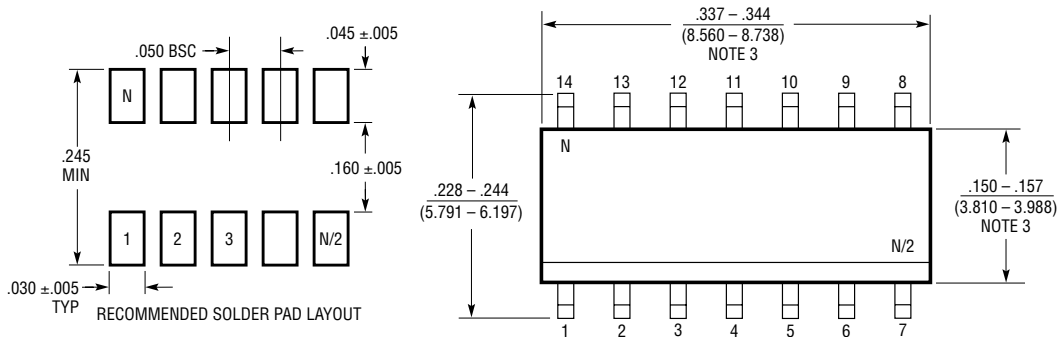
S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



- NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
 2. DRAWING NOT TO SCALE
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED $.006''$ (0.15mm)

S08 0303

S Package 14-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



- NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
 2. DRAWING NOT TO SCALE
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED $.006''$ (0.15mm)

S14 0502

sn16789 16789fs