Single/Dual, 7ns, Low Power, 3V/5V/±5V Rail-to-Rail Comparators

FEATURES

- **Ultrafast: 7ns at 20mV Overdrive**
  8.5ns at 5mV Overdrive
- **Rail-to-Rail Inputs**
- **Rail-to-Rail Complementary Outputs (TTL/CMOS Compatible)**
- **Specified at 2.7V, 5V and ±5V Supplies**
- Low Power (Per Comparator): 5mA
- Output Latch
- Inputs Can Exceed Supplies Without Phase Reversal
- LT1713: 8-Lead MSOP Package
- LT1714: 16-Lead Narrow SSOP Package

APPLICATIONS

- High Speed Automatic Test Equipment
- Current Sense for Switching Regulators
- Crystal Oscillator Circuits
- High Speed Sampling Circuits
- High Speed A/D Converters
- Pulse Width Modulators
- Window Comparators
- Extended Range V/F Converters
- Fast Pulse Height/Width Discriminators
- Line Receivers
- High Speed Triggers

DESCRIPTION

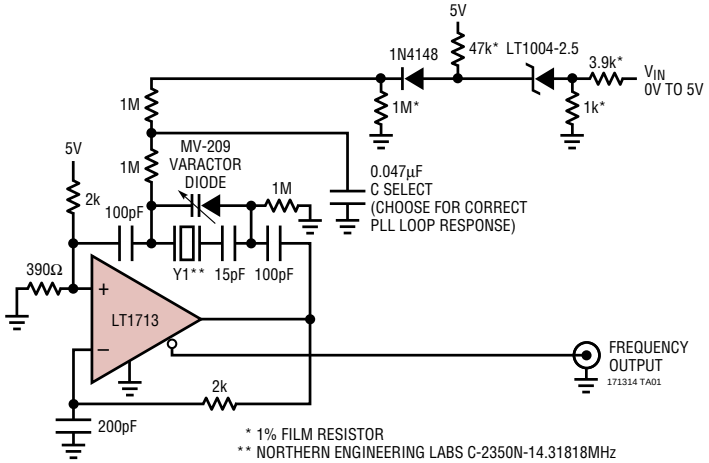
The LT®1713/LT1714 are UltraFast™ 7ns, single/dual comparators featuring rail-to-rail inputs, rail-to-rail complementary outputs and an output latch. Optimized for 3V and 5V power supplies, they operate over a single supply voltage range from 2.4V to 12V or from ±2.4V to ±6V dual supplies.

The LT1713/LT1714 are designed for ease of use in a variety of systems. In addition to wide supply voltage flexibility, rail-to-rail input common mode range extends 100mV beyond both supply rails and the outputs are protected against phase reversal for inputs extending further beyond the rails. Also, the rail-to-rail inputs may be taken to opposite rails with no significant increase in input current. The rail-to-rail matched complementary outputs interface directly to TTL or CMOS logic and can sink 10mA to within 0.5V of GND or source 10mA to within 0.7V of V^+.

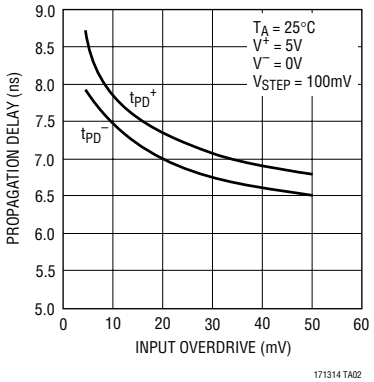
The LT1713/LT1714 have internal TTL/CMOS compatible latches for retaining data at the outputs. Each latch holds data as long as its latch pin is held high. Latch pin hysteresis provides protection against slow moving or noisy latch signals. The LT1713 is available in the 8-lead MSOP package. The LT1714 is available in the 16-lead narrow SSOP package.

TYPICAL APPLICATION

A 4× NTSC Subcarrier Voltage-Tunable Crystal Oscillator



LT1713/LT1714 Propagation Delay vs Input Overdrive

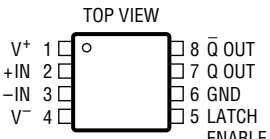


ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage
- V^+ to V^- 12.6V
- V^+ to GND 12.6V
- V^- to GND ..... –10V to 0.3V

Differential Input Voltage ..... ±12.6V
Latch Pin Voltage 7V
Input and Latch Current ..... ±10mA
Output Current (Continuous) ..... ±20mA
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range (Note 2) ... –40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

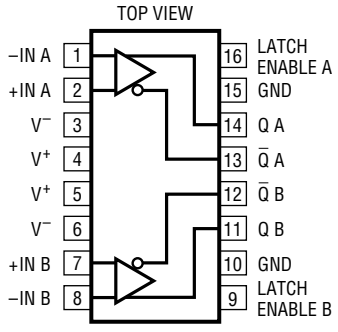
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 250°C/W

ORDER PART NUMBER
LT1713CMS8 LT1713IMS8
MS8 PART MARKING
LTRD LTUK



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 120°C/W

ORDER PART NUMBER
LT1714CGN LT1714IGN
GN PART MARKING
1714 1714I

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 2.7V or V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_{LATCH} = 0.8V, C_{LOAD} = 10pF, $V_{OVERDRIVE}$ = 20mV, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V^+	Positive Supply Voltage Range		●	2.4		7	V
V_{OS}	Input Offset Voltage (Note 4)	R_S = 50Ω, V_{CM} = V^+/2			0.5	4	mV
		R_S = 50Ω, V_{CM} = V^+/2 (Note 11)	●			5	mV
		R_S = 50Ω, V_{CM} = 0V			0.7		mV
		R_S = 50Ω, V_{CM} = V^+			1		mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift		●		5		µV/°C
I_{OS}	Input Offset Current				0.1	1	µA
			●			2	µA
I_B	Input Bias Current (Note 5)			–7	–1.5	2	µA
			●	–15		5	µA
V_{CM}	Input Voltage Range (Note 9)		●	–0.1		V^+ + 0.1	V
CMRR	Common Mode Rejection Ratio	V^+ = 5V, 0V ≤ V_{CM} ≤ 5V		60	70		dB
		V^+ = 5V, 0V ≤ V_{CM} ≤ 5V	●	58			dB
		V^+ = 2.7V, 0V ≤ V_{CM} ≤ 2.7V		57	70		dB
		V^+ = 2.7V, 0V ≤ V_{CM} ≤ 2.7V	●	55			dB

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 2.7V or V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_{LATCH} = 0.8V, C_{LOAD} = 10pF, $V_{OVERDRIVE}$ = 20mV, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$PSRR^+$	Positive Power Supply Rejection Ratio	2.4V ≤ V^+ ≤ 7V, V_{CM} = 0V	 ●	65 60	80		dB dB
$PSRR^-$	Negative Power Supply Rejection Ratio	−7V ≤ V^- ≤ 0V, V^+ = 5V, V_{CM} = 5V	 ●	65 60	80		dB dB
A_V	Small-Signal Voltage Gain (Note 10)			1.5	3		V/mV
V_{OH}	Output Voltage Swing HIGH	I_{OUT} = 1mA, V^+ = 5V, $V_{OVERDRIVE}$ = 50mV I_{OUT} = 10mA, V^+ = 5V, $V_{OVERDRIVE}$ = 50mV	● ●	V^+ – 0.5 V^+ – 0.7	V^+ – 0.2 V^+ – 0.4		V V
V_{OL}	Output Voltage Swing LOW	I_{OUT} = −1mA, $V_{OVERDRIVE}$ = 50mV I_{OUT} = −10mA, $V_{OVERDRIVE}$ = 50mV	● ●		0.20 0.35	0.4 0.5	V V
I^+	Positive Supply Current (Per Comparator)	V^+ = 5V, $V_{OVERDRIVE}$ = 1V	 ●		5	6.5 8.0	mA mA
I^-	Negative Supply Current (Per Comparator)	V^+ = 5V, $V_{OVERDRIVE}$ = 1V	 ●		3	4.0 4.5	mA mA
V_{IH}	Latch Pin High Input Voltage		●	2.4			V
V_{IL}	Latch Pin Low Input Voltage		●			0.8	V
I_{IL}	Latch Pin Current	V_{LATCH} = V^+	●			10	µA
t_{PD}	Propagation Delay (Note 6)	ΔV_{IN} = 100mV, $V_{OVERDRIVE}$ = 20mV ΔV_{IN} = 100mV, $V_{OVERDRIVE}$ = 20mV ΔV_{IN} = 100mV, $V_{OVERDRIVE}$ = 5mV	 ● 		8.0 9.0	11.0 12.5 	ns ns ns
Δt_{PD}	Differential Propagation Delay (Note 6)	ΔV_{IN} = 100mV, $V_{OVERDRIVE}$ = 20mV			0.5	3	ns
t_r	Output Rise Time	10% to 90%			4		ns
t_f	Output Fall Time	90% to 10%			4		ns
t_{LPD}	Latch Propagation Delay (Note 7)				8		ns
t_{SU}	Latch Setup Time (Note 7)				1.5		ns
t_H	Latch Hold Time (Note 7)				0		ns
t_{DPW}	Minimum Latch Disable Pulse Width (Note 7)				8		ns
f_{MAX}	Maximum Toggle Frequency	V_{IN} = 100mV_{P-P} Sine Wave			65		MHz
t_{JITTER}	Output Timing Jitter	V_{IN} = 630mV_{P-P} (0dBm) Sine Wave, f = 30MHz			15		ps_{RMS}

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = −5V, V_{CM} = 0V, V_{LATCH} = 0.8V, C_{LOAD} = 10pF, $V_{OVERDRIVE}$ = 20mV, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V^+	Positive Supply Voltage Range		●	2.4		7	V
V^-	Negative Supply Voltage Range (Note 3)		●	–7		0	V
V_{OS}	Input Offset Voltage (Note 4)	R_S = 50Ω, V_{CM} = 0V R_S = 50Ω, V_{CM} = 0V R_S = 50Ω, V_{CM} = −5V R_S = 50Ω, V_{CM} = 5V	 ● 		0.5 0.7 1	3 4 	mV mV mV mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift		●		5		µV/°C
I_{OS}	Input Offset Current		 ●		0.1	1 2	µA µA
I_B	Input Bias Current (Note 5)		 ●	–7 –15	–1.5	2 5	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = –5V, V_{CM} = 0V, V_{LATCH} = 0.8V, C_{LOAD} = 10pF, $V_{OVERDRIVE}$ = 20mV, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CM}	Input Voltage Range		●	–5.1		5.1	V
CMRR	Common Mode Rejection Ratio	–5V ≤ V_{CM} ≤ 5V	 ●	62 60	70		dB dB
$PSRR^+$	Positive Power Supply Rejection Ratio	2.4V ≤ V^+ ≤ 7V, V_{CM} = –5V	 ●	68 65	80		dB dB
$PSRR^-$	Negative Power Supply Rejection Ratio	–7V ≤ V^- ≤ 0V, V_{CM} = 5V	 ●	65 60	80		dB dB
A_V	Small-Signal Voltage Gain (Note 10)	1V ≤ V_{OUT} ≤ 4V, R_L = ∞		1.5	3		V/mV
V_{OH}	Output Voltage Swing HIGH (Note 8)	I_{OUT} = 1mA, $V_{OVERDRIVE}$ = 50mV I_{OUT} = 10mA, $V_{OVERDRIVE}$ = 50mV	● ●	4.5 4.3	4.8 4.6		V V
V_{OL}	Output Voltage Swing LOW (Note 8)	I_{OUT} = –1mA, $V_{OVERDRIVE}$ = 50mV I_{OUT} = –10mA, $V_{OVERDRIVE}$ = 50mV	● ●		0.20 0.35	0.4 0.5	V V
I^+	Positive Supply Current (Per Comparator)	$V_{OVERDRIVE}$ = 1V	 ●		5.5	7.5 9.0	mA mA
I^-	Negative Supply Current (Per Comparator)	$V_{OVERDRIVE}$ = 1V	 ●		3.5	4.5 5.0	mA mA
V_{IH}	Latch Pin High Input Voltage		●	2.4			V
V_{IL}	Latch Pin Low Input Voltage		●			0.8	V
I_{IL}	Latch Pin Current	V_{LATCH} = V^+	●			10	µA
t_{PD}	Propagation Delay (Note 6)	ΔV_{IN} = 100mV, $V_{OVERDRIVE}$ = 20mV ΔV_{IN} = 100mV, $V_{OVERDRIVE}$ = 20mV ΔV_{IN} = 100mV, $V_{OVERDRIVE}$ = 5mV	 ● 		7 8.5	10 12 	ns ns ns
Δt_{PD}	Differential Propagation Delay (Note 6)	ΔV_{IN} = 100mV, $V_{OVERDRIVE}$ = 20mV			0.5	3	ns
t_r	Output Rise Time	10% to 90%			4		ns
t_f	Output Fall Time	90% to 10%			4		ns
t_{LPD}	Latch Propagation Delay (Note 7)				8		ns
t_{SU}	Latch Setup Time (Note 7)				1.5		ns
t_H	Latch Hold Time (Note 7)				0		ns
t_{DPW}	Minimum Latch Disable Pulse Width (Note 7)				8		ns
f_{MAX}	Maximum Toggle Frequency	V_{IN} = 100mV_{P-P} Sine Wave			65		MHz
t_{JITTER}	Output Timing Jitter	V_{IN} = 630mV_{P-P} (0dBm) Sine Wave, f = 30MHz			15		ps_{RMS}

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LT1713C/LT1714C are guaranteed to meet specified performance from 0°C to 70°C. They are designed, characterized and expected to meet specified performance from –40°C to 85°C but are not tested or QA sampled at these temperatures. The LT1713I/LT1714I are guaranteed to meet specified performance from –40°C to 85°C.

Note 3: The negative supply should not be greater than the ground pin voltages and the maximum voltage across the positive and negative supplies should not be greater than 12V.

Note 4: Input offset voltage (V_{OS}) is defined as the average of the two voltages measured by forcing first one output, then the other to $V^+/2$.

Note 5: Input bias current (I_B) is defined as the average of the two input currents.

Note 6: Propagation delay (t_{PD}) is measured with the overdrive added to the actual V_{OS}. Differential propagation delay is defined as: $\Delta t_{PD} = t_{PD}^+ - t_{PD}^-$. Load capacitance is 10pF. Due to test system requirements, the LT1713/LT1714 propagation delay is specified with a 1kΩ load to ground for ±5V supplies, or to mid-supply for 2.7V or 5V single supplies.

Note 7: Latch propagation delay (t_{LPD}) is the delay time for the output to respond when the latch pin is deasserted. Latch setup time (t_{SU}) is the interval in which the input signal must remain stable prior to asserting the latch signal. Latch hold time (t_H) is the interval after the latch is asserted in which the input signal must remain stable. Latch disable pulse width (t_{DPW}) is the width of the negative pulse on the latch enable pin that latches in new data on the data inputs.

ELECTRICAL CHARACTERISTICS

Note 8: Output voltage swings are characterized and tested at V^+ = 5V and V^- = 0V. They are designed and expected to meet these same specifications at V^- = –5V.

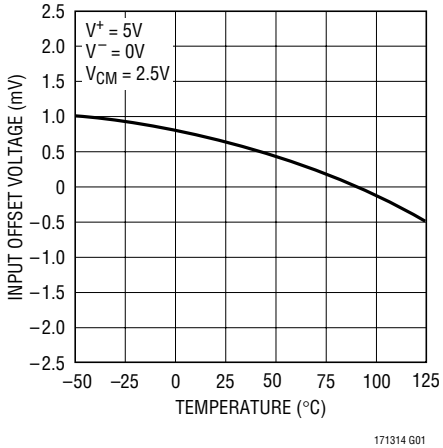
Note 9: The input voltage range is tested under the more demanding conditions of V^+ = 5V and V^- = –5V. The LT1713/LT1714 are designed and expected to meet these specifications at V^- = 0V.

Note 10: The LT1713/LT1714 voltage gain is tested at V^+ = 5V and V^- = –5V only. Voltage gain at single supply V^+ = 5V and V^+ = 2.7V is guaranteed by design and correlation.

Note 11: Input offset voltage over temperature at V^+ = 2.7V is guaranteed by design and characterization.

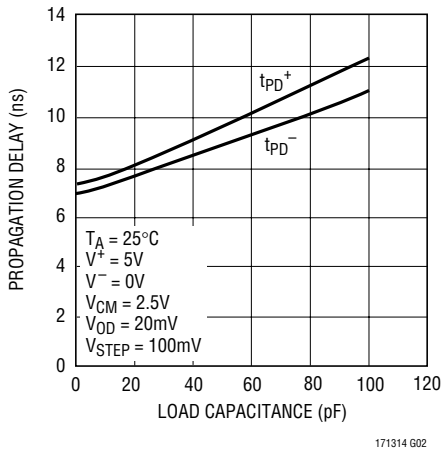
TYPICAL PERFORMANCE CHARACTERISTICS

Input Offset Voltage vs Temperature



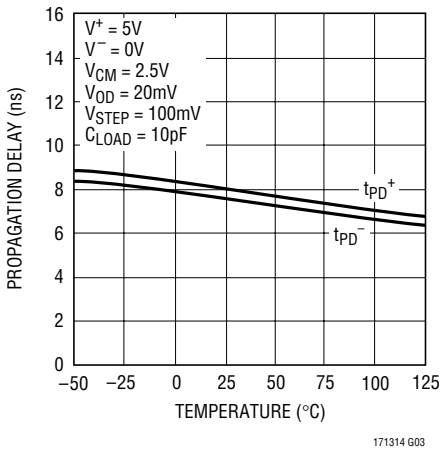
171314 G01

Propagation Delay vs Load Capacitance



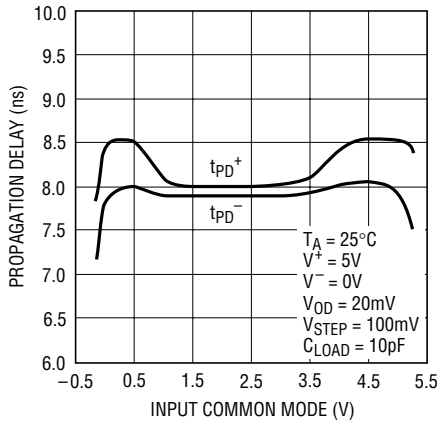
171314 G02

Propagation Delay vs Temperature



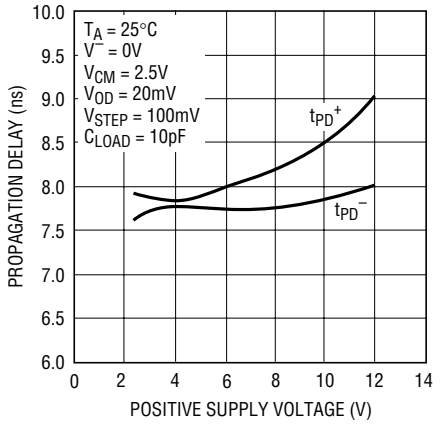
171314 G03

Propagation Delay vs Input Common Mode Voltage



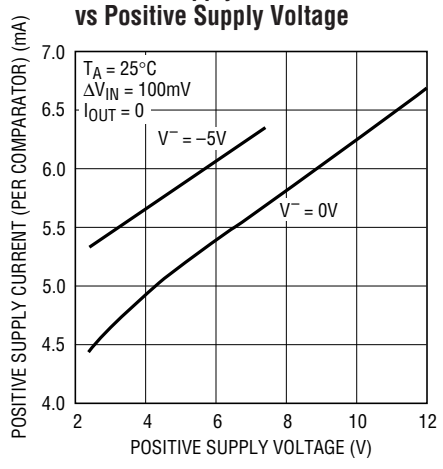
171314 G04

Propagation Delay vs Positive Supply Voltage



171314 G05

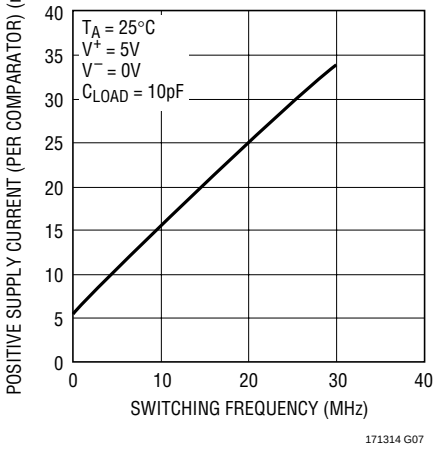
Positive Supply Current vs Positive Supply Voltage



171314 G06

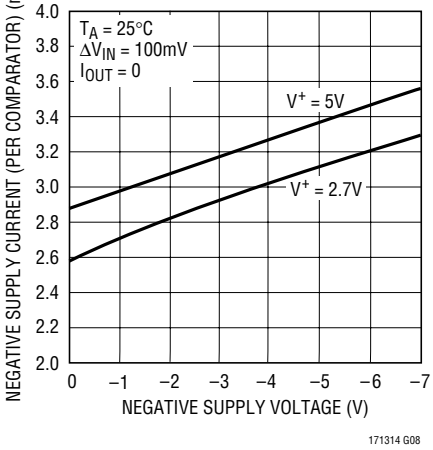
TYPICAL PERFORMANCE CHARACTERISTICS

Positive Supply Current vs Switching Frequency



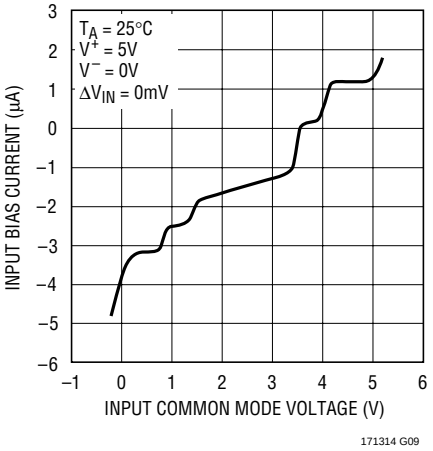
171314 G07

Negative Supply Current vs Negative Supply Voltage



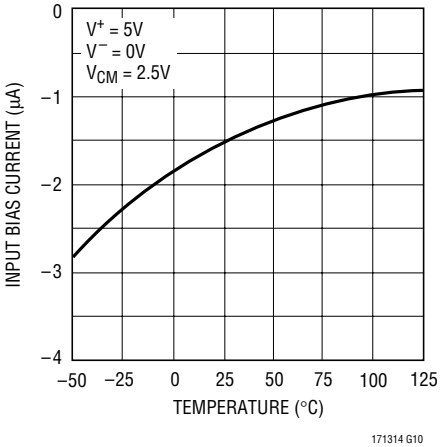
171314 G08

Input Bias Current vs Input Common Mode Voltage



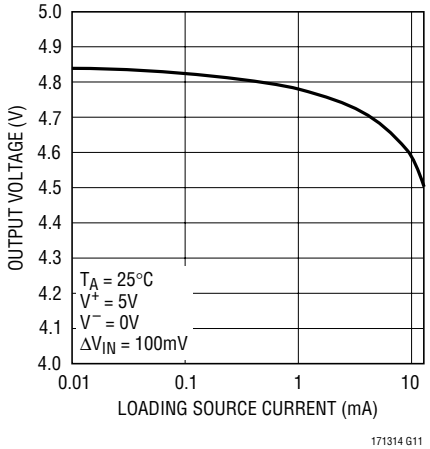
171314 G09

Input Bias Current vs Temperature



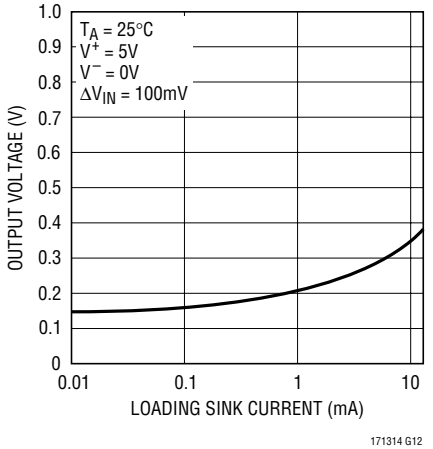
171314 G10

Output High Voltage vs Source Current



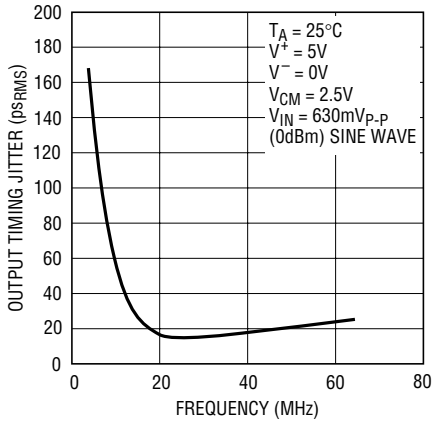
171314 G11

Output Low Voltage vs Sink Current



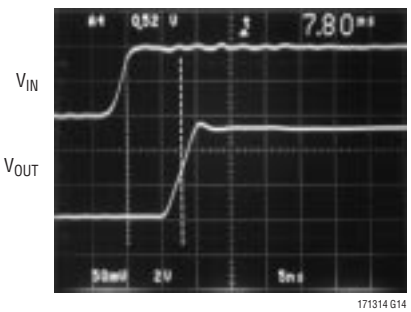
171314 G12

Output Timing Jitter vs Switching Frequency



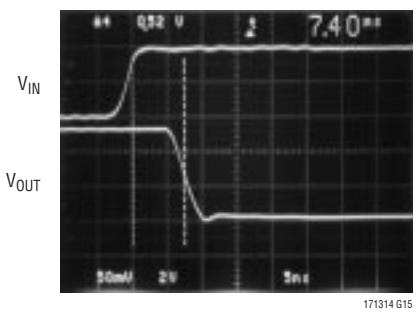
171314 G13

Output Rising Edge, 5V Supply



171314 G14

Output Falling Edge, 5V Supply



171314 G15

PIN FUNCTIONS

LT1713

V^+ (Pin 1): Positive Supply Voltage, Usually 5V.

+IN (Pin 2): Noninverting Input.

–IN (Pin 3): Inverting Input.

V^- (Pin 4): Negative Supply Voltage, Usually 0V or –5V.

LATCH ENABLE (Pin 5): Latch Enable Input. With a logic high the output is latched.

GND (Pin 6): Ground Supply Voltage, Usually 0V.

Q (Pin 7): Noninverting Output.

$\overline{Q}$ (Pin 8): Inverting Output.

LT1714

–IN A (Pin 1): Inverting Input of A Channel Comparator.

+IN A (Pin 2): Noninverting Input of A Channel Comparator.

V^- (Pins 3, 6): Negative Supply Voltage, Usually –5V. Pins 3 and 6 should be connected together externally.

V^+ (Pins 4, 5): Positive Supply Voltage, Usually 5V. Pins 4 and 5 should be connected together externally.

+IN B (Pin 7): Noninverting Input of B Channel Comparator.

–IN B (Pin 8): Inverting Input of B Channel Comparator.

LATCH ENABLE B (Pin 9): Latch Enable Input of B Channel Comparator. With a logic high, the B output is latched.

GND (Pin 10): Ground Supply Voltage of B Channel Comparator, Usually 0V.

Q B (Pin 11): Noninverting Output of B Channel Comparator.

$\overline{Q}$ B (Pin 12): Inverting Output of B Channel Comparator.

$\overline{Q}$ A (Pin 13): Inverting Output of A Channel Comparator.

Q A (Pin 14): Noninverting Output of A Channel Comparator.

GND (Pin 15): Ground Supply Voltage of A Channel Comparator, Usually 0V

LATCH ENABLE A (Pin 16): Latch Enable Input of A Channel Comparator. With a logic high, the A output is latched.

APPLICATIONS INFORMATION

Common Mode Considerations

The LT1713/LT1714 are specified for a common mode range of –5.1V to 5.1V on a ±5V supply, or a common mode range of –0.1V to 5.1V on a single 5V supply. A more general consideration is that the common mode range is from 100mV below the negative supply to 100mV above the positive supply, independent of the actual supply voltage. The criteria for common mode limit is that the output still responds correctly to a small differential input signal.

When either input signal falls outside the common mode limit, the internal PN diode formed with the substrate can turn on resulting in significant current flow through the die. Schottky clamp diodes between the inputs and the supply rails speed up recovery from excessive overdrive conditions by preventing these substrate diodes from turning on.

Input Bias Current

Input bias current is measured with the outputs held at 2.5V with a 5V supply voltage. As with any rail-to-rail differential input stage, the LT1713/LT1714 bias current flows into or out of the device depending upon the common mode level. The input circuit consists of an NPN pair and a PNP pair. For inputs near the negative rail, the NPN pair is inactive, and the input bias current flows out of the device; for inputs near the positive rail, the PNP pair is inactive, and these currents flow into the device. For inputs far enough away from the supply rails, the input bias current will be some combination of the NPN and PNP bias currents. As the differential input voltage increases, the input current of each pair will increase for one of the inputs and decrease for the other input. Large differential input voltages result in different input currents as the input stage enters various regions of operation. To reduce the influence of these changing input currents on system operation, use a low source resistance.

Latch Pin Dynamics

The internal latches of the LT1713/LT1714 comparators retain the input data (output latched) when their respective latch pin goes high. The latch pin will float to a low state when disconnected, but it is better to ground the latch when a flow-through condition is desired. The latch pin is designed to be driven with either a TTL or CMOS output. It has built-in hysteresis of approximately 100mV, so that slow moving or noisy input signals do not impact latch performance. For the LT1714, if only one of the comparators is being used at a given time, it is best to latch the second comparator to avoid any possibility of interactions between the two comparators in the same package.

High Speed Design Techniques

A substantial amount of design effort has made the LT1713/LT1714 relatively easy to use. As with most high speed comparators, careful attention to PC board layout and design is important in order to prevent oscillations. The most common problem involves power supply bypassing which is necessary to maintain low supply impedance. Resistance and inductance in supply wires and PC traces can quickly build up to unacceptable levels, thereby allowing the supply voltages to move as the supply current changes. This movement of the supply voltages will often result in improper operation. In addition, adjacent devices connected through an unbypassed supply can interact with each other through the finite supply impedances.

Bypass capacitors furnish a simple solution to this problem by providing a local reservoir of energy at the device, thus keeping supply impedance low. Bypass capacitors should be as close as possible to the LT1713/LT1714 supply pins. A good high frequency capacitor, such as a 0.1µF ceramic, is recommended in parallel with a larger capacitor, such as a 4.7µF tantalum.

APPLICATIONS INFORMATION

Poor trace routes and high source impedances are also common sources of problems. Keep trace lengths as short as possible and avoid running any output trace adjacent to an input trace to prevent unnecessary coupling. If output traces are longer than a few inches, provide proper termination impedances (typically 100Ω to 400Ω) to eliminate any reflections that may occur. Also keep source impedances as low as possible, preferably much less than 1kΩ.

The input and output traces should also be isolated from one another. Power supply traces can be used to achieve this isolation as shown in Figure 1, a typical topside layout of the LT1713/LT1714 on a multilayer PC board. Shown is the topside metal etch including traces, pin escape vias and the land pads for a GN16 LT1713/LT1714 and its adjacent X7R 0805 bypass capacitors. The V^+, V^- and GND traces all shield the inputs from the outputs. Although the two V^- pins are connected internally, they should be shorted together externally as well in order for both to function as shields. The same is true for the two V^+ pins. The two GND pins are not connected internally, but in most applications they are both connected directly to the ground plane.

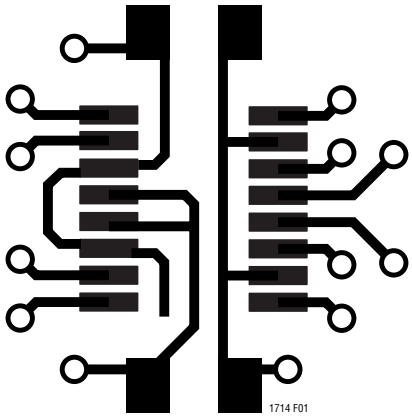


Figure 1. Typical LT1714 Topside Metal for Multilayer PCB Layout

APPLICATIONS INFORMATION

Hysteresis

Another useful technique to avoid oscillations is to provide positive feedback, also known as hysteresis, from the output to the input. Increased levels of hysteresis, however, reduce the sensitivity of the device to input voltage levels, so the amount of positive feedback should be tailored to particular system requirements. The LT1713/LT1714 are completely flexible regarding the application of hysteresis, due to rail-to-rail inputs and the complementary outputs. Specifically, feedback resistors can be connected from one or both outputs to their corresponding inputs without regard to common mode considerations. Figure 2 shows several configurations.

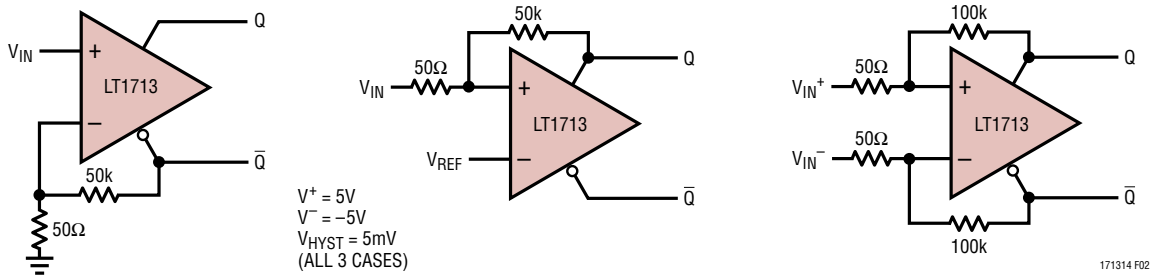


Figure 2. Various Configurations for Introducing Hysteresis

TYPICAL APPLICATIONS

Simultaneous Full Duplex 75Mbaud Interface with Only Two Wires

The circuit of Figure 3 shows a simple, fully bidirectional, differential 2-wire interface that gives good results to 75Mbaud, using the LT1714. Eye diagrams under conditions of unidirectional and bidirectional communication are shown in Figures 4 and 5. Although not as pristine as the unidirectional performance of Figure 4, the performance under simultaneous bidirectional operation is still excellent. Because the LT1714 input voltage range extends 100mV beyond both supply rails, the circuit works with a full ±3V (one whole V_S up or down) of ground potential difference.

The circuit works well with the resistor values shown, but other sets of values can be used. The starting point is the characteristic impedance, Z_0, of the twisted-pair cable. The input impedance of the resistive network should match the characteristic impedance and is given by:

$$R_{IN} = 2 \bullet R_0 \bullet \frac{R1 || (R2 + R3)}{R_0 + 2 \bullet [R1 || (R2 + R3)]}$$

This comes out to 120Ω for the values shown. The Thevenin equivalent source voltage is given by:

$$V_{TH} = V_S \bullet \frac{(R2 + R3 - R1)}{(R2 + R3 + R1)} \bullet \frac{R_0}{R_0 + 2 \bullet [R1 || (R2 + R3)]}$$

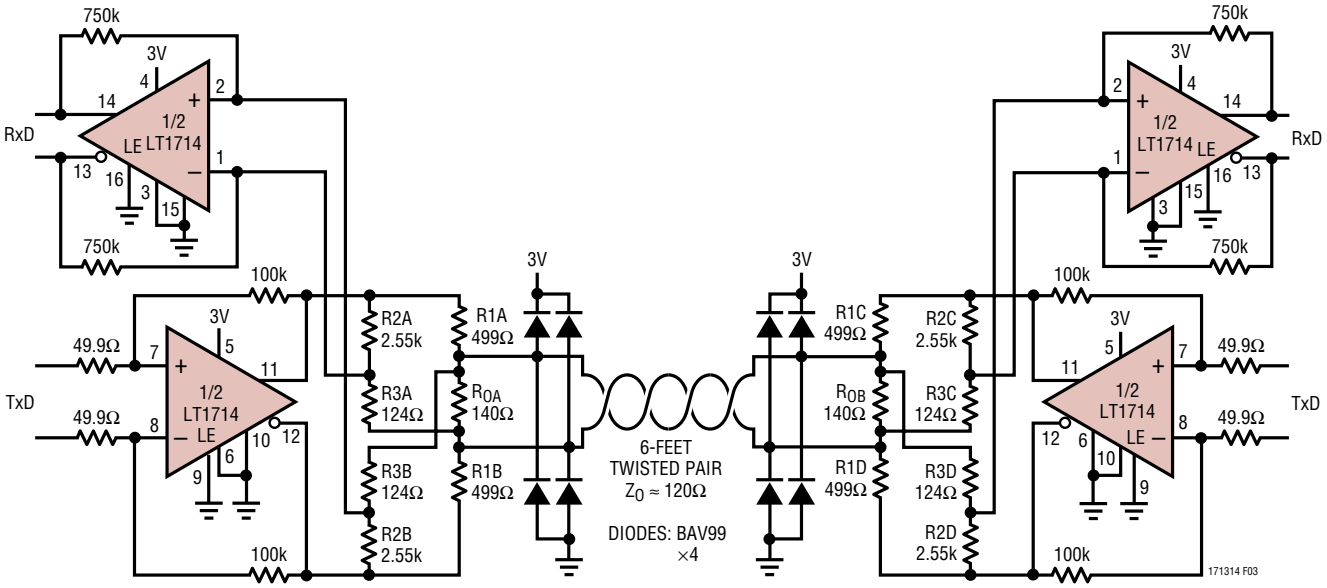


Figure 3. 75Mbaud Full Duplex Interface on Two Wires

TYPICAL APPLICATIONS

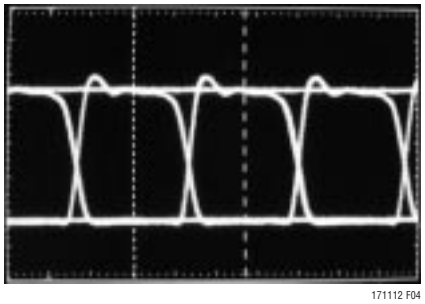


Figure 4. Performance of Figure 3's Circuit When Operated Unidirectionally. Eye is Wide Open

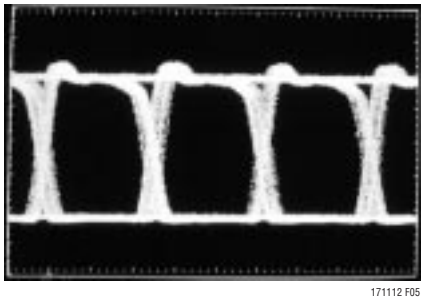


Figure 5. Performance When Operated Simultaneous Bidirectionally (Full Duplex). Crosstalk Appears as Noise. Eye is Slightly Shut But Performance is Still Excellent

This amounts to an attenuation factor of 0.0978 with the values shown. (The actual voltage on the lines will be cut in half again due to the 120Ω Z_0.) The reason this attenuation factor is important is that it is the key to deciding the ratio between the R2-R3 resistor divider in the receiver path. This divider allows the receiver to reject the large signal of the local transmitter and instead sense the attenuated signal of the remote transmitter. Note that in the above equations, R2 and R3 are not yet fully determined because they only appear as a sum. This allows the designer to now place an additional constraint on their values. The R2-R3 divide ratio should be set to equal half the attenuation factor mentioned above or:

$R3/R2 = 1/2 \bullet 0.0976$[1].

Having already designed R2 + R3 to be 2.653k (by allocating input impedance across R_0, R1 and R2 + R3 to get the requisite 120Ω), R2 and R3 then become 2529Ω and 123.5Ω respectively. The nearest 1% value for R2 is 2.55k and that for R3 is 124Ω.

Voltage-Tunable Crystal Oscillator

The front page application is a variant of a basic crystal oscillator that permits voltage tuning of the output frequency. Such voltage-controlled crystal oscillators (VCXO) are often employed where slight variation of a stable carrier is required. This example is specifically intended to provide a 4× NTSC sub-carrier tunable oscillator suitable for phase locking.

The LT1713 is set up as a crystal oscillator. The varactor diode is biased from the tuning input. The tuning network is arranged so a 0V to 5V drive provides a reasonably symmetric, broad tuning range around the 14.31818MHz center frequency. The indicated selected capacitor sets tuning bandwidth. It should be picked to complement loop response in phase locking applications. Figure 6 is a plot of tuning input voltage versus frequency deviation. Tuning deviation from the 4× NTSC 14.31818MHz center frequency exceeds ±240ppm for a 0V to 5V input.

[1] Using the design value of R2 + R3 = 2.653k rather than the implementation value of 2.55k + 124Ω = 2.674k.

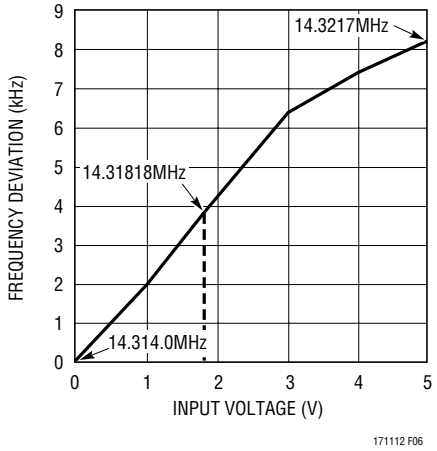


Figure 6. Control Voltage vs Output Frequency for the First Page Application Circuit. Tuning Deviation from Center Frequency Exceeds ±240ppm

TYPICAL APPLICATIONS

1MHz Series Resonant Crystal Oscillator with Square and Sinusoid Outputs

Figure 7 shows a classic 1MHz series resonant crystal oscillator. At series resonance, the crystal is a low impedance and the positive feedback connection is what brings about oscillation at the series resonant frequency. The RC feedback around the other path ensures that the circuit does not find a stable DC operating point and refuse to oscillate. The comparator output is a 1MHz square wave (top trace of Figure 8) with jitter measured at better than $28ps_{RMS}$ on a 5V supply and $40ps_{RMS}$ on a 3V supply. At Pin 2 of the comparator, on the other side of the crystal, is a clean sine wave except for the presence of the small high frequency glitch (middle trace of Figure 8). This glitch is caused by the fast edge of the comparator output feeding back through crystal capacitance. Amplitude stability of the sine wave is maintained by the fact that the sine wave is basically a filtered version of the square wave. Hence, the usual amplitude control loops associated with sinusoidal oscillators are not necessary.[2] The sine wave is filtered and buffered by the fast, low noise LT1806 op amp. To remove the glitch, the LT1806 is configured as a bandpass filter with a Q of 5 and unity-gain center frequency of 1MHz, with its output shown as the bottom trace of Figure 8. Distortion was measured at –70dBc and –60dBc on the second and third harmonics, respectively.

[2] Amplitude will be a linear function of comparator output swing, which is supply dependent and therefore adjustable. The important difference here is that any added amplitude stabilization or control loop will not be faced with the classical task of avoiding regions of nonoscillation versus clipping.

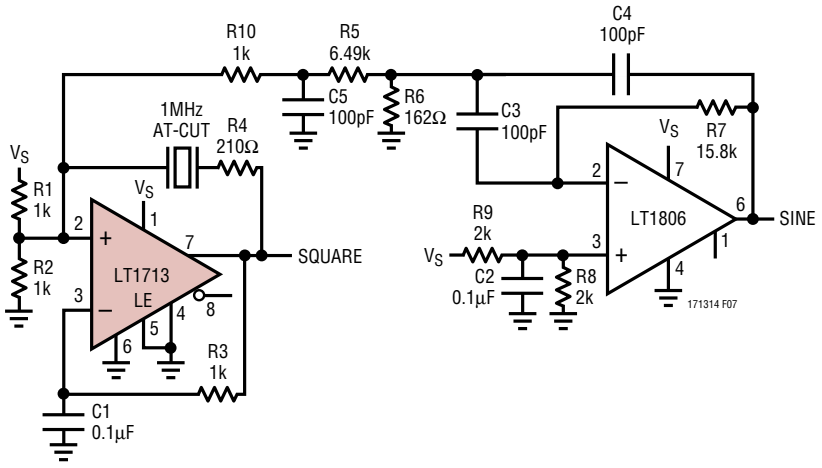


Figure 7. LT1713 Comparator is Configured as a Series Resonant Xtal Oscillator. LT1806 Op Amp is Configured in a Q = 5 Bandpass with f_C = 1MHz

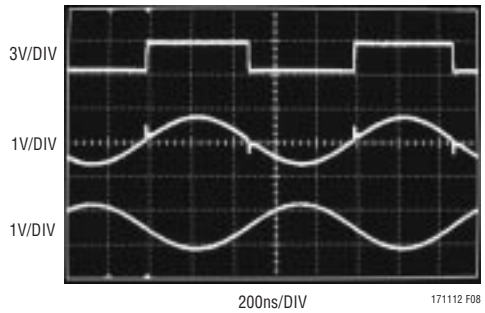
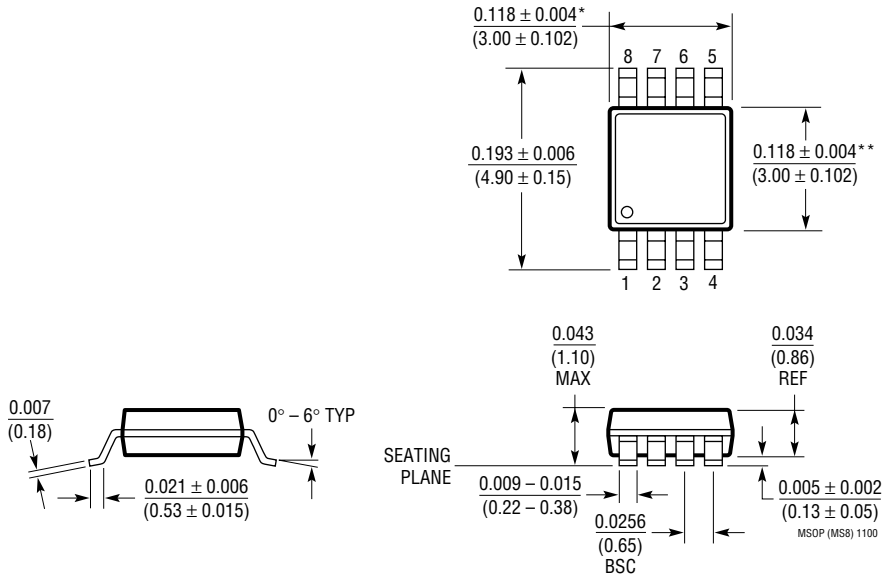


Figure 8. Oscillator Waveforms with V_S = 3V. Top is Comparator Output. Middle is Xtal Feedback to Pin 2 at LT1713 (Note the Glitches). Bottom is Buffered, Inverted and Bandpass Filtered with a Q = 5 by LT1806

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)



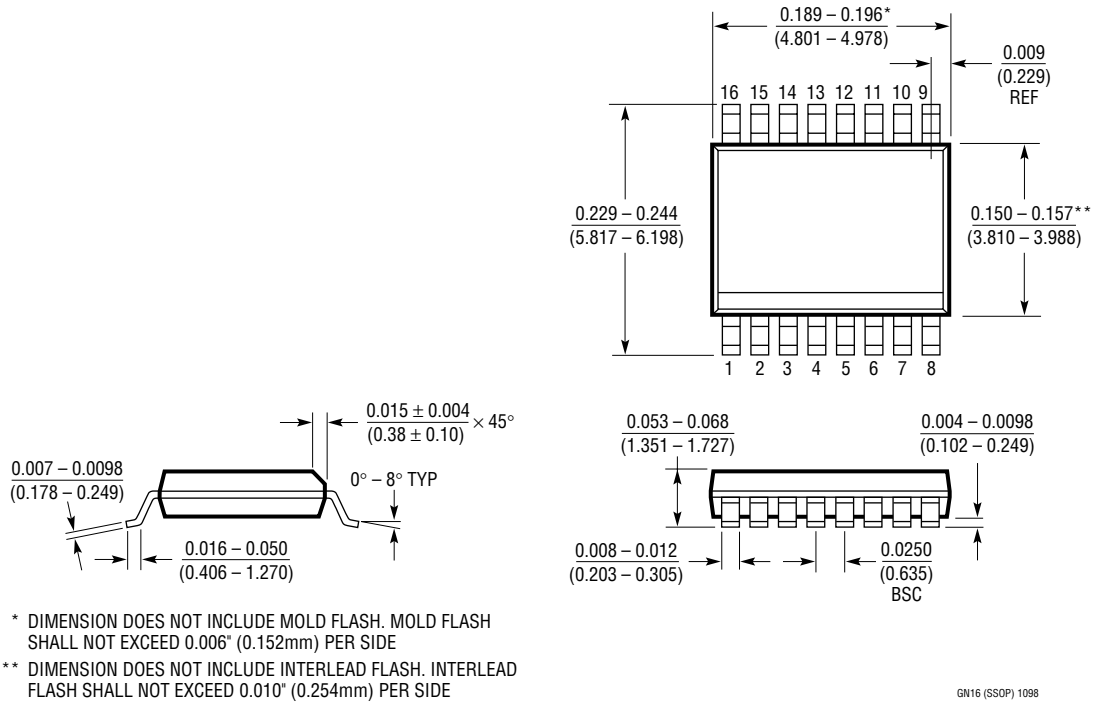
* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 1098

TYPICAL APPLICATION

Rail-to-Rail Pulse Width Modulator Using the LT1714

Binary modulation schemes are used in order to improve efficiency and reduce physical circuit size. They do this by reducing the power dissipation in the output driver transistors. In a normal Class A or Class AB amplifier, voltage drop and current flow exist simultaneously in the output transistors and power losses proportional to V • I occur. In a binary modulation scheme, the output transistors, whether bipolar or FET, are switched hard-on and hard-off so that voltage drops do not occur simultaneously with current flow. The circuit of Figure 9 shows an example of a binary modulation scheme, in this case pulse width modulation.

The LT1809 is configured as an integrator in order to generate nice linear rail-to-rail voltage ramps. The polarity of the ramp is determined by the output of the LT1714's comparator A into R4. The heavy hysteresis of R1 around the LT1714's comparator A combined with the feedback of the LT1809 force the devices to perpetually reverse each other, resulting in a 1MHz triangle wave. This constitutes the usual first half of any pulse width modulator, but the