4ns, 150MHz Dual Comparator with Independent Input/Output Supplies

FEATURES

- **UltraFast: 4ns at 20mV Overdriven**
- **150MHz Toggle Frequency**
- **Separate Input and Output Power Supplies**
- **Low Power: 4.6mA per Comparator at 3V**
- Pinout Optimized for High Speed Use
- Output Optimized for 3V and 5V Supplies
- TTL/CMOS Compatible Rail-to-Rail Output
- Input Voltage Range Extends 100mV Below Negative Rail
- Internal Hysteresis with Specified Limits
- Specified for –40°C to 125°C Temperature Range
- Available in the 10-pin MSOP Package

APPLICATIONS

- High Speed Differential Line Receivers
- Level Translators
- Window Comparators
- Crystal Oscillator Circuits
- Threshold Detectors/Discriminators
- High Speed Sampling Circuits
- Delay Lines

DESCRIPTION

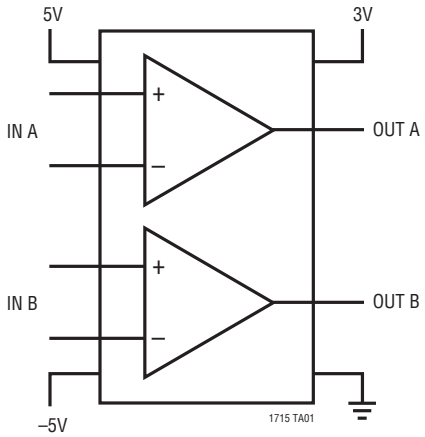
The LT®1715 is an UltraFast™ dual comparator optimized for low voltage operation. Separate supplies allow independent analog input ranges and output logic levels with no loss of performance. The input voltage range extends from 100mV below V_{EE} to 1.2V below V_{CC}. Internal hysteresis makes the LT1715 easy to use even with slow moving input signals. The rail-to-rail outputs directly interface toTTL and CMOS. The symmetric output drive results in similar rise and fall times that can be harnessed for analog applications or for easy translation to other single supply logic levels.

The LT1715 is available in the 10-pin MSOP package. The pinout of the LT1715 minimizes parasitic effects by placing the most sensitive inputs away from the outputs, shielded by the power rails.

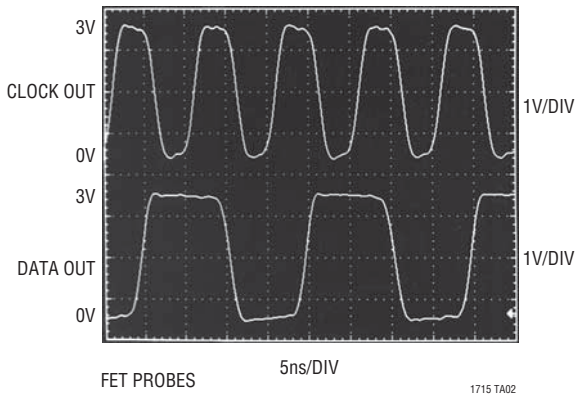
For a dual/quad single supply comparator with similar propagation delay, see the LT1720/LT1721. For a single comparator with similar propagation delay, see the LT1719.

TYPICAL APPLICATION

100MHz Dual Differential Line Receiver



Line Receiver Response to 100MHz Clock, 50MHz Data Both with 25mV$_{P-P}$ Inputs



ABSOLUTE MAXIMUM RATINGS

(Note 1)

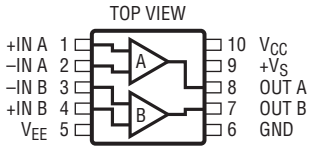
Supply Voltage
- $+V_S$ to GND 7V
- V_{CC} to V_{EE} 13.2V
- $+V_S$ to V_{EE} 13.2V
- V_{EE} to GND ..... –13.2V to 0.3V

Input Current (+IN, –IN) ..... ±10mA
Output Current (Continuous) ..... ±20mA
Operating Temperature Range (Note 2)
- LT1715C ..... –40°C to 85°C
- LT1715I ..... –40°C to 85°C
- LT1715H ..... –40°C to 125°C

Specified Temperature Range (Note 3)
- LT1715C ..... 0°C to 70°C
- LT1715I ..... –40°C to 85°C
- LT1715H ..... –40°C to 125°C

Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 120°C/W (NOTE 4)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1715CMS#PBF	LT1715CMS#TRPBF	LTVQ	10-Lead Plastic MSOP	0°C to 70°C
LT1715IMS#PBF	LT1715IMS#TRPBF	LTVV	10-Lead Plastic MSOP	–40°C to 85°C
LT1715HMS#PBF	LT1715HMS#TRPBF	LTVV	10-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{EE} = –5V, $+V_S$ = 5V, V_{CM} = 1V, C_{OUT} = 10pF, $V_{OVERDRIVE}$ = 20mV, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
$V_{CC} – V_{EE}$	Input Supply Voltage			●	2.7		12	V
$+V_S$	Output Supply Voltage			●	2.7		6	V
V_{CMR}	Input Voltage Range	(Note 5)		●	V_{EE} – 0.1		V_{CC} – 1.2	V
V_{TRIP}^+	Input Trip Points	(Note 6)	LT1715C, LT1715I LT1715H	● ●	–1.5 –1.8		5.5 6	mV mV
V_{TRIP}^-	Input Trip Points	(Note 6)	LT1715C, LT1715I LT1715H	● ●	–5.5 –6		1.5 1.8	mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{EE} = –5V, $+V_S$ = 5V, V_{CM} = 1V, C_{OUT} = 10pF, $V_{OVERDRIVE}$ = 20mV, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 6)			0.4	2.5	mV
		LT1715C, LT1715I	●			3.5	mV
		LT1715H	●			4	mV
V_{HYST}	Input Hysteresis Voltage	(Note 6) LT1715C, LT1715I	●	2	3.5	6	mV
		LT1715H	●	2		7	mV
$V_{OS}/\Delta T$	Input Offset Voltage Drift		●		10		µV/°C
I_B	Input Bias Current	LT1715C, LT1715I	●	–6	–2.5	0	µA
		LT1715H	●	–7		0	µA
I_{OS}	Input Offset Current	LT1715C, LT1715I	●		0.2	0.6	µA
		LT1715H	●			1	µA
CMRR	Common Mode Rejection Ratio	(Note 7) LT1715C, LT1715I	●	60	70		dB
		LT1715H	●	55			dB
PSRR	Power Supply Rejection Ratio	(Note 8)	●	65	80		dB
A_V	Voltage Gain	(Note 9)			∞		
V_{OH}	Output High Voltage	I_{SOURCE} = 4mA, $V_{IN} = V_{TRIP}^+ + 20mV$	●	$+V_S – 0.4$			V
V_{OL}	Output Low Voltage	I_{SINK} = 10mA, $V_{IN} = V_{TRIP}^- – 20mV$	●			0.4	V
f_{MAX}	Maximum Toggle Frequency	(Note 10)			150		MHz
t_{PD20}	Propagation Delay	$V_{OVERDRIVE}$ = 20mV (Note 11), V_{CC} = 5V, V_{EE} = –5V LT1715C, LT1715I	●	2.8	4	6	ns
		LT1715C, LT1715I	●	2.8		7	ns
		LT1715H	●	2.8		8	ns
		$V_{OVERDRIVE}$ = 20mV, V_{CC} = 5V, V_{EE} = 0V			4.4		ns
		$V_{OVERDRIVE}$ = 20mV, V_{CC} = 3V, V_{EE} = 0V		3	4.8	6.5	ns
		LT1715C, LT1715I	●	3		7.5	ns
		LT1715H	●	3		8	ns
t_{PD5}	Propagation Delay	$V_{OVERDRIVE}$ = 5mV, V_{EE} = 0V (Notes 11, 12)			6	9	ns
			●			12	ns
t_{SKEW}	Propagation Delay Skew	(Note 13) Between t_{PD}^+/t_{PD}^-, V_{EE} = 0V	●		0.5	1.5	ns
Δt_{PD}	Differential Propagation Delay	(Note 14) Between Channels	●		0.3	1	ns
t_r	Output Rise Time	10% to 90%			2		ns
t_f	Output Fall Time	90% to 10%			2		ns
t_{JITTER}	Output Timing Jitter	V_{IN} = 1.2V_{P-P} (6dBm), Z_{IN} = 50 t_{PD}^+			15		ps_{RMS}
		f = 20MHz (Note 15) t_{PD}^-			11		ps_{RMS}
I_{CC}	Positive Input Stage Supply Current (per Comparator)	$+V_S = V_{CC}$ = 5V, V_{EE} = –5V LT1715C, LT1715I	●		1	2	mA
		LT1715H	●			2.2	mA
		$+V_S = V_{CC}$ = 3V, V_{EE} = 0V LT1715C, LT1715I	●		0.9	1.6	mA
		LT1715H	●			1.8	mA
I_{EE}	Negative Input Stage Supply Current (per Comparator)	$+V_S = V_{CC}$ = 5V, V_{EE} = –5V LT1715C, LT1715I	●	–4.8	–2.9		mA
		LT1715H	●	–5.3			mA
		$+V_S = V_{CC}$ = 3V, V_{EE} = 0V LT1715C, LT1715I	●	–3.8	–2.4		mA
		LT1715H	●	–4.3			mA
I_S	Positive Output Stage Supply Current (per Comparator)	$+V_S = V_{CC}$ = 5V, V_{EE} = –5V LT1715C, LT1715I	●		4.6	7.5	mA
		LT1715H	●			8	mA
		$V_S = V_{CC}$ = 3V, V_{EE} = 0V LT1715C, LT1715I	●		3.7	6	mA
		LT1715H	●			6.5	mA

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT1715C is guaranteed functional over the operating range of –40°C to 85°C.

Note 3: The LT1715C is guaranteed to meet specified performance from 0°C to 70°C. The LT1715°C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LT1715I is guaranteed to meet specified performance from –40°C to 85°C. The LT1715H is guaranteed to meet specified performance from –40°C to 125°C.

Note 4: Thermal resistances vary depending upon the amount of PC board metal attached to Pin 5 of the device. θ_{JA} is specified for a 2500mm^2 3/32" FR-4 board covered with 2oz copper on both sides and with 100mm^2 of copper attached to Pin 5. Thermal performance can be improved beyond the given specification by using a 4-layer board or by attaching more metal area to Pin 5.

Note 5: If one input is within these common mode limits, the other input can go outside the common mode limits and the output will be valid.

Note 6: The LT1715 comparator includes internal hysteresis. The trip points are the input voltage needed to change the output state in each direction. The offset voltage is defined as the average of V_{TRIP}^+ and V_{TRIP}^-, while the hysteresis voltage is the difference of these two.

Note 7: The common mode rejection ratio is measured with V_{CC} = 5V, V_{EE} = –5V and is defined as the change in offset voltage measured from V_{CM} = –5.1V to V_{CM} = 3.8V, divided by 8.9V.

Note 8: The power supply rejection ratio is measured with V_{CM} = 1V and is defined as the worst of: the change in offset voltage from V_{CC} = $+V_S$ = 2.7V to V_{CC} = $+V_S$ = 6V (with V_{EE} = 0V) divided by 3.3V or the change in offset voltage from V_{EE} = 0V to V_{EE} = –6V (with V_{CC} = $+V_S$ = 6V) divided by 6V.

Note 9: Because of internal hysteresis, there is no small-signal region in which to measure gain. Proper operation of internal circuity is ensured by measuring V_{OH} and V_{OL} with only 20mV of overdrive.

Note 10: Maximum toggle rate is defined as the highest frequency at which a 100mV sinusoidal input results in an error free output toggling to greater than 4V when high and to less than 1V when low on a 5V output supply.

Note 11: Propagation delay measurements made with 100mV steps. Overdrive is measured relative to $V_{TRIP}^{\pm}$.

Note 12: t_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The LT1715 is 100% tested with a 100mV step and 20mV overdrive. Correlation tests have shown that t_{PD} limits can be guaranteed with this test.

Note 13: Propagation Delay Skew is defined as:

$$t_{SKEW} = |t_{PDLH} - t_{PDHL}|$$

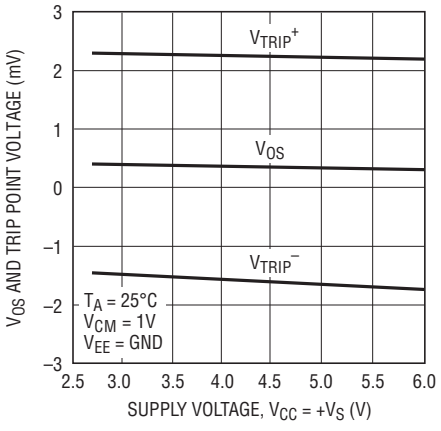
Note 14: Differential propagation delay is defined as the larger of the two:

$$\Delta t_{PDLH} = |t_{PDLHA} - t_{PDLHB}|$$
$$\Delta t_{PDHL} = |t_{PDHLA} - t_{PDHLB}|$$

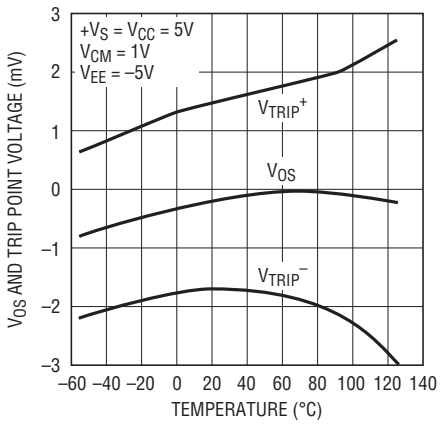
Note 15: Package inductances combined with asynchronous activity on the other channel can increase the output jitter. See Channel Interactions in Applications Information. Specification above is with one channel active only.

TYPICAL PERFORMANCE CHARACTERISTICS

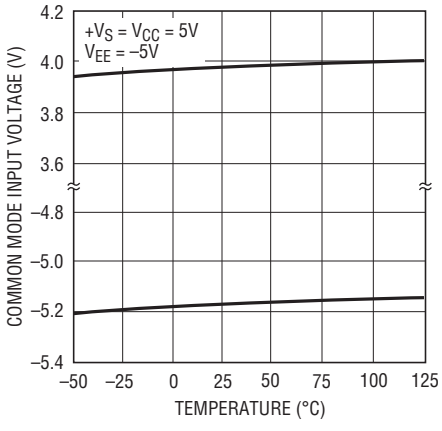
Input Offset and Trip Voltages vs Supply Voltage



Input Offset and Trip Voltages vs Temperature

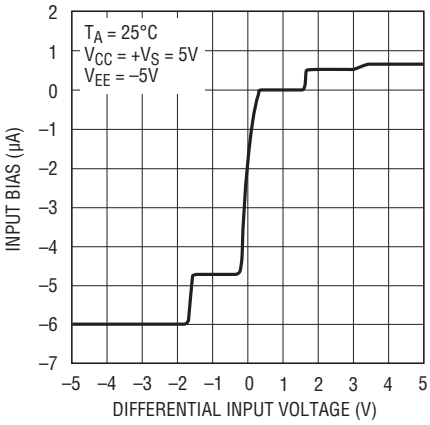


Input Common Mode Limits vs Temperature



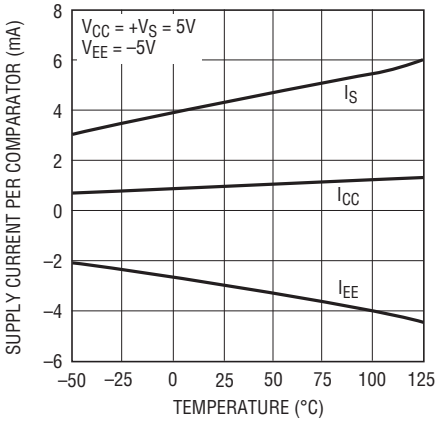
TYPICAL PERFORMANCE CHARACTERISTICS

Input Current vs Differential Input Voltage



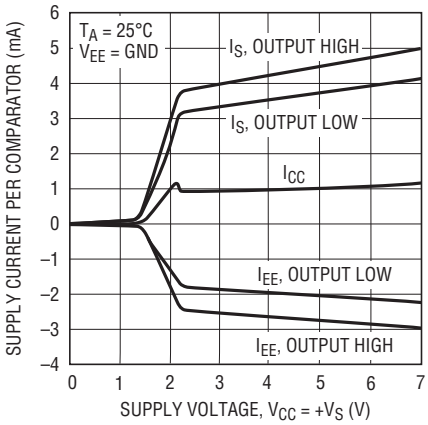
1715 G04

Quiescent Supply Current vs Temperature



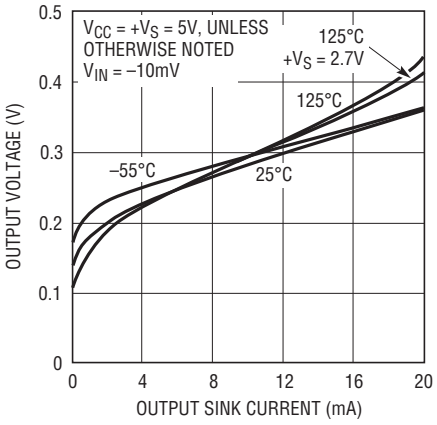
1715 G05

Quiescent Supply Current vs Supply Voltage



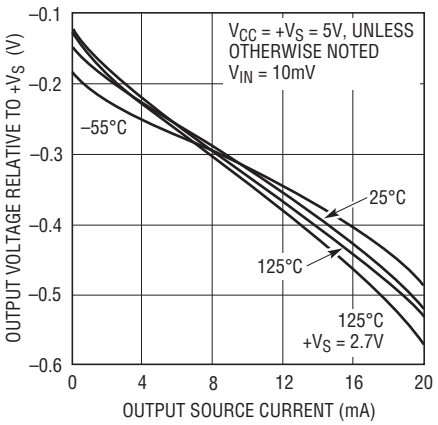
1715 G06

Output Low Voltage vs Load Current



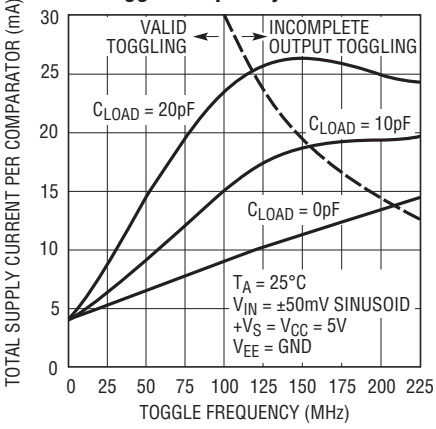
1715 G07

Output High Voltage vs Load Current



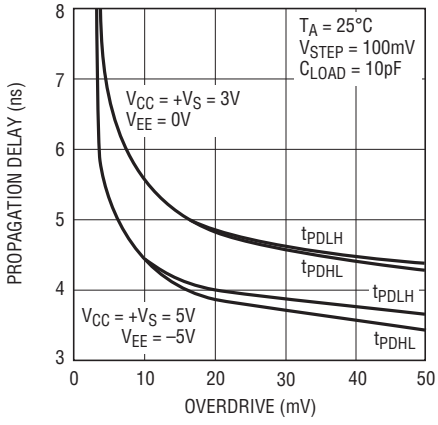
1715 G08

Supply Current vs Toggle Frequency



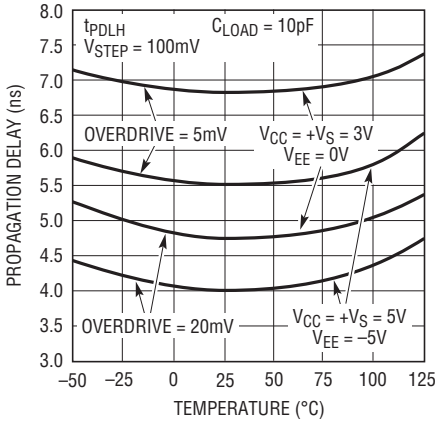
1715 G09

Propagation Delay vs Overdrive



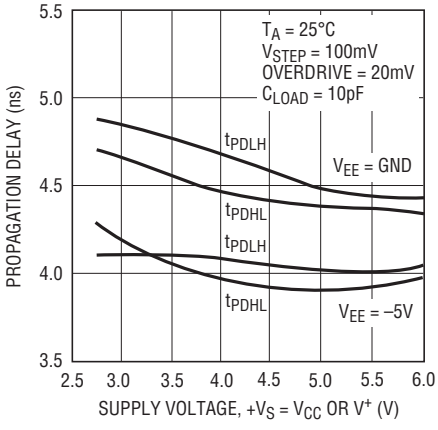
1715 G10

Propagation Delay vs Temperature



1715 G11

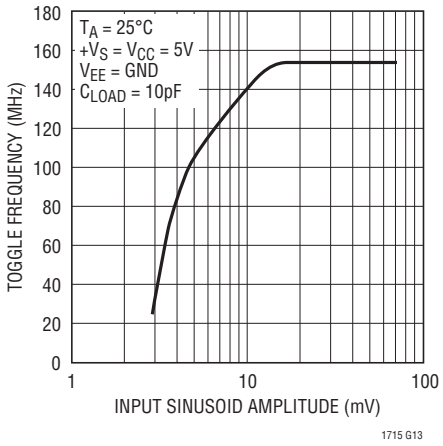
Propagation Delay vs Supply Voltage



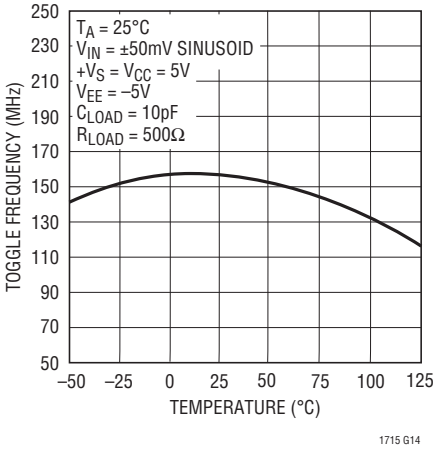
1715 G12

TYPICAL PERFORMANCE CHARACTERISTICS

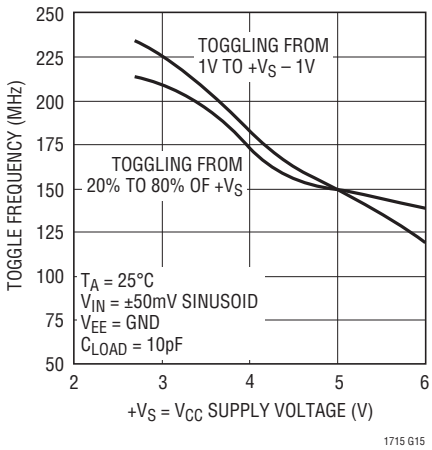
Maximum Toggle Rate vs Input Amplitude



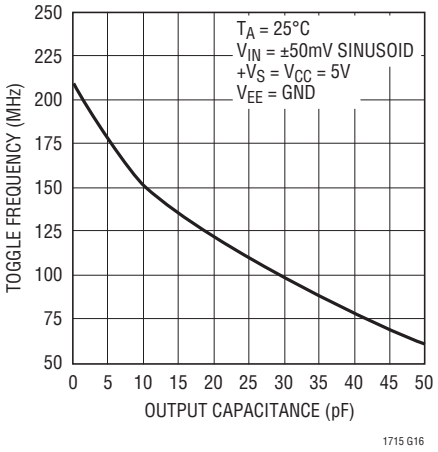
Maximum Toggle Rate vs Temperature



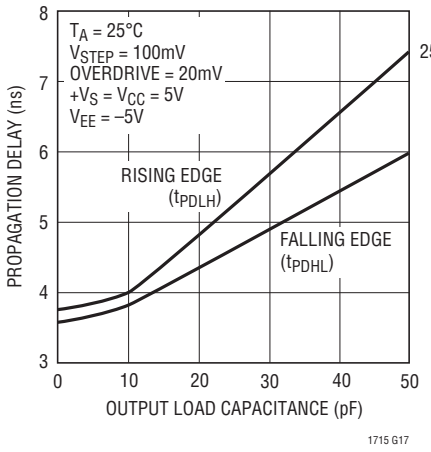
Maximum Toggle Rate vs Supply Voltage



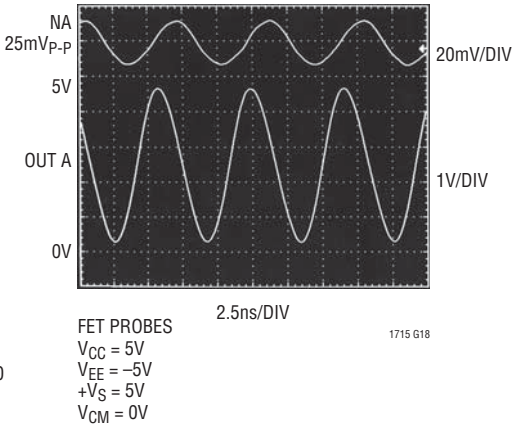
Maximum Toggle Rate vs Load Capacitance



Propagation Delay vs Load Capacitance



Response to 150MHz 25mV$_{P-P}$ Sine Wave Driving 10pF



PIN FUNCTIONS

+IN A (Pin 1): Noninverting Input of Comparator A.

–IN A (Pin 2): Inverting Input of Comparator A.

–IN B (Pin 3): Inverting Input of Comparator B.

+IN B (Pin 4): Noninverting Input of Comparator B.

V_{EE} (Pin 5): Negative Supply Voltage for Input Stage and Substrate.

GND (Pin 6): Ground for Output Stage.

OUT B (Pin 7): Output of Comparator B.

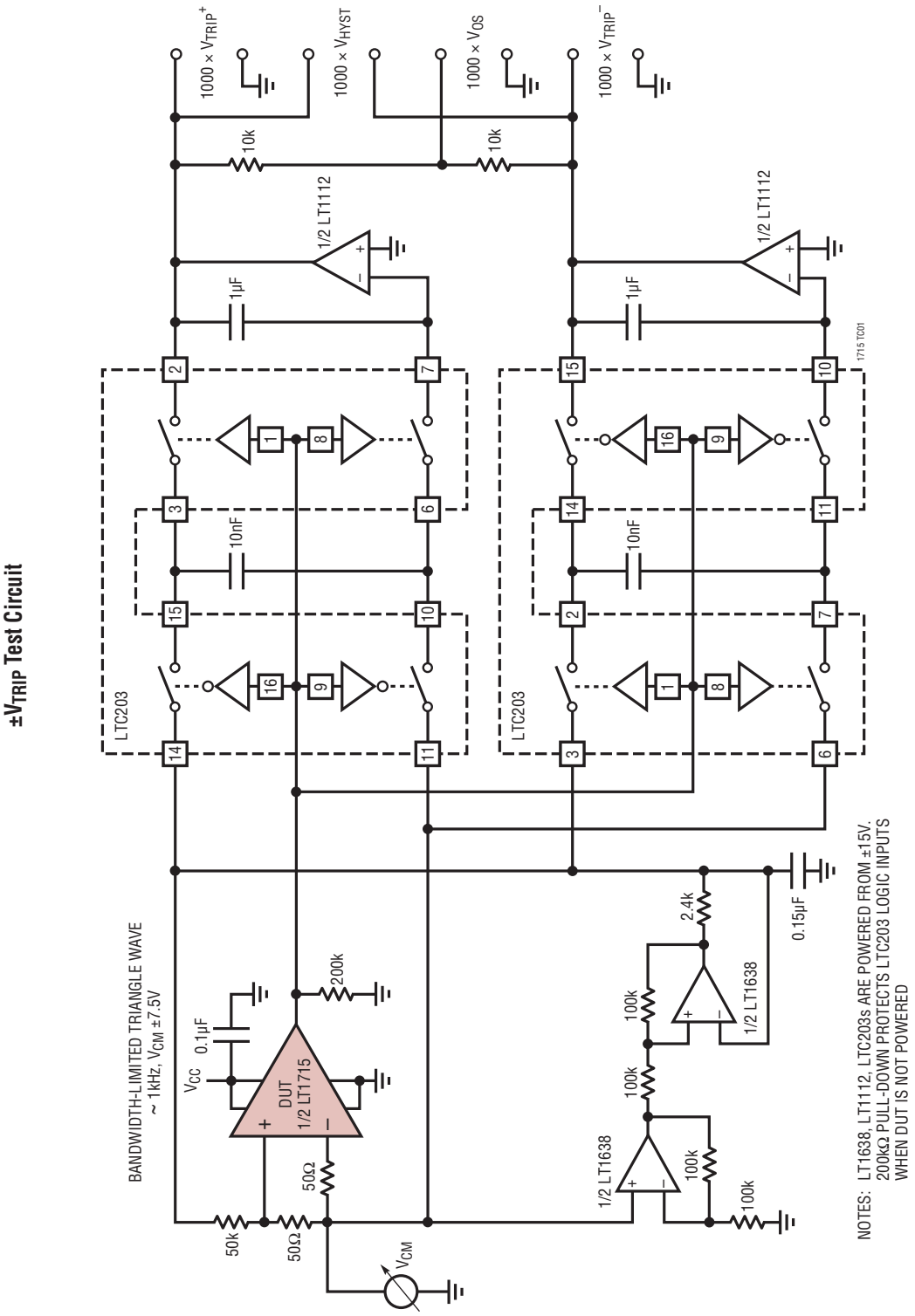
OUT A (Pin 8): Output of Comparator A.

$+V_S$ (Pin 9): Positive Supply Voltage for Output Stage.

V_{CC} (Pin 10): Positive Supply Voltage for Input Stage.

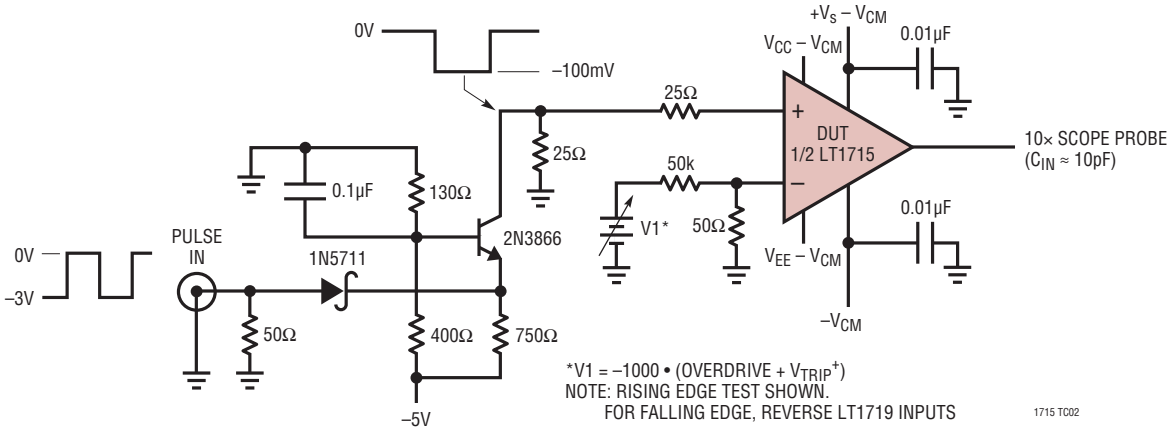
TEST CIRCUITS

±V_{TRIP} Test Circuit



TEST CIRCUITS

Response Time Test Circuit



APPLICATIONS INFORMATION

Power Supply Configurations

The LT1715 has separate supply pins for the input and output stages that allow flexible operation, accommodating separate voltage ranges for the analog input and the output logic. Of course, a single 3V/5V supply may be used by tying $+V_S$ and V_{CC} together as well as GND and V_{EE}.

The minimum voltage requirement can be simply stated as both the output and the input stages need at least 2.7V and the V_{EE} pin must be equal to or less than ground.

The following rules must be adhered to in any configuration:

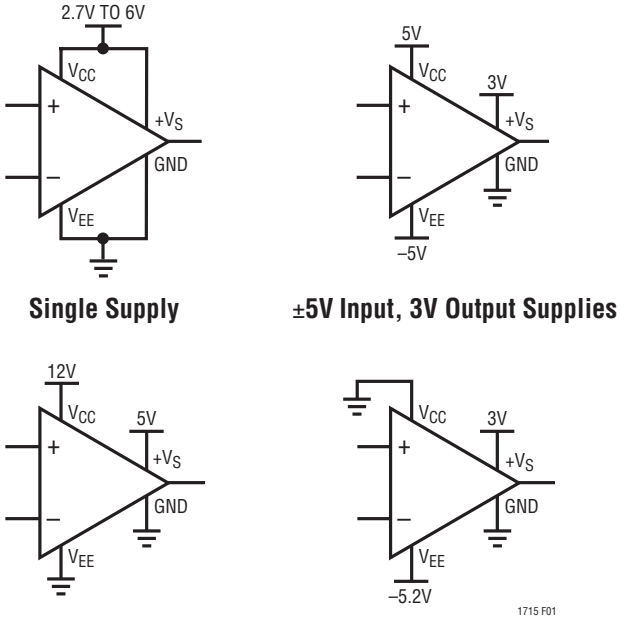
$2.7V \leq (V_{CC} - V_{EE}) \leq 12V$

$2.7V \leq (+V_S - GND) \leq 6V$

$(+V_S - V_{EE}) \leq 12V$

$V_{EE} \leq Ground$

Although the ground pin need not be tied to system ground, most applications will use it that way. Figure 1 shows three common configurations. The final one is uncommon, but it will work and may be useful as a level translator; the input stage is run from –5.2V and ground while the output stage is run from 3V and ground. In this case the common mode input voltage range does not include ground, so it may be helpful to tie V_{CC} to 3V. Conversely, V_{CC} may also be tied below ground, as long as the above rules are not violated.



Single Supply | **±5V Input, 3V Output Supplies**

12V Input, 5V Output Supplies | **Front End Entirely Negative**

Figure 1. Variety of Power Supply Configurations

Input Voltage Considerations

The LT1715 is specified for a common mode range of –100mV to 3.8V when used with a single 5V supply. A more general consideration is that the common mode range is 100mV below V_{EE} to 1.2V below V_{CC}. The criterion for this common mode limit is that the output still responds correctly to a small differential input signal. If one input is within the common mode limit, the other input signal can go outside the common mode limits, up to the absolute maximum limits, and the output will retain the correct polarity.

When either input signal falls below the negative common mode limit, the internal PN diode formed with the substrate can turn on, resulting in significant current flow through the die. An external Schottky clamp diode between the input and the negative rail can speed uprecovery from negative overdrive by preventing the substrate diode from turning on.

When both input signals are below the negative common mode limit, phase reversal protection circuitry prevents false output inversion to at least –400mV common mode. However, the offset and hysteresis in this mode will increase dramatically, to as much as 15mV each. The input bias currents will also increase.

When one input signal goes above the common mode range without exceeding a diode drop above the input supply rail, the input stage will remain biased and the comparator will maintain correct output polarity. Above this voltage, the input stage current source will saturate completely and the ESD protection diode will forward conduct. Once the aberrant input falls back into the common mode range, the comparator will respond correctly to valid input signals within less than 10ns.

APPLICATIONS INFORMATION

When both input signals are above the positive common mode limit, the input stage will get debiased and the output polarity will be random. However, the internal hysteresis will hold the output to a valid logic level. When at least one of the inputs returns to within the common mode limits, recovery from this state will take as long as 1µs.

The propagation delay does not increase significantly when driven with large differential voltages, but with low levels of overdrive, an apparent increase may be seen with large source resistances due to an RC delay caused by the 2pF typical input capacitance.

Input Protection

The input stage is protected against damage from large differential signals, up to and beyond a differential voltage equal to the supply voltage, limited only by the absolute maximum currents noted. External input protection circuitry is only needed if currents would otherwise exceed these absolute maximums. The internal catch diodes can conduct current up to these rated maximums without latchup, even when the supply voltages are at the absolute maximum ratings.

The LT1715 input stage has general purpose internal ESD protection for the human body model. For use as a line receiver, additional external protection may be required. As with most integrated circuits, the level of immunity to ESD is much greater when residing on a printed circuit board where the power supply decoupling capacitance will limit the voltage rise caused by an ESD pulse.

Input Bias Current

Input bias current is measured with both inputs held at 1V. As with any PNP differential input stage, the LT1715 bias current flows out of the device. It will go to zero on the higher of the two inputs and double on the lower of the two inputs. With more than two diode drops of differential input voltage, the LT1715's input protection circuitry activates, and current out of the lower input will increase an additional 30% and there will be a small bias current into the higher of the two input pins, of 4µA or less. See the Typical Performance curve "Input Current vs Differential Input Voltage."

High Speed Design Considerations

Application of high speed comparators is often plagued by oscillations. The LT1715 has 4mV of internal hysteresis, which will prevent oscillations as long as parasitic output to input feedback is kept below 4mV. However, with the 2V/ns slew rate of the LT1715 outputs, a 4mV step can be created at a 100Ω input source with only 0.02pF of output to input coupling. The LT1715's pinout has been arranged to minimize problems by placing the sensitive inputs away from the outputs, shielded by the power rails. The input and output traces of the circuit board should also be separated, and the requisite level of isolation is readily achieved if a topside ground plane runs between the output and the inputs. For multilayer boards where the ground plane is internal, a topside ground or supply trace should be run between the inputs and the output.

The ground pin of the LT1715 can disturb the ground plane potential while toggling due to the extremely fast on and off times of the output stage. Therefore, using a ground for input termination or filtering that is separate from the LT1715 Pin 6 ground can be highly beneficial. For example, a ground plane tied to Pin 6 and directly adjacent to a 1" long input trace can capacitively couple 4mV of disturbance into the input. In this scenario, cutting the ground plane between the GND pin and the inputs will cut the capacitance and the disturbance down substantially.

Figure 2 shows a typical topside layout of the LT1715 on such a multilayer board. Shown is the topside metal etch including traces, pin escape vias, and the land pads for an MS10 LT1715 and its adjacent X7R 10nF bypass capacitors in the 0805 case.

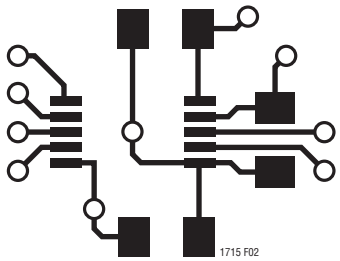


Figure 2. Typical Topside Metal for Multilayer PCB Layouts

APPLICATIONS INFORMATION

The ground trace from Pin 6 runs under the device up to the bypass capacitor, shielding the inputs from the outputs. Note the use of a common via for the LT1715 and the bypass capacitors, which minimizes interference from high frequency energy running around the ground plane or power distribution traces.

The supply bypass should include an adjacent 10nF ceramic capacitor and a 2.2µF tantalum capacitor no farther than 5cm away; use more capacitance on $+V_S$ if driving more than 4mA loads. To prevent oscillations, it is helpful to balance the impedance at the inverting and noninverting inputs; source impedances should be kept low, preferably 1kΩ or less.

The outputs of the LT1715 are capable of very high slew rates. To prevent overshoot, ringing and other problems with transmission line effects, keep the output traces shorter than 10cm, or be sure to terminate the lines to maintain signal integrity. The LT1715 can drive DC terminations of 200Ω or more, but lower characteristic impedance traces can be used with series termination or AC termination topologies.

Channel Interactions

The LT1715's two channels are designed to be entirely independent. However, at frequencies approaching and exceeding 100MHz, bond wire inductance begins to interfere with overlapping switching edges on the two channels. Figure 3 shows one channel of the comparator toggling at 100MHz with the other channel driven low with the scope set to display infinite persistence. Jitter is almost nonexistent. Figure 4 displays the same channel at 100MHz with infinite persistence, but the other channel ofthe comparator is toggling as well at frequencies swept from 60MHz to 160MHz. Jitter will occur as rising and falling edges align for any non harmonic or non fundamental frequency of the high frequency signal.

At frequencies well beyond 100MHz, the toggling of one channel may be impaired by toggling on the other. This is a rather complex interaction of supply bypassing and bond inductance, and it cannot be entirely prevented. However, good bypassing and board layout techniques will effectively minimize it.

Power Supply Sequencing

The LT1715 is designed to tolerate any power supply sequencing at system turn-on and power down. In any of the previously shown power supply configurations, the various supplies can activate in any order without excessive current drain by the LT1715.

As always, the Absolute Maximum Ratings must not be exceeded, either on the power supply terminals or the input terminals. Power supply sequencing problems can occur when input signals are powered from supplies that are independent of the LT1715's supplies. No problems should occur if the input signals are powered from the same V_{CC} and V_{EE} supplies as the LT1715.

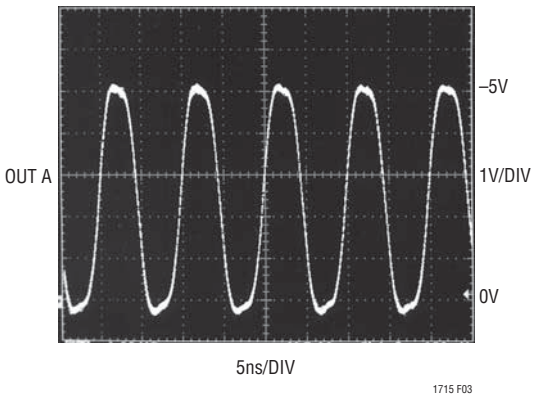


Figure 3. Clean 100MHz Toggling

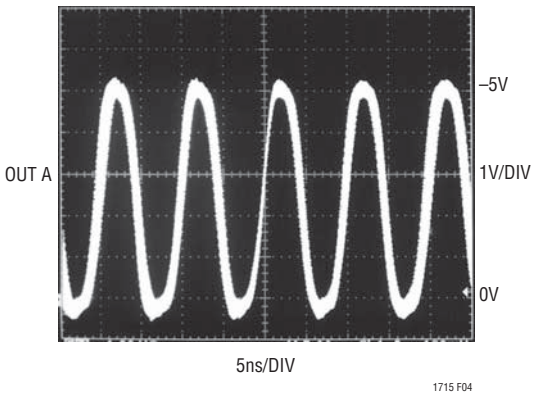


Figure 4. 100MHz Jitter with Both Channels Driven

APPLICATIONS INFORMATION

Unused Comparators

If a comparator is unused, its output should be left floatingto minimize load current. The unused inputs can be tied off to the rails and power consumption can be further minimized if the inputs are connected to the power rails to induce an output low. Connecting the inverting input to V_{CC} and the noninverting input to V_{EE} will likely be the easiest method.

Hysteresis

The LT1715 includes internal hysteresis, which makes it easier to use than many other similar speed comparators. The input-output transfer characteristic is illustrated in Figure 5 showing the definitions of V_{OS} and V_{HYST} based upon the two measurable trip points. The hysteresis band makes the LT1715 well behaved, even with slowly moving inputs.

The exact amount of hysteresis will vary from part to part as indicated in the specifications table. The hysteresis level will also vary slightly with changes in supply voltage and common mode voltage. A key advantage of the LT1715 is the significant reduction in these effects, which is important whenever an LT1715 is used to detect a threshold crossing in one direction only. In such a case, the relevant trip point will be all that matters, and a stable offset voltage with an unpredictable level of hysteresis, as seen in competing comparators, is useless. The LT1715 is many times better than prior generation comparators in these regards. In fact, the CMRR and PSRR tests are performed by checking for changes in either trip point to the limits indicated in the specifications table. Because the offset voltage is the average of the trip points, the CMRR and PSRR of the offset voltage is therefore guaranteed to be at least as good as those limits. This more stringent test also puts a limit on the common mode and power supply dependence of the hysteresis voltage.

Additional hysteresis may be added externally. The rail-to-rail outputs of the LT1715 make this more predictable than with TTL output comparators due to the LT1715's small variability of V_{OH} (output high voltage).

To add additional hysteresis, set up positive feedback by adding additional external resistor R3 as shown in Figure 6. Resistor R3 adds a portion of the output to the threshold set by the resistor string. The LT1715 pulls the outputs to $+V_S$ and ground to within 200mV of the rails with light loads, and to within 400mV with heavy loads. For the load of most circuits, a good model for the voltage on the right side of R3 is 300mV or $+V_S$ – 300mV, for a total voltage swing of ($+V_S$ – 300mV) – (300mV) = $+V_S$ – 600mV.

With this in mind, calculation of the resistor values needed is a two-step process. First, calculate the value of R3 based on the additional hysteresis desired, the output voltage swing and the impedance of the primary bias string:

$$R3 = (R1||R2)(+V_S - 0.6V)/(\text{additional hysteresis})$$

Additional hysteresis is the desired overall hysteresis less the internal 4mV hysteresis.

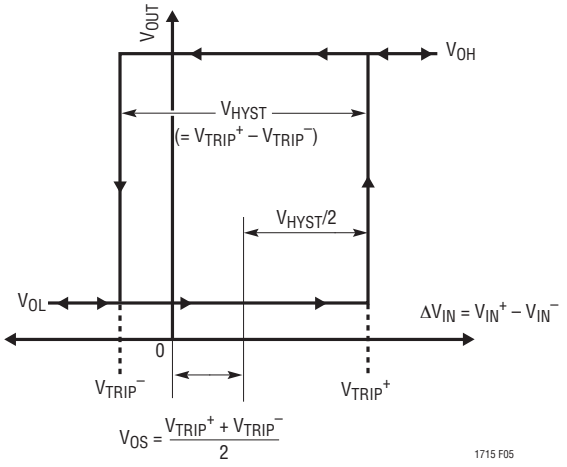


Figure 5. Hysteresis I/O Characteristics

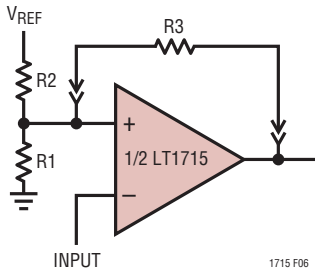


Figure 6. Additional External Hysteresis

APPLICATIONS INFORMATION

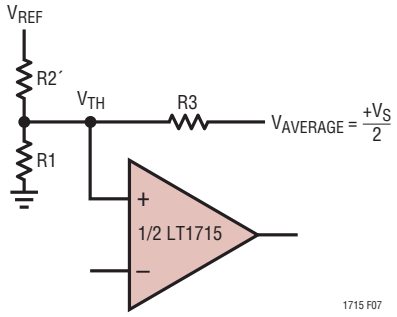


Figure 7. Model for Additional Hysteresis Calculations

The second step is to recalculate R2 to set the same average threshold as before. The average threshold before was set at $V_{TH} = (V_{REF})(R1)/(R1 + R2)$. The new R2 is calculated based on the average output voltage ($+V_S/2$)and the simplified circuit model in Figure 7. To assure that the comparator's noninverting input is, on average, the same V_{TH} as before:

$$R2' = (V_{REF} – V_{TH})/(V_{TH}/R1 + (V_{TH} – V_S/2)/R3)$$

For additional hysteresis of 10mV or less, it is not uncommon for R2´ to be the same as R2 within 1% resistor tolerances.

This method will work for additional hysteresis of up to a few hundred millivolts. Beyond that, the impedance of R3 is low enough to effect the bias string, and adjustment of R1 may also be required. Note that the currents through the R1/R2 bias string should be many times the input currents of the LT1715. For 5% accuracy, the current must be at least 20 times the input current, more for higher accuracy.

Interfacing the LT1715 to ECL

The LT1715's comparators can be used in high speed applications where Emitter-Coupled Logic (ECL) is deployed. To interface the output of the LT1715 to ECL logic inputs, standard TTL/CMOS to ECL level translators such as the 10H124, 10H424 and 100124 can be used. The secomponents come at a cost of a few nanoseconds additional delay as well as supply currents of 50mA or more, and are only available in quads. A faster, simpler and lower power translator can be constructed with resistors as shown in Figure 8.

Figure 8a shows the standard TTL to Positive ECL (PECL) resistive level translator. This translator cannot be used forthe LT1715, or with CMOS logic, because it depends on the 820Ω resistor to limit the output swing (V_{OH}) of the all-NPNTTL gate with its so-called totem-pole output. The LT1715is fabricated in a complementary bipolar process and the output stage has a PNP driver that pulls the output nearly all the way to the supply rail, even when sourcing 10mA.

Figure 8b shows a three resistor level translator for interfacing the LT1715 to ECL running off the same supply rail. No pull-down on the output of the LT1715 is needed, but pull-down R3 limits the V_{IH} seen by the PECL gate. This is needed because ECL inputs have both a minimum and maximum V_{IH} specification for proper operation. Resistor values are given for both ECL interface types; in both cases it is assumed that the LT1715 operates from the same supply rail.

Figure 8c shows the case of translating to PECL from an LT1715 powered by a 3V supply rail. Again, resistor values are given for both ECL interface types. This time four resistors are needed, although with 10KH/E, R3 is not needed. In that case, the circuit resembles the standard TTL translator of Figure 8a, but the function of the new resistor, R4, is much different. R4 loads the LT1715 output when high so that the current flowing through R1 doesn't forward bias the LT1715's internal ESD clamp diode. Although this diode can handle 20mA without damage, normal operation and performance of the output stage can be impaired above 100µA of forward current. R4 prevents this with the minimum additional power dissipation.

Finally, Figure 8d shows the case of driving standard, negative-rail, ECL with the LT1715. Resistor values are given for both ECL interface types and for both a 5V and 3V LT1715 supply rail. Again, a fourth resistor, R4 is needed to prevent the low state current from flowing out of the LT1715, turning on the internal ESD/substrate diodes. Resistor R4 again prevents this with the minimum additional power dissipation.

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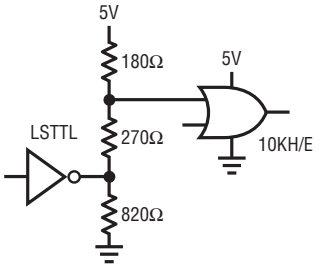
Of course, if the V_{EE} of the LT1715 is the same as the ECL negative supply, the GND pin can be tied to it as well and $+V_S$ grounded. Then the output stage has the same powerrails as the ECL and the circuits of Figure 8b can be used.

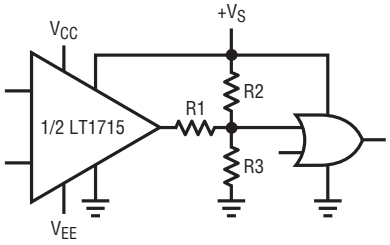
For all the dividers shown, the output impedance is about 110Ω. This makes these fast, less than a nanosecond,with most layouts. Avoid the temptation to use speed up capacitors. Not only can they foul up the operation of the ECL gate because of overshoots, they can damage the ECL inputs, particularly during power-up of separate supply configurations.

The level translator designs assume one gate load. Multiple gates can have significant I_{IH} loading, and the transmission line routing and termination issues also make this case difficult.



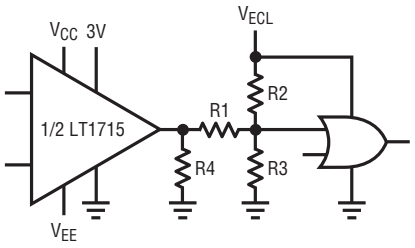
DO NOT USE FOR LT1715
LEVEL TRANSLATION. SEE TEXT

(a) STANDARD TTL TO PECL TRANSLATOR



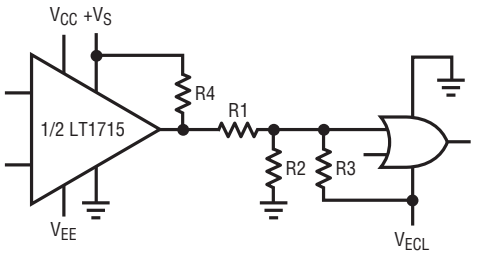
	$+V_S$	R1	R2	R3
10KH/E	5V OR 5.2V	510Ω	180Ω	750Ω
100K/E	4.5V	620Ω	180Ω	510Ω

(b) LT1715 OUTPUT TO PECL TRANSLATOR



	V_{ECL}	R1	R2	R3	R4
10KH/E	5V OR 5.2V	300Ω	180Ω	OMIT	560Ω
100K/E	4.5V	330Ω	180Ω	1500Ω	1000Ω

(c) 3V LT1715 OUTPUT TO PECL TRANSLATOR



ECL FAMILY	V_{ECL}	$+V_S$	R1	R2	R3	R4
10KH/E	–5.2V	5V	560Ω	270Ω	330Ω	1200Ω
		3V	270Ω	510Ω	300Ω	330Ω
100K/E	–4.5V	5V	680Ω	270Ω	300Ω	1500Ω
		3V	330Ω	390Ω	270Ω	430Ω

1715 F08

(d) LT1715 OUTPUT TO STANDARD ECL TRANSLATOR

Figure 8

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ECL, and particularly PECL, is valuable technology for high speed system design, but it must be used with care. With less than a volt of swing, the noise margins need to be evaluated carefully. Note that there is some degradation of noise margin due to the ±5% resistor selections shown. With 10KH/E, there is no temperature compensation of the logic levels, whereas the LT1715 and the circuits shown give levels that are stable with temperature. This will lower the noise margin over temperature. In some configurations it is possible to add compensation with diode or transistor junctions in series with the resistors of these networks.

For more information on ECL design, refer to the ECLiPS data book (DL140), the 10KH system design handbook (HB205) and PECL design (AN1406), all from Motorola, now ON Semiconductor.

Circuit Description

The block diagram of the LT1715 is shown in Figure 9. The circuit topology consists of a differential input stage, again stage with hysteresis and a complementary common-emitter output stage. All of the internal signal paths utilize low voltage swings for high speed at low power.

The input stage topology maximizes the input dynamic range available without requiring the power, complexity and die area of two complete input stages such as are found in rail-to-rail input comparators. With a single 2.7V supply, the LT1715 still has a respectable 1.6V of input common mode range. The differential input voltage rangeis rail-to-rail, without the large input currents found incompeting devices. The input stage also features phase reversal protection to prevent false outputs when the inputs are driven below the –100mV common mode voltage limit.

The internal hysteresis is implemented by positive, nonlinear feedback around a second gain stage. Until this point, the signal path has been entirely differential. The signal path is then split into two drive signals for the upper and lower output transistors. The output transistors are connected common emitter for rail-to-rail output operation. The Schottky clamps limit the output voltages at about 300mV from the rail, not quite the 50mV or 15mV of Linear Technology's rail-to-rail amplifiers and other products. But the output of a comparator is digital, and this output stage can drive TTL or CMOS directly. It can also drive ECL, as described earlier, or analog loads.

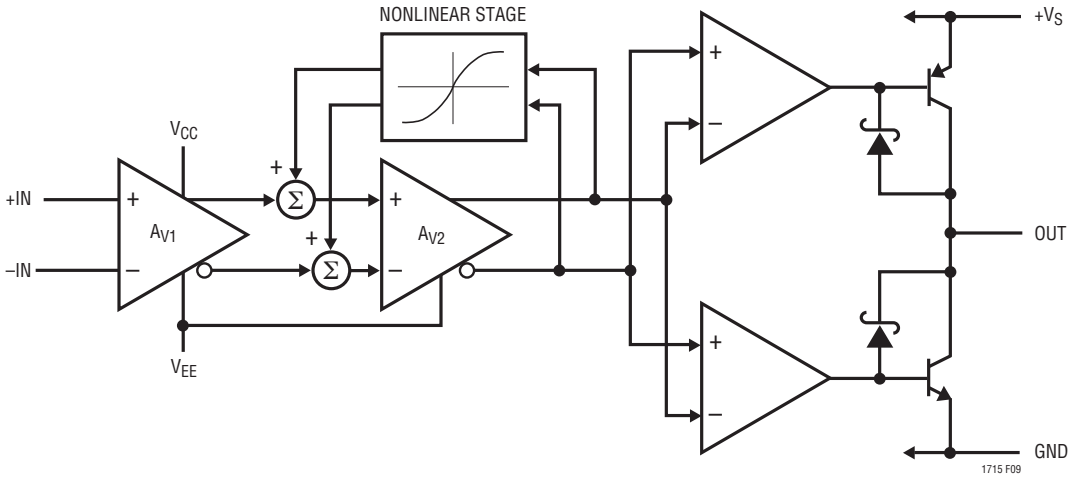

Figure 9. LT1715 Block Diagram

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The bias conditions and signal swings in the output stage are designed to turn their respective output transistors off faster than on. This helps minimize the surge of current from $+V_S$ to ground that occurs at transitions, to minimize the frequency-dependent increase in power consumption. The frequency dependence of the supply current is shown in the Typical Performance Characteristics.

Speed Limits

The LT1715 comparator is intended for high speed applications, where it is important to understand a few limitations. These limitations can roughly be divided into three categories: input speed limits, output speed limits, and internal speed limits.

There are no significant input speed limits except the shunt capacitance of the input nodes. If the 2pF typical input nodes are driven, the LT1715 will respond.

The output speed is constrained by three mechanisms, the first of which is the slew currents available from the output transistors. To maintain low power quiescent operation, the LT1715 output transistors are sized to deliver 35mA to 60mA typical slew currents. This is sufficient to drive small capacitive loads and logic gate inputs at extremely high speeds. But the slew rate will slow dramatically with heavy capacitive loads. Because the propagation delay (t_{PD}) definition ends at the time the output voltage is halfway between the supplies, the fixed slew current makes the LT1715 faster at 3V than 5V with large capacitive loads and sufficient input overdrive.

Another manifestation of this output speed limit is skew, the difference between t_{PD}^+ and t_{PD}^-. The slew currents of the LT1715 vary with the process variations of the PNP and NPN transistors, for rising edges and falling edges respectively. The typical 0.5ns skew can have either polarity, rising edge or falling edge faster. Again, the skew will increase dramatically with heavy capacitive loads.

A final limit to output speed is the turn-on and turn-off time of the output devices. Each device has substantial base charge that requires one nanosecond or more of active charging or discharging by the bias current of the Darlington driver stage. When toggle rates are high enough that insufficient time is allowed for this turn-on or turn-off, glitches may occur leading to dropout or runt pulses. Furthermore, power consumption may increase nonlinearly if devices are not turned off before the opposing cycle. However, once the toggle frequency increases or decreases, the part will easily leave this undesired operating mode no worse for the wear provided there is adequate heat sinking toprevent thermal overload. At frequencies well beyond the maximum toggle rate, the part will toggle with limited output swing and well controlled power consumption.

The internal speed limits manifest themselves as dispersion. All comparators have some degree of dispersion, defined as a change in propagation delay versus input overdrive. The propagation delay of the LT1715 will vary with overdrive, from a typical of 4ns at 20mV overdrive to 6ns at 5mV overdrive (typical). The LT1715's primary source of dispersion is the hysteresis stage. As a change of polarity arrives at the gain stage, the positive feedback of the hysteresis stage subtracts from the overdrive available. Only when enough time has elapsed for a signal to propagate forward through the gain stage, backwards through the hysteresis path and forward through the gain stage again, will the output stage receive the same level of overdrive that it would have received in the absence of hysteresis.

The LT1715 is several hundred picoseconds faster when $V_{EE} = –5V$, relative to single supply operation. This is due to the internal speed limit; the gain stage operates between V_{EE} and $+V_S$, and it is faster with higher reverse voltage bias due to reduced silicon junction capacitances.

In many applications, as shown in the following examples, there is plenty of input overdrive. Even in applications providing low levels of overdrive, the LT1715 is fast enough that the absolute dispersion of 2ns (= 6 – 4) is often small enough to ignore.

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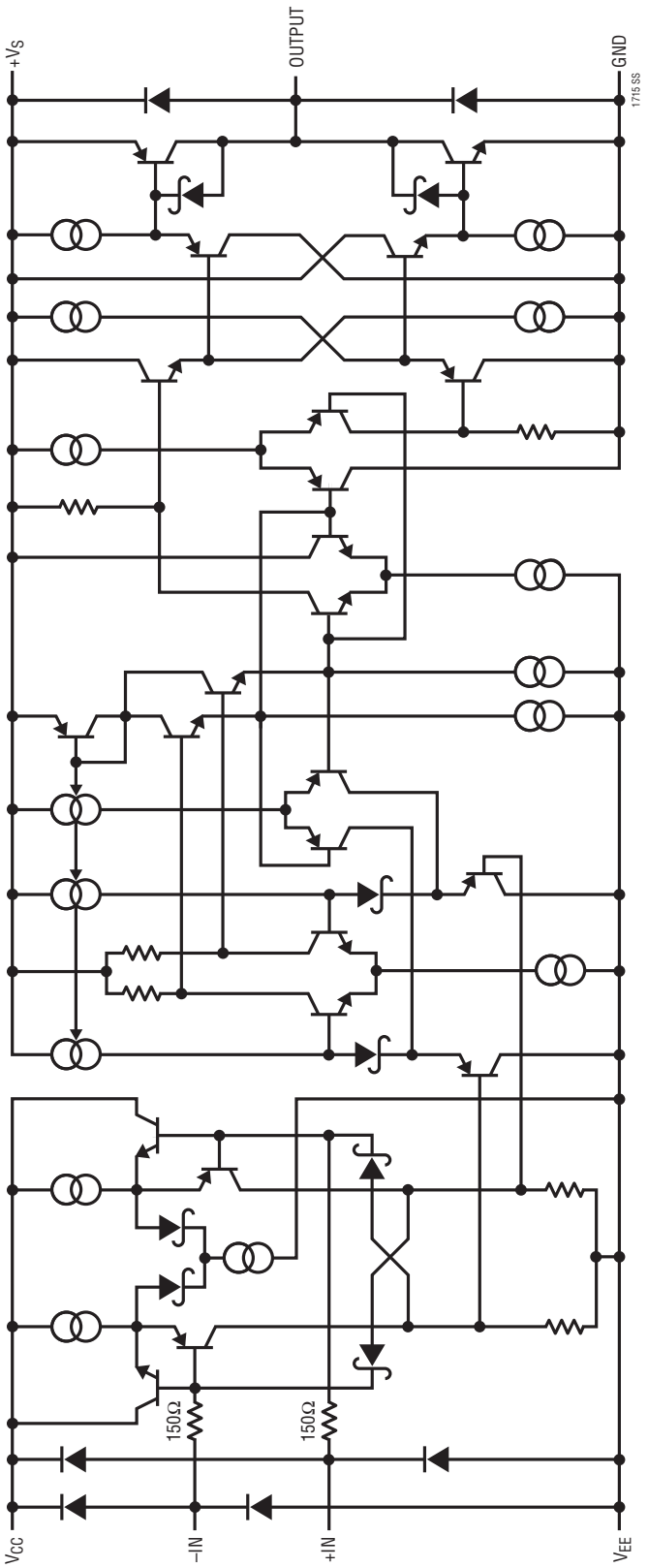
The gain and hysteresis stage of the LT1715 is simple, short and high speed to help prevent parasitic oscillations while adding minimum dispersion. This internal "self-latch" can be usefully exploited in many applications because it occurs early in the signal chain, in a low power, fully differential stage. It is therefore highly immune to disturbances from other parts of the circuit, such as the output, or on the supply lines. Once a high speed signal trips the hysteresis, the output will respond, after some propagation delay, without regard to these external influences that can cause trouble in nonhysteretic comparators.

$\pm V_{TRIP}$ Test Circuit

The input trip points test circuit uses a 1kHz triangle wave to repeatedly trip the comparator being tested. The LT1715 output is used to trigger switched capacitor sampling of the triangle wave, with a sampler for each direction.

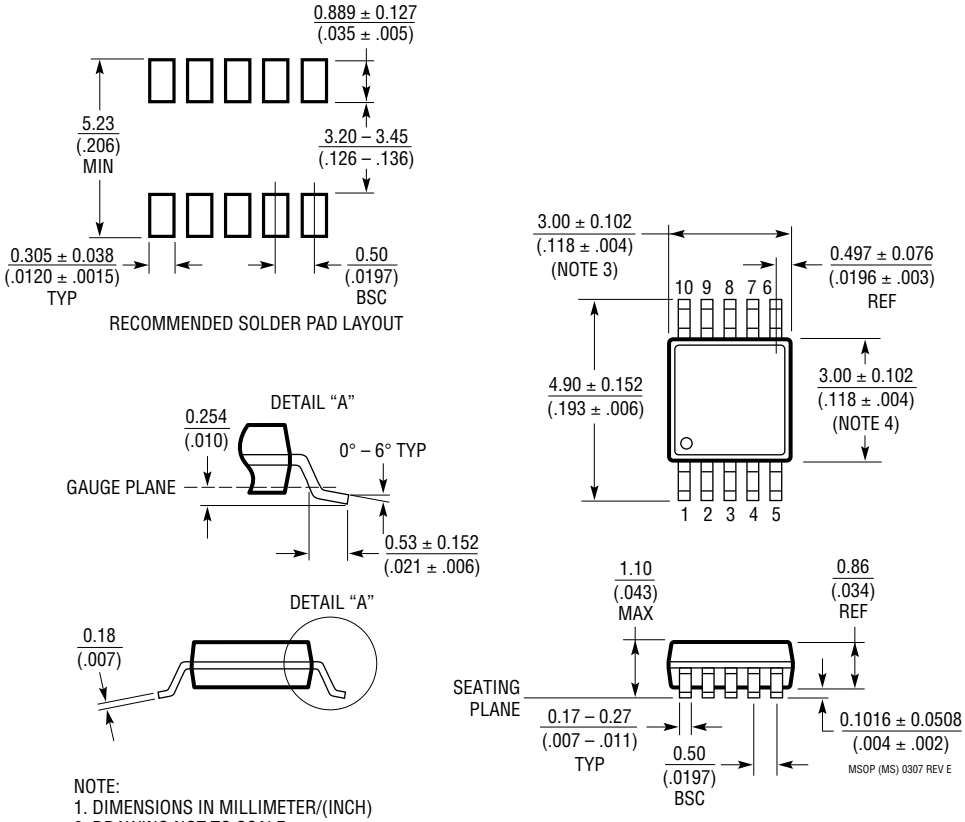
Because the triangle wave is attenuated 1000:1 and fed to the LT1715's differential input, the sampled voltages are therefore 1000 times the input trip voltages. The hysteresis and offset are computed from the trip points as shown.

SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX