4.5ns Single/Dual Supply 3V/5V Comparator with Rail-to-Rail Output

FEATURES

- **UltraFast: 4.5ns at 20mV Overdrive**
  7ns at 5mV Overdrive
- **Low Power: 4.2mA at 3V**
- Separate Input and Output Power Supplies (SO-8 Only)
- Output Optimized for 3V and 5V Supplies
- TTL/CMOS Compatible Rail-to-Rail Output
- Low Power Shutdown Mode: 0.1µA
- Low Profile (1mm) SOT-23 (ThinSOT™) Package

APPLICATIONS

- High Speed Differential Line Receiver
- Crystal Oscillator Circuits
- Level Translators
- Threshold Detectors/Discriminators
- Zero-Crossing Detectors
- High Speed Sampling Circuits
- Delay Lines

DESCRIPTION

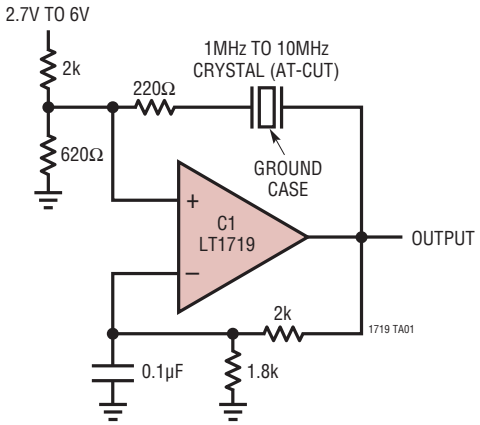
The LT®1719 is an UltraFast™ comparator optimized for low voltage operation. The input voltage range extends from 100mV below V_{EE} to 1.2V below V_{CC}. Internal hysteresis makes the LT1719 easy to use even with slow moving input signals. The rail-to-rail outputs directly interface to TTL and CMOS. Alternatively the symmetric output drive can be harnessed for analog applications or for easy translation to other single supply logic levels. A shutdown control allows for reduced power consumption and extended battery life in portable applications.

The LT1719 is available in the SO-8 and 6-lead SOT-23 package. The SO-8 package has separate supplies which allow flexible operation, accomodating separate analog input ranges and output logic levels.

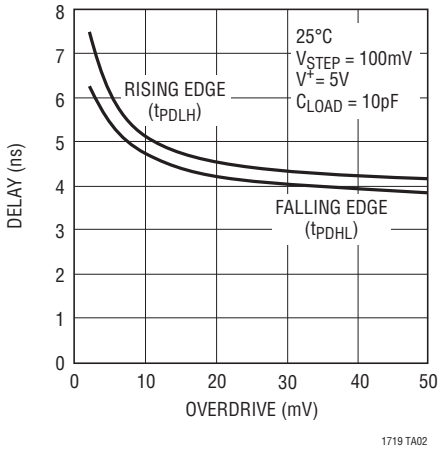
For a dual/quad comparator with similar performance, see the LT1720/LT1721.

TYPICAL APPLICATION

2.7V to 6V Crystal Oscillator with TTL/CMOS Output



Propagation Delay vs Overdrive



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- $+V_S$ to GND (LT1719S8) 7V
- V_{CC} to V_{EE} (LT1719S8) 12V
- $+V_S$ to V_{EE} (LT1719S8) 12V
- V_{EE} to GND (LT1719S8) ..... –12V to 0.3V
- V^+ to V^- (LT1719S6) 7V

Input Current (+IN, –IN or SHDN)..... ±10mA

Output Current (Continuous) ..... ±20mA

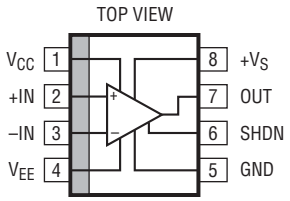
Operating Temperature Range
- C-Grade ..... 0°C to 70°C
- I-Grade ..... –40°C to 85°C

Junction Temperature ..... 150°C

Storage Temperature Range..... –65°C to 150°C

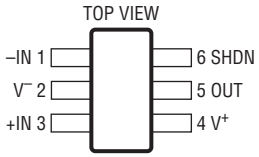
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 110°C/W



S6 PACKAGE
6-LEAD PLASTIC TSOT-23

T_{JMAX} = 150°C, θ_{JA} = 230°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1719CS8#PBF	LT1719CS8#TRPBF	1719	8-Lead Plastic SO	0°C to 70°C
LT1719IS8#PBF	LT1719IS8#TRPBF	1719I	8-Lead Plastic SO	–40°C to 85°C
LT1719CS6#PBF	LT1719CS6#TRPBF	LTHW	6-Lead Plastic TSOT-23	0°C to 70°C
LT1719IS6#PBF	LT1719IS6#TRPBF	LTJF	6-Lead Plastic TSOT-23	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CM} = 1V, V_{SHDN} = 0.5V, $V_{OVERDRIVE}$ = 20mV, C_{OUT} = 10pF and for the LT1719S8 V_{CC} = $+V_S$ = 5V and V_{EE} = –5V, for the LT1719S6 V^+ = 5V, V^- = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CC} – V_{EE}$	Input Supply Voltage	(LT1719S8 Only)	●	2.7		10.5	V
$+V_S$	Output Supply Voltage	(LT1719S8 Only)	●	2.7		6	V
$V^+ – V^-$	Supply Voltage	(LT1719CS6 Only)	●	2.7		6	V
V_{CMR}	Input Voltage Range	(Note 2) (LT1719S8) (LT1719S6)	● ●	V_{EE} – 0.1 V^- – 0.1		V_{CC} – 1.2 V^+ – 1.2	V V
V_{TRIP}^+ V_{TRIP}^-	Input Trip Points	(Note 3)	● ●	–1.5 –5.5		5.5 1.5	mV mV
V_{OS}	Input Offset Voltage	(Note 3)	 ●		0.4	2.5 3.5	mV mV
V_{HYST}	Input Hysteresis Voltage	(Note 3)	●	2.0	3.5	7	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift		●		10		µV/°C
I_B	Input Bias Current		●	–6	–2.5	0	µA
I_{OS}	Input Offset Current		●		0.2	0.6	µA
CMRR	Common Mode Rejection Ratio	(Note 4) (LT1719S8) (Note 5) (LT1719S6)	● ●	55 55	70 65		dB dB
PSRR	Power Supply Rejection Ratio	(Note 6) (LT1719S8) (Note 7) (LT1719S6)		65 65	80 80		dB dB
A_V	Voltage Gain	(Note 8)			∞		
V_{OH}	Output High Voltage	I_{SOURCE} = 4mA, V_{IN} = V_{TRIP}^+ + 10mV (LT1719S8) (LT1719S6)	● ●	$+V_S$ – 0.4 V^+ – 0.4			V V
V_{OL}	Output Low Voltage	I_{SINK} = 10mA, V_{IN} = V_{TRIP}^- – 10mV	●			0.4	V
t_{PD20}	Propagation Delay	$V_{OVERDRIVE}$ = 20mV (Note 9) V_{EE} = 0V(LT1719S8) V^- = 0V(LT1719S6)	 ●		4.5	6.5 8.0	ns ns
		$V_{OVERDRIVE}$ = 20mV, V_{EE} = –5V (LT1719S8 Only)			4.2		ns
t_{PD5}	Propagation Delay	$V_{OVERDRIVE}$ = 5mV (Notes 9, 10) V_{EE} = 0V(LT1719S8) V^- = 0V(LT1719S6)	 ●		7	10 13	ns ns
t_{SKEW}	Propagation Delay Skew	(Note 11)			0.5	1.5	ns
t_r	Output Rise Time	10% to 90%			2.5		ns
t_f	Output Fall Time	90% to 10%			2.2		ns
t_{JITTER}	Output Timing Jitter	V_{IN} = 1.2V_{P-P} (6dBm), Z_{IN} = 50Ω t_{PD}^+ f = 20MHz t_{PD}^-			15 11		ps_{RMS} ps_{RMS}
f_{MAX}	Maximum Toggle Frequency	$V_{OVERDRIVE}$ = 50mV, $+V_S$ or V^+ = 3V $V_{OVERDRIVE}$ = 50mV, $+V_S$ or V^+ = 5V			70 62.5		MHz MHz
t_{OFF}	Turn-Off Delay	Time to Z_{OUT} ≥10kΩ			75		ns
t_{ON}	Wake-Up Delay	Time to V_{OH} or V_{OL}, I_{LOAD} = 1mA			350		ns
I_{CC}	Positive Input Stage Supply Current	$+V_S$ = V_{CC} = 5V, V_{EE} = –5V	●		1	2.2	mA
	(LT1719S8 Only)	$+V_S$ = V_{CC} = 3V, V_{EE} = 0V	●		0.9	1.8	mA
I_{EE}	Negative Input Stage Supply Current	$+V_S$ = V_{CC} = 5V, V_{EE} = –5V	●	–4.8	–2.6		mA
	(LT1719S8 Only)	$+V_S$ = V_{CC} = 3V, V_{EE} = 0V	●	–3.8	–2.2		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CM} = 1V, V_{SHDN} = 0.5V, $V_{OVERDRIVE}$ = 20mV, C_{OUT} = 10pF and for the LT1719S8 V_{CC} = +V_S = 5V and V_{EE} = –5V, for the LT1719S6 V^+ = 5V, V^- = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_S	Positive Output Stage Supply Current	+V_S = V_{CC} = 5V, V_{EE} = –5V	●		4.2	8	mA
	(LT1719S8 Only)	V_S = V_{CC} = 3V, V_{EE} = 0V	●		3.3	6	mA
I^+	Supply Current (LT1719S6)	V^+ = 5V	●		4.6	9	mA
		V^+ = 3V	●		4.2	7	mA
I_{SHDN5}	Shutdown Pin Current	+V_S or V^+ = 5V	●	–300	–110	–30	µA
I_{SHDN3}	Shutdown Pin Current	+V_S or V^+ = 3V	●	–200	–80	–20	µA
I_{CCS}	Disabled Supply Currents (LT1719S8)	+V_S = 6V, V_{CC} = 5V, V_{EE} = –5V	●		0.2	30	µA
I_{SS}	(LT1719S8)	V_{SHDN} = +V_S – 0.5V	●		7	50	µA
I_{EES}	(LT1719S8)		●	–30	–0.2		µA
I^+_S	(LT1719S6)	V^+ = 6V, V_{SHDN} = +V_S – 0.5V	●		7	80	µA
I_{CCSO}	(LT1719S8)	+V_S = 6V, V_{CC} = 5V, V_{EE} = –5V	●		0.1	20	µA
I_{SSO}	(LT1719S8)	Shutdown Pin Open	●		0.1	20	µA
I_{EEO}	(LT1719S8)		●	–20	0.1		µA
I^+_O	(LT1719S6)	V^+ = 6V, Shutdown Pin Open	●		0.2	40	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: If one input is within these common mode limits, the other input can go outside the common mode limits and the output will be valid.

Note 3: The LT1719 comparator includes internal hysteresis. The trip points are the input voltage needed to change the output state in each direction. The offset voltage is defined as the average of V_{TRIP}^+ and V_{TRIP}^-, while the hysteresis voltage is the difference of these two.

Note 4: The LT1719S8 common mode rejection ratio is measured with V_{CC} = 5V, V_{EE} = –5V and is defined as the change in offset voltage measured from V_{CM} = –5.1V to V_{CM} = 3.8V, divided by 8.9V.

Note 5: The LT1719S6 common mode rejection ratio is measured with V^+ = 5V and is defined as the change in offset voltage measured from V_{CM} = –0.1V to V_{CM} = 3.8V, divided by 3.9V.

Note 6: The LT1719S8 power supply rejection ratio is measured with V_{CM} = 1V and is defined as the worst of: the change in offset voltage from V_{EE} = –5.5V to V_{EE} = 0V divided by 5.5V, or the change in offset voltage from V_{CC} = +V_S = 2.7V to V_{CC} = +V_S = 6V (with V_{EE} = 0V) divided by 3.3V.

Note 7: The LT1719S6 power supply rejection ratio is measured with V_{CM} = 1V and is defined as the change in offset voltage measured from V^+ = 2.7V to V^+ = 6V, divided by 3.3V.

Note 8: Because of internal hysteresis, there is no small-signal region in which to measure gain. Proper operation of internal circuity is ensured by measuring V_{OH} and V_{OL} with only 10mV of overdrive.

Note 9: Propagation delay measurements made with 100mV steps. Overdrive is measured relative to $V_{TRIP}^{\pm}$.

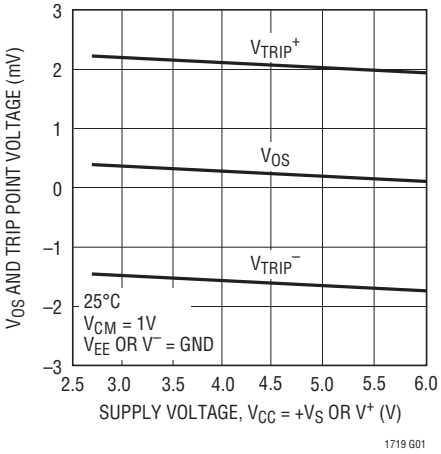
Note 10: t_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The LT1719 is 100% tested with a 100mV step and 20mV overdrive. Correlation tests have shown that t_{PD} limits can be guaranteed with this test, if additional DC tests are performed to guarantee that all internal bias conditions are correct.

Note 11: Propagation Delay Skew is defined as:

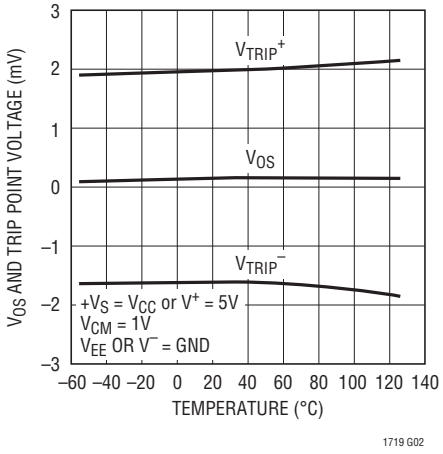
$$t_{SKEW} = |t_{PDLH} - t_{PDHL}|$$

TYPICAL PERFORMANCE CHARACTERISTICS

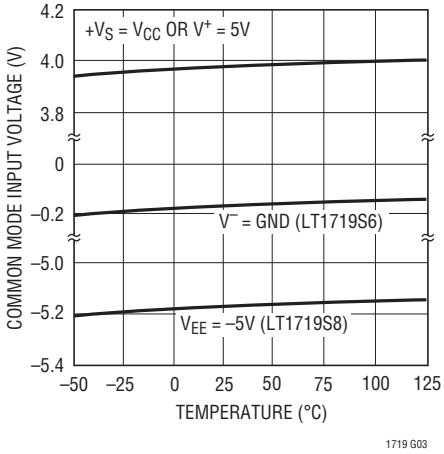
Input Offset and Trip Voltages vs Supply Voltage



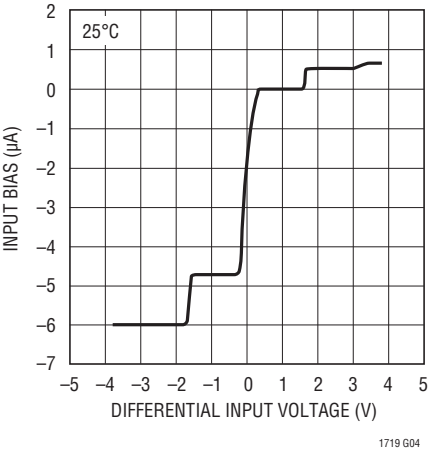
Input Offset and Trip Voltages vs Temperature



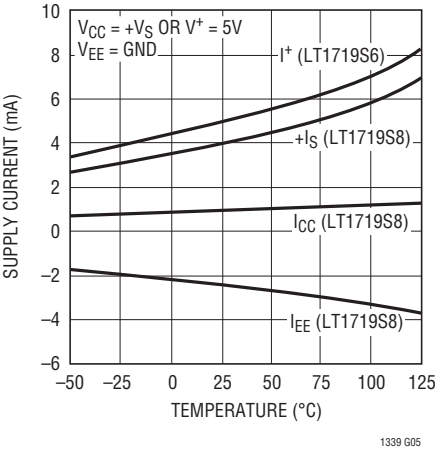
Input Common Mode Limits vs Temperature



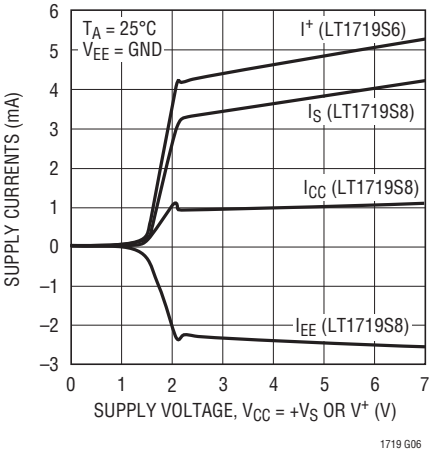
Input Current vs Differential Input Voltage



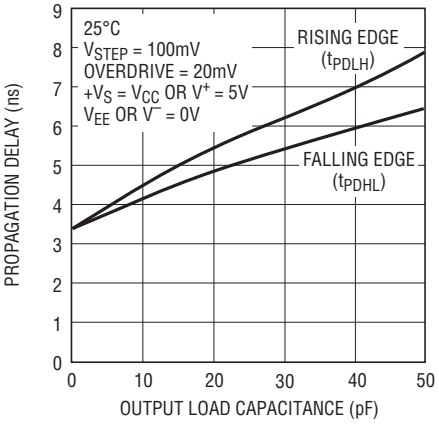
Quiescent Supply Current vs Temperature



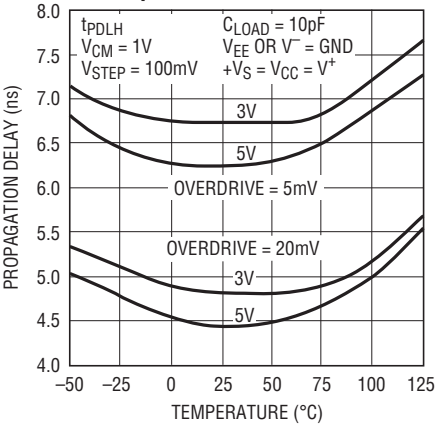
Quiescent Supply Current vs Supply Voltage



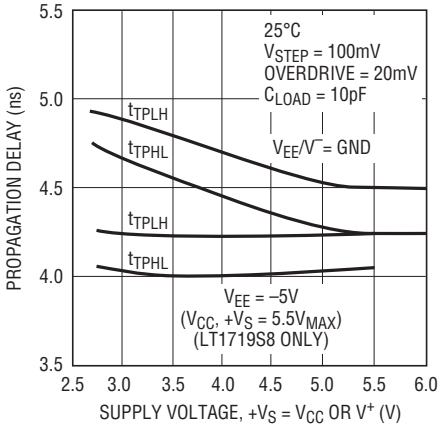
Propagation Delay vs Load Capacitance



Propagation Delay vs Temperature

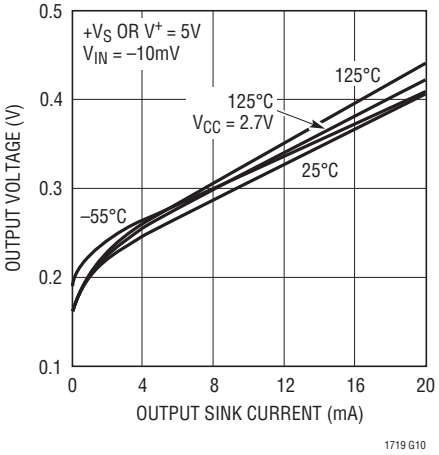


Propagation Delay vs Supply Voltage



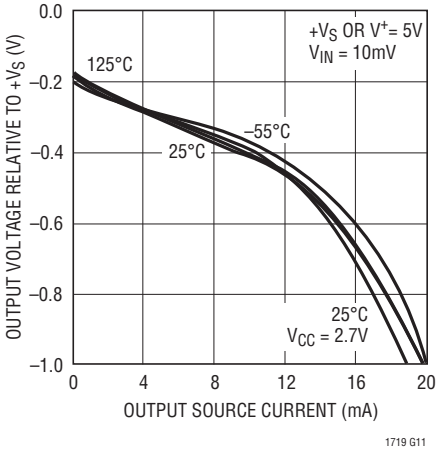
TYPICAL PERFORMANCE CHARACTERISTICS

Output Low Voltage vs Load Current



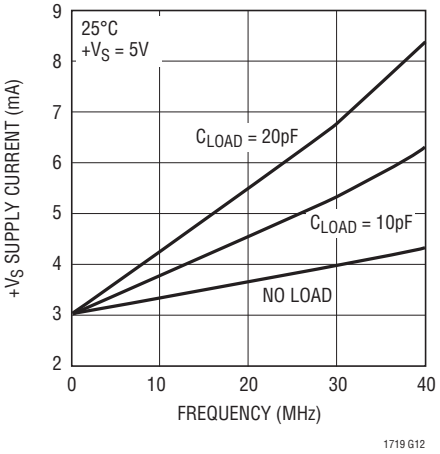
1719 G10

Output High Voltage vs Load Current



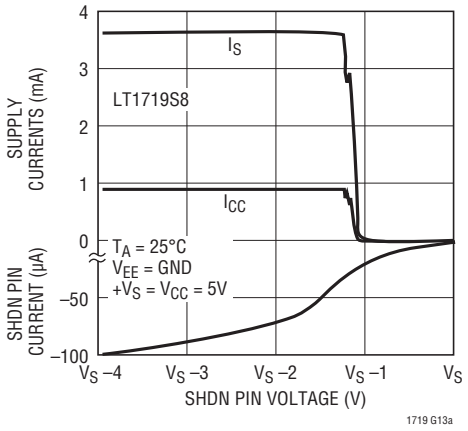
1719 G11

Supply Current vs Frequency



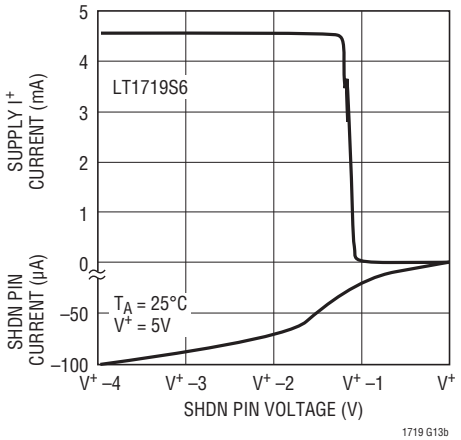
1719 G12

Shutdown Currents vs Shutdown Voltage



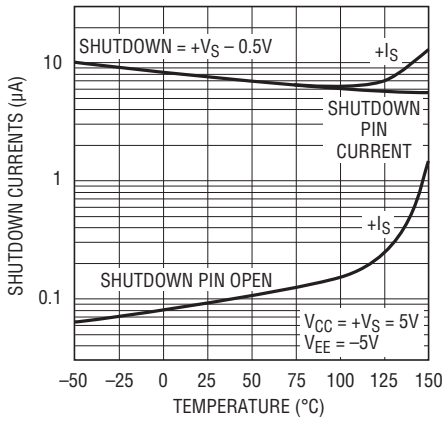
1719 G13a

Shutdown Currents vs Shutdown Voltage



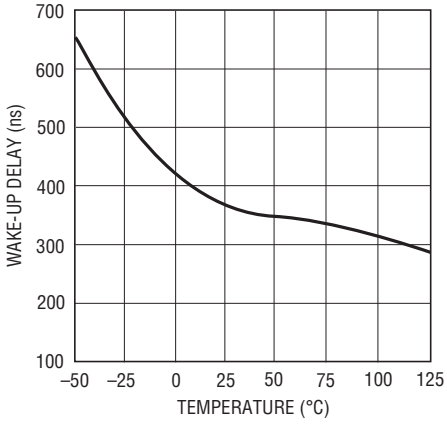
1719 G13b

Shutdown Currents vs Temperature



1719 G14

Wake-Up Delay vs Temperature



1719 G15

PIN FUNCTIONS

LT1719S8

V_{CC} (Pin 1): Positive Supply Voltage for Input Stage.

+IN (Pin 2): Noninverting Input of Comparator.

–IN (Pin 3): Inverting Input of Comparator.

V_{EE} (Pin 4): Negative Supply Voltage for Input Stage and Chip Substrate.

GND (Pin 5): Ground.

SHDN (Pin 6): Shutdown. Pull to ground to enable comparator.

OUT (Pin 7): Output of Comparator.

+V_S (Pin 8): Positive Supply Voltage for Output Stage.

LT1719S6

–IN (Pin 1): Inverting Input of Comparator.

V^- (Pin 2): Negative Supply, Usually Grounded.

+IN (Pin3): Noninverting Input of Comparator.

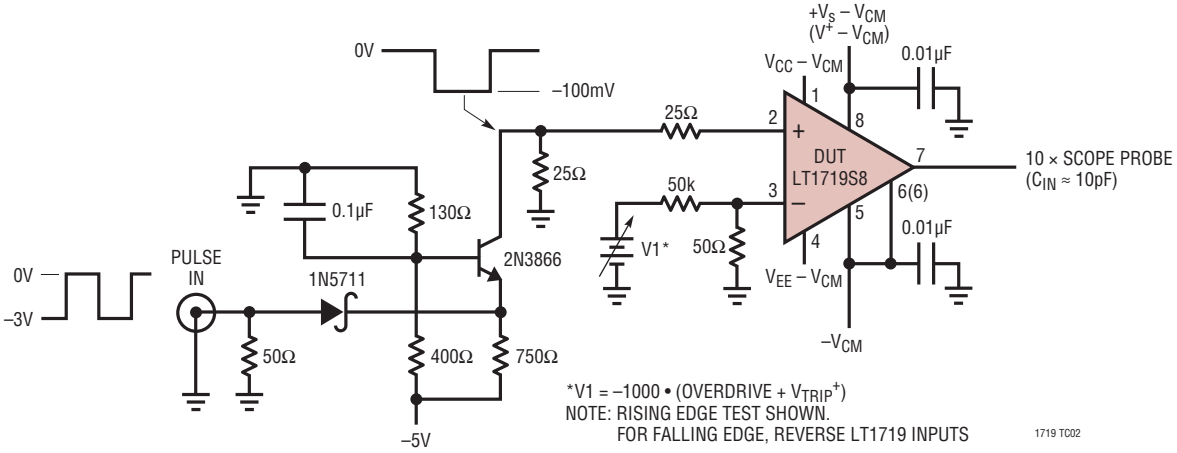
V^+ (Pin 4): Positive Supply Voltage.

OUT (Pin 5): Output of Comparator.

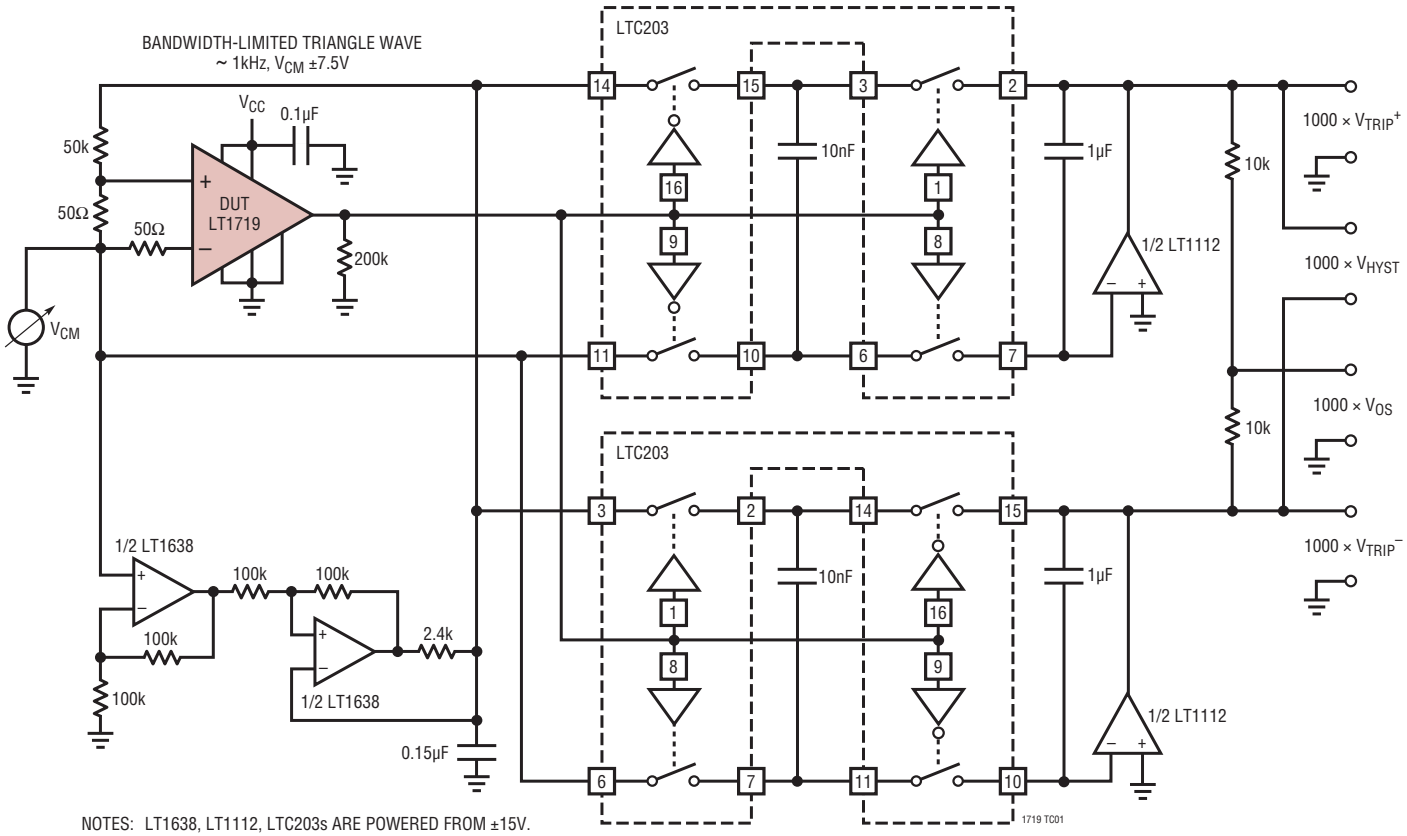
SHDN (Pin 6): Shutdown. Pull to ground to enable comparator.

TEST CIRCUITS

Response Time Test Circuit



±V_{TRIP} Test Circuit



NOTES: LT1638, LT1112, LTC203s ARE POWERED FROM ±15V.
200kΩ PULL-DOWN PROTECTS LTC203 LOGIC INPUTS
WHEN DUT IS NOT POWERED

APPLICATIONS INFORMATION

Power Supply Configurations (SO-8 Package)

The LT1719S8 has separate supply pins for the input and output stages that allow flexible operation, accommodating separate voltage ranges for the analog input and the output logic. Of course, a single 3V/5V supply may be used by tying $+V_S$ and V_{CC} together as well as GND and V_{EE}.

The minimum voltage requirement can be simply stated as both the output and the input stages need at least 2.7V and the V_{EE} pin must be equal to or less than ground.

The following rules must be adhered to in any configuration:

$2.7V \le (V_{CC} - V_{EE}) \le 10.5V$

$2.7V \le (+V_S - GND) \le 6V$

$(+V_S - V_{EE}) \le 10.5V$

$V_{EE} \le Ground$

Although the ground pin need not be tied to system ground, most applications will use it that way. Figure 1 shows three common configurations. The final one is uncommon, but it will work and may be useful as a level translator; the input stage is run from –5.2V and ground while the output stage is run from 3V and ground. In this case the common mode input voltage range does not include ground, so it may be helpful to tie V_{CC} to 3V anyway. Conversely, V_{CC} may also be tied below ground, as long as the above rules are not violated.

Input Voltage Considerations

The LT1719 is specified for a common mode range of –100mV to 3.8V when used with a single 5V supply. A more general consideration is that the common mode range is 100mV below V_{EE}/V^- to 1.2V below V_{CC}/V^+. The criterion for this common mode limit is that the output still responds correctly to a small differential input signal. If one input is within the common mode limit, the other input signal can go outside the common mode limits, up to the absolute maximum limits, and the output will retain the correct polarity.

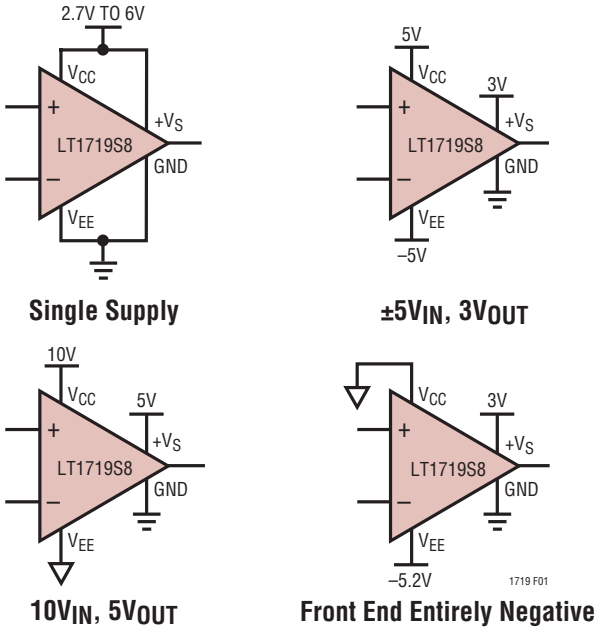


Figure 1. Variety of SO-8 Power Supply Configurations

When either input signal falls below the negative common mode limit, the internal PN diode formed with the substrate can turn on, resulting in significant current flow through the die. An external Schottky clamp diode between the input and the negative rail can speed up recovery from negative overdrive by preventing the substrate diode from turning on.

When both input signals are below the negative common mode limit, phase reversal protection circuitry prevents false output inversion to at least –400mV common mode. However, the offset and hysteresis in this mode will increase dramatically, to as much as 15mV each. The input bias currents will also increase.

When both input signals are above the positive common mode limit, the input stage will get debiased and the output polarity will be random. However, the internal hysteresis will hold the output to a valid logic level. When at least one of the inputs returns to within the common mode limits, recovery from this state can take as long as 1µs.

APPLICATIONS INFORMATION

The propagation delay does not increase significantly when driven with large differential voltages, but with low levels of overdrive, an apparent increase may be seen with large source resistances due to an RC delay caused by the 2pF typical input capacitance.

Input Protection

The input stage is protected against damage from large differential signals, up to and beyond a differential voltage equal to the supply voltage, limited only by the absolute maximum currents noted. External input protection circuitry is only needed if currents would otherwise exceed these absolute maximums. The internal catch diodes can conduct current up to these rated maximums without latchup, even when the supply voltage is at the absolute maximum rating.

The LT1719 input stage has general purpose internal ESD protection for the human body model. For use as a line receiver, additional external protection may be required. As with most integrated circuits, the level of immunity to ESD is much greater when residing on a printed circuit board where the power supply decoupling capacitance will limit the voltage rise caused by an ESD pulse.

Input Bias Current

Input bias current is measured with both inputs held at 1V. As with any PNP differential input stage, the LT1719 bias current flows out of the device. It will go to zero on the higher of the two inputs and double on the lower of the two inputs. With more than two diode drops of differential input voltage, the LT1719's input protection circuitry activates, and current out of the lower input will increase an additional 30% and there will be a small bias current into the higher of the two input pins, of 4µA or less. See the Typical Performance curve Input Current vs Differential Input Voltage.

High Speed Design Considerations

Application of high speed comparators is often plagued by oscillations. The LT1719 has 4mV of internal hysteresis, which will prevent oscillations as long as parasitic output to input feedback is kept below 4mV. However, with the 2V/ns slew rate of the LT1719 outputs, a 4mV step can be created at a 100Ω input source with only 0.02pF of output to input coupling. The LT1719's pinout has been arranged to minimize problems by placing the sensitive inputs away from the outputs, shielded by the power rails. The input and output traces of the circuit board should also be separated, and the requisite level of isolation is readily achieved if a topside ground plane runs between the output and the inputs. For multilayer boards where the ground plane is internal, a topside ground or supply trace should be run between the inputs and the output.

Figure 2 shows a typical topside layout of the LT1719S8 on such a multilayer board. Shown is the topside metal etch including traces, pin escape vias, and the land pads for an SO-8 LT1719 and its adjacent X7R 10nF bypass capacitors in the 1206 case. The same principles should be used with the SOT 23-6.

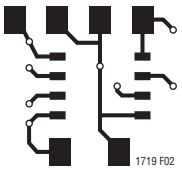


Figure 2. Typical Topside Metal for Multilayer PCB Layouts

The ground trace from Pin 5 runs under the device up to the bypass capacitor, shielding the inputs from the outputs. Note the use of a common via for the LT1719 and the bypass capacitors, which minimizes interference from high frequency energy running around the ground plane or power distribution traces.

The supply bypass should include an adjacent 10nF ceramic capacitor and a 2.2µF tantalum capacitor no farther than 5cm away; use more capacitance on $+V_S$ if driving more than 4mA loads. To prevent oscillations, it is helpful to balance the impedance at the inverting and noninverting inputs; source impedances should be kept low, preferably 1kΩ or less.

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The outputs of the LT1719 are capable of very high slew rates. To prevent overshoot, ringing and other problems with transmission line effects, keep the output traces shorter than 10cm, or be sure to terminate the lines to maintain signal integrity. The LT1719 can drive DC terminations of 200Ω or more, but lower characteristic impedance traces can be used with series termination or AC termination topologies.

Shutdown Control

The LT1719 features a shutdown control pin for reduced quiescent current when the comparator is not needed. During shutdown, the inputs and the outputs become high impedances. The LT1719 is enabled when the shutdown input is pulled low with a threshold roughly two diode drops below $+V_S$ or V^+. Therefore, if driven by a standard TTL gate, a pull-up resistor should be used. Because shutdown is active high, this resistor adds little power drain during shutdown. A logic high disables the comparator. The LT1719S8 logic interface is based on the output power rails, $+V_S$ and GND.

For applications that do not use the shutdown feature, it may be helpful to tie the shutdown control to ground through a 100Ω resistor rather than directly. This allows the SHDN pin to be pulled high during debug or in-circuit test (bed of nails) so that the output node can be wiggled without damaging the low impedance output driver of the LT1719.

The shutdown state is not guaranteed to be useful as a multiplexer. Digital signals can have extremely fast edge rates that may be enough to momentarily activate the LT1719 output stage via internal capacitive coupling. No damage to the LT1719 will result, but this could prove deleterious to the intended recipient of the signal.

The LT1719 includes a FET pull-up on the shutdown control pin (see the Simplified Schematic) as well as other internal structures to make the shutdown state current drain <<1µA. Shutdown is guaranteed with an open circuit on the shutdown control pin. When the shutdown control pin is driven to $+V_S/V^+ – 0.5V$, the 70kΩ linear region impedance of the pull-up FET will cause a current flow of 7µA (typ) into the $+V_S/V^+$ pin and out the shutdown pin. Currents in all other power supply terminals will be <1µA.

Power Supply Sequencing

The LT1719S8 is designed to tolerate any power supply sequencing at system turn-on and power down. In any of the previously shown power supply configurations, the various supplies can activate in any order without excessive current drain by the LT1719.

As always, the Absolute Maximum Ratings must not be exceeded, either on the power supply terminals or the input terminals. Power supply sequencing problems can occur when input signals are powered from supplies that are independent of the LT1719's supplies. For the comparator inputs, the signals should be powered from the same V_{CC} and V_{EE} supplies as the LT1719. For the shutdown input, the signal should be powered from the same $+V_S$ as the LT1719.

Hysteresis

The LT1719 includes internal hysteresis, which makes it easier to use than many other similar speed comparators.

The input-output transfer characteristic is illustrated in Figure 3 showing the definitions of V_{OS} and V_{HYST} based upon the two measurable trip points. The hysteresis band makes the LT1719 well behaved, even with slowly moving inputs.

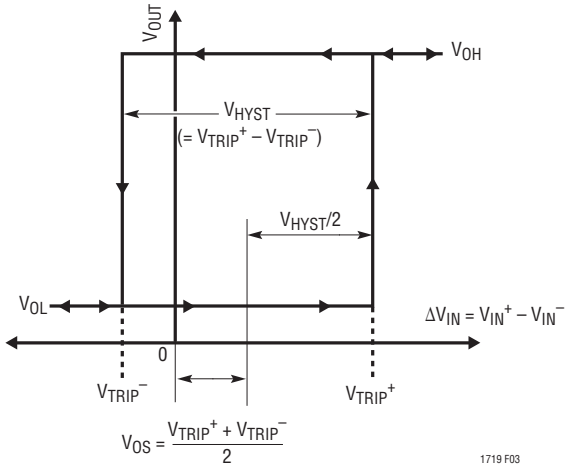


Figure 3. Hysteresis I/O Characteristics

APPLICATIONS INFORMATION

The exact amount of hysteresis will vary from part to part as indicated in the specifications table. The hysteresis level will also vary slightly with changes in supply voltage and common mode voltage. A key advantage of the LT1719 is the significant reduction in these effects, which is important whenever an LT1719 is used to detect a threshold crossing in one direction only. In such a case, the relevant trip point will be all that matters, and a stable offset voltage with an unpredictable level of hysteresis, as seen in competing comparators, is useless. The LT1719 is many times better than prior comparators in these regards. In fact, the CMRR and PSRR tests are performed by checking for changes in either trip point to the limits indicated in the specifications table. Because the offset voltage is the average of the trip points, the CMRR and PSRR of the offset voltage is therefore guaranteed to be at least as good as those limits. This more stringent test also puts a limit on the common mode and power supply dependence of the hysteresis voltage.

Additional hysteresis may be added externally. The rail-to-rail outputs of the LT1719 make this more predictable than with TTL output comparators due to the LT1719's small variability of V_{OH} (output high voltage).

To add additional hysteresis, set up positive feedback by adding additional external resistor R3 as shown in Figure 4. Resistor R3 adds a portion of the output to the threshold set by the resistor string. The LT1719 pulls the outputs to $+V_S$ and ground to within 200mV of the rails with light loads, and to within 400mV with heavy loads. For the load of most circuits, a good model for the voltage on the right side of R3 is 300mV or $+V_S$ – 300mV, for a total voltage swing of ($+V_S$ – 300mV) – (300mV) = $+V_S$ – 600mV.

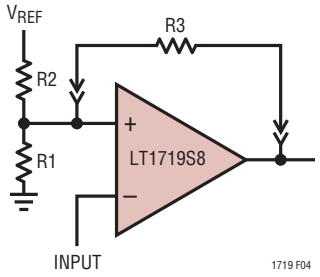


Figure 4. Additional External Hysteresis

APPLICATIONS INFORMATION

With this in mind, calculation of the resistor values needed is a two-step process. First, calculate the value of R3 based on the additional hysteresis desired, the output voltage swing and the impedance of the primary bias string:

$$R3 = (R1 \,||\, R2)(+V_S - 0.6V)/(\text{additional hysteresis})$$

Additional hysteresis is the desired overall hysteresis less the internal 4mV hysteresis.

The second step is to recalculate R2 to set the same average threshold as before. The average threshold before was set at $V_{TH} = (V_{REF})(R1)/(R1 + R2)$. The new R2 is calculated based on the average output voltage $(+V_S/2)$ and the simplified circuit model in Figure 5. To assure that the comparator's noninverting input is, on average, the same V_{TH} as before:

$$R2' = (V_{REF} - V_{TH})/(V_{TH}/R1 + [V_{TH} - (+V_S)/2]/R3)$$

For additional hysteresis of 10mV or less, it is not uncommon for R2′ to be the same as R2 within 1% resistor tolerances.

This method will work for additional hysteresis of up to a few hundred millivolts. Beyond that, the impedance of R3 is low enough to effect the bias string, and adjustment of R1 may also be required. Note that the currents through the R1/R2 bias string should be many times the input currents of the LT1719. For 5% accuracy, the current must be at least 20 times the input current, more for higher accuracy. This illustration used an LT1719S8; with an LT1719S6 the same procedure is used with V^+ substituted for $+V_S$.

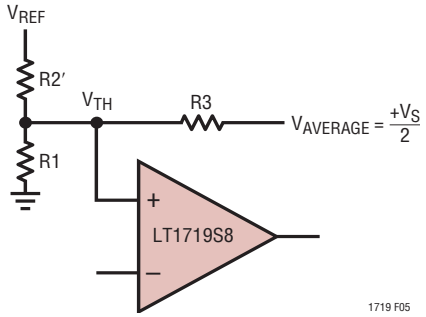


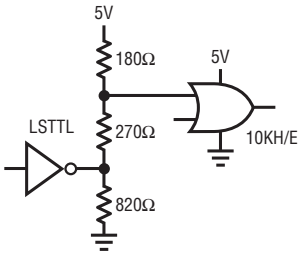
Figure 5. Model for Additional Hysteresis Calculations

APPLICATIONS INFORMATION

Interfacing the LT1719 to ECL

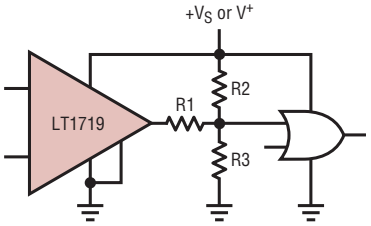
The LT1719 comparators can be used in high speed applications where emitter-coupled logic (ECL) is deployed. To interface the output of the LT1719 to ECL logic inputs, standard TTL/CMOS to ECL level translators such as the 10H124, 10H424 and 100124 can be used. These components come at a cost of a few nanoseconds additional delay as well as supply currents of 50mA or more, and are only available in quads. A faster, simpler and lower power translator can be constructed with resistors as shown in Figure 6.

Figure 6a shows the standard TTL to Positive ECL (PECL) resistive level translator. This translator cannot be used for the LT1719, or with CMOS logic, because it depends on the 820Ω resistor to limit the output swing (V_{OH}) of the all-NPN TTL gate with its so-called totem-pole output. The LT1719 is fabricated in a complementary bipolar process and the output stage has a PNP driver that pulls the output nearly all the way to the supply rail, even when sourcing 10mA.



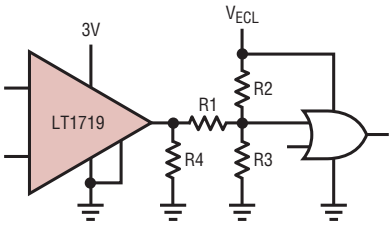
DO NOT USE FOR LT1719
LEVEL TRANSLATION. SEE TEXT

(a) STANDARD TTL TO PECL TRANSLATOR



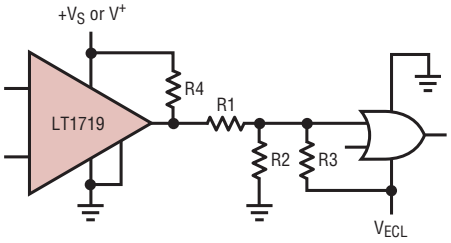
	+V_S OR V^+	R1	R2	R3
10KH/E	5V OR 5.2V	510Ω	180Ω	750Ω
100K/E	4.5V	620Ω	180Ω	510Ω

(b) LT1719 OUTPUT TO PECL TRANSLATOR



	V_{ECL}	R1	R2	R3	R4
10KH/E	5V OR 5.2V	300Ω	180Ω	OMIT	560Ω
100K/E	4.5V	330Ω	180Ω	1500Ω	1000Ω

(c) 3V LT1719 OUTPUT TO PECL TRANSLATOR



ECL FAMILY	V_{ECL}	+V_S OR V^+	R1	R2	R3	R4
10KH/E	–5.2V	5V	560Ω	270Ω	330Ω	1200Ω
		3V	270Ω	510Ω	300Ω	330Ω
100K/E	–4.5V	5V	680Ω	270Ω	300Ω	1500Ω
		3V	330Ω	390Ω	270Ω	430Ω

1719 F06

(d) LT1719 OUTPUT TO STANDARD ECL TRANSLATOR

Figure 6

APPLICATIONS INFORMATION

Figure 6b shows a three resistor level translator for interfacing the LT1719 to ECL running off the same supply rail. No pull-down on the output of the LT1719 is needed, but pull-down R3 limits the V_{IH} seen by the PECL gate. This is needed because ECL inputs have both a minimum and maximum V_{IH} specification for proper operation. Resistor values are given for both ECL interface types; in both cases it is assumed that the LT1719 operates from the same supply rail.

Figure 6c shows the case of translating to PECL from an LT1719 powered by a 3V supply rail. Again, resistor values are given for both ECL interface types. This time four resistors are needed, although with 10KH/E, R3 is not needed. In that case, the circuit resembles the standard TTL translator of Figure 6a, but the function of the new resistor, R4, is much different. R4 loads the LT1719 output when high so that the current flowing through R1 doesn't forward bias the LT1719's internal ESD clamp diode. Although this diode can handle 20mA without damage, normal operation and performance of the output stage can be impaired above 100µA of forward current. R4 prevents this with the minimum additional power dissipation.

Finally, Figure 6d shows the case of driving standard, negative-rail, ECL with the LT1719. Resistor values are given for both ECL interface types and for both a 5V and 3V LT1719 supply rail. Again, a fourth resistor, R4 is needed to prevent the low state current from flowing out of the LT1719, turning on the internal ESD/substrate diodes. Resistor R4 again prevents this with the minimum additional power dissipation.

Of course, in the SO-8 package, if the V_{EE} of the LT1719 is the same as the ECL negative supply, the GND pin can be tied to it as well and $+V_S$ grounded. Then the output stage has the same power rails as the ECL and the circuits of Figure 6b can be used.

For all the dividers shown, the output impedance is about 110Ω. This makes these fast, less than a nanosecond, with most layouts. Avoid the temptation to use speedup capacitors. Not only can they foul up the operation of the ECL gate because of overshoots, they can damage the ECL inputs, particularly during power-up of separate supply configurations.

Similar circuits can be used with the emerging LVECL and LVPECL standards.

The level translator designs shown assume one gate load. Multiple gates can have significant I_{IH} loading, and the transmission line routing and termination issues also make this case difficult.

ECL, and particularly PECL, is valuable technology for high speed system design, but it must be used with care. With less than a volt of swing, the noise margins need to be evaluated carefully. Note that there is some degradation of noise margin due to the ±5% resistor selections shown. With 10KH/E, there is no temperature compensation of the logic levels, whereas the LT1719 and the circuits shown give levels that are stable with temperature. This will lower the noise margin over temperature. In some configurations it is possible to add compensation with diode or transistor junctions in series with the resistors of these networks.

For more information on ECL design, refer to the ECLiPS data book (DL140), the 10KH system design handbook (HB205) and PECL design (AN1406), all from Motorola, now ON Semiconductor.

APPLICATIONS INFORMATION

Circuit Description

The block diagram of the LT1719 is shown in Figure 7. The circuit topology consists of a differential input stage, a gain stage with hysteresis and a complementary common-emitter output stage. All of the internal signal paths utilize low voltage swings for high speed at low power.

The input stage topology maximizes the input dynamic range available without requiring the power, complexity and die area of two complete input stages such as are found in rail-to-rail input comparators. With a single 2.7V supply, the LT1719 still has a respectable 1.6V of input common mode range. The differential input voltage range is rail-to-rail, without the large input currents found in competing devices. The input stage also features phase reversal protection to prevent false outputs when the inputs are driven below the –100mV common mode voltage limit.

The internal hysteresis is implemented by positive, nonlinear feedback around a second gain stage. Until this point, the signal path has been entirely differential. The signal path is then split into two drive signals for the upper and lower output transistors. The output transistors are connected common emitter for rail-to-rail output operation. The Schottky clamps limit the output voltages at about 300mV from the rail, not quite the 50mV or 15mV of Linear Technology's rail-to-rail amplifiers and other products. But the output of a comparator is digital, and this output stage can drive TTL or CMOS directly. It can also drive ECL, as described earlier, or analog loads as demonstrated in the applications to follow.

The bias conditions and signal swings in the output stage are designed to turn their respective output transistors off faster than on. This helps minimize the surge of current from $+V_S/V^+$ to ground that occurs at transitions, to minimize the frequency-dependent increase in power consumption. The frequency dependence of the supply current is shown in the Typical Performance Characteristics.

Speed Limits

The LT1719 comparator is intended for high speed applications, where it is important to understand a few limitations. These limitations can roughly be divided into

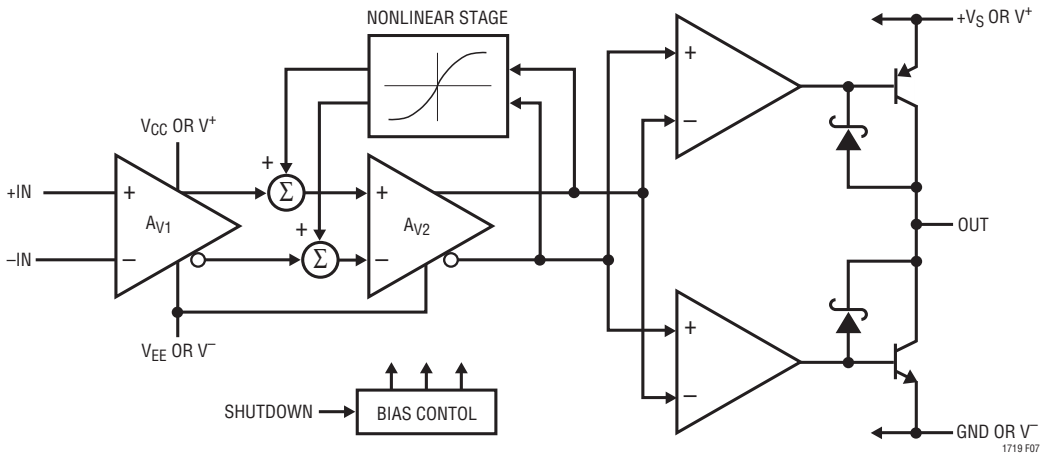


Figure 7. LT1719 Block Diagram

APPLICATIONS INFORMATION

three categories: input speed limits, output speed limits, and internal speed limits.

There are no significant input speed limits except the shunt capacitance of the input nodes. If the 2pF typical input nodes are driven, the LT1719 will respond.

The output speed is constrained by two mechanisms, the first of which is the slew currents available from the output transistors. To maintain low power quiescent operation, the LT1719 output transistors are sized to deliver 25mA to 45mA typical slew currents. This is sufficient to drive small capacitive loads and logic gate inputs at extremely high speeds. But the slew rate will slow dramatically with heavy capacitive loads. Because the propagation delay (t_{PD}) definition ends at the time the output voltage is halfway between the supplies, the fixed slew current makes the LT1719 faster at 3V than 5V with large capacitive loads and sufficient input overdrive.

Another manifestation of this output speed limit is skew, the difference between t_{PD}^+ and t_{PD}^-. The slew currents of the LT1719 vary with the process variations of the PNP and NPN transistors, for rising edges and falling edges respectively. The typical 0.5ns skew can have either polarity, rising edge or falling edge faster. Again, the skew will increase dramatically with heavy capacitive loads.

A separate output speed limit is the clamp turnaround. The LT1719 output is optimized for fast initial response, with some loss of turnaround speed, limiting the toggle frequency. The output transistors are idled in a low power state once V_{OH} or V_{OL} is reached, by detecting the Schottky clamp action. It is only when the output has slewed from the old voltage to the new voltage, and the clamp circuitry has settled, that the idle state is reached and the LT1719 is fully ready to toggle again. This is typically 8ns for each direction, resulting in a maximum toggle frequency of 62.5MHz. With higher frequencies, dropout and runt pulses can result. Increases in capacitive load will increase the time needed for slewing due to the limited slew currents and the maximum toggle frequency will decrease further. For high toggle frequency applications, consider the LT1394, whose linear output stage can toggle at 100MHz typical.

The internal speed limits manifest themselves as dispersion. All comparators have some degree of dispersion, defined as a change in propagation delay versus input overdrive. The propagation delay of the LT1719 will vary with overdrive, from a typical of 4.5ns at 20mV overdrive to 7ns at 5mV overdrive (typical). The LT1719's primary source of dispersion is the hysteresis stage. As a change of polarity arrives at the gain stage, the positive feedback of the hysteresis stage subtracts from the overdrive available. Only when enough time has elapsed for a signal to propagate forward through the gain stage, backwards through the hysteresis path and forward through the gain stage again, will the output stage receive the same level of overdrive that it would have received in the absence of hysteresis.

The LT1719S8 is several hundred picoseconds faster when $V_{EE} = -5V$, relative to single supply operation. This is due to the internal speed limit; the gain stage operates between V_{EE} and $+V_S$, and it is faster with higher reverse voltage bias due to reduced silicon junction capacitances.

In many applications, as shown in the following examples, there is plenty of input overdrive. Even in applications providing low levels of overdrive, the LT1719 is fast enough that the absolute dispersion of 2.5ns (= 7 – 4.5) is often small enough to ignore.

The gain and hysteresis stage of the LT1719 is simple, short and high speed to help prevent parasitic oscillations while adding minimum dispersion. This internal "self-latch" can be usefully exploited in many applications because it occurs early in the signal chain, in a low power, fully differential stage. It is therefore highly immune to disturbances from other parts of the circuit, such as the output, or on the supply lines. Once a high speed signal trips the hysteresis, the output will respond, after a fixed propagation delay, without regard to these external influences that can cause trouble in nonhysteretic comparators.

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$\pm V_{TRIP}$ Test Circuit

The input trip points test circuit uses a 1kHz triangle wave to repeatedly trip the comparator being tested. The LT1719 output is used to trigger switched capacitor sampling of the triangle wave, with a sampler for each direction. Because the triangle wave is attenuated 1000:1 and fed to the LT1719's differential input, the sampled voltages are therefore 1000 times the input trip voltages. The hysteresis and offset are computed from the trip points as shown.

Crystal Oscillator

A simple crystal oscillator using an LT1719 is shown on the first page of this data sheet. The 2k-620Ω resistor pair set a bias point at the comparator's noninverting input. The 2k-1.8k-0.1µF path sets the inverting input node at an appropriate DC average level based on the output. The crystal's path provides resonant positive feedback and stable oscillation occurs. Although the LT1719 will give the correct logic output when one input is outside the common mode range, additional delays may occur when it is so operated, opening the possibility of spurious operating modes. Therefore, the DC bias voltages at the inputs are set near the center of the LT1719's common mode range and the 220Ω resistor attenuates the feedback to the noninverting input. The circuit will operate with any AT-cut crystal from 1MHz to 10MHz over a 2.7V to 6V supply range. As the power is applied, the circuit remains off until the LT1719 bias circuits activate, at a typical V_{CC} of 2V to 2.2V (25°C), at which point the desired frequency output is generated.

The output duty cycle of this circuit is roughly 50%, but it is affected by resistor tolerances and to a lesser extent, by comparator offsets and timings. If a 50% duty cycle is required, the circuit of Figure 8 forces a 50% duty cycle. Crystals are narrow-band elements, so the feedback to the noninverting input is a filtered analog version of the square wave output. Changing the noninverting reference level can therefore vary the duty cycle. C1 operates as in the previous example while A1 compares a band-limited version of the output and biases C1's negative input. C1's only degree of freedom to respond is variation of pulse width; hence the output is forced to 50% duty cycle. Again, the circuit operates from 2.7V to 6V. There is a slight duty cycle dependence on comparator loading, so minimal capacitive and resistive loading should be used in critical applications.

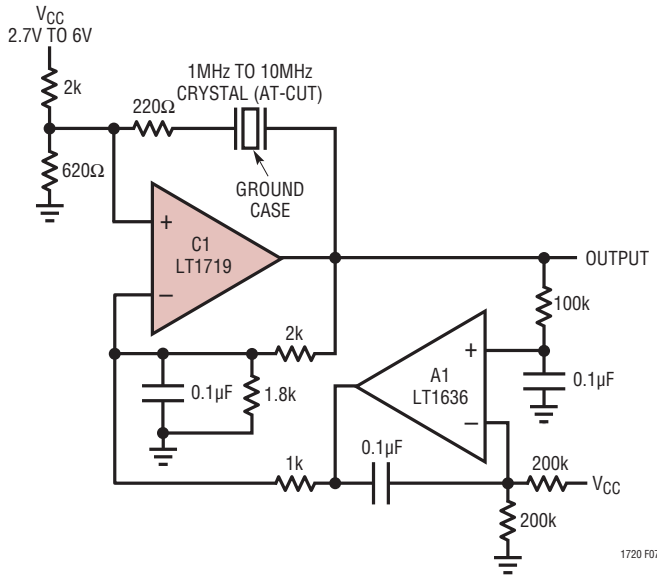
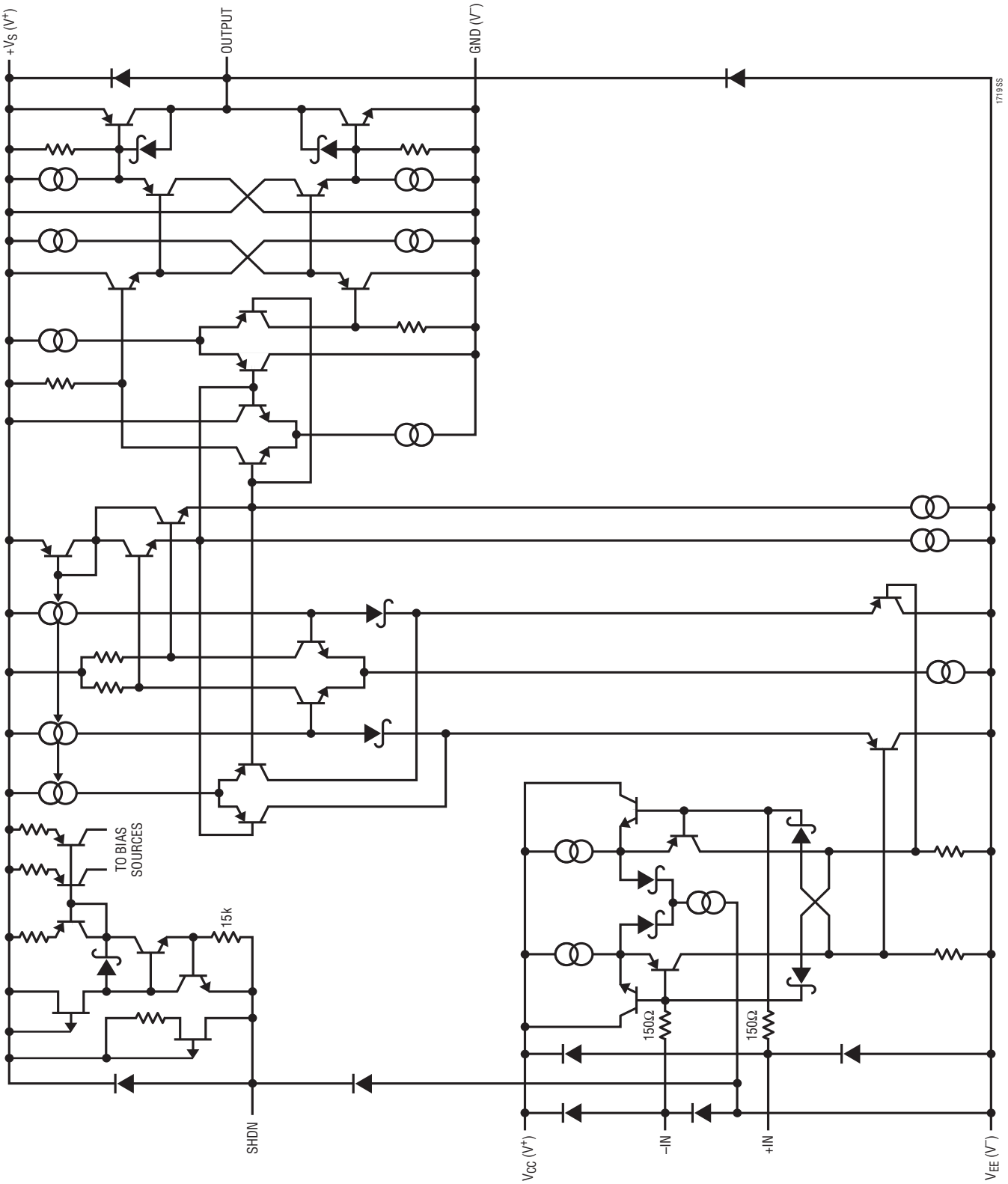


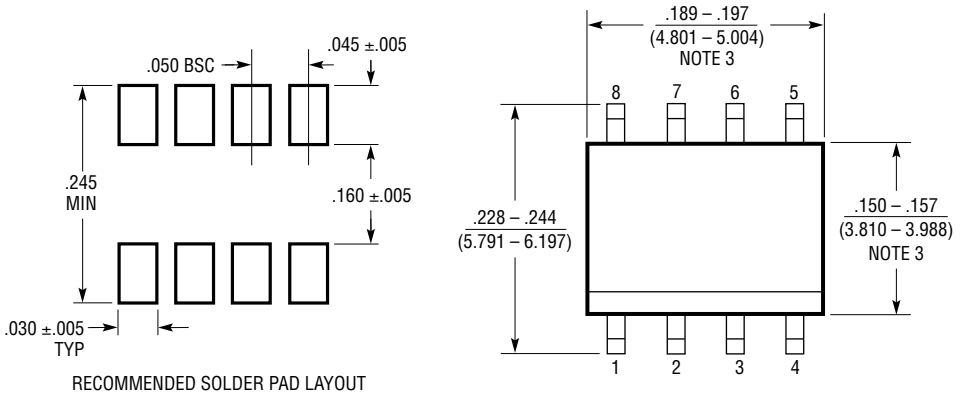
Figure 8. Crystal Oscillator with a Forced 50% Duty Cycle

SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

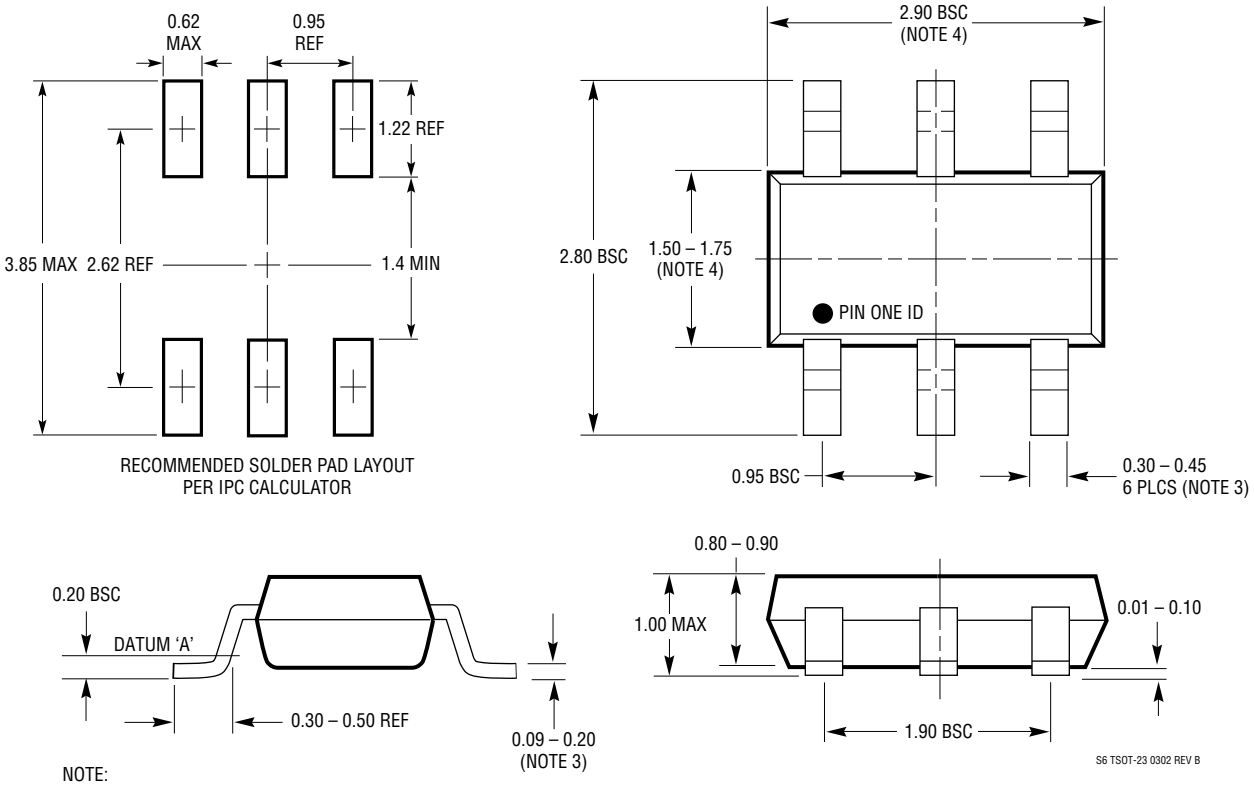


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

PACKAGE DESCRIPTION

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193