Single, Dual, Quad 200MHz Low Noise Precision Op Amps

FEATURES

- **3.8nV/√Hz Input Noise Voltage**
- **3.7mA Supply Current**
- **200MHz Gain Bandwidth**
- **Low Total Harmonic Distortion: –85dBc at 1MHz**
- 70V/µs Slew Rate
- 400µV Maximum Input Offset Voltage
- 300nA Maximum Input Bias Current
- Unity-Gain Stable
- Capacitive Load Stable Up to 100pF
- 23mA Minimum Output Current
- Specified at ±5V and Single 5V
- Low Profile (1mm) SOT-23 (ThinSot™) Package

APPLICATIONS

- Video and RF Amplification
- ADSL, HDSL II, VDSL Receivers
- Active Filters
- Wideband Amplifiers
- Buffers
- Data Acquisition Systems

DESCRIPTION

The LT®1722/LT1723/LT1724 are single/dual/quad, low noise, low power, high speed operational amplifiers. These products feature lower input offset voltage, lower input bias current and higher DC gain than devices with comparable bandwidth. The 200MHz gain bandwidth ensures high open-loop gain at video frequencies.

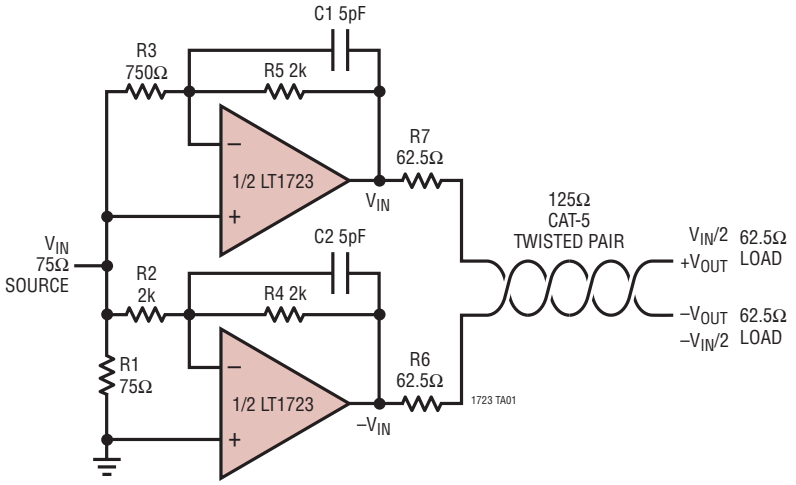
The low input noise voltage is achieved with reduced supply current. The total noise is optimized for a source resistance between 0.8k and 12k. Due to the input bias current cancellation technique used, the resistance seen by each input does not need to be balanced.

The output drives a 150Ω load to ±3V with ±5V supplies. On a single 5V supply the output swings from 1.5V to 3.5V with a 500Ω load connected to 2.5V. The amplifier is unity-gain stable ($C_{LOAD} \leq 100pF$).

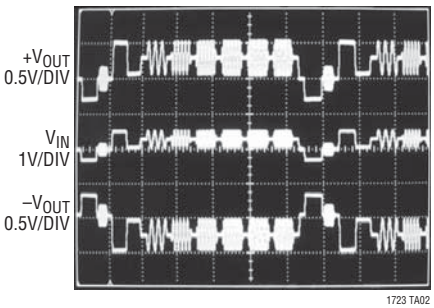
The LT1722/LT1723/LT1724 are manufactured on Linear Technology's advanced low voltage complementary bipolar process. The LT1722 is available in the SO-8 and 5-pin SOT-23 packages. The LT1723 is available in the SO-8 and MS8 packages. The LT1724 is available in the 14-lead SO package.

TYPICAL APPLICATION

Differential Video Line Driver



Line Driver Mulitburst Video Signal



ABSOLUTE MAXIMUM RATINGS

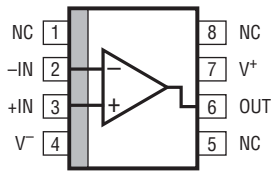
(Note 1)

Total Supply Voltage (V^+ to V^-) 12.6V
Input Voltage..... $\pm V_S$
Differential Input Voltage (Note 2) ..... ±0.7V
Input Current (Note 2)..... ±10mA
Output Short-Circuit Duration (Note 3) ..... Indefinite

Operating Temperature Range (Note 4) ...–40°C to 85°C
Specified Temperature Range (Note 5) ....–40°C to 85°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

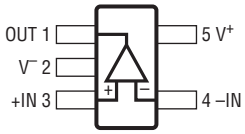
PIN CONFIGURATION

LT1722



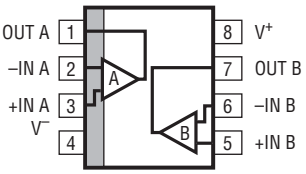
S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 150°C/W

LT1722



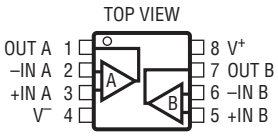
S5 PACKAGE
5-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 250°C/W

LT1723



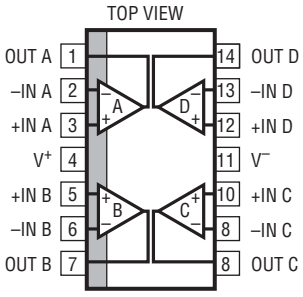
S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 190°C/W

LT1723



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 250°C/W

LT1724



S PACKAGE
14-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1722CS8#PBF	LT1722CS8#TRPBF	1722	8-Lead Plastic SO	0°C to 70°C
LT1722IS8#PBF	LT1722IS8#TRPBF	1722I	8-Lead Plastic SO	–40°C to 85°C
LT1722CS5#PBF	LT1722CS5#TRPBF	LTZB	5-Lead Plastic TSOT-23	0°C to 70°C
LT1722IS5#PBF	LT1722IS5#TRPBF	LTZB	5-Lead Plastic TSOT-23	–40°C to 85°C
LT1723CS8#PBF	LT1723CS8#TRPBF	1723	8-Lead Plastic SO	0°C to 70°C
LT1723IS8#PBF	LT1723IS8#TRPBF	1723I	8-Lead Plastic SO	–40°C to 85°C
LT1723CMS8#PBF	LT1723CMS8#TRPBF	LTYC	8-Lead Plastic MSOP	0°C to 70°C
LT1723IMS8#PBF	LT1723IMS8#TRPBF	LTZA	8-Lead Plastic MSOP	–40°C to 85°C
LT1724CS#PBF	LT1724CS#TRPBF	LT1724CS	14-Lead Plastic SO	0°C to 70°C
LT1724IS#PBF	LT1724IS#TRPBF	LT1724IS	14-Lead Plastic SO	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±5V, V_{CM} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 6) LT1722 SOT-23 and LT1723 MS8		100 150	400 650	µV µV
I_{OS}	Input Offset Current			40	300	nA
I_B	Input Bias Current			40	300	nA
e_n	Input Noise Voltage	f = 10kHz		3.8		nV/√Hz
i_n	Input Noise Current	f = 10kHz		1.2		pA/√Hz
R_{IN}	Input Resistance	V_{CM} = ±3.5V Differential	5	35 50		MΩ kΩ
C_{IN}	Input Capacitance			2		pF
	Input Voltage Range + Input Voltage Range –		3.5	4 –4	 –3.5	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3.5V	80	100		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.3V to ±5.5V	78	90		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±3V, R_L = 500Ω V_{OUT} = ±3V, R_L = 150Ω	10 7	17 14		V/mV V/mV
V_{OUT}	Output Swing	R_L = 500Ω, V_{IN} = ±10mV R_L = 150Ω, V_{IN} = ±10mV	±3.2 ±3.1	±3.8 ±3.4		V V
I_{OUT}	Output Current	V_{OUT} = ±3V, 10mV Overdrive	23	50		mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±1V	35	90		mA
SR	Slew Rate	A_V = –1, (Note 7)	45	70		V/µs
	Full Power Bandwidth	3V Peak, (Note 8)		3.7		MHz
GBW	Gain Bandwidth	f = 200kHz	115	200		MHz
t_S	Settling Time	A_V = –1, 2V, 0.1% A_V = –1, 2V, 0.01%		91 112		ns ns
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10% to 90%, V_{IN} = 0.2V_{P-P}, R_L = 150Ω		6		ns
	Overshoot	A_V = 1, V_{IN} = 0.2V_{P-P}, R_L = 150Ω, R_F = 0Ω		15		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT} = 0.2V_{P-P}, R_L = 150Ω		3		ns
R_O	Output Resistance	A_V = 1, f = 1MHz		0.15		Ω
	Channel Separation	V_{OUT} = ±3V, R_L = 150Ω	82	90		dB
I_S	Supply Current	Per Amplifier		3.7	4.5	mA

T_A = 25°C. V_S = 5V, V_{CM} = 2.5V, R_L to 2.5V, unless otherwise noted.

V_{OS}	Input Offset Voltage	(Note 6) LT1722 SOT-23 and LT1723 MS8		250 350	550 800	µV µV
I_{OS}	Input Offset Current			20	300	nA
I_B	Input Bias Current			20	300	nA
e_n	Input Noise Voltage	f = 10kHz		4		nV/√Hz
i_n	Input Noise Current	f = 10kHz		1.1		pA/√Hz
R_{IN}	Input Resistance	V_{CM} = 1.5V to 3.5V Differential	5	32 55		MΩ kΩ
C_{IN}	Input Capacitance			2		pF
	Input Voltage Range + Input Voltage Range –		3.5	4 1	 1.5	V V

ELECTRICAL CHARACTERISTICS

T_A = 25°C. V_S = 5V, V_{CM} = 2.5V, R_L to 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	V_{CM} = 1.5V to 3.5V	80	100		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = 1.5V to 3.5V, R_L = 500Ω	4	10		V/mV
V_{OUT}	Output Swing+ Output Swing–	R_L = 500Ω, V_{IN} = ±10mV R_L = 500Ω, V_{IN} = ±10mV	3.6	3.8 0.9	 1.4	V V
I_{OUT}	Output Current	V_{OUT} = 3.5V or 1.5V, 10mV Overdrive	10	20		mA
I_{SC}	Short-Circuit Current	V_{OUT} = 2.5V, V_{IN} = ±1V	22	55		mA
SR	Slew Rate	A_V = –1, (Note 7)	40	70		V/µs
	Full Power Bandwidth	1V Peak, (Note 8)		8.7		MHz
GBW	Gain Bandwidth (Note 10)	f = 200kHz	115	180		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10% to 90%, V_{IN} = 0.2V_{P-P}, R_L = 500Ω		5		ns
	Overshoot	A_V = 1, V_{IN} = 0.2V_{P-P}, R_L = 500Ω		16		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V, R_L = 500Ω		3		ns
R_O	Output Resistance	A_V = 1, f = 1MHz		0.19		Ω
	Channel Separation	V_{OUT} = 1.5V to 3.5V, R_L = 500Ω	82	90		dB
I_S	Supply Current	Per Amplifier		3.8	5	mA

The ● denotes the specifications which apply over the temperature range of 0°C ≤ T_A ≤ 70°C. V_S = ±5V, V_{CM} = 0V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 6) LT1722 SOT-23 and LT1723 MS8	● ●			700 850	µV µV
	Input V_{OS} Drift	(Note 9)	●		3	7	µV/°C
I_{OS}	Input Offset Current		●			350	nA
I_B	Input Bias Current		●			350	nA
	Input Voltage Range + Input Voltage Range –		● ●	3.5		 –3.5	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3.5V	●	75			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.3V to ±5.5V	●	76			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±3V, R_L = 500Ω V_{OUT} = ±3V, R_L = 150Ω	● ●	9 6			V/mV V/mV
V_{OUT}	Output Swing	R_L = 500Ω, V_{IN} = ±10mV R_L = 150Ω, V_{IN} = ±10mV	● ●	±3.15 ±3.05			V V
I_{OUT}	Output Current	V_{OUT} = ±3V, 10mV Overdrive	●	22			mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±1V	●	30			mA
SR	Slew Rate	A_V = –1, (Note 7)	●	35			V/µs
GBW	Gain Bandwidth	f = 200kHz	●	100			MHz
	Channel Separation	V_{OUT} = ±3V, R_L = 150Ω	●	81			dB
I_S	Supply Current	Per Amplifier	●			5.45	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range of 0°C ≤ T_A ≤ 70°C. V_S = 5V, V_{CM} = 2.5V, R_L to 2.5V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 6) LT1722 SOT-23 and LT1723 MS8	● ●			850 950	µV µV
	Input V_{OS} Drift	(Note 9)	●		3	7	µV/°C
I_{OS}	Input Offset Current		●			350	nA
I_B	Input Bias Current		●			350	nA
	Input Voltage Range + Input Voltage Range –		● ●	3.5		 1.5	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = 1.5V to 3.5V	●	75			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = 1.5V to 3.5V, R_L = 500Ω	●	3			V/mV
V_{OUT}	Output Swing+ Output Swing–	R_L = 500Ω, V_{IN} = ±10mV R_L = 500Ω, V_{IN} = ±10mV	● ●	3.55		 1.45	V V
I_{OUT}	Output Current	V_{OUT} = 3.5V, or 1.5V, 10mV Overdrive	●	9			mA
I_{SC}	Short-Circuit Current	V_{OUT} = 2.5V, V_{IN} = ±1V	●	11			mA
SR	Slew Rate	A_V = –1, (Note 7)	●	30			V/µs
GBW	Gain Bandwidth (Note 10)	f = 200kHz	●	100			MHz
	Channel Separation	V_{OUT} = 1.5V to 3.5V, R_L = 500Ω	●	81			dB
I_S	Supply Current		●			5.95	mA

The ● denotes the specifications which apply over the temperature range of –40°C ≤ T_A ≤ 85°C. V_S = ±5V, V_{CM} = 0V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 6) LT1722 SOT-23 and LT1723 MS8	● ●			900 1100	µV µV
	Input V_{OS} Drift	(Note 9)	●		3	10	µV/°C
I_{OS}	Input Offset Current		●			400	nA
I_B	Input Bias Current		●			400	nA
	Input Voltage Range + Input Voltage Range –		● ●	3.5		 –3.5	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3.5V	●	75			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.0V to ±5.5V	●	75			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±3V, R_L = 500Ω V_{OUT} = ±3V, R_L = 150Ω	● ●	8 5			V/mV V/mV
V_{OUT}	Output Swing	R_L = 500Ω, V_{IN} = ±10mV R_L = 150Ω, V_{IN} = ±10mV	● ●	±3.1 ±3.0			V V
I_{OUT}	Output Current	V_{OUT} = ±3V, 10mV Overdrive	●	20			mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±1V	●	25			mA
SR	Slew Rate	A_V = –1, (Note 7)	●	25			V/µs
GBW	Gain Bandwidth	f = 200kHz	●	90			MHz
	Channel Separation	V_{OUT} = ±3V, R_L = 150Ω	●	80			dB
I_S	Supply Current		●			5.95	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range of –40°C ≤ T_A ≤ 85°C. V_S = 5V, V_{CM} = 2.5V, R_L to 2.5V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 6) LT1722 SOT-23 and LT1723 MS8	● ●			1000 1200	µV µV
	Input V_{OS} Drift	(Note 9)	●		3	10	µV/°C
I_{OS}	Input Offset Current		●			400	nA
I_B	Input Bias Current		●			400	nA
	Input Voltage Range + Input Voltage Range –		● ●	3.5		 1.5	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = 1.5V to 3.5V	●	75			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = 1.5V to 3.5V, R_L = 500Ω	●	2			V/mV
V_{OUT}	Output Swing+ Output Swing–	R_L = 500Ω, V_{IN} = ±10mV R_L = 500Ω, V_{IN} = ±10mV	● ●	3.5		 1.5	V V
I_{OUT}	Output Current	V_{OUT} = 3.5V or 1.5V, 30mV Overdrive	●	8			mA
I_{SC}	Short-Circuit Current	V_{OUT} = 2.5V, V_{IN} = ±1V	●	10			mA
SR	Slew Rate	A_V = –1, (Note 7)	●	20			V/µs
GBW	Gain Bandwidth (Note 10)	f = 200kHz	●	90			MHz
	Channel Separation	V_{OUT} = 1.5V to 3.5V, R_L = 500Ω	●	80			dB
I_S	Supply Current		●			6.45	mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by back-to-back diodes. If the differential input voltage exceeds 0.7V, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LT1722C/LT1722I, LT1723C/LT1723I, LT1724C/LT1724I are guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 5: The LT1722C/LT1723C/LT1724C are guaranteed to meet specified performance from 0°C to 70°C. The LT1722C/LT1723C/LT1724C are designed, characterized and expected to meet specified performance from –40°C to 85°C but are not tested or QA sampled at these temperatures. The LT1722I/LT1723I/LT1724I are guaranteed to meet specified performance from –40°C to 85°C.

Note 6: Input offset voltage is pulse tested and is exclusive of warm-up drift.

Note 7: Slew rate is measured between ±2V on the output with ±3V input for ±5V supplies and ±1V on the output with ±1.5V input for single 5V supply. (For 5V supply, the voltage levels are 2.5V referred.)

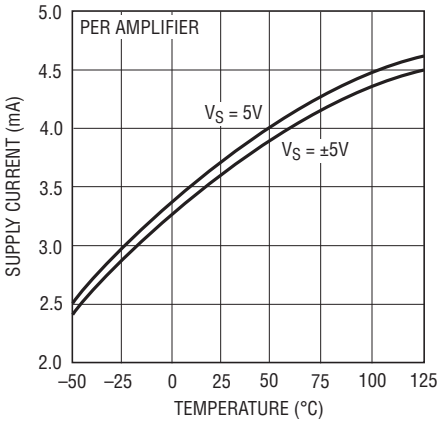
Note 8: Full power bandwidth is calculated from the slew rate:
$FPBW = SR/2\pi V_P$

Note 9 : This parameter is not 100% tested.

Note 10 : This parameter is guaranteed through correlation with slew rate.

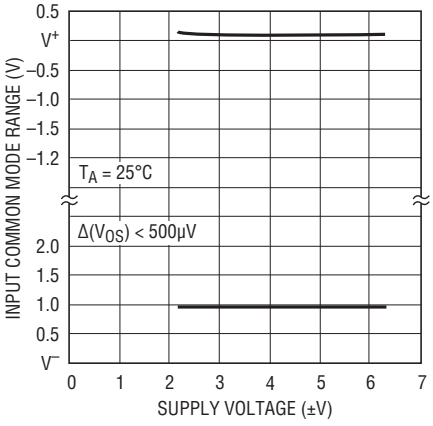
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Temperature



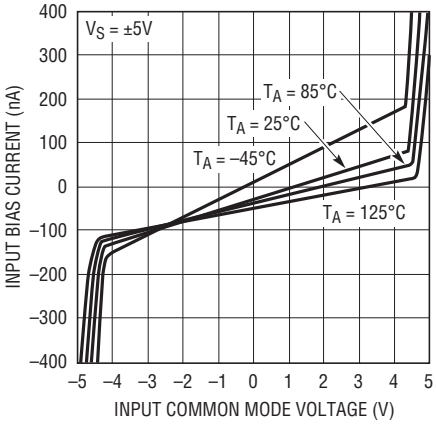
1723 G01

Input Common Mode Range vs Supply Voltage



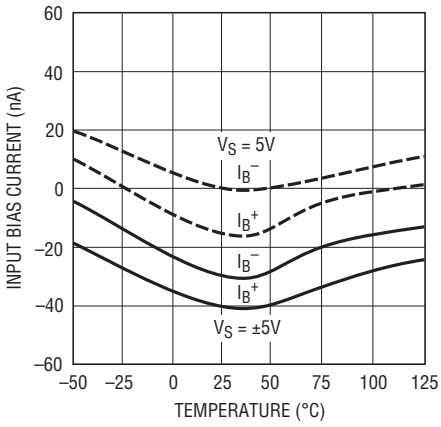
1723 G02

Input Bias Current vs Common Mode Voltage



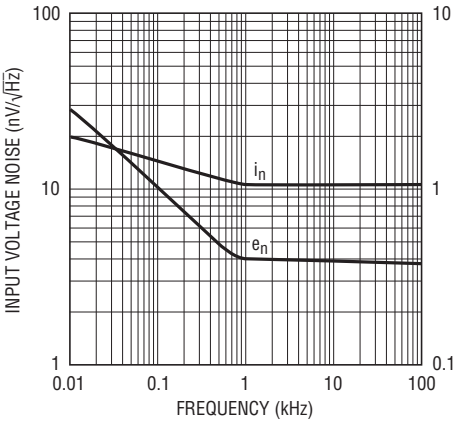
1723 G03

Input Bias Current vs Temperature



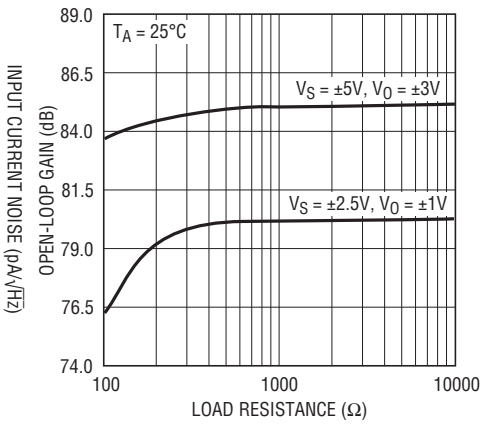
1723 G04

Input Noise Spectral Density



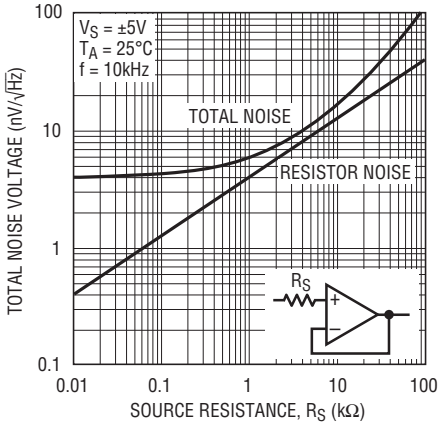
1723 G05

Open-Loop Gain vs Resistive Load



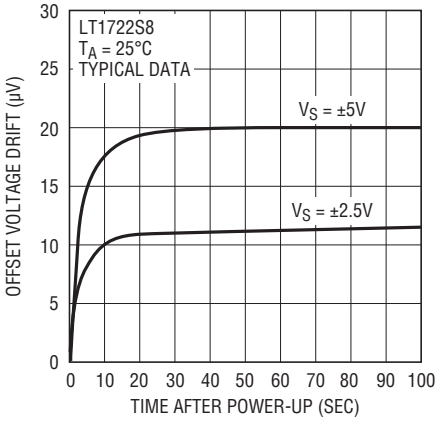
1723 G06

Total Noise vs Unmatched Source Resistance



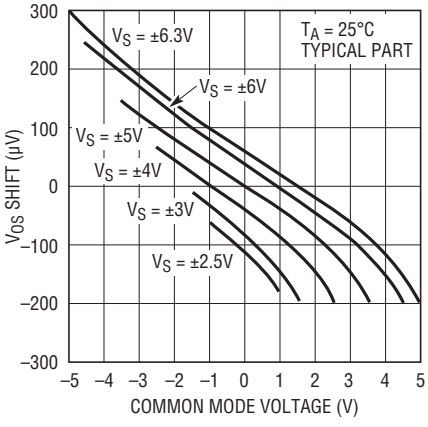
1723 G07

Warm-Up Drift vs Time



1723 G08

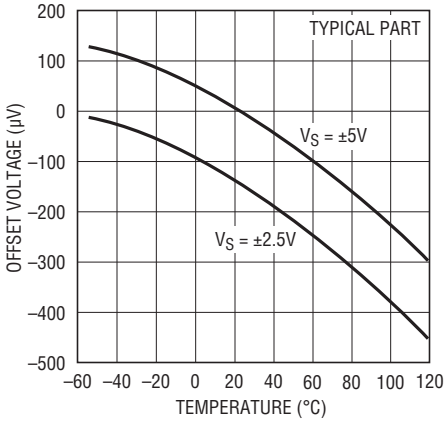
V_{OS} Shift vs V_{CM} and V_S



1723 G09

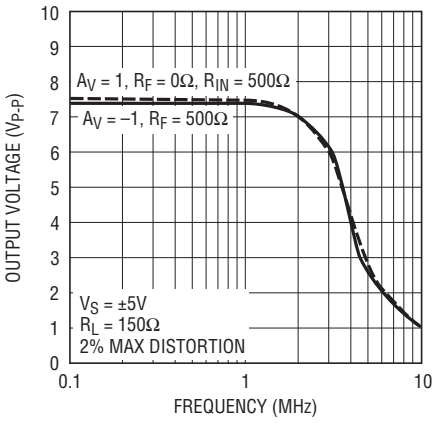
TYPICAL PERFORMANCE CHARACTERISTICS

V_{OS} vs Temperature



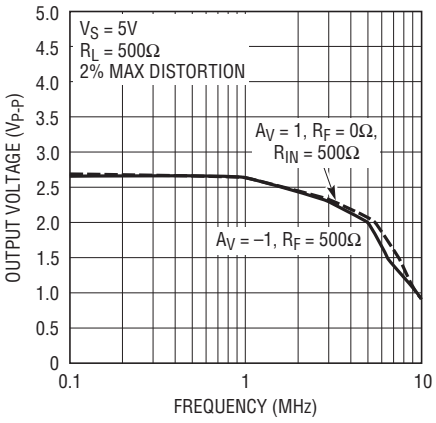
1723 G10

Undistorted Output Swing vs Frequency



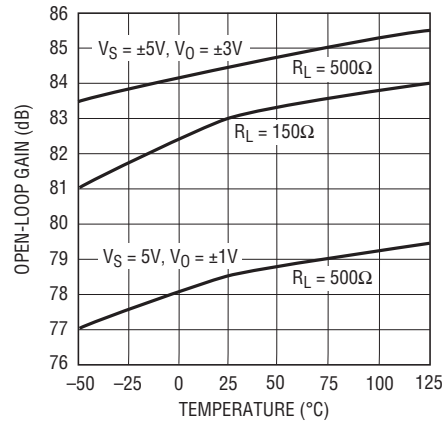
1723 G11

Undistorted Output Swing vs Frequency



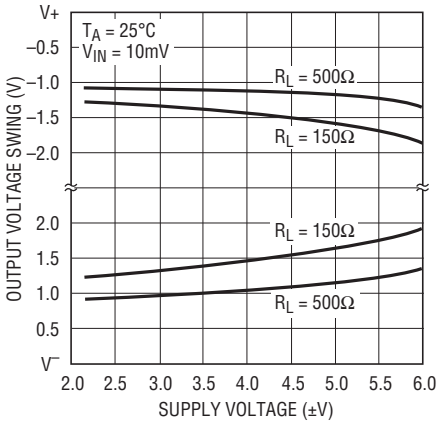
1723 G12

Open-Loop Gain vs Temperature



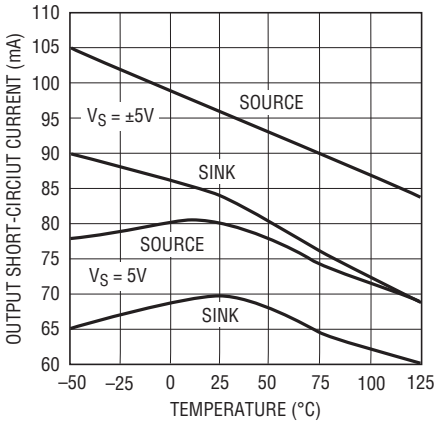
1723 G13

Output Voltage Swing vs Supply Voltage



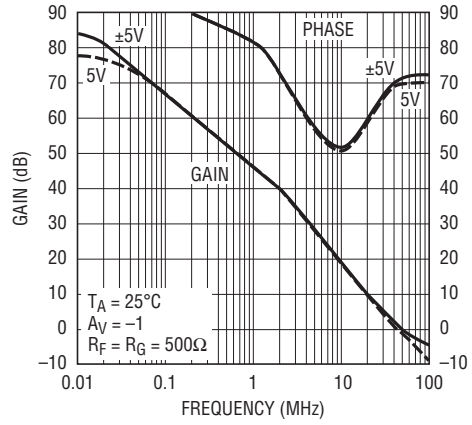
1723 G08

Output Short-Circuit Current vs Temperature



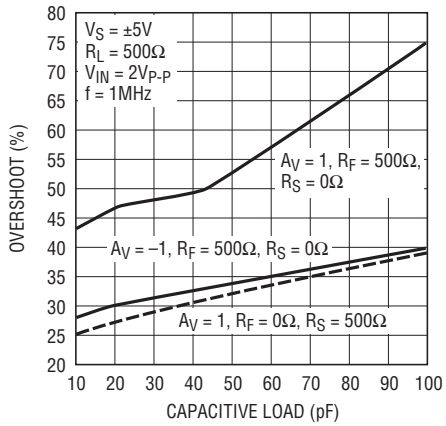
1723 G15

Gain and Phase vs Frequency



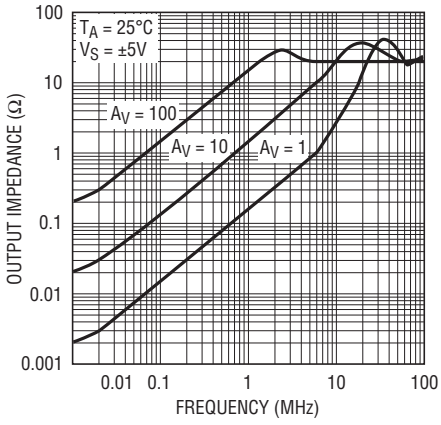
1723 G16

Overshoot vs Capacitive Load



1723 G17

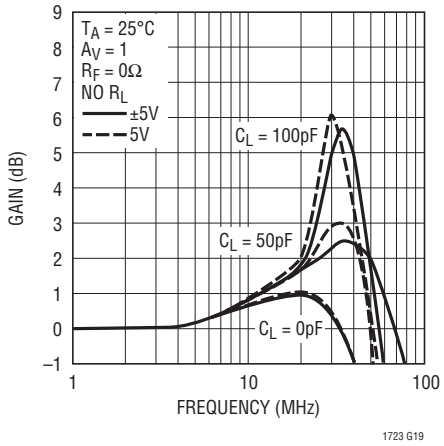
Output Impedance vs Frequency



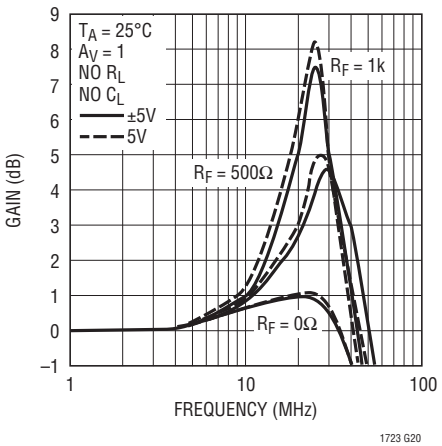
1723 G18

TYPICAL PERFORMANCE CHARACTERISTICS

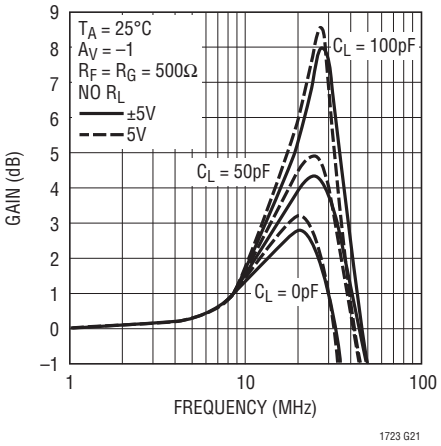
Gain vs Frequency, $A_V = 1$



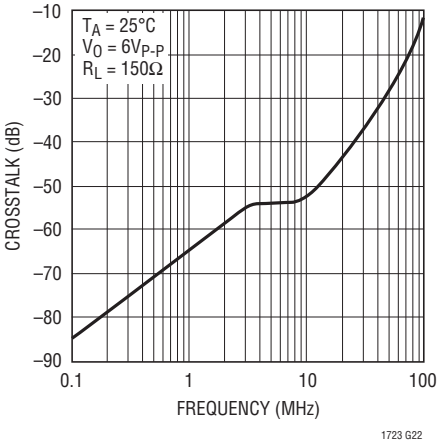
Gain vs Frequency, $A_V = 1$



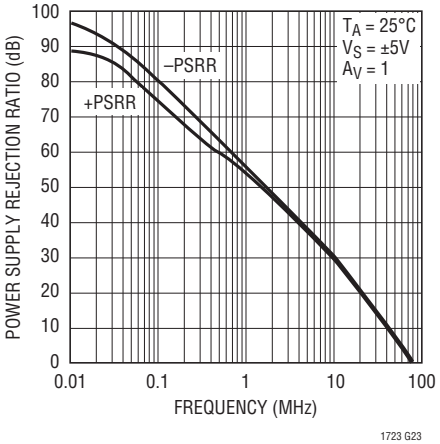
Gain vs Frequency, $A_V = -1$



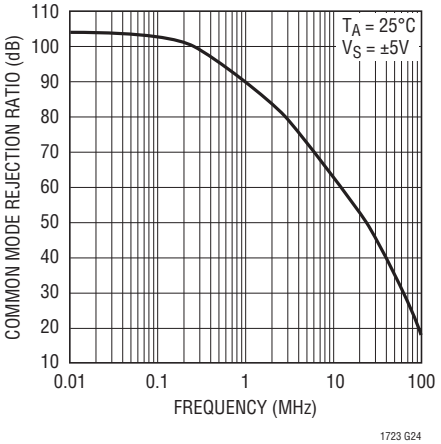
Channel Separation vs Frequency



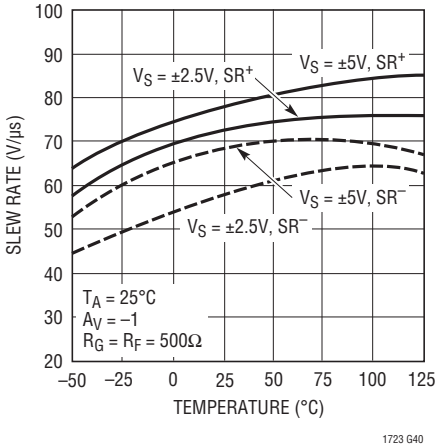
Power Supply Rejection Ratio vs Frequency



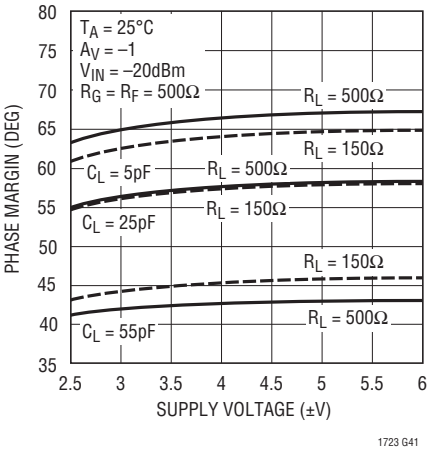
Common Mode Rejection Ratio vs Frequency



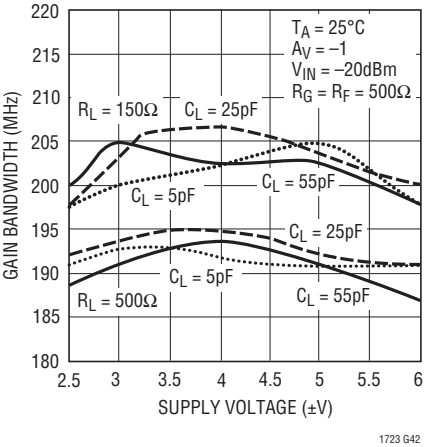
Slew Rate vs Temperature



Phase Margin vs Supply Voltage

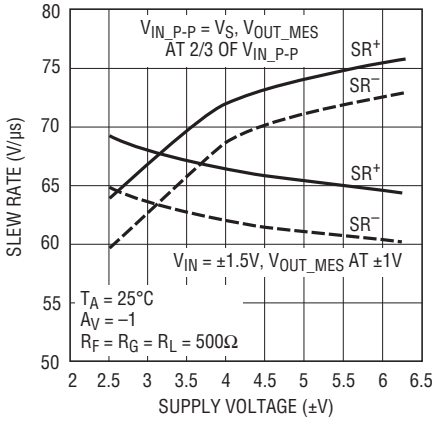


Gain Bandwidth vs Supply Voltage



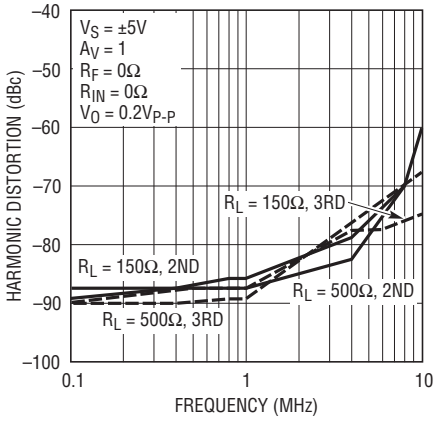
TYPICAL PERFORMANCE CHARACTERISTICS

Slew Rate vs Supply Voltage



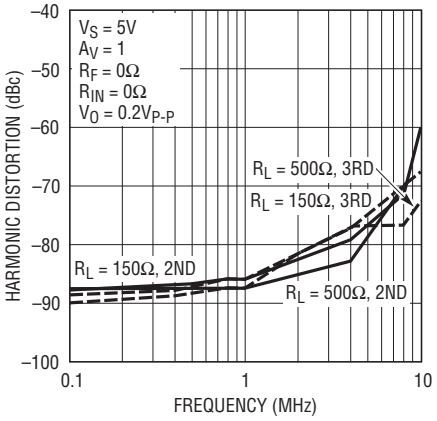
1723 G25

Harmonic Distortion vs Frequency
A_V = 1, V_O = 0.2V_{P-P}



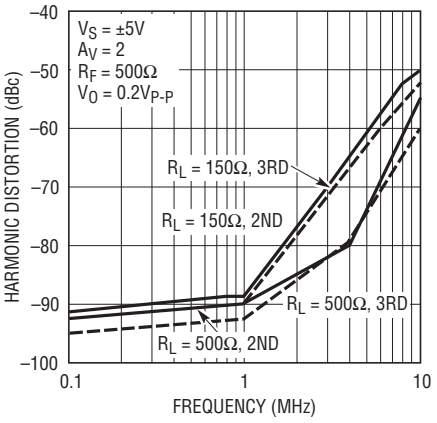
1723 G26

Harmonic Distortion vs Frequency
A_V = 1, V_O = 0.2V_{P-P}



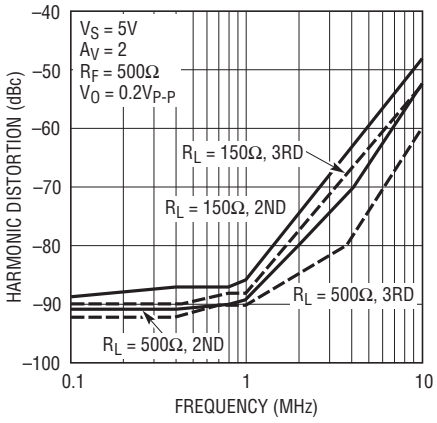
1723 G27

Harmonic Distortion vs Frequency
A_V = 2, V_O = 0.2V_{P-P}



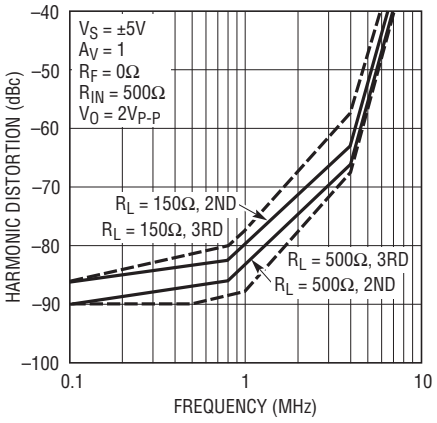
1723 G28

Harmonic Distortion vs Frequency
A_V = 2, V_O = 0.2V_{P-P}



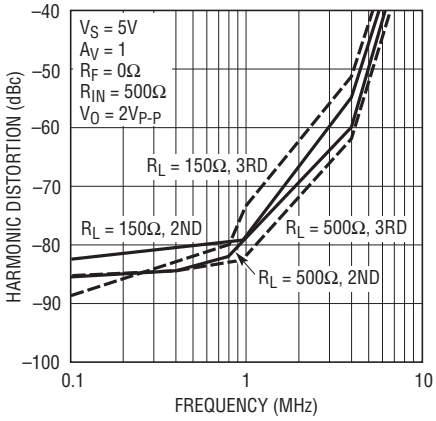
1723 G29

Harmonic Distortion vs Frequency
A_V = 1, V_O = 2V_{P-P}



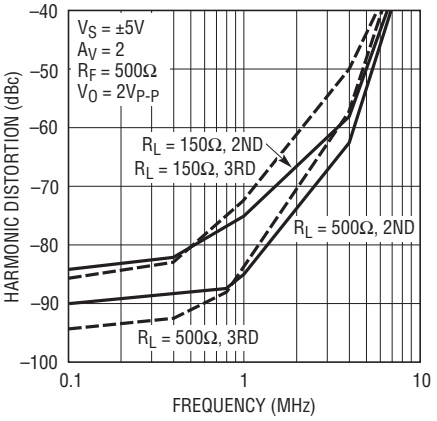
1723 G30

Harmonic Distortion vs Frequency
A_V = 1, V_O = 2V_{P-P}



1723 G31

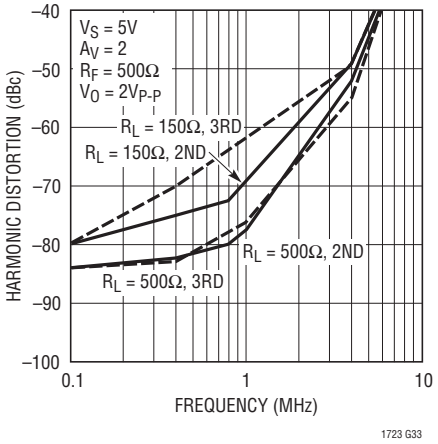
Harmonic Distortion vs Frequency
A_V = 2, V_O = 2V_{P-P}



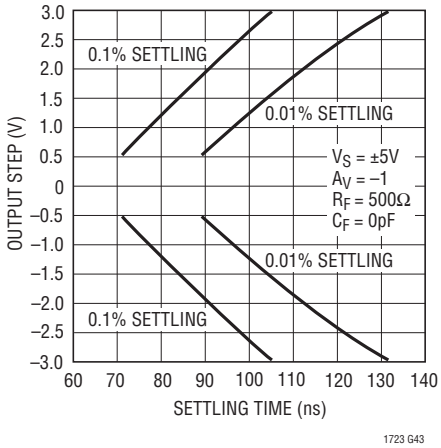
1723 G32

TYPICAL PERFORMANCE CHARACTERISTICS

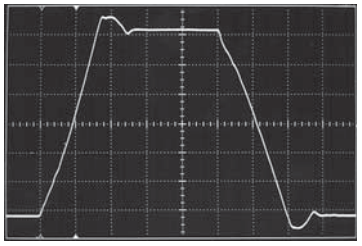
Harmonic Distortion vs Frequency
$A_V = 2$, $V_O = 2V_{P-P}$



Settling Time vs Output Step

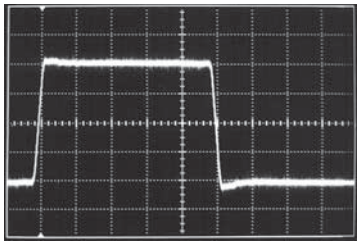


Large-Signal Transient, $A_V = 1$



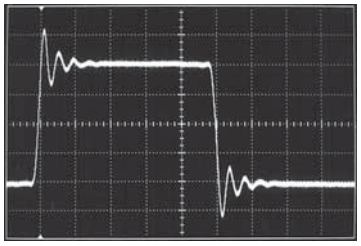
$A_V = 1$
$R_S = 500\Omega$
$R_F = 0\Omega$

Small-Signal Transient, $A_V = 1$



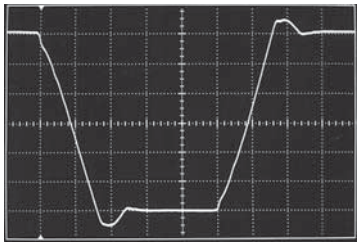
$A_V = 1$
$R_S = 0\Omega$
$R_F = 0\Omega$
$C_L = 0pF$

Small-Signal Transient, $A_V = 1$



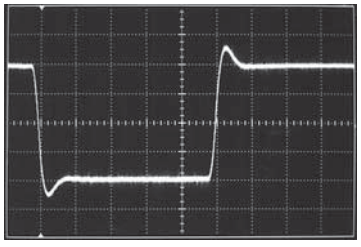
$A_V = 1$
$R_S = 0\Omega$
$R_F = 0\Omega$
$C_L = 100pF$

Large-Signal Transient, $A_V = –1$



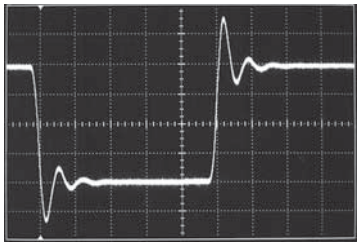
$A_V = –1$
$R_G = 500\Omega$
$R_F = 500\Omega$

Small-Signal Transient, $A_V = –1$



$A_V = –1$
$R_G = 500\Omega$
$R_F = 500\Omega$
$C_L = 0pF$

Small-Signal Transient, $A_V = –1$



$A_V = –1$
$R_G = 500\Omega$
$R_F = 500\Omega$
$C_L = 100pF$

APPLICATIONS INFORMATION

The LT1722/LT1723/LT1724 may be inserted directly into many operational amplifier applications improving both DC and AC performance, as well as noise and distortion.

Layout and Passive Components

The LT1722/LT1723/LT1724 amplifiers are more tolerant of less than ideal layouts than other high speed amplifiers. For maximum performance (for example, fast settling time) use a ground plane, short lead lengths and RF quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications, use low ESR supply bypass capacitors (1µF to 10µF tantalum). The output/input parasitic coupling should be minimized when high frequency performance is required.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole that can cause peaking or even oscillations. In parallel with the feedback resistor, a capacitor of value:

$$C_F > R_G \bullet C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a feedback resistor is used, such as an I-to-V converter, C_F should be five times greater than C_{IN}; an optimum value for C_F is 10pF.

Input Considerations

Each of the LT1722/LT1723/LT1724 inputs is protected with back-to-back diodes across the bases of the NPN input devices. If greater than 0.7V differential input voltages are anticipated, the input current must be limited to less than 10mA with an external series resistor. Each input also has two ESD clamp diodes—one to each supply. If an input is driven beyond the supply, limit the current with an external resistor to less than 10mA. The input stage protection circuit is shown in Figure 1.

The input currents of the LT1722/LT1723/LT1724 are typically in the tens of nA range due to the bias current cancellation technique used at the input. As the input offset current can be greater than either input current, adding resistance to balance source resistance is not recommended. The value of the source resistor should be below 12k as it actually degrades DC accuracy and also increases noise.

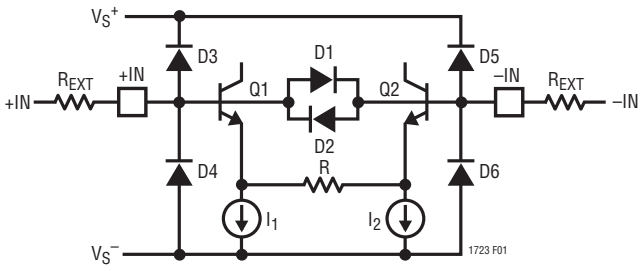


Figure 1. Input Stage Protection

Total Input Noise

The total input noise of the LT1722/LT1723/LT1724 is optimized for a source resistance between 0.8k and 12k. Within this range, the total input noise is dominated by the noise of the source resistance itself. When the source resistance is below 0.8k, voltage noise of the amplifier dominates. When the source resistance is above 12k, the input noise current is the dominant contributor.

Capacitive Loading

The LT1722/LT1723/LT1724 drive capacitive loads up to 100pF with unity gain. As the capacitive load increases, both the bandwidth and the phase margin decrease causing peaking in the frequency response and overshoot in the transient response. When there is a need to drive a larger capacitive load, a 25Ω series resistance assures stability with any value of load capacitor. A feedback capacitor also helps to reduce any peaking.

Power Dissipation

The LT1722/LT1723/LT1724 combine high speed and large output drive in a small package. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A), power dissipation per amplifier (P_D) and number of amplifiers (n) as follows:

$$T_J = T_A + (n \bullet P_D \bullet \theta_{JA})$$

APPLICATIONS INFORMATION

Power dissipation is composed of two parts. The first is due to the quiescent supply current and the second is due to on-chip dissipation caused by the load current.

Worst-case instantaneous power dissipation for a given resistive load in one amplifier occurs at the maximum supply current and when the output voltage is at half of either supply voltage (or the maximum swing if less than half supply voltage).

Therefore $P_{D(MAX)}$ in one amplifier is:

$$P_{D(MAX)} = (V^+ - V^-)(I_{S(MAX)}) + (V^+/2)^2/R_L$$

or

$$P_{D(MAX)} = (V^+ - V^-)(I_{S(MAX)}) + (V^+ - V_{O(MAX)})(V_{O(MAX)}/R_L)$$

Example. Worst-case conditions are: both op amps in the LT1723IS8 are at $T_A = 85°C$, $V_S = \pm 5V$, $R_L = 150\Omega$, $V_{OUT} = 2.5V$.

$$P_{D(MAX)} = 2 \bullet [(10V)(5.95mA) + (2.5V)^2/150\Omega] = 203mW$$
$$T_{J(MAX)} = 85°C + (203mW)(190°C/W) = 124°C$$

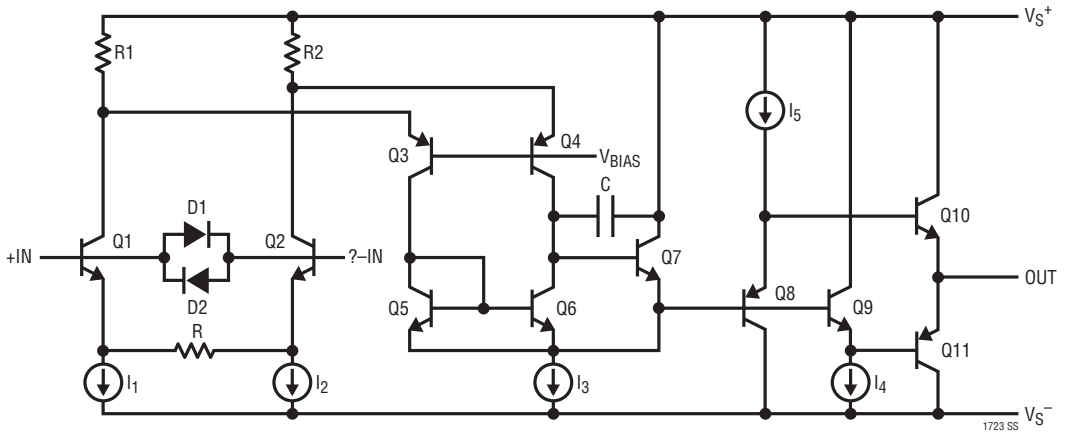
which is less than the absolute maximum rating at 150°C.

Circuit Operation

The LT1722/LT1723/LT1724 circuit topology is a voltage feedback amplifier. The operation of the circuit can be understood by referring to the Simplified Schematic. The first stage is a folded cascode formed by the transistors Q1 through Q4. A degeneration resistor, R, is used in the input stage. The current mirror Q5, Q6 is bootstrapped by Q7. The capacitor, C, assures the bandwidth and the slew rate performance. The output stage is formed by complementary emitter followers, Q8 through Q11. The diodes D1 and D2 protect against input reversed biasing. The remaining part of the circuit assures optimum voltage and current biases for all stages.

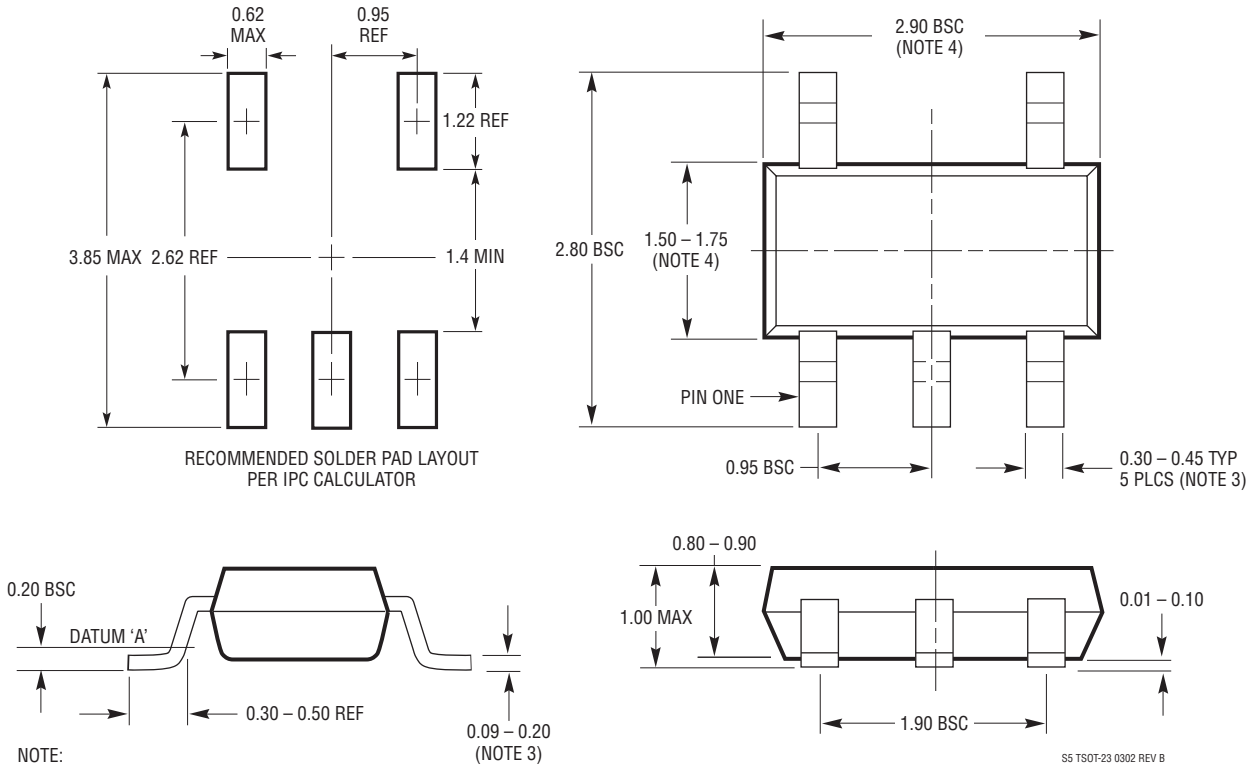
Low noise, reduced current supply, high speed and DC accurate parameters are distinctive features of the LT1722/LT1723/LT1724.

SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

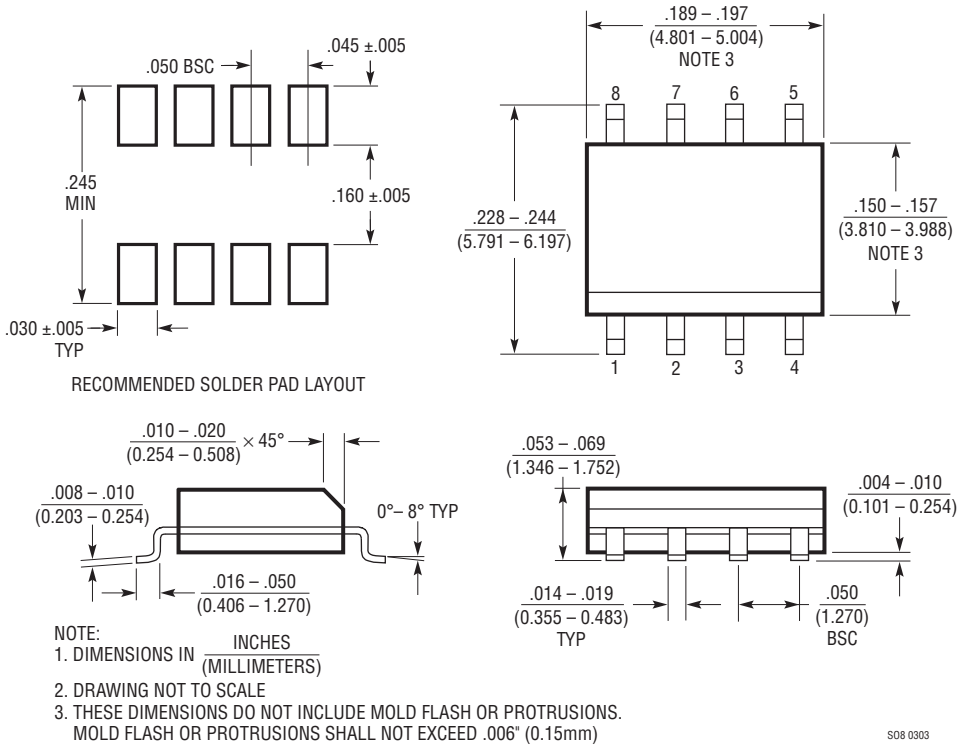
S5 Package
5-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1635)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

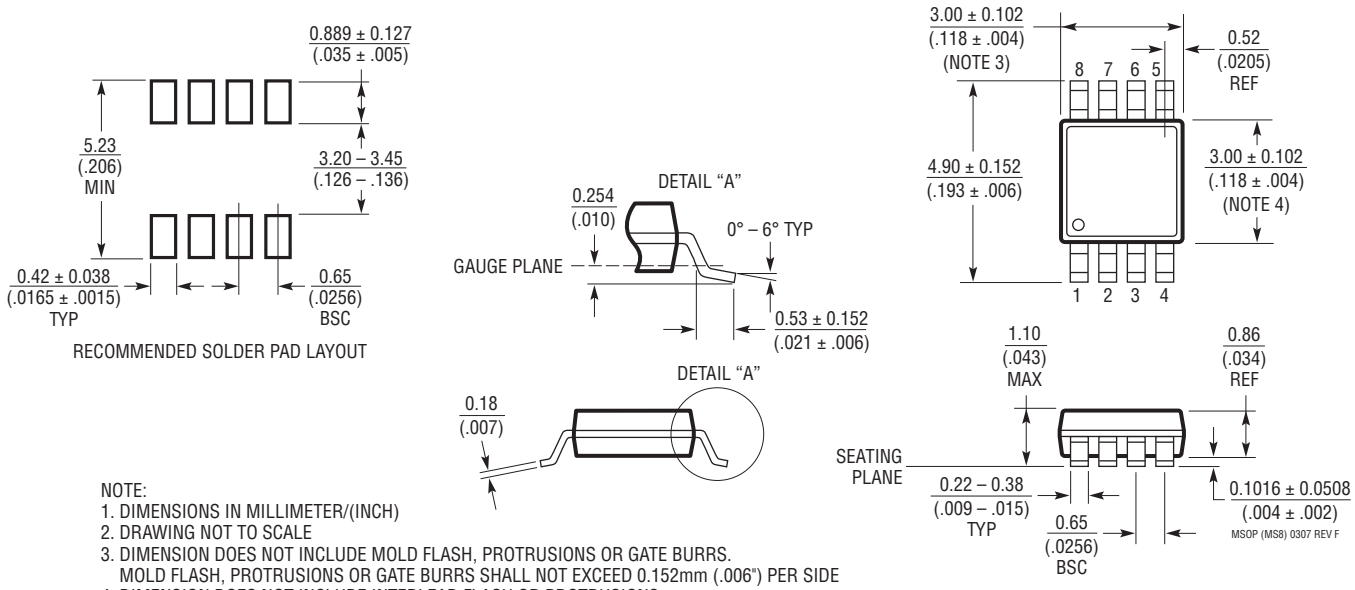
S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S08 0303

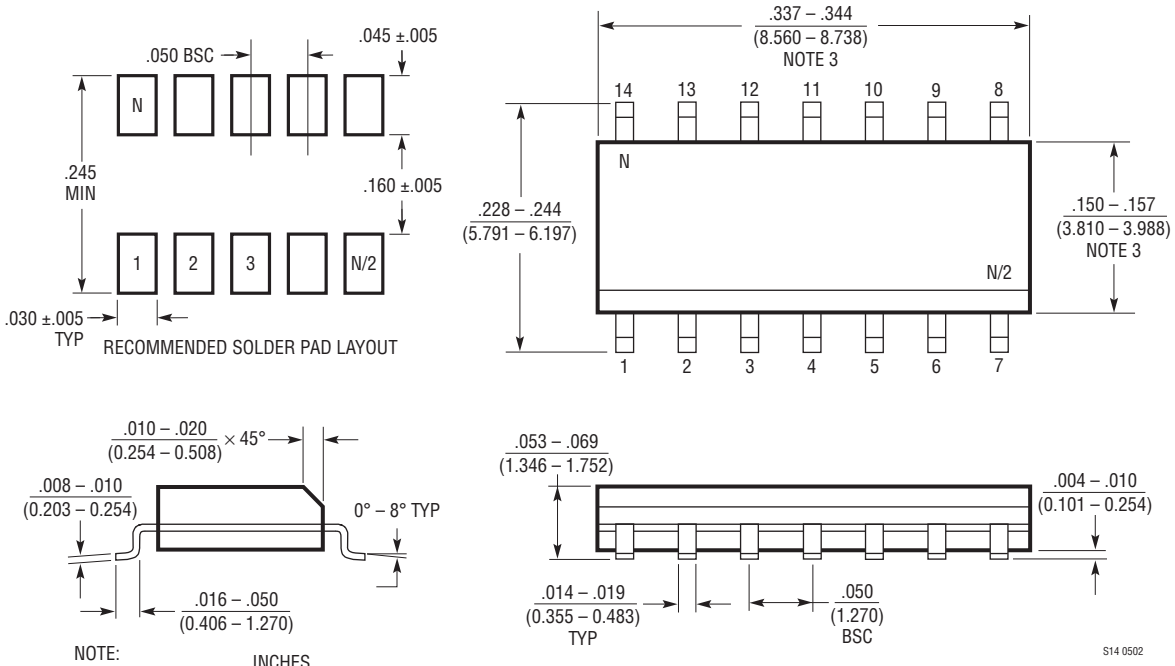
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

S Package
14-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)