General Purpose Isolated Flyback Controller

FEATURES

- **Drives External Power MOSFET with External I_{SENSE} Resistor**
- **Application Input Voltage Limited Only by External Power Components**
- **Senses Output Voltage Directly from Primary Side Winding—No Optoisolator Required**
- Accurate Regulation Without User Trims
- Regulation Maintained Well into Discontinuous Mode
- Switching Frequency from 50kHz to 250kHz with External Capacitor
- Optional Load Compensation
- Optional Undervoltage Lockout
- Available in 16-Pin SO and SSOP Packages

APPLICATIONS

- Telecom Isolated Converters
- Offline Isolated Power Supplies
- Instrumentation Power Supplies

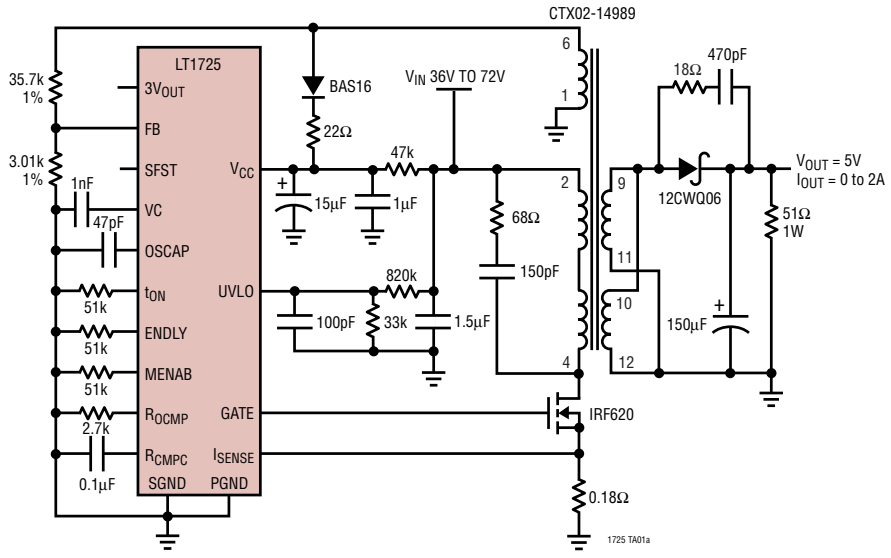
DESCRIPTION

The LT®1725 is a monolithic switching regulator controller specifically designed for the isolated flyback topology. It drives the gate of an external MOSFET and is generally powered from a third transformer winding. These features allow for an application input voltage limited only by external power path components. The third transformer winding also provides output voltage feedback information, such that an optoisolator is not required. Its gate drive capability coupled with a suitable external MOSFET can deliver load power up to tens of watts.

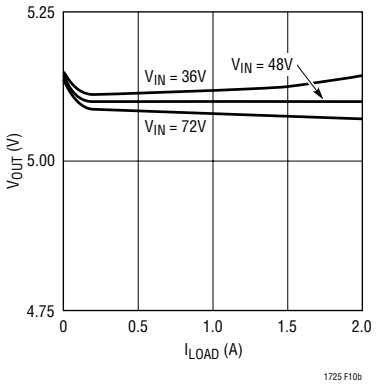
The LT1725 has a number of features not found on most other switching regulator ICs. By utilizing current mode switching techniques, it provides excellent AC and DC line regulation. Its unique control circuitry can maintain regulation well into discontinuous mode in most applications. Optional load compensation circuitry allows for improved load regulation. An optional undervoltage lockout pin halts operation when the application input voltage is too low. An optional external capacitor implements a soft-start function. A 3V output is available at up to several mA for powering primary side application circuitry.

TYPICAL APPLICATION

48V to Isolated 5V Converter



Output Load Regulation

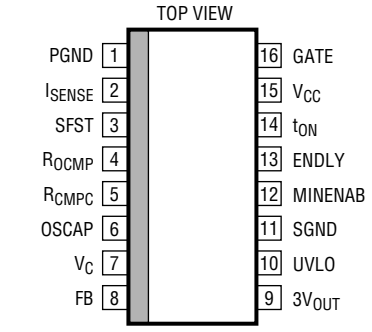


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} Supply Voltage 22V
UVLO Pin Voltage ..... V_{CC}
I_{SENSE} Pin Voltage 2V
FB Pin Current ..... ±2mA
Operating Junction
Temperature Range
LT1725C ..... 0°C to 100°C
LT1725I ..... –40°C TO 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 110°C/W (GN)
T_{JMAX} = 125°C, θ_{JA} = 100°C/W (SO)

ORDER PART NUMBER	GN PART MARKING
LT1725CGN LT1725IGN LT1725CS LT1725IS	1725 1725I

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 14V, GATE open, V_C = 1.4V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{CC}	V_{CC} Turn-On Voltage		●	14.0	15.1	16.0	V
	V_{CC} Turn-Off Voltage		●	8	9.7	11	V
	V_{CC} Hysteresis (Note 3)	($V_{TURN-ON}$ – $V_{TURN-OFF}$)	●	4.0	5.4	6.5	V
I_{CC}	Supply Current	V_C = Open	●	6	10	15	mA
	Start-Up Current		●		120	280	µA
Feedback Amplifier							
V_{FB}	Feedback Voltage			1.230	1.245	1.260	V
			●	1.220		1.270	V
I_{FB}	Feedback Pin Input Current				500		nA
g_m	Feedback Amplifier Transconductance	ΔI_C = ±10µA	●	400	1000	1800	µmho
I_{SRC}, I_{SNK}	Feedback Amplifier Source or Sink Current		●	30	50	80	µA
V_{CL}	Feedback Amplifier Clamp Voltage				2.5		V
	Reference Voltage/Current Line Regulation	12V ≤ V_{IN} ≤ 18V	●		0.01	0.05	%/V
	Voltage Gain	V_C = 1V to 2V			2000		V/V
	Soft-Start Charging Current	V_{SFST} = 0V		25	40	50	µA
	Soft-Start Discharge Current	V_{SFST} = 1.5V, V_{UVLO} = 0V		0.8	1.5		mA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 14V, GATE open, V_C = 1.4V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Output							
V_{GATE}	Output High Level	I_{GATE} = 100mA I_{GATE} = 500mA	● ●	11.5 11.0	12.1 11.8		V V
	Output Low Level	I_{GATE} = 100mA I_{GATE} = 500mA	● ●		0.3 0.6	0.45 1.0	V V
I_{GATE}	Output Sink Current in Shutdown, V_{UVLO} = 0V	V_{GATE} = 2V	●	1.2	2.5		mA
t_r	Rise Time	C_L = 1000pF			30		ns
t_f	Fall Time	C_L = 1000pF			30		ns
Current Amplifier							
V_C	Control Pin Threshold	Duty Cycle = Min	 ●	0.90 0.80	1.12	1.25 1.35	V V
V_{ISENSE}	Switch Current Limit	Duty Cycle ≤ 30% Duty Cycle ≤ 30% Duty Cycle = 80%	 ● 	220 200	250 220	270 280 	mV mV mV
	$\Delta V_{ISENSE}/\Delta V_C$				0.30		mV
Timing							
f	Switching Frequency	C_{OSCAP} = 100pF	 ●	90 80	100	115 125	kHz kHz
C_{OSCAP}	Oscillator Capacitor Value	(Note 2)		33		200	pF
t_{ON}	Minimum Switch On Time	R_{tON} = 50k			200		ns
t_{ED}	Flyback Enable Delay Time	R_{ENDLY} = 50k			200		ns
t_{EN}	Minimum Flyback Enable Time	R_{MENAB} = 50k			200		ns
R_t	Timing Resistor Value	(Note 2)		24		200	kΩ
	Maximum Switch Duty Cycle		●	85	90		%
Load Compensation							
	Sense Offset Voltage				2	5	mV
	Current Gain Factor			0.80	0.95	1.05	mV
UVLO Function							
V_{UVLO}	UVLO Pin Threshold		●	1.21	1.25	1.29	V
I_{UVLO}	UVLO Pin Bias Current	V_{UVLO} = 1.2V V_{UVLO} = 1.3V		−0.25 −4.50	+0.1 −3.5	+0.25 −2.50	µA µA
3V Output Function							
V_{REF}	Reference Output Voltage	I_{LOAD} = 1mA	●	2.8	3.0	3.2	V
	Output Impedance				10		Ω
	Current Limit		●	8	15		mA

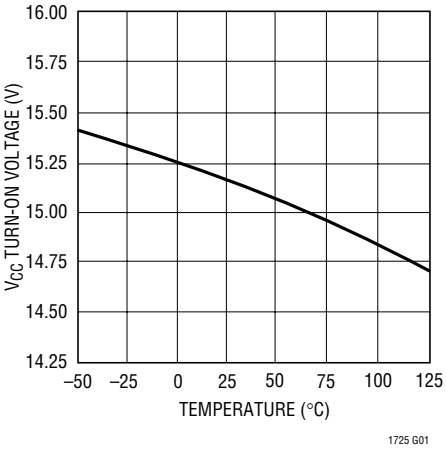
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Component value range guaranteed by design.

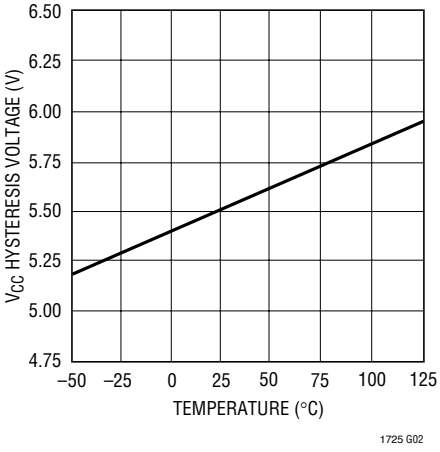
Note 3: The V_{CC} turn-on/turn-off voltages and hysteresis voltage are proportional in magnitude to each other-guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

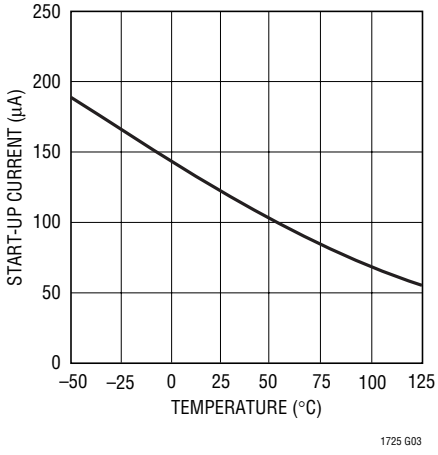
V_{CC} Turn-On Voltage vs Temperature



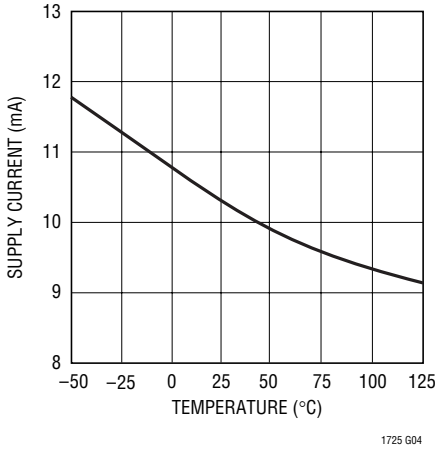
V_{CC} Hysteresis Voltage vs Temperature



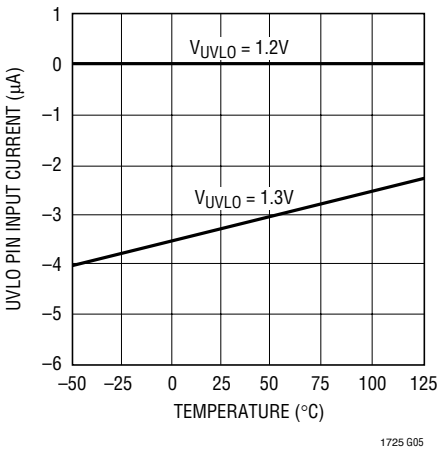
Start-Up Current vs Temperature



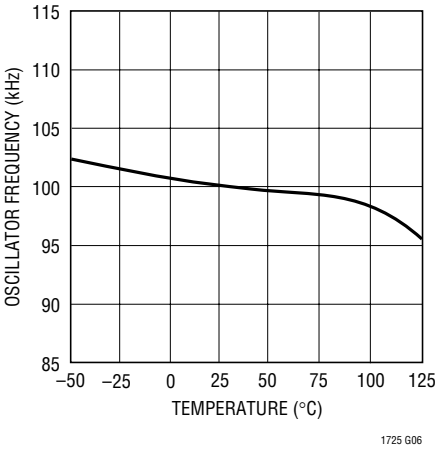
Supply Current vs Temperature



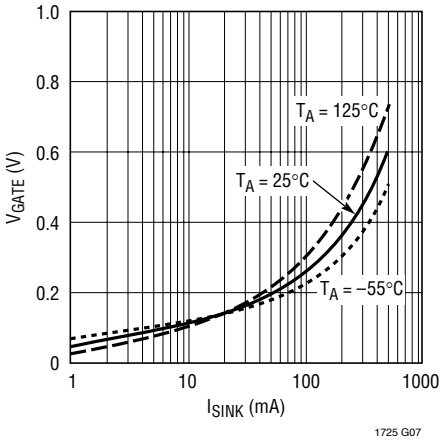
UVLO Pin Input Current vs Temperature



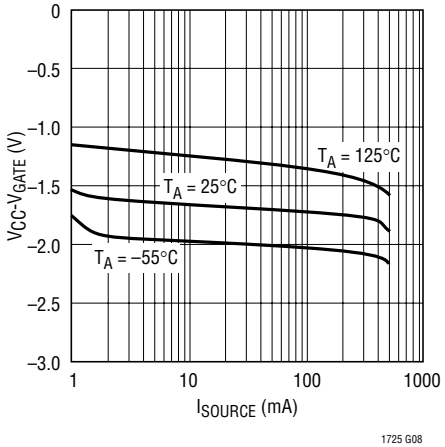
Oscillator Frequency vs Temperature



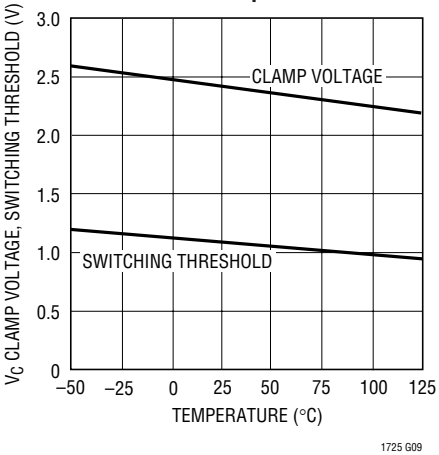
V_{GATE} vs I_{SINK}



V_{CC}-V_{GATE} vs I_{SOURCE}

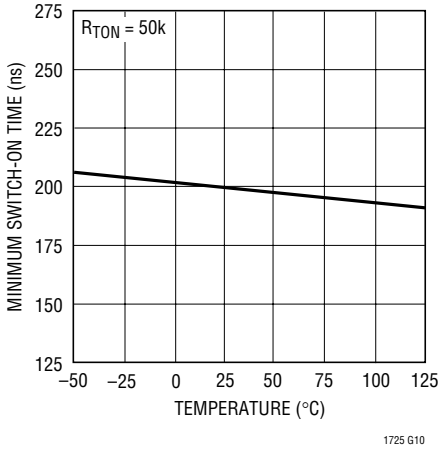


V_C Clamp Voltage, Switching Threshold vs Temperature

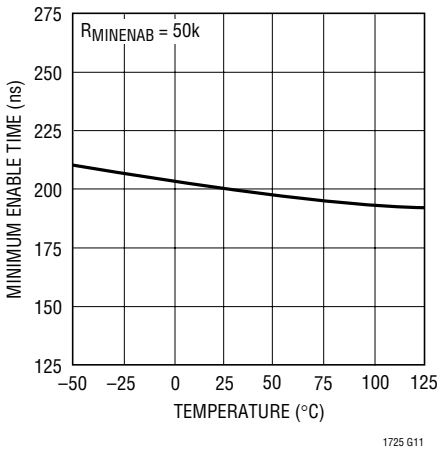


TYPICAL PERFORMANCE CHARACTERISTICS

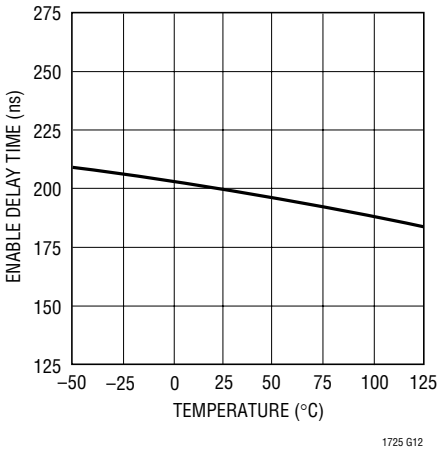
Minimum Switch-On Time vs Temperature



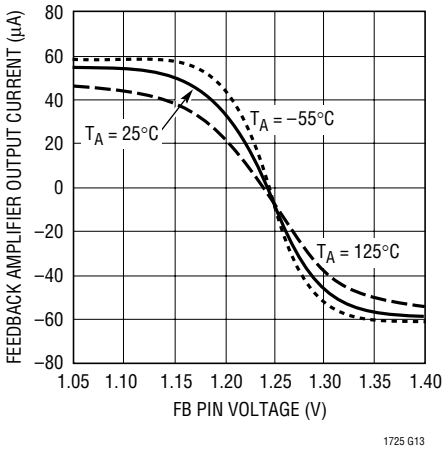
Minimum Enable Time vs Temperature



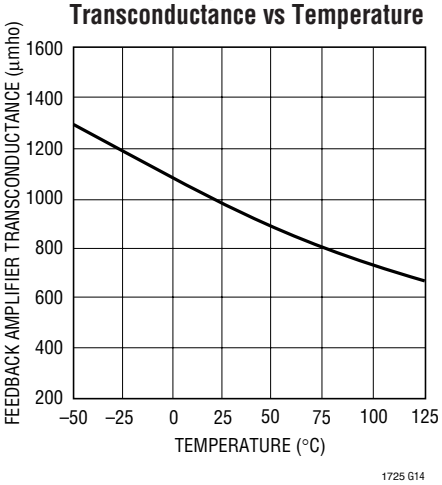
Enable Delay Time vs Temperature



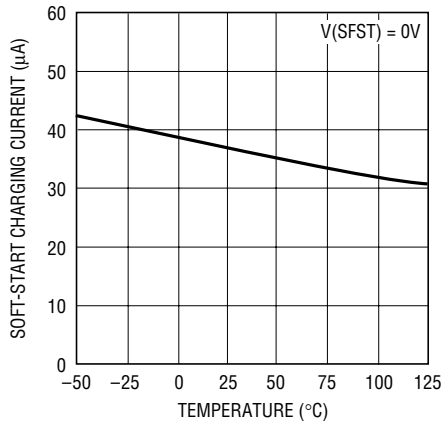
Feedback Amplifier Output Current vs FB Pin Voltage



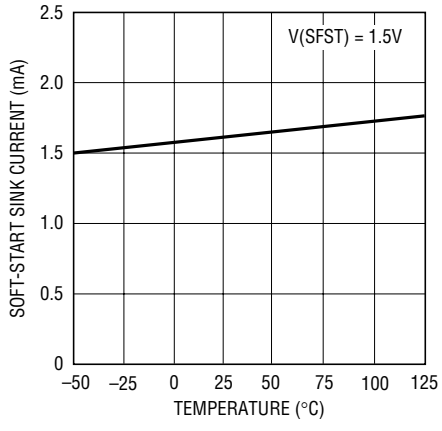
Feedback Amplifier Transconductance vs Temperature



Soft-Start Charging Current vs Temperature



Soft-Start Sink Current vs Temperature



PIN FUNCTIONS

PGND (Pin 1): The power ground pin carries the GATE node discharge current. This is typically a current spike of several hundred mA with a duration of tens of nanoseconds. It should be connected directly to a good quality ground plane.

I_{SENSE} (Pin 2): Pin to measure switch current with external sense resistor. The sense resistor should be of a noninductive construction as high speed performance is essential. Proper grounding technique is also required to avoid distortion of the high speed current waveform. A preset internal limit of nominally 250mV at this pin effects a switch current limit.

SFST (Pin 3): Pin for optional external capacitor to effect soft-start function. See Applications Information for details.

R_{OCMP} (Pin 4): Input pin for optional external load compensation resistor. Use of this pin allows nominal compensation for nonzero output impedance in the power transformer secondary circuit, including secondary winding impedance, output Schottky diode impedance and output capacitor ESR. In less demanding applications, this resistor is not needed. See Applications Information for more details.

R_{CMPC} (Pin 5): Pin for external filter capacitor for optional load compensation function. A common 0.1μF ceramic capacitor will suffice for most applications. See Applications Information for further details.

OSCAP (Pin 6): Pin for external timing capacitor to set oscillator switching frequency. See Applications Information for details.

V_C (pin 7): This is the control voltage pin which is the output of the feedback amplifier and the input of the current comparator. Frequency compensation of the overall loop is effected in most cases by placing a capacitor between this node and ground.

FB (Pin 8): Input pin for external "feedback" resistor divider. The ratio of this divider, times the internal bandgap (V_{BG}) reference, times the effective output-to-third winding transformer turns ratio is the primary determinant of the output voltage. The Thevenin equivalent resistance of the feedback divider should be roughly 3k. See Applications Information for more details.

$3V_{OUT}$ (Pin 9): Output pin for nominal 3V reference. This facilitates various user applications. This node is internally current limited for protection and is intended to drive either moderate capacitive loads of several hundred pF or less, or, very large capacitive loads of 0.1μF or more. See Applications Information for more details.

UVLO (Pin 10): This pin allows the use of an optional external resistor divider to set an undervoltage lockout based upon V_{IN} (not V_{CC}) level. (Note: If the V_{CC} voltage is sufficient to allow the part to start up, but the UVLO pin is held below its threshold, output switching action will be disabled, but the part will draw its normal quiescent current from V_{CC}. This typically causes a benign relaxation oscillation action on the V_{CC} pin in the conventional "trickle-charge" bootstrapped configuration.)

The bias current on this pin is a function of the state of the UVLO comparator; as the threshold is exceeded, the bias current increases. This creates a hysteresis band equal to the change in bias current times the Thevenin impedance of the user's resistive divider. The user may thereby adjust the impedance of the UVLO divider to achieve a desired degree of hysteresis. A 100pF capacitor to ground is recommended on this pin. See Applications Information for details.

SGND (Pin 11): The signal ground pin is a clean ground. The internal reference, oscillator and feedback amplifier are referred to it. Keep the ground path connection to the FB pin, OSCAP capacitor and the V_C compensation capacitor free of large ground currents.

MINENAB (Pin 12): Pin for external programming resistor to set minimum enable time. See Applications Information for details.

PIN FUNCTIONS

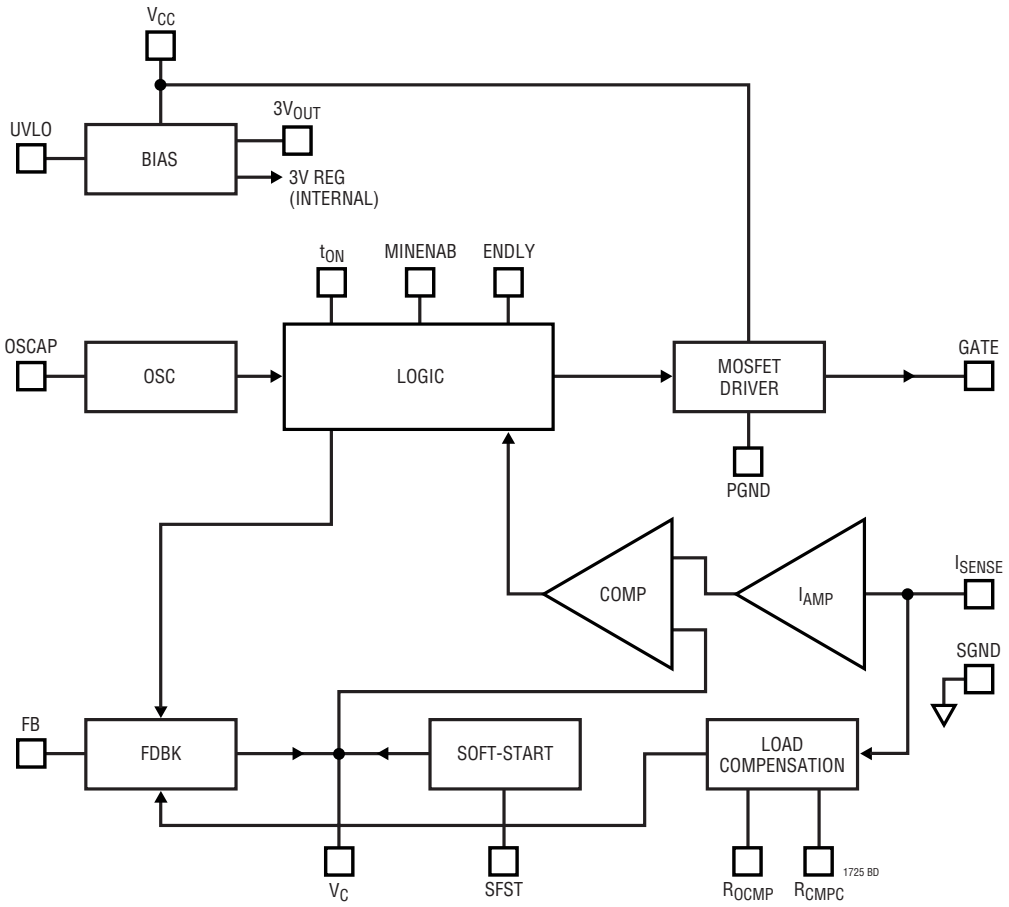
ENDLY (Pin 13): Pin for external programming resistor to set enable delay time. See Applications Information for details.

t_{ON} (Pin 14): Pin for external programming resistor to set switch minimum on time. See Applications Information for details.

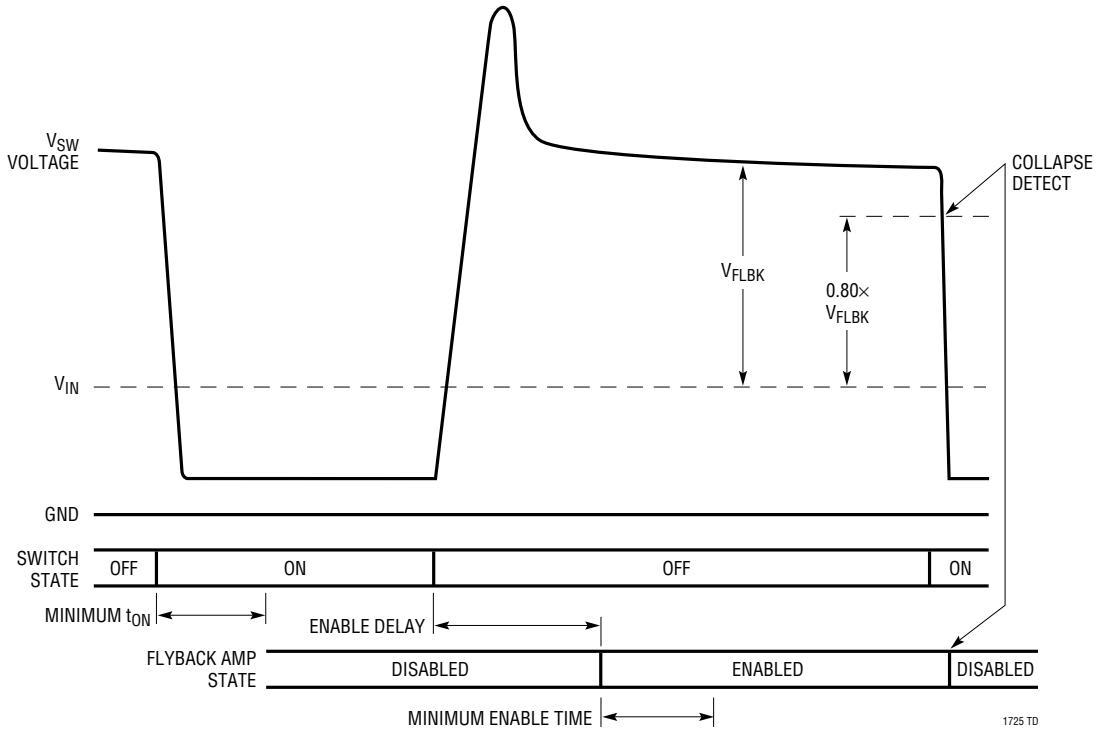
V_{CC} (Pin 15): Supply voltage for the LT1725. Bypass this pin to ground with 1μF or more.

GATE (Pin 16): This is the gate drive to the external power MOSFET switch and has large dynamic currents flowing through it. Keep the trace to the MOSFET as short as possible to minimize electromagnetic radiation and voltage spikes. A series resistance of 5Ω or more may help to dampen ringing in less than ideal layouts.

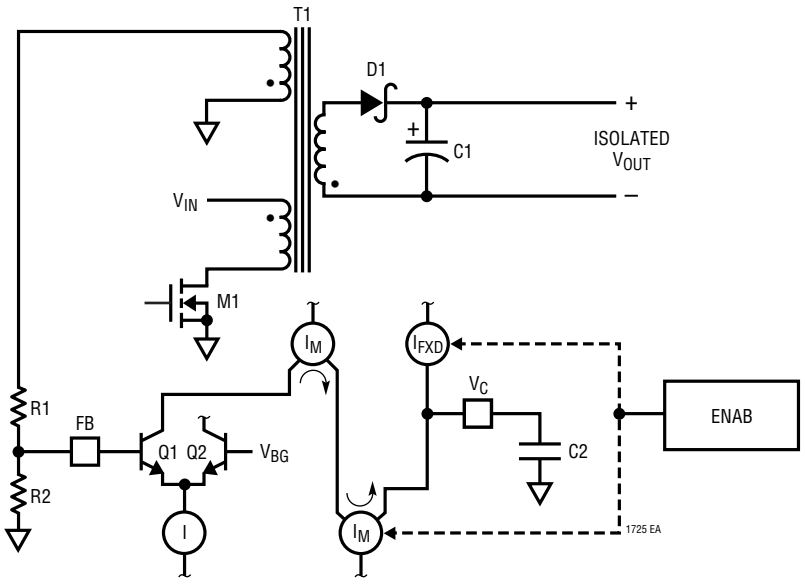
BLOCK DIAGRAM



TIMING DIAGRAM



FLYBACK ERROR AMPLIFIER



OPERATION

The LT1725 is a current mode switcher controller IC designed specifically for the isolated flyback topology. The Block Diagram shows an overall view of the system. Many of the blocks are similar to those found in traditional designs, including: Internal Bias Regulator, Oscillator, Logic, Current Amplifier and Comparator, Driver and Output Switch. The novel sections include a special Flyback Error Amplifier and a Load Compensation mechanism. Also, due to the special dynamic requirements of flyback control, the Logic system contains additional functionality not found in conventional designs.

The LT1725 operates much the same as traditional current mode switchers, the major difference being a different type of error amplifier that derives its feedback information from the flyback pulse. Due to space constraints, this discussion will not reiterate the basics of current mode switcher/controllers and isolated flyback converters. A good source of information on these topics is Application Note AN19.

ERROR AMPLIFIER—PSEUDO DC THEORY

Please refer to the simplified diagram of the Flyback Error Amplifier. Operation is as follows: when MOSFET output switch M1 turns off, its drain voltage rises above the V_{IN} rail. The amplitude of this flyback pulse as seen on the third winding is given as:

$$V_{FLBK} = \frac{(V_{OUT} + V_F + I_{SEC} \bullet ESR)}{N_{ST}}$$

V_F = D1 forward voltage

I_{SEC} = transformer secondary current

ESR = total impedance of secondary circuit

N_{ST} = transformer effective secondary-to-third winding turns ratio

The flyback voltage is then scaled by external resistor divider R1/R2 and presented at the FB pin. This is then compared to the internal bandgap reference by the differential transistor pair Q1/Q2. The collector current from Q1 is mirrored around and subtracted from fixed current source I_{FXD} at the V_C pin. An external capacitor integrates this net current to provide the control voltage to set the current mode trip point.

The relatively high gain in the overall loop will then cause the voltage at the FB pin to be nearly equal to the bandgap reference V_{BG}. The relationship between V_{FLBK} and V_{BG} may then be expressed as:

$$V_{FLBK} = \frac{(R1+R2)}{R2} V_{BG}$$

Combination with the previous V_{FLBK} expression yields an expression for V_{OUT} in terms of the internal reference, programming resistors, transformer turns ratio and diode forward voltage drop:

$$V_{OUT} = V_{BG} \frac{(R1+R2)}{R2} (N_{ST}) - V_F - I_{SEC} \bullet ESR$$

Additionally, it includes the effect of nonzero secondary output impedance, which is discussed below in further detail, see Load Compensation Theory. The practical aspects of applying this equation for V_{OUT} are found in the Applications Information section.

So far, this has been a pseudo-DC treatment of flyback error amplifier operation. But the flyback signal is a pulse, not a DC level. Provision must be made to enable the flyback amplifier only when the flyback pulse is present. This is accomplished by the dotted line connections to the block labeled “ENAB”. Timing signals are then required to enable and disable the flyback amplifier.

ERROR AMPLIFIER—DYNAMIC THEORY

There are several timing signals which are required for proper LT1725 operation. Please refer to the Timing Diagram.

Minimum Output Switch On Time

The LT1725 affects output voltage regulation via flyback pulse action. If the output switch is not turned on at all, there will be no flyback pulse and output voltage information is no longer available. This would cause irregular loop response and start-up/latchup problems. The solution chosen is to require the output switch to be on for an absolute minimum time per each oscillator cycle. This in turn establishes a minimum load requirement to maintain regulation. See Applications Information for further details.

OPERATION

Enable Delay

When the output switch shuts off, the flyback pulse appears. However, it takes a finite time until the transformer primary side voltage waveform approximately represents the output voltage. This is partly due to rise time on the MOSFET drain node, but more importantly, due to transformer leakage inductance. The latter causes a voltage spike on the primary side not directly related to output voltage. (Some time is also required for internal settling of the feedback amplifier circuitry.)

In order to maintain immunity to these phenomena, a fixed delay is introduced between the switch turnoff command and the enabling of the feedback amplifier. This is termed "enable delay". In certain cases where the leakage spike is not sufficiently settled by the end of the enable delay period, regulation error may result. See Applications Information for further details.

Collapse Detect

Once the feedback amplifier is enabled, some mechanism is then required to disable it. This is accomplished by a collapse detect comparator, which compares the flyback voltage (FB referred) to a fixed reference, nominally 80% of V_{BG}. When the flyback waveform drops below this level, the feedback amplifier is disabled. This action accommodates both continuous and discontinuous mode operation.

Minimum Enable Time

The feedback amplifier, once enabled, stays enabled for a fixed minimum time period termed "minimum enable time." This prevents lockup, especially when the output voltage is abnormally low, e.g., during start-up. The minimum enable time period ensures that the V_C node is able to "pump up" and increase the current mode trip point to the level where the collapse detect system exhibits proper operation. The "minimum enable time" often determines the low load level at which output voltage regulation is lost. See Applications Information for details.

Effects of Variable Enable Period

It should now be clear that the flyback amplifier is enabled during only a portion of the cycle time. This can vary from the fixed "minimum enable time" described to a maximum of roughly the "off" switch time minus the enable delay time. Certain parameters of flyback amp behavior will then be directly affected by the variable enable period. These include effective transconductance and V_C node slew rate.

LOAD COMPENSATION THEORY

The LT1725 uses the flyback pulse to obtain information about the isolated output voltage. A potential error source is caused by transformer secondary current flow through the real life nonzero impedances of the output rectifier,

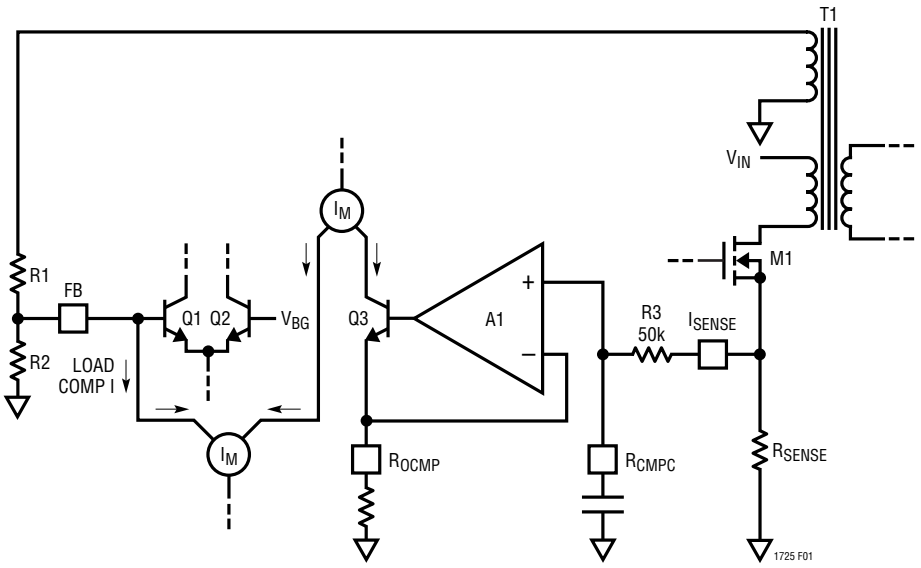


Figure 1. Load Compensation Diagram

OPERATION

transformer secondary and output capacitor. This has been represented previously by the expression "I_{SEC} • ESR." However, it is generally more useful to convert this expression to an effective output impedance. Because the secondary current only flows during the off portion of the duty cycle, the effective output impedance equals the lumped secondary impedance times the inverse of the OFF duty cycle. That is:

$$R_{OUT} = ESR\left(\frac{1}{DC_{OFF}}\right) \text{ where}$$

R_{OUT} = effective supply output impedance

ESR = lumped secondary impedance

DC_{OFF} = OFF duty cycle

Expressing this in terms of the ON duty cycle, remembering $DC_{OFF} = 1 – DC$,

$$R_{OUT} = ESR\left(\frac{1}{1-DC}\right)$$

DC = ON duty cycle

In less critical applications, or if output load current remains relatively constant, this output impedance error may be judged acceptable and the external FB resistor divider adjusted to compensate for nominal expected error. In more demanding applications, output impedance error may be minimized by the use of the load compensation function.

To implement the load compensation function, a voltage is developed that is proportional to average output switch current. This voltage is then impressed across the external R_{OCMP} resistor, and the resulting current acts to increase the V_{BG} reference used by the flyback error amplifier. As output loading increases, average switch current increases to maintain rough output voltage regulation. This causes an increase in R_{OCMP} resistor current which effects a corresponding increase in target output voltage.

Assuming a relatively fixed power supply efficiency, Eff,

Power Out = Eff • Power In

$V_{OUT} • I_{OUT} = Eff • V_{IN} • I_{IN}$

Average primary side current may be expressed in terms of output current as follows:

$$I_{IN} = \left(\frac{V_{OUT}}{V_{IN} • EFF}\right) • I_{OUT}$$

combining the efficiency and voltage terms in a single variable:

$I_{IN} = K1 • I_{OUT}$, where

$$K1 = \left(\frac{V_{OUT}}{V_{IN} • EFF}\right)$$

Switch current is converted to voltage by the external sense resistor and averaged/lowpass filtered by R3 and the external capacitor on R_{CMPC}. This voltage is then impressed across the external R_{OCMP} resistor by op amp A1 and transistor Q3. This produces a current at the collector of Q3 which is then mirrored around and then subtracted from the FB node. This action effectively increases the voltage required at the top of the R1/R2 feedback divider to achieve equilibrium. So the effective change in V_{OUT} target is:

$$\Delta V_{OUT} = (K1 • \Delta I_{OUT})\left(\frac{R_{SENSE}}{R_{OCMP}}\right) • R1 • N_{ST} \text{ or}$$

$$\frac{\Delta V_{OUT}}{\Delta I_{OUT}} = K1\left(\frac{R_{SENSE}}{R_{OCMP}}\right) • R1 • N_{ST}$$

Nominal output impedance cancellation is obtained by equating this expression with R_{OUT}:

$$R_{OUT} = \frac{ESR}{1-DC} = K1\left(\frac{R_{SENSE}}{R_{OCMP}}\right) • R1 • N_{ST}$$

$$R_{OCMP} = K1 • R_{SENSE} • \frac{(1-DC)}{ESR} • R1 • N_{ST}$$

K1 = dimensionless variable related to V_{IN}, V_{OUT} and efficiency as above

R_{SENSE} = external sense resistor

R_{OUT} = uncompensated output impedance

The practical aspects of applying this equation to determine an appropriate value for the R_{OCMP} resistor are found in the Applications Information section.

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TRANSFORMER DESIGN CONSIDERATIONS

Transformer specification and design is perhaps the most critical part of applying the LT1725 successfully. In addition to the usual list of caveats dealing with high frequency isolated power supply transformer design, the following information should prove useful.

Turns Ratios

Note that due to the use of the external feedback resistor divider ratio to set output voltage, the user has relative freedom in selecting transformer turns ratio to suit a given application. In other words, "screwball" turns ratios like "1.736:1.0" can scrupulously be avoided! In contrast, simpler ratios of small integers, e.g., 1:1, 2:1, 3:2, etc. can be employed which yield more freedom in setting total turns and mutual inductance. Turns ratio can then be chosen on the basis of desired duty cycle. However, remember that the input supply voltage plus the secondary-to-primary referred version of the flyback pulse (including leakage spike) must not exceed the allowed external MOSFET breakdown rating.

Leakage Inductance

Transformer leakage inductance (on either the primary or secondary) causes a spike after output switch turnoff. This is increasingly prominent at higher load currents, where more stored energy must be dissipated. In many cases a "snubber" circuit will be required to avoid overvoltage breakdown at the output switch node. Application Note AN19 is a good reference on snubber design.

In situations where the flyback pulse extends beyond the enable delay time, the output voltage regulation will be affected to some degree. It is important to realize that the feedback system has a deliberately limited input range, roughly ±50mV referred to the FB node, and this works to the user's advantage in rejecting large, i.e., higher voltage, leakage spikes. In other words, once a leakage spike is several volts in amplitude, a further increase in amplitude has little effect on the feedback system. So the user is generally advised to arrange the snubber circuit to clamp at as high a voltage as comfortably possible, observing MOSFET breakdown, such that leakage spike duration is as short as possible.

As a rough guide, total leakage inductances of several percent (of mutual inductance) or less may require a snubber, but exhibit little to no regulation error due to leakage spike behavior. Inductances from several percent up to perhaps ten percent cause increasing regulation error.

Severe leakage inductances in the double digit percentage range should be avoided if at all possible as there is a potential for abrupt loss of control at high load current. This curious condition potentially occurs when the leakage spike becomes such a large portion of the flyback waveform that the processing circuitry is fooled into thinking that the leakage spike itself is the real flyback signal! It then reverts to a potentially stable state whereby the top of the leakage spike is the control point, and the trailing edge of the leakage spike triggers the collapse detect circuitry. This will typically reduce the output voltage abruptly to a fraction, perhaps between one-third to two-thirds of its correct value. If load current is reduced sufficiently, the system will snap back to normal operation. When using transformers with considerable leakage inductance, it is important to exercise this worst-case check for potential bistability:

1. Operate the prototype supply at maximum expected load current.
2. Temporarily short circuit the output.
3. Observe that normal operation is restored.

If the output voltage is found to hang up at a abnormally low value, the system has a problem. This will usually be evident by simultaneously monitoring the V_{SW} waveform on an oscilloscope to observe leakage spike behavior firsthand. A final note—the susceptibility of the system to bistable behavior is somewhat a function of the load I/V characteristics. A load with resistive, i.e., I = V/R behavior is the most susceptible to bistability. Loads which exhibit "CMOSsy", i.e., $I = V^2/R$ behavior are less susceptible.

Secondary Leakage Inductance

In addition to the previously described effects of leakage inductance in general, leakage inductance on the secondary in particular exhibits an additional phenomenon. It forms an inductive divider on the transformer secondary,

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which reduces the size of the primary-referred flyback pulse used for feedback. This will increase the output voltage target by a similar percentage. Note that unlike leakage spike behavior, this phenomena is load independent. To the extent that the secondary leakage inductance is a constant percentage of mutual inductance (over manufacturing variations), this can be accommodated by adjusting the feedback resistor divider ratio.

Winding Resistance Effects

Resistance in either the primary or secondary will act to reduce overall efficiency (P_{OUT}/P_{IN}). Resistance in the secondary increases effective output impedance which degrades load regulation, (at least before load compensation is employed).

Bifilar Winding

A bifilar or similar winding technique is a good way to minimize troublesome leakage inductances. However remember that this will increase primary-to-secondary capacitance and limit the primary-to-secondary breakdown voltage, so bifilar winding is not always practical.

Finally, the LTC Applications group is available to assist in the choice and/or design of the transformer. Happy Winding!

SELECTING FEEDBACK RESISTOR DIVIDER VALUES

The expression for V_{OUT} developed in the Operation section can be rearranged to yield the following expression for the R1/R2 ratio:

$$\frac{(R1+R2)}{R2}=\frac{(V_{OUT}+V_F+I_{SEC}\bullet ESR)}{V_{BG}\bullet N_{ST}}$$

where:

V_{OUT} = desired output voltage

V_F = switching diode forward voltage

I_{SEC} • ESR = secondary resistive losses

V_{BG} = data sheet reference voltage value

N_{ST} = effective secondary-to-third winding turns ratio

The above equation defines only the ratio of R1 to R2, not their individual values. However, a "second equation for two unknowns" is obtained from noting that the Thevenin impedance of the resistor divider should be roughly 3k for bias current cancellation and other reasons.

SELECTING R_{OCMP} RESISTOR VALUE

The Operation section previously derived the following expressions for R_{OUT}, i.e., effective output impedance and R_{OCMP}, the external resistor value required for its nominal compensation:

$$R_{OUT}=ESR\left(\frac{1}{1-DC}\right)$$

$$R_{OCMP}=K1\left(\frac{R_{SENSE}}{R_{OUT}}\right)(R1\bullet N_{ST})$$

While the value for R_{OCMP} may therefore be theoretically determined, it is usually better in practice to employ empirical methods. This is because several of the required input variables are difficult to estimate precisely. For instance, the ESR term above includes that of the transformer secondary, but its effective ESR value depends on high frequency behavior, not simply DC winding resistance. Similarly, K1 appears to be a simple ratio of V_{IN} to V_{OUT} times (differential) efficiency, but theoretically estimating efficiency is not a simple calculation. The suggested empirical method is as follows:

Build a prototype of the desired supply using the eventual secondary components. Temporarily ground the R_{CMPC} pin to disable the load compensation function. Operate the supply over the expected range of output current loading while measuring the output voltage deviation. Approximate this variation as a single value of R_{OUT} (straight line approximation). Calculate a value for the K1 constant based on V_{IN}, V_{OUT} and the measured (differential) efficiency. These are then combined with R_{SENSE} as indicated to yield a value for R_{OCMP}.

Verify this result by connecting a resistor of roughly this value from the R_{OCMP} pin to ground. (Disconnect the ground short to R_{CMPC} and connect the requisite 0.1µF filter capacitor to ground.) Measure the output impedance

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with the new compensation in place. Modify the original R_{OCMP} value if necessary to increase or decrease the effective compensation.

SELECTING OSCILLATOR CAPACITOR VALUE

The switching frequency of the LT1725 is set by an external capacitor connected between the OSCAP pin and ground. Recommended values are between 200pF and 33pF, yielding switching frequencies between 50kHz and 250kHz. Figure 2 shows the nominal relationship between external capacitance and switching frequency. To minimize stray capacitance and potential noise pickup, this capacitor should be placed as close as possible to the IC and the OSCAP node length/area minimized.

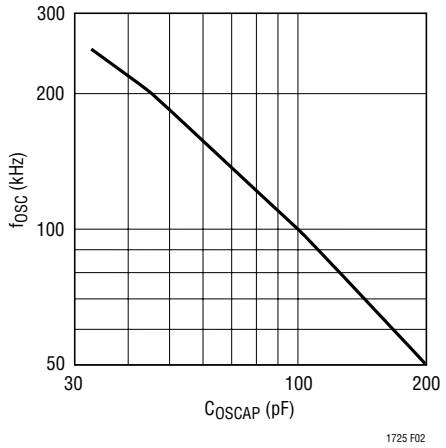

Figure 2. f_{OSC} vs OSCAP Value

SELECTING TIMING RESISTOR VALUES

There are three internal "one-shot" times that are programmed by external application resistors: minimum on time, enable delay time and minimum enable time. These are all part of the isolated flyback control technique, and their functions have been previously outlined in the Theory of Operation section. Figures 3 shows nominal observed time versus external resistor value for these functions.

The following information should help in selecting and/or optimizing these timing values.

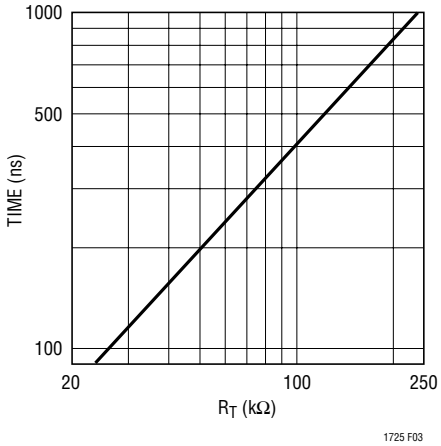

Figure 3. "One Shot" Times vs Programming Resistor

Minimum On Time

This time defines a period whereby the normal switch current limit is ignored. This feature provides immunity to the leading edge current spike often seen at the source node of the external power MOSFET, due to rapid charging of its gate/source capacitance. This current spike is not indicative of actual current level in the transformer primary, and may cause irregular current mode switching action, especially at light load.

However, the user must remember that the LT1725 does not "skip cycles" at light loads. Therefore, minimum on time will set a limit on minimum delivered power and consequently a minimum load requirement to maintain regulation (see Minimum Load Considerations). Similarly, minimum on time has a direct affect on short-circuit behavior (see Maximum Load/Short-Circuit Considerations).

The user is normally tempted to set the minimum on time to be short to minimize these load related consequences. (After all, a smaller minimum on time approaches the ideal case of zero, or no minimum.) However, a longer time may be required in certain applications based on MOSFET switching current spike considerations.

Enable Delay Time

This function provides a programmed delay between turnoff of the gate drive node and the subsequent enabling of the feedback amplifier. At high loads, a primary side voltage spike after MOSFET turnoff may be observed due

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to transformer leakage inductance. This spike is not indicative of actual output voltage (see Figure 4B). Delaying the enabling of the feedback amplifier allows this system to effectively ignore most or all of the voltage spike and maintain proper output voltage regulation. The enable delay time should therefore be set to the maximum expected duration of the leakage spike. This may have implications regarding output voltage regulation at minimum load (see Minimum Load Considerations).

A second benefit of the enable delay time function occurs at light load. Under such conditions the amount of energy stored in the transformer is small. The flyback waveform becomes "lazy" and some time elapses before it indicates the actual secondary output voltage (see Figure 4C). So the enable delay time should also be set long enough to ignore the "irrelevant" portion of the flyback waveform at light load.

Additionally, there are cases wherein the gate output is called upon to drive a large geometry MOSFET such that the turnoff transition is slowed significantly. Under such circumstances, the enable delay time may be increased to accommodate for the lengthy transition.

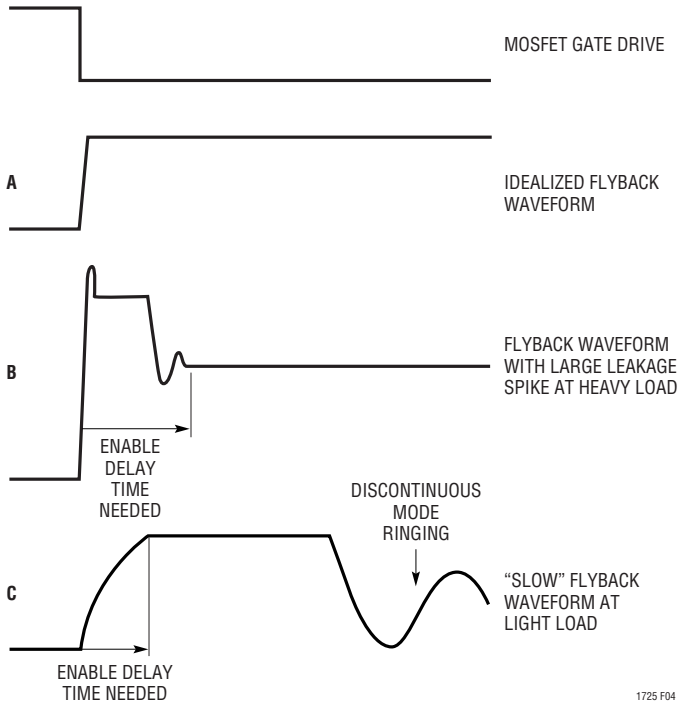

Figure 4

Minimum Enable Time

This function sets a minimum duration for the expected flyback pulse. Its primary purpose is to provide a minimum source current at the V_C node to avoid start-up problems.

$$\text{Average "start-up" } V_C \text{ current} = \frac{\text{Minimum Enable Time}}{\text{Switching Frequency}} \bullet I_{SRC}$$

Minimum enable time can also have implications at light load (see Minimum Load Considerations). The temptation is to set the minimum enable time to be fairly short, as this is the least restrictive in terms of minimum load behavior. However, to provide a "reliable" minimum start-up current of say, nominally 1μA, the user should set the minimum enable time at no less that 2% of the switching period (= 1/switching frequency).

CURRENT SENSE RESISTOR CONSIDERATIONS

The external current sense resistor allows the user to optimize the current limit behavior for the particular application under consideration. As the current sense resistor is varied from several ohms down to tens of milliohms, peak switch current goes from a fraction of an ampere to tens of amperes. Care must be taken to ensure proper circuit operation, especially with small current sense resistor values.

For example, a peak switch current of 10A requires a sense resistor of 0.025Ω. Note that the instantaneous peak power in the sense resistor is 2.5W, and it must be rated accordingly. The LT1725 has only a single sense line to this resistor. Therefore, any parasitic resistance in the ground side connection of the sense resistor will increase its apparent value. In the case of a 0.025Ω sense resistor, *one milliohm* of parasitic resistance will cause a 4% reduction in peak switch current. So resistance of printed circuit copper traces and vias cannot necessarily be ignored.

An additional consideration is parasitic inductance. Inductance in series with the current sense resistor will accentuate the high frequency components of the current waveform. In particular, the gate switching spike and multimegahertz ringing at the MOSFET can be considerably

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amplified. If severe enough, this can cause erratic operation. For example, assume 3nH of parasitic inductance (equivalent to about 0.1 inch of wire in free space) is in series with an ideal 0.025Ω sense resistor. A "zero" will be formed at f = R/(2πL), or 1.3MHz. Above this frequency the sense resistor will behave like an inductor.

Several techniques can be used to tame this potential parasitic inductance problem. First, any resistor used for current sensing purposes must be of an inherently non-inductive construction. Mounting this resistor directly above an unbroken ground plane and minimizing its ground side connection will serve to absolutely minimize parasitic inductance. In the case of low valued sense resistors, these may be implemented as a parallel combination of several resistors for the thermal considerations cited above. The parallel combination will help to lower the parasitic inductance. Finally, it may be necessary to place a "pole" between the current sense resistor and the LT1725 I_{SENSE} pin to undo the action of the inductive zero (see Figure 5). A value of 51Ω is suggested for the resistor, while the capacitor is selected empirically for the particular application and layout. Using good high frequency measurement techniques, the I_{SENSE} pin waveform may be observed directly with an oscilloscope while the capacitor value is varied.

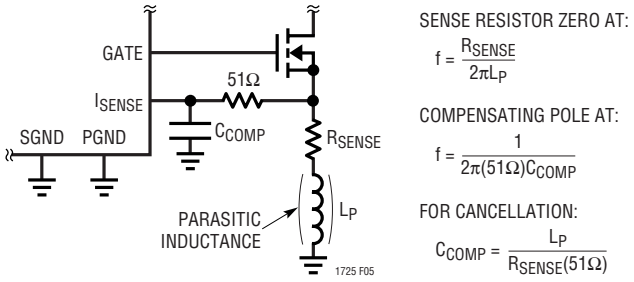

Figure 5

SOFT-START FUNCTION

The LT1725 contains an optional soft-start function that is enabled by connecting an explicit external capacitor between the SFST pin and ground. Internal circuitry prevents the control voltage at the V_C pin from exceeding that on the SFST pin.

The soft-start function is enagaged whenever V_{CC} power is removed, or as a result of either undervoltage lockout or thermal (overtemperature) shutdown. The SFST node is then discharged to roughly a V_{BE} above ground. (Remember that the V_C pin control node switching threshold is deliberately set at a V_{BE} *plus* several hundred millivolts.) When this condition is removed, a nominal 40μA current acts to charge up the SFST node towards roughly 3V. So, for example, a 0.1μF soft-start capacitor will place a 0.4V/ms limit on the ramp rate at the V_C node.

UVLO PIN FUNCTION

The UVLO pin effects an undervoltage lockout function with at threshold of roughly 1.25V. An external resistor divider between the input supply and ground can then be used to achieve a user-programmable undervoltage lockout (see Figure 6a).

An additional feature of this pin is that there is a change in the input bias current at this pin as a function of the state of the internal UVLO comparator. As the pin is brought above the UVLO threshold, the bias current sourced by the part increases. This positive feedback effects a hysteresis band for reliable switching action. Note that the size of the hysteresis is proportional to the Thevenin impedance of the external UVLO resistor divider network, which makes it user programmable. As a rough rule of thumb, each 4k or so of impedance generates about 1% of hysteresis. (This is based on roughly 1.25V for the threshold and 3μA for the bias current shift.)

Even in good quality ground plane layouts, it is common for the switching node (MOSFET drain) to couple to the UVLO pin with a stray capacitance of several *thousandths* of a pF. To ensure proper UVLO action, a 100pF capacitor is recommended from this pin to ground as shown in Figure 6b. This will typically reduce the coupled noise to a few millivolts. The UVLO filter capacitor should not be made much larger than a few hundred pF, however, as the hysteresis action will become too slow. In cases where further filtering is required, e.g., to attenuate high speed supply ripple, the topology in Figure 6c is recommended. Resistor R1 has been split into two equal parts. This provides a node for effecting capacitor filtering of high

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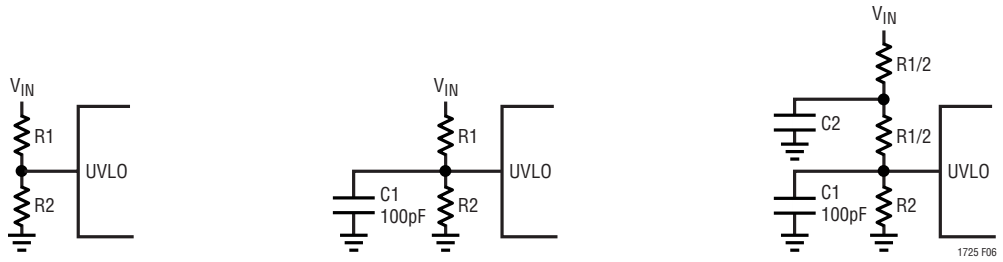

(6a) "Standard" UVLO Divider Topology

(6b) Filter Capacitor Directly On UVLO Node

(6c) Recommended Topology to Filter High Frequency Ripple

Figure 6

speed supply ripple, while leaving the UVLO pin node impedance relatively unchanged at high frequency.

INTERNAL WIDE HYSTERESIS UNDERVOLTAGE LOCKOUT

The LT1725 is designed to implement isolated DC/DC converters operating from input voltages of typically 48V or more. The standard operating topology utilizes a third transformer winding on the primary side that provides both feedback information and local power for the LT1725 via its V_{CC} pin. However, this arrangement is not inherently self-starting. Start-up is effected by the use of an external "trickle-charge" resistor and the presence of an internal wide hysteresis undervoltage lockout circuit that monitors V_{CC} pin voltage (see Figure 7). Operation is as follows:

"Trickle charge" resistor R1 is connected to V_{IN} and supplies a small current, typically on the order of a single mA, to charge C1. At first, the LT1725 is off and draws only its start-up current. After some time, the voltage on C1 (V_{CC}) reaches the V_{CC} turn-on threshold. The LT1725 then turns on abruptly and draws its normal supply current. Switching action commences at the GATE pin and the MOSFET begins to deliver power. The voltage on C1 begins to decline as the LT1725 draws its normal supply current, which greatly exceeds that delivered by R1. After some time, typically tens of milliseconds, the output voltage approaches its desired value. By this time, the third transformer winding is providing virtually all the supply current required by the LT1725.

One potential design pitfall is undersizing the value of capacitor C1. In this case, the normal supply current

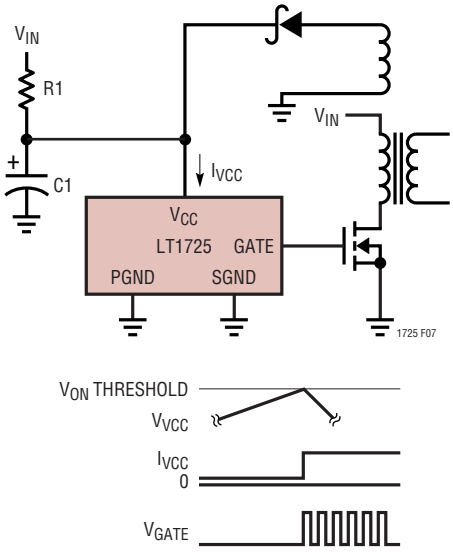

Figure 7

drawn by the LT1725 will discharge C1 too rapidly; before the third winding drive becomes effective, the V_{CC} turn-off threshold will be reached. The LT1725 turns off, and the V_{CC} node begins to charge via R1 back up to the turn-on threshold. Depending upon the particular situation, this may result in either several on-off cycles before proper operation is reached, or, permanent relaxation oscillation at the V_{CC} node.

Component selection is as follows:

Resistor R1 should be selected to yield a worst-case minimum charging current greater than the maximum rated LT1725 start-up current, and a worst-case maximum charging current less than the minimum rated LT1725 supply current.

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Capacitor C1 should then be made large enough to avoid the relaxation oscillatory behavior described above. This is complicated to determine theoretically as it depends on the particulars of the secondary circuit and load behavior. Empirical testing is recommended. (Use of the optional soft-start function will lengthen the power-up timing and require a correspondingly larger value for C1.)

A further note—certain users may wish to utilize the general functionality of the LT1725, but may have an available input voltage significantly lower than, say, 48V. If this input voltage is within the allowable V_{CC} range, i.e., perhaps 20V maximum, the internal wide hysteresis range UVLO function becomes counterproductive. In such cases it is simply better to operate the LT1725 directly from the available DC input supply. The LT1737 is identical to the LT1725, with the exception that it lacks the internal wide hysteresis UVLO function. It is therefore designed to operate directly from DC input supplies in the range of 4.5V to 20V. See the LT1737 data sheet for further information.

FREQUENCY COMPENSATION

Loop frequency compensation is performed by connecting a capacitor from the output of the error amplifier (V_C pin) to ground. An additional series resistor, often required in traditional current mode switcher controllers, is usually not required and can even prove detrimental. The phase margin improvement traditionally offered by this extra resistor will usually be already accomplished by the nonzero secondary circuit impedance, which adds a "zero" to the loop response.

In further contrast to traditional current mode switchers, V_C pin ripple is generally not an issue with the LT1725. The dynamic nature of the clamped feedback amplifier forms an effective track/hold type response, whereby the V_C voltage changes during the flyback pulse, but is then "held" during the subsequent "switch on" portion of the next cycle. This action naturally holds the V_C voltage stable during the current comparator sense action (current mode switching).

OUTPUT VOLTAGE ERROR SOURCES

Conventional nonisolated switching power supply ICs typically have only two substantial sources of output voltage error: the internal or external resistor divider network that connects to V_{OUT} and the internal IC reference. The LT1725, which senses the output voltage in both a dynamic and an isolated manner, exhibits additional potential error sources to contend with. Some of these errors are proportional to output voltage, others are fixed in an absolute millivolt sense. Here is a list of possible error sources and their effective contribution.

Internal Voltage Reference

The internal bandgap voltage reference is, of course, imperfect. Its error, both at 25°C and over temperature is already included in the specifications.

User Programming Resistors

Output voltage is controlled by the user-supplied feedback resistor divider ratio. To the extent that the resistor ratio differs from the ideal value, the output voltage will be proportionally affected. Highest accuracy systems will demand 1% components.

Schottky Diode Drop

The LT1725 senses the output voltage from the transformer primary side during the flyback portion of the cycle. This sensed voltage therefore includes the forward drop, V_F, of the rectifier (usually a Schottky diode). The nominal V_F of this diode should therefore be included in feedback resistor divider calculations. Lot to lot and ambient temperature variations will show up as output voltage shift/drift.

Secondary Leakage Inductance

Leakage inductance on the transformer secondary reduces the effective secondary-to-third winding turns ratio (N_S/N_T) from its ideal value. This will increase the output voltage target by a similar percentage. To the extent that secondary leakage inductance is constant from part to part, this can be accommodated by adjusting the feedback resistor ratio.

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Output Impedance Error

An additional error source is caused by transformer secondary current flow through the real life nonzero impedances of the output rectifier, transformer secondary and output capacitor. Because the secondary current only flows during the off portion of the duty cycle, the effective output impedance equals the "DC" lumped secondary impedance times the inverse of the off duty cycle. If the output load current remains relatively constant, or, in less critical applications, the error may be judged acceptable and the feedback resistor divider ratio adjusted for nominal expected error. In more demanding applications, output impedance error may be minimized by the use of the load compensation function (see Load Compensation).

MINIMUM LOAD CONSIDERATIONS

The LT1725 generally provides better low load performance than previous generation switcher/controllers utilizing indirect output voltage sensing techniques. Specifically, it contains circuitry to detect flyback pulse "collapse," thereby supporting operation well into discontinuous mode. Nevertheless, there still remain constraints to ultimate low load operation. These relate to the minimum switch on time and the minimum enable time. Discontinuous mode operation will be assumed in the following theoretical derivations.

As outlined in the Operation section, the LT1725 utilizes a minimum output switch on time, t_{ON}. This value can be combined with expected V_{IN} and switching frequency to yield an expression for minimum delivered power.

$$\text{Minimum Power} = \frac{1}{2}\left(\frac{f}{L_{PRI}}\right)\left(V_{IN} \bullet t_{ON}\right)^2 = V_{OUT} \bullet I_{OUT}$$

This expression then yields a minimum output current constraint:

$$I_{OUT(MIN)} = \frac{1}{2}\left(\frac{f}{L_{PRI} \bullet V_{OUT}}\right)\left(V_{IN} \bullet t_{ON}\right)^2 \text{ where}$$

f = switching frequency

L_{PRI} = transformer primary side inductance

V_{IN} = input voltage

V_{OUT} = output voltage

t_{ON} = output switch minimum on time

An additional constraint has to do with the minimum enable time. The LT1725 derives its output voltage information from the flyback pulse. If the internal minimum enable time pulse extends beyond the flyback pulse, loss of regulation will occur. The onset of this condition can be determined by setting the width of the flyback pulse equal to the sum of the flyback enable delay, t_{ED}, plus the minimum enable time, t_{EN}. Minimum power delivered to the load is then:

$$\text{Minimum Power} = \frac{1}{2}\left(\frac{f}{L_{SEC}}\right)\left[V_{OUT} \bullet \left(t_{EN} + t_{ED}\right)\right]^2 = V_{OUT} \bullet I_{OUT}$$

Which yields a minimum output constraint:

$$I_{OUT(MIN)} = \frac{1}{2}\left(\frac{f \bullet V_{OUT}}{L_{SEC}}\right)\left(t_{ED} + t_{EN}\right)^2 \text{ where}$$

f = switching frequency

L_{SEC} = transformer secondary side inductance

V_{OUT} = output voltage

t_{ED} = enable delay time

t_{EN} = minimum enable time

Note that generally, depending on the particulars of input and output voltages and transformer inductance, one of the above constraints will prove more restrictive. In other words, the minimum load current in a particular application will be either "output switch minimum on time" constrained, or "minimum flyback pulse time" constrained. (A final note—L_{PRI} and L_{SEC} refer to transformer inductance as seen from the primary or secondary side respectively. This general treatment allows these expressions to be used when the transformer turns ratio is nonunity.)

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MAXIMUM LOAD/SHORT-CIRCUIT CONSIDERATIONS

The LT1725 is a current mode controller. It uses the V_C node voltage as an input to a current comparator which turns off the output switch on a cycle-by-cycle basis as this peak current is reached. The internal clamp on the V_C node, nominally 2.5V, then acts as an output switch peak current limit.

This 2.5V at the V_C pin corresponds to a value of 250mV at the I_{SENSE} pin, when the (ON) switch duty cycle is less than 40%. For a duty cycle above 40%, the internal slope compensation mechanism lowers the effective I_{SENSE} voltage limit. For example, at a duty cycle of 80%, the nominal I_{SENSE} voltage limit is 220mV. This action becomes the switch current limit specification. Maximum available output power is then determined by the switch current limit, which is somewhat duty cycle dependent due to internal slope compensation action.

Overcurrent conditions are handled by the same mechanism. The output switch turns on, the peak current is quickly reached and the switch is turned off. Because the output switch is only on for a small fraction of the available period, power dissipation is controlled.

Loss of current limit is possible under certain conditions. Remember that the LT1725 normally exhibits a minimum switch on time, irrespective of current trip point. If the duty cycle exhibited by this minimum on time is greater than the ratio of secondary winding voltage (referred-to-primary) divided by input voltage, then peak current will not be controlled at the nominal value, and will cycle-by-cycle ratchet up to some higher level. Expressed mathematically, the requirement to maintain short-circuit control is:

$$t_{ON} \bullet f < \frac{\left(V_F + I_{SC} \bullet R_{SEC}\right)}{V_{IN} \bullet N_{SP}} \text{ where}$$

t_{ON} = output switch minimum on time

f = switching frequency

I_{SC} = short-circuit output current

V_F = output diode forward voltage at I_{SC}

R_{SEC} = resistance of transformer secondary

V_{IN} = input voltage

N_{SP} = secondary-to-primary turns ratio (N_{SEC}/N_{PRI})

Trouble is typically only encountered in applications with a relatively high product of input voltage times secondary-to-primary turns ratio and/or a relatively long minimum switch on time. (Additionally, several real world effects such as transformer leakage inductance, AC winding losses, and output switch voltage drop combine to make this simple theoretical calculation a conservative estimate.)

THERMAL CONSIDERATIONS

Care should be taken to ensure that the worst-case input voltage condition does not cause excessive die temperatures. The 16-lead SO package is rated at 100°C/W, and the 16-lead GN at 110°C/W.

Average supply current is simply the sum of quiescent current given in the specifications section plus gate drive current. Gate drive current can be computed as:

$I_G = f \bullet Q_G$ where

Q_G = total gate charge

f = switching frequency

(Note: Total gate charge is more complicated than $C_{GS} \bullet V_G$ as it is frequently dominated by Miller effect of the C_{GD}. Furthermore, both capacitances are nonlinear in practice. Fortunately, most MOSFET data sheets provide figures and graphs which yield the total gate charge directly per operating conditions.) Nearly all gate drive power is dissipated in the IC, except for a small amount in the external gate series resistor, so total IC dissipation may be computed as:

$P_{D(TOTAL)} = V_{CC} (I_Q + \bullet f \bullet Q_G)$, where

I_Q = quiescent current (from specifications)

Q_G = total gate charge

f = switching frequency

V_{CC} = LT1725 supply voltage

APPLICATIONS INFORMATION

SWITCH NODE CONSIDERATIONS

For maximum efficiency, gate drive rise and fall times are made as short as practical. To prevent radiation and high frequency resonance problems, proper layout of the components connected to the IC is essential, especially the power paths (primary and secondary). B field (magnetic) radiation is minimized by keeping MOSFET leads, output diode, and output bypass capacitor leads as short as possible. E field radiation is kept low by minimizing the length and area of all similar traces. A ground plane should always be used under the switcher circuitry to prevent interplane coupling.

The high speed switching current paths are shown schematically in Figure 8. Minimum lead length in these paths are essential to ensure clean switching and minimal EMI. The path containing the input capacitor, transformer primary and MOSFET, and the path containing the transformer secondary, output diode and output capacitor contain "nanosecond" rise and fall times. Keep these paths as short as possible.

GATE DRIVE RESISTOR CONSIDERATIONS

The gate drive circuitry internal to the LT1725 has been designed to have as low an output impedance as practically possible—only a few ohms. A strong L/C resonance is potentially presented by the inductance of the path leading to the gate of the power MOSFET and its overall gate capacitance. For this reason the path from the GATE package pin to the physical MOSFET gate should be kept as short as possible, and good layout/ground plane practice used to minimize the parasitic inductance.

An explicit series gate drive resistor may be useful in some applications to damp out this potential L/C resonance (typically tens of MHz). A minimum value of perhaps several ohms is suggested, and higher values (typically a few tens of ohms) will offer increased damping. However, as this resistor value becomes too large, gate voltage rise time will increase to unacceptable levels, and efficiency will suffer due to the sluggish switching action.

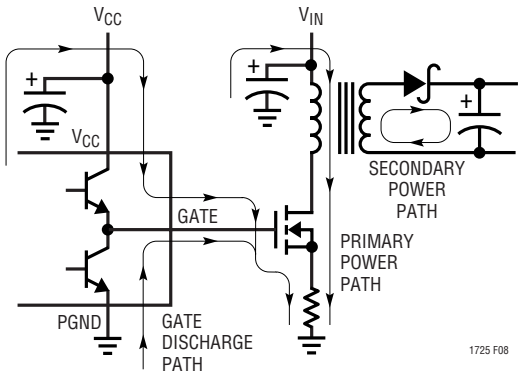


Figure 8. High Speed Current Switching Paths

TYPICAL APPLICATIONS

TELECOM 48V TO ISOLATED 15V APPLICATION

The design in Figure 9 accepts an input voltage in the range of 36V to 72V and outputs an isolated 15V at up to 2A. Transformer T1 is an off-the-shelf VERSA-PAK™ #VP5-0155, produced by Coiltronics. As manufactured, it consists of six ideally identical independent windings. In this application, three windings are stacked in series on the primary side and two are placed in parallel on the secondary side. This arrangement provides a 3:1 primary-to-secondary turns ratio while maximizing overall efficiency. The remaining winding provides a primary-side ground-referred version of the flyback voltage waveform for both feedback information and providing power to the LT1725 itself.

Capacitor C7 sets the switching frequency at approximately 200kHz. Optimal load compensation for the transformer and secondary circuit components is set by resistor R8. Output voltage regulation and overall efficiency are shown in the accompanying graphs. The resistor divider formed by R14 and R15 sets the undervoltage lockout threshold at about 32V, with a hysteresis band of about 2V. The soft-start and $3V_{OUT}$ features are unused as shown.

VERSA-PAK is a trademark of Coiltronics, Inc

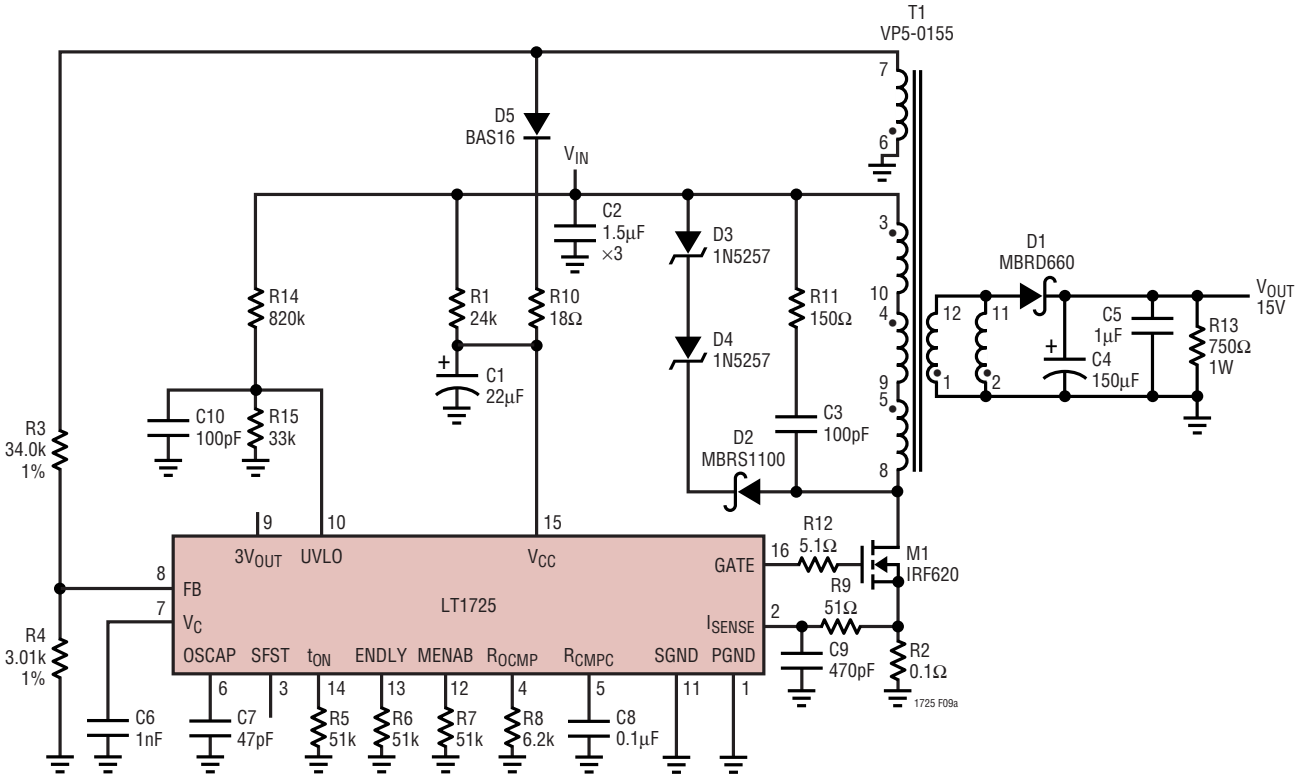
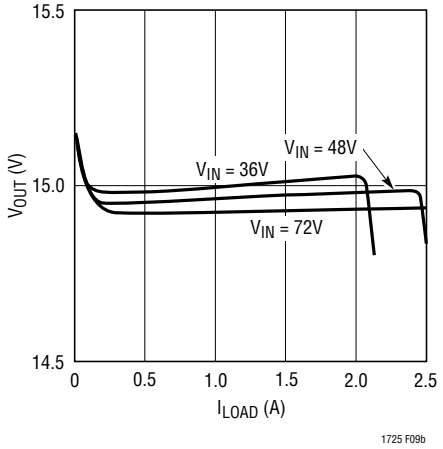


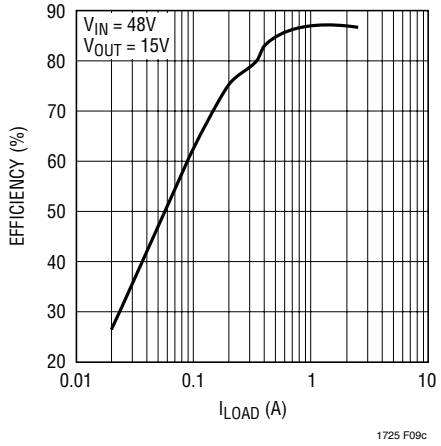
Figure 9. 48V to Isolated 15V Converter

TYPICAL APPLICATIONS

Application Regulation



Application Efficiency



48V to Isolated 15V Application Parts List

T1: Coiltronics VP5-0155 VERSA-PAK

M1: International Rectifier IRF620. 200V, 0.8Ω N-channel MOSFET

D1: Motorola MBRD660. 6A, 60V Schottky diode

D2: Motorola MBRS1100. 1A, 100V Schottky diode

D3, D4: 1N5257. 33V, 500mW Zener diode

D5: BAS16. 75V rectifier diode

C1: AVX TPSD226M025R0200. 22µF, 25V tantalum capacitor

C2a, C2b, C2c: Vishay/Vitramon VJ1825Y155MXB. 1.5µF, 100V X7R ceramic capacitor

C3: 100pF, 100V, X7R ceramic capacitor

C4: Sanyo 20SV150M. 150µF, 20V, OS-CON electrolytic capacitor

C5: 1µF, 25V, Z5U ceramic capacitor

C6: 1nF, 25V, X7R ceramic capacitor

C7: 47pF, 25V NPO/COG ceramic capacitor

C8: 0.1µF, 25V, Z5U ceramic capacitor

C9: 470pF, 25V, X7R ceramic capacitor

C10: 100pF, 25V, X7R ceramic capacitor

R1: 24k, 1/4W, 5% resistor

R2: IRC LR2010. 0.1Ω, 1/2W current sense resistor

R3: 34.0k, 1% resistor

R4: 3.01k, 1% resistor

R5, R6, R7: 51k, 5% resistor

R8: 6.2k, 5% resistor

R9: 51Ω, 5% resistor

R10: 18Ω, 5% resistor

R11: 150Ω, 1/4W, 5% resistor

R12: 5.1Ω, 5% resistor

R13a, R13b: 1.5k, 1/2W, 5% resistor

R14: 820k, 5% resistor

R15: 33k, 5% resistor

TYPICAL APPLICATIONS

TELECOM 48V TO ISOLATED 5V APPLICATION

The design in Figure 10 accepts an input voltage in the range of 36V to 72V and outputs an isolated 5V at up to 2A. Transformer T1 is available as a Coiltronics CTX02-14989. Capacitor C7 sets the switching frequency at approximately 275kHz. Optimal load compensation for the transformer and secondary circuit components is set by resistor R8. Output voltage regulation and overall efficiency are shown in the accompanying graphs. Efficiency is shown both with and without the R11 preload. The resistor divider formed by R13 and R14 sets the undervoltage lockout threshold at about 32V, with a hysteresis band of about 2V. The soft-start and $3V_{OUT}$ features are unused as shown.

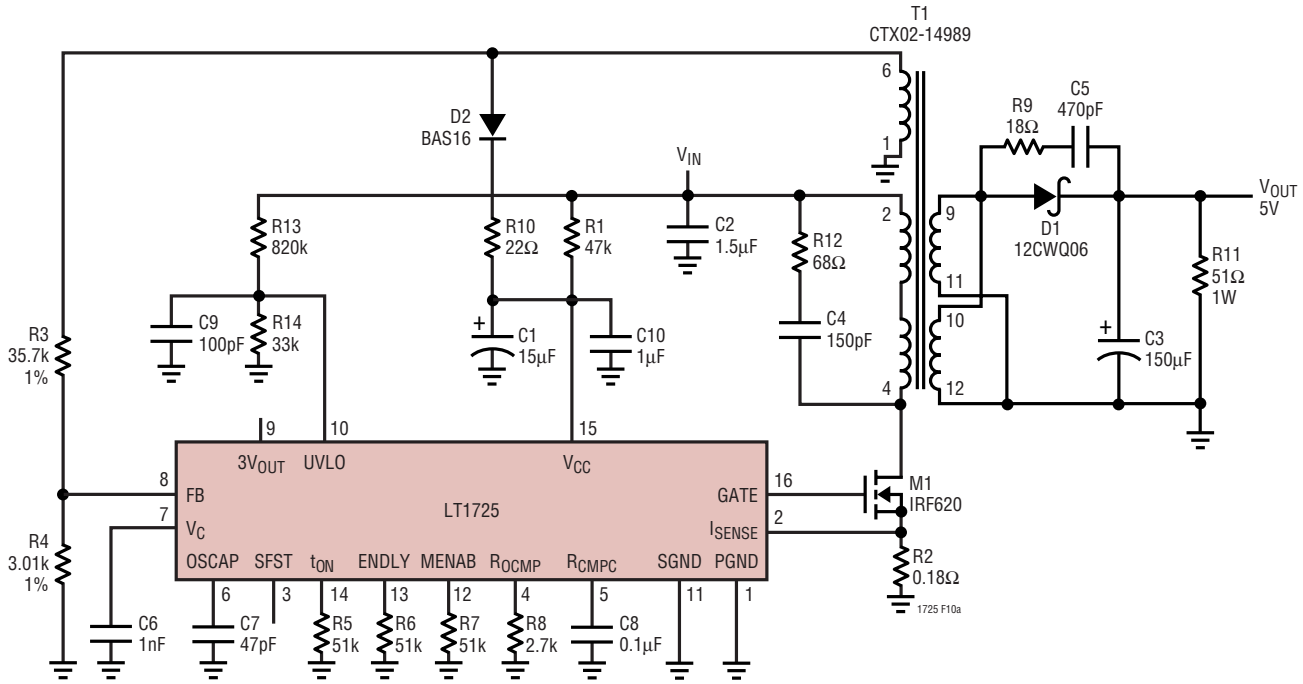
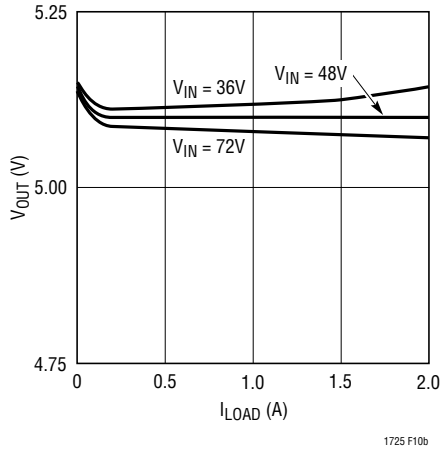
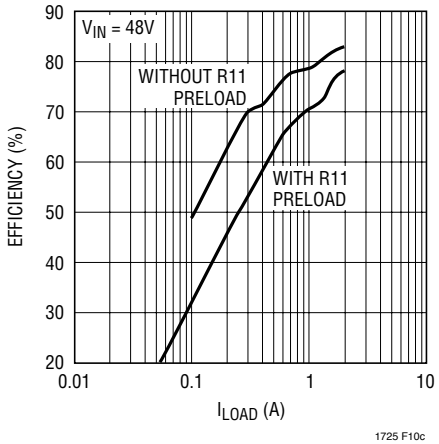


Figure 10. 48V to Isolated 5V Converter

Application Regulation



Application Efficiency



TYPICAL APPLICATIONS

48V to Isolated 5V Application Parts List

T1: Coiltronics CTX02-14989

M1: International Rectifier IRF620. 200V, 0.8Ω N-channel MOSFET

D1: International Rectifier 12CWQ06FN. 12A, 60V Schottky diode

D2: BAS16. 75V switching diode

C1: AVX TPSD156M035R0300. 15µF, 35V tantalum capacitor

C2: Vishay/Vitramon VJ1825Y155MXB. 1.5µF, 100V, X7R ceramic capacitor

C3: Sanyo 6SA150M. 150µF, 6.3V, OS-CON electrolytic capacitor

C4: 150pF, 100V, X7R ceramic capacitor

C5: 470pF, 50V, X7R ceramic capacitor

C6: 1nF, 25V X7R ceramic capacitor

C7: 47pF, 25V, NPO ceramic capacitor

C8: 0.1µF, 25V, Z5U ceramic capacitor

C9: 100pF, 25V, X7R ceramic capacitor

C10: 1µF, 25V, Z5U ceramic capacitor

R1: 47k, 1/4W, 5% resistor

R2: Panasonic type ERJ-14RSJ. 0.18Ω, 1/4W, 5% resistor

R3: 35.7k, 1% resistor

R4: 3.01k, 1% resistor

R5, R6, R7: 51k, 5% resistor

R8: 2.7k, 5% resistor

R9: 18Ω, 5% resistor

R10: 22Ω, 5% resistor

R11: 51Ω, 1W, 5% resistor

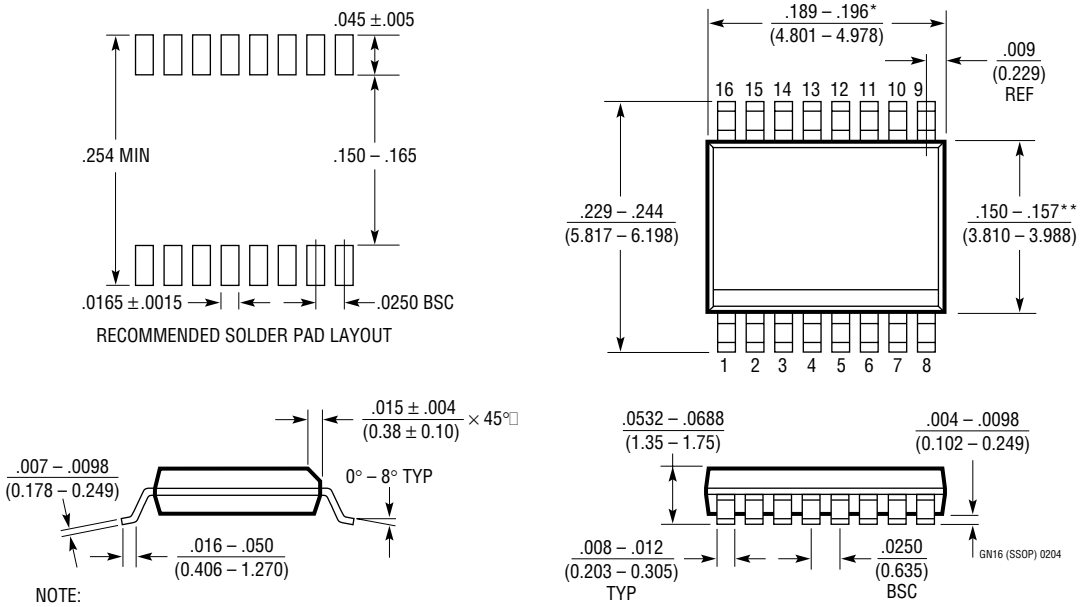
R12: 68Ω, 5% resistor

R13: 820k, 5% resistor

R14: 33k, 5% resistor

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



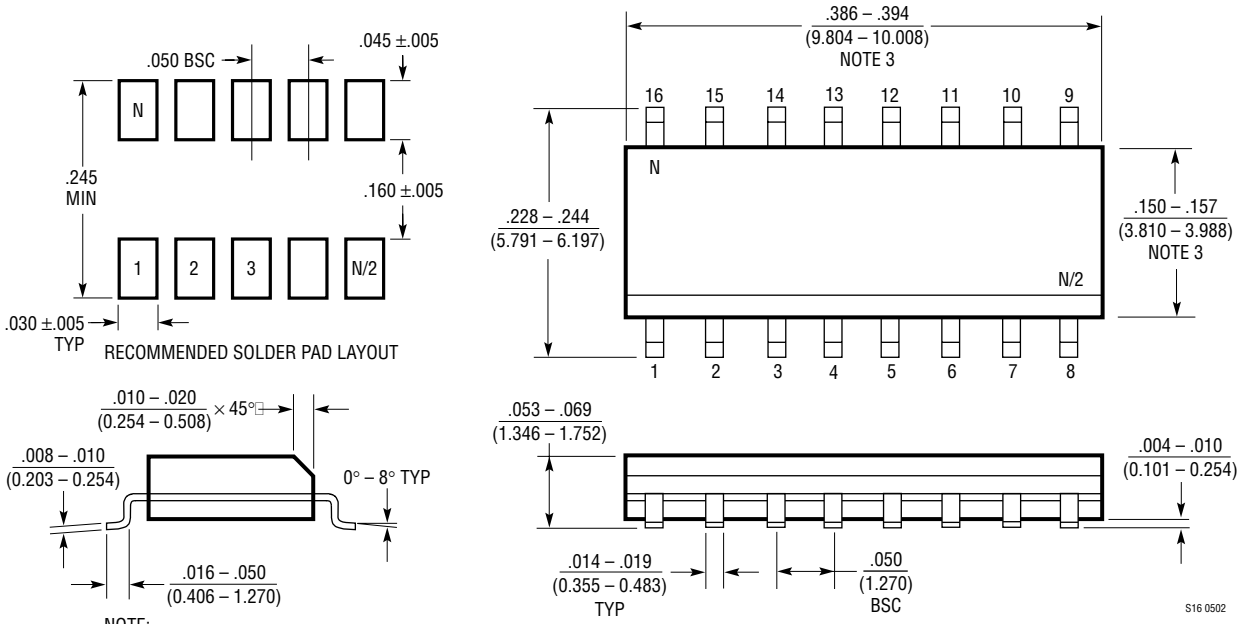
NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

S Package
16-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)