

Micropower, Single Supply Rail-to-Rail Output Instrumentation Amplifiers

FEATURES

- **Micropower: 95µA Supply Current Max**
- **Low Input Offset Voltage: 100µV Max**
- **Low Input Offset Voltage Drift: 0.5µV/°C Max**
- **Single Gain Set Resistor:**
 - G = 1 to 1000 (LT1789-1)**
 - G = 10 to 1000 (LT1789-10)**
- **Inputs Common Mode to V⁻**
- **Wide Supply Range: 2.2V to 36V Total Supply**
- **CMRR at G = 10: 96dB Min**
- **Gain Error: G = 10, 0.25% Max**
- **Gain Nonlinearity: G = 10, 40ppm Max**
- **Input Bias Current: 40nA Max**
- **PSRR at G = 10: 100dB Min**
- **1kHz Voltage Noise: 48nV/√Hz**
- **0.1Hz to 10Hz Noise: 1.5µV_{P-P}**

APPLICATIONS

- Portable Instrumentation
- Bridge Amplifiers
- Strain Gauge Amplifiers
- Thermocouple Amplifiers
- Differential to Single-Ended Converters
- Medical Instrumentation

DESCRIPTION

The LT[®]1789-1/LT1789-10 are micropower, precision instrumentation amplifiers that are optimized for single supply operation from 2.2V to 36V. The quiescent current is 95µA max, the inputs common mode to ground and the output swings within 110mV of ground. The gain is set with a single external resistor for a gain range of 1 to 1000 for the LT1789-1 and 10 to 1000 for the LT1789-10.

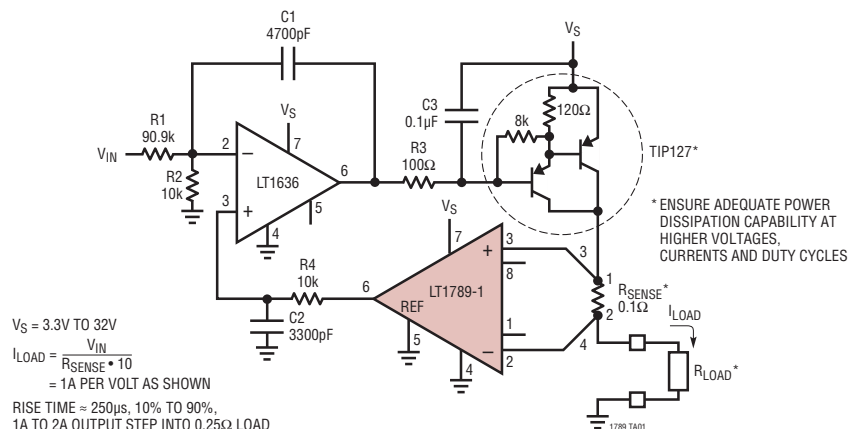
The high accuracy of the LT1789-1 (40ppm maximum non-linearity and 0.25% max gain error) is unmatched by other micropower instrumentation amplifiers. The LT1789-10 maximizes both the input common mode range and dynamic output range when an amplification of 10 or greater is required, allowing precise signal processing where other instrumentation amplifiers fail to operate. The LT1789-1/LT1789-10 are laser trimmed for very low input offset voltage, low input offset voltage drift, high CMRR and high PSRR. The output can handle capacitive loads up to 400pF (LT1789-1), 1000pF (LT1789-10) in any gain configuration while the inputs are ESD protected up to 10kV (human body).

The LT1789-1/LT1789-10 are offered in the 8-pin SO package, requiring significantly less PC board area than discrete multi op amp and resistor designs.

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TYPICAL APPLICATION

0.5A to 4A Voltage Controlled Current Source



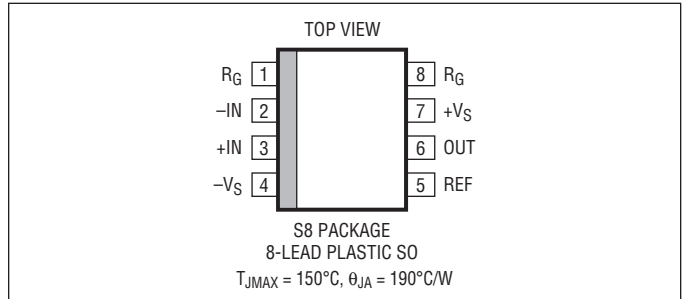
LT1789-1/LT1789-10

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V^+ to V^-).....	36V
Input Differential Voltage	36V
Input Current (Note 3).....	$\pm 20\text{mA}$
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	-40°C to 85°C
Specified Temperature Range (Note 4)	
LT1789C-1, LT1789C-10	-40°C to 85°C
LT1789I-1, LT1789I-10	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec).....	300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1789CS8-1#PBF	LT1789CS8-1#TRPBF	17891	8-Lead Plastic SO	-40°C to 85°C
LT1789IS8-1#PBF	LT1789IS8-1#TRPBF	1789I1	8-Lead Plastic SO	-40°C to 85°C
LT1789CS8-10#PBF	LT1789CS8-10#TRPBF	178910	8-Lead Plastic SO	-40°C to 85°C
LT1789IS8-10#PBF	LT1789IS8-10#TRPBF	789I10	8-Lead Plastic SO	-40°C to 85°C
LEAD BASED FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1789CS8-1	LT1789CS8-1#TR	17891	8-Lead Plastic SO	-40°C to 85°C
LT1789IS8-1	LT1789IS8-1#TR	1789I1	8-Lead Plastic SO	-40°C to 85°C
LT1789CS8-10	LT1789CS8-10#TR	178910	8-Lead Plastic SO	-40°C to 85°C
LT1789IS8-10	LT1789IS8-10#TR	789I10	8-Lead Plastic SO	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

3V AND 5V ELECTRICAL CHARACTERISTICS

$V_S = 3\text{V}, 0\text{V}; V_S = 5\text{V}, 0\text{V}; R_L = 20\text{k}, V_{\text{CM}} = V_{\text{REF}} = \text{half supply}, T_A = 25^\circ\text{C}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1789-1			LT1789-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
G	Gain Range	LT1789-1, $G = 1 + (200\text{k}/R_G)$ LT1789-10, $G = 10 \cdot [1 + (200\text{k}/R_G)]$	1		1000	10		1000	
	Gain Error (Note 6)	$G = 1, V_0 = 0.1\text{V to } (+V_S) - 1\text{V}$		0.02	0.20				%
		LT1789-1, $V_0 = 0.1\text{V to } (+V_S) - 0.3\text{V}$ LT1789-10, $V_0 = 0.2\text{V to } (+V_S) - 0.3\text{V}$							
$G = 10$ (Note 2) $G = 100$ (Note 2) $G = 1000$ (Note 2)			0.06 0.06 0.13	0.25 0.27	0.01 0.09 0.16	0.25 0.30	% % %		
Gain Nonlinearity (Note 6)	$G = 1, V_0 = 0.1\text{V to } (+V_S) - 1\text{V}$ LT1789-1, $V_0 = 0.1\text{V to } (+V_S) - 0.3\text{V}$ LT1789-10, $V_0 = 0.2\text{V to } 4.7\text{V}, V_S = 5\text{V}$ (Note 8) $G = 10$ $G = 100$ $G = 1000$		35	100				ppm	
			12 18 90	40 75	15 20 100	100	ppm ppm ppm		

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3V AND 5V ELECTRICAL CHARACTERISTICS $V_S = 3V, 0V; V_S = 5V, 0V; R_L = 20k, V_{CM} = V_{REF} = \text{half supply}, T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1789-1			LT1789-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OST}	Total Input Referred Offset Voltage	$V_{OST} = V_{OSI} + V_{OSO}/G$							
V_{OSI}	Input Offset Voltage	$G = 1000$		15	100		20	160	μV
V_{OSO}	Output Offset Voltage	$G = 1$ (LT1789-1), $G = 10$ (LT1789-10)		150	750		650	3000	μV
I_{OS}	Input Offset Current	(Note 6)		0.2	4		0.2	4	nA
I_B	Input Bias Current	(Note 6)		19	40		19	40	nA
e_n	Input Noise Voltage, RTI (Referred to Input)	$G = 1, f_0 = 0.1\text{Hz to }10\text{Hz}$ $G = 10$ $G = 100, 1000$		5.0					μV_{P-P}
				1.5			4.6		μV_{P-P}
				1.0			1.1		μV_{P-P}
Total RTI Noise = $\sqrt{e_{ni}^2 + (e_{no}/G)^2}$									
e_{ni}	Input Noise Voltage Density, RTI	$f_0 = 1\text{kHz}$ (Note 7)		48	85		52	90	nV/\sqrt{Hz}
e_{no}	Output Noise Voltage Density, RTI	$f_0 = 1\text{kHz}$ (Note 3)		330			270		nV/\sqrt{Hz}
i_n	Input Noise Current	$f_0 = 0.1\text{Hz to }10\text{Hz}$		16			16		pA_{P-P}
	Input Noise Current Density	$f_0 = 1\text{kHz}$		62			62		fA/\sqrt{Hz}
R_{IN}	Input Resistance	$V_{IN} = 0V \text{ to } (+V_S) - 1V$ (Note 6)	0.75	1.6		0.75	1.6		$G\Omega$
C_{IN}	Input Capacitance	Differential Common Mode		1.6			1.6		pF
				1.6			1.6		pF
V_{CM}	Input Voltage Range		0		$+V_S - 1$	0		$+V_S - 1.2$	V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance (Note 6) LT1789-1, $V_{CM} = 0V \text{ to } (+V_S) - 1V$ LT1789-10, $V_{CM} = 0V \text{ to } (+V_S) - 1.2V$ $G = 1$ $G = 10$ $G = 100$ $G = 1000$		79	88				dB
				96	106		88	105	dB
				100	114		98	113	dB
				100	114		98	113	dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.5V \text{ to } 12.5V, V_{CM} = V_{REF} = 1V$ $G = 1$ $G = 10$ $G = 100$ $G = 1000$		90	100				dB
				100	113		94	109	dB
				102	116		102	120	dB
				102	116		102	120	dB
	Minimum Supply Voltage			2.2	2.5		2.2	2.5	V
I_S	Supply Current	(Note 7)		67	95		67	95	μA
V_{OL}	Output Voltage Swing LOW	(Note 7)		54	100		62	110	mV
V_{OH}	Output Voltage Swing HIGH	(Note 7)		$+V_S - 0.3$	$+V_S - 0.19$		$+V_S - 0.3$	$+V_S - 0.19$	V
I_{SC}	Short-Circuit Current	Short to GND Short to $+V_S$		2.2			2.2		mA
				8.5			8.5		mA
BW	Bandwidth	$G = 1$ $G = 10$ $G = 100$ $G = 1000$		60					kHz
				30			25		kHz
				3			12		kHz
				0.2			1.5		kHz
SR	Slew Rate	$G = 10, V_{OUT} = 0.5V \text{ to } 4.5V$		0.023			0.062		$V/\mu s$
	Settling Time to 0.01%	4V Step		240			190		μs
R_{REFIN}	Reference Input Resistance			220			220		k Ω
I_{REFIN}	Reference Input Current	$V_{REF} = 0V$		2.7			2.7		μA
AV_{REF}	Reference Gain to Output			1 ± 0.0001			1 ± 0.0001		

LT1789-1/LT1789-10

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range of $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$. $V_S = 3\text{V}, 0\text{V}$; $V_S = 5\text{V}, 0\text{V}$; $R_L = 20\text{k}$, $V_{\text{REF}} = \text{half supply}$, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LT1789-1			LT1789-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Gain Error (Note 6)	$G = 1, V_O = 0.3\text{V to } (+V_S) - 1\text{V}$	●		0.25				%
		$V_O = 0.3\text{V to } (+V_S) - 0.5\text{V}$	●		0.53		0.30	%	
		$G = 10$ (Note 2) $G = 100$ (Note 2)	●		0.55		0.53	%	
	Gain Nonlinearity (Note 6)	$G = 1, V_O = 0.3\text{V to } (+V_S) - 1\text{V}$	●		185				ppm
		LT1789-1, $V_O = 0.3\text{V to } (+V_S) - 0.5\text{V}$ LT1789-10, $V_O = 0.3\text{V to } 4.7\text{V}, V_S = 5\text{V}$ (Note 8)	●		90		130	ppm	
		$G = 10$ $G = 100$	●		120		130	ppm	
G/T	Gain vs Temperature	$G < 1000$ (Notes 2, 3)	●	5	50	5	50	ppm/ $^{\circ}\text{C}$	
V_{OST}	Total Input Referred Offset Voltage	$V_{\text{OST}} = V_{\text{OSI}} + V_{\text{OSO}}/G$							
V_{OSI}	Input Offset Voltage	$G = 1000$	●		150		190	μV	
V_{OSIH}	Input Offset Voltage Hysteresis	(Notes 3, 5)	●	3	10	3	10	μV	
V_{OSO}	Output Offset Voltage	$G = 1$ (LT1789-1), $G = 10$ (LT1789-10)	●		950		3700	μV	
V_{OSOH}	Output Offset Voltage Hysteresis	(Notes 3, 5)	●	50	100	300	900	μV	
V_{OSI}/T	Input Offset Voltage Drift (RTI)	(Note 3)	●	0.2	0.5	0.3	0.7	$\mu\text{V}/^{\circ}\text{C}$	
V_{OSO}/T	Output Offset Voltage Drift	(Note 3)	●	1.5	4	7	20	$\mu\text{V}/^{\circ}\text{C}$	
I_{OS}	Input Offset Current	(Note 6)	●		4.5		4.5	nA	
I_{OS}/T	Input Offset Current Drift		●	3		3		pA/ $^{\circ}\text{C}$	
I_{B}	Input Bias Current	(Note 6)	●		45		45	nA	
I_{B}/T	Input Bias Current Drift		●	50		50		pA/ $^{\circ}\text{C}$	
V_{CM}	Input Voltage Range		●	0.2	$(+V_S) - 1$	0.2	$(+V_S) - 1.5$	V	
CMRR	Common Mode Rejection Ratio	1k Source Imbalance (Note 6)	●						
		LT1789-1, $V_{\text{CM}} = 0.2\text{V to } (+V_S) - 1\text{V}$	●	77				dB	
		LT1789-10, $V_{\text{CM}} = 0.2\text{V to } (+V_S) - 1.5\text{V}$	●	94		85		dB	
		$G = 1$ $G = 10$ $G = 100, 1000$	●	98		96		dB	
PSRR	Power Supply Rejection Ratio	$V_S = 2.5\text{V to } 12.5\text{V}, V_{\text{CM}} = V_{\text{REF}} = 1\text{V}$	●						
		$G = 1$	●	88				dB	
		$G = 10$	●	98		92		dB	
		$G = 100, 1000$	●	100		100		dB	
	Minimum Supply Voltage		●		2.5		2.5	V	
I_{S}	Supply Current	(Note 7)	●		115		115	μA	
V_{OL}	Output Voltage Swing LOW	(Note 7)	●		110		120	mV	
V_{OH}	Output Voltage Swing HIGH	(Note 7)	●	$+V_S - 0.38$		$+V_S - 0.38$		V	

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the temperature range of $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$. $V_S = 3\text{V}, 0\text{V}$; $V_S = 5\text{V}, 0\text{V}$; $R_L = 20\text{k}$, $V_{\text{REF}} = \text{half supply}$, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LT1789-1			LT1789-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Gain Error (Note 6)	$G = 1, V_O = 0.3\text{V to } (+V_S) - 1\text{V}$	●		0.30				%
		$V_O = 0.3\text{V to } (+V_S) - 0.5\text{V}$	●		0.57		0.35	%	
		$G = 10$ (Note 2) $G = 100$ (Note 2)	● ●		0.59		0.62	%	
	Gain Nonlinearity (Note 6)	$G = 1, V_O = 0.3\text{V to } (+V_S) - 1\text{V}$	●		250				ppm
		LT1789-1, $V_O = 0.3\text{V to } (+V_S) - 0.5\text{V}$ LT1789-10, $V_O = 0.3\text{V to } 4.7\text{V}, V_S = 5\text{V}$ (Note 8)	●		105		150	ppm	
		$G = 10$ $G = 100$	● ●		160		170	ppm	
G/T	Gain vs Temperature	$G < 1000$ (Notes 2, 3)	●	5	50	5	50	ppm/°C	
V_{OST}	Total Input Referred Offset Voltage	$V_{\text{OST}} = V_{\text{OSI}} + V_{\text{OSO}}/G$							
V_{OSI}	Input Offset Voltage	$G = 1000$	●		175		205	μV	
V_{OSIH}	Input Offset Voltage Hysteresis	(Notes 3, 5)	●	3	10	3	10	μV	
V_{OSO}	Output Offset Voltage	$G = 1$ (LT1789-1), $G = 10$ (LT1789-10)	●		1050		4000	μV	
V_{OSOH}	Output Offset Voltage Hysteresis	(Notes 3, 5)	●	50	100	300	900	μV	
V_{OSI}/T	Input Offset Voltage Drift (RTI)	(Note 3)	●	0.2	0.5	0.3	0.7	μV/°C	
V_{OSO}/T	Output Offset Voltage Drift	(Note 3)	●	1.5	4	7	20	μV/°C	
I_{OS}	Input Offset Current	(Note 6)	●		5		5	nA	
I_{OS}/T	Input Offset Current Drift		●	3		3		pA/°C	
I_B	Input Bias Current	(Note 6)	●		50		50	nA	
I_B/T	Input Bias Current Drift		●	50		50		pA/°C	
V_{CM}	Input Voltage Range		●	0.2	$+V_S - 1$	0.2	$+V_S - 1.5$	V	
CMRR	Common Mode Rejection Ratio	1k Source Imbalance (Note 6)	●						
		LT1789-1, $V_{\text{CM}} = 0.2\text{V to } (+V_S) - 1\text{V}$	●	75				dB	
		LT1789-10, $V_{\text{CM}} = 0.2\text{V to } (+V_S) - 1.5\text{V}$	●	92		84		dB	
		$G = 1$ $G = 10$ $G = 100, 1000$	● ● ●	96		94		dB	
PSRR	Power Supply Rejection Ratio	$V_S = 2.5\text{V to } 12.5\text{V}, V_{\text{CM}} = V_{\text{REF}} = 1\text{V}$	●						
		$G = 1$	●	86				dB	
		$G = 10$	●	96		90		dB	
		$G = 100, 1000$	●	98		98		dB	
	Minimum Supply Voltage		●		2.5		2.5	V	
I_S	Supply Current	(Note 7)	●		125		125	μA	
V_{OL}	Output Voltage Swing LOW	(Note 7)	●		120		130	mV	
V_{OH}	Output Voltage Swing HIGH	(Note 7)	●	$+V_S - 0.40$		$+V_S - 0.40$		V	

LT1789-1/LT1789-10

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $R_L = 20k$, $V_{CM} = V_{OUT} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1789-1			LT1789-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
G	Gain Range	LT1789-1, $G = 1 + (200k/R_G)$ LT1789-10, $G = 10 \cdot [1 + (200k/R_G)]$	1		1000	10		1000	
	Gain Error	$V_O = \pm 10V$ $G = 1$		0.01	0.10				%
		$G = 10$ (Note 2)		0.04	0.15	0.01	0.15		%
$G = 100$ (Note 2)			0.04	0.15	0.03	0.20		%	
$G = 1000$ (Note 2)			0.07	0.20	0.03	0.25		%	
Gain Nonlinearity	$V_O = \pm 10V$ $G = 1$		8	20				ppm	
	$G = 10$		1	10	5	40		ppm	
	$G = 100$		6	20	5	40		ppm	
	$G = 1000$		20	100	25	160		ppm	
V_{OST}	Total Input Referred Offset Voltage	$V_{OST} = V_{OSI} + V_{OSO}/G$							
V_{OSI}	Input Offset Voltage	$G = 1000$		30	235	30	295		μV
V_{OSO}	Output Offset Voltage	$G = 1$ (LT1789-1), $G = 10$ (LT1789-10)		0.2	1	0.6	3.3		mV
I_{OS}	Input Offset Current			0.2	4	0.2	4		nA
I_B	Input Bias Current			17	40	17	40		nA
e_n	Input Noise Voltage, RTI	$f_0 = 0.1Hz$ to 10Hz							
		$G = 1$		5.0					μV_{P-P}
		$G = 10$		1.5		4.6			μV_{P-P}
		$G = 100, 1000$		1.0		1.1			μV_{P-P}
Total RTI Noise = $\sqrt{e_{ni}^2 + (e_{no}/G)^2}$									
e_{ni}	Input Noise Voltage Density, RTI	$f_0 = 1kHz$		49	90	53	95		nV/\sqrt{Hz}
e_{no}	Output Noise Voltage Density, RTI	$f_0 = 1kHz$		330		270			nV/\sqrt{Hz}
i_n	Input Noise Current	$f_0 = 0.1Hz$ to 10Hz		19		19			pA_{P-P}
	Input Noise Current Density	$f_0 = 1kHz$		62		62			fA/\sqrt{Hz}
R_{IN}	Input Resistance		2	4.7		2	4.7		$G\Omega$
C_{IN}	Input Capacitance	Differential		20		20			pF
		Common Mode		17		17			pF
V_{CM}	Input Voltage Range		-15		-14	-15		-14	V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, $V_{CM} = -15V$ to 14V							
		$G = 1$	80	89					dB
		$G = 10$	98	108	93	108			dB
PSRR	Power Supply Rejection Ratio	LT1789-1 $V_S = \pm 1.25V$ to $\pm 16V$ LT1789-10 $V_S = \pm 1.50V$ to $\pm 16V$							
		$G = 1$	94	107					dB
		$G = 10$	104	118	100	115			dB
	Minimum Supply Voltage				± 1.25			± 1.50	V
I_S	Supply Current			85	130	85	130		μA
V_O	Output Voltage Swing		± 14.5	± 14.7		± 14.5	± 14.7		V
I_{SC}	Short-Circuit Current	Short to $-V_S$		2.2		2.2			mA
		Short to $+V_S$		8.5		8.5			mA

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $R_L = 20k$, $V_{CM} = V_{OUT} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1789-1			LT1789-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
BW	Bandwidth	$G = 1$		60					kHz
		$G = 10$		30			25		kHz
		$G = 100$		3			12		kHz
		$G = 1000$		0.2			1.5		kHz
SR	Slew Rate	$V_{OUT} = \pm 10V$	0.012	0.026		0.028	0.066		V/ μs
	Settling Time to 0.01%	10V Step		460			270		μs
R_{REFIN}	Reference Input Resistance			220			220		k Ω
I_{REFIN}	Reference Input Current	$V_{REF} = 0V$		2.7			2.7		μA
AV_{REF}	Reference Gain to Output			1 ± 0.0001			1 ± 0.0001		

The ● denotes the specifications which apply over the temperature range of $0^\circ C \leq T_A \leq 70^\circ C$. $V_S = \pm 15V$, $R_L = 20k$, $V_{CM} = V_{REF} = 0V$, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LT1789-1			LT1789-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Gain Error	$V_O = \pm 10V$							
		$G = 1$	●		0.15				%
		$G = 10$ (Note 2)	●		0.38			0.20	%
		$G = 100$ (Note 2)	●		0.38			0.43	%
		$G = 1000$ (Note 2)	●		0.43			0.48	%
	Gain Nonlinearity	$V_O = \pm 10V$							
		$G = 1$	●		25				ppm
		$G = 10$	●		15			45	ppm
		$G = 100$	●		25			45	ppm
		$G = 1000$	●		120			180	ppm
G/T	Gain vs Temperature	$G < 1000$ (Notes 2, 3)	●	5	50		5	50	ppm/ $^\circ C$
V_{OST}	Total Input Referred Offset Voltage	$V_{OST} = V_{OSI} + V_{OSO}/G$							
V_{OSI}	Input Offset Voltage	$G = 1000$	●		285			325	μV
V_{OSIH}	Input Offset Voltage Hysteresis	(Notes 3, 5)	●	8	30		8	30	μV
V_{OSO}	Output Offset Voltage	$G = 1$	●		1.2			4	mV
V_{OSOH}	Output Offset Voltage Hysteresis	(Notes 3, 5)	●	50	120		400	1000	μV
V_{OSI}/T	Input Offset Voltage Drift (RTI)	(Note 3)	●	0.2	0.7		0.3	0.8	$\mu V/^\circ C$
V_{OSO}/T	Output Offset Voltage Drift	(Note 3)	●	1.5	5		8	22	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●		4.5			4.5	nA
I_{OS}/T	Input Offset Current Drift		●	2			2		pA/ $^\circ C$
I_B	Input Bias Current		●		45			45	nA
I_B/T	Input Bias Current Drift		●	35			35		pA/ $^\circ C$
V_{CM}	Input Voltage Range	$G = 1$, Other Input Grounded	●	-14.8	14		-14.8	14	V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, $V_{CM} = -14.8V$ to 14V							
		$G = 1$	●	78					dB
		$G = 10$	●	96			91		dB
		$G = 100, 1000$	●	100			100		dB

LT1789-1/LT1789-10

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range of $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, $R_L = 20\text{k}$, $V_{CM} = V_{REF} = 0\text{V}$, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LT1789-1			LT1789-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
PSRR	Power Supply Rejection Ratio	LT1789-1, $V_S = \pm 1.25\text{V}$ to $\pm 16\text{V}$ LT1789-10, $V_S = \pm 1.50\text{V}$ to $\pm 16\text{V}$ $G = 1$ ● $G = 10$ ● $G = 100, 1000$ ●		92 102 104		98 104		dB dB dB	
	Minimum Supply Voltage				± 1.25		± 1.50	V	
I_S	Supply Current				150		150	μA	
V_O	Output Voltage Swing		± 14.25			± 14.25		V	
SR	Slew Rate	$V_{OUT} = \pm 10\text{V}$	0.010			0.026		$\text{V}/\mu\text{s}$	

The ● denotes the specifications which apply over the temperature range of $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, $R_L = 20\text{k}$, $V_{CM} = V_{REF} = 0\text{V}$, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LT1789-1			LT1789-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Gain Error	$V_O = \pm 10\text{V}$ $G = 1$ ● $G = 10$ (Note 2) ● $G = 100$ (Note 2) ● $G = 1000$ (Note 2) ●			0.20 0.57 0.57 0.62			0.25 0.62 0.67	% % % %
	Gain Nonlinearity	$V_O = \pm 10\text{V}$ $G = 1$ ● $G = 10$ ● $G = 100$ ● $G = 1000$ ●			30 20 30 130			50 50 200	ppm ppm ppm ppm
G/T	Gain vs Temperature	$G < 1000$ (Notes 2, 3)		5	50		5	50	$\text{ppm}/^{\circ}\text{C}$
V_{OST}	Total Input Referred Offset Voltage	$V_{OST} = V_{OSI} + V_{OSO}/G$							
V_{OSI}	Input Offset Voltage	$G = 1000$			305			340	μV
V_{OSIH}	Input Offset Voltage Hysteresis	(Notes 3, 5)		8	30		8	30	μV
V_{OSO}	Output Offset Voltage	$G = 1$			1.3			4.2	mV
V_{OSOH}	Output Offset Voltage Hysteresis	(Notes 3, 5)		50	120		400	1000	μV
V_{OSI}/T	Input Offset Voltage Drift (RTI)	(Note 3)		0.2	0.7		0.3	0.8	$\mu\text{V}/^{\circ}\text{C}$
V_{OSO}/T	Output Offset Voltage Drift	(Note 3)		1.5	5		8	22	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current				5			5	nA
I_{OS}/T	Input Offset Current Drift			2			2		$\text{pA}/^{\circ}\text{C}$
I_B	Input Bias Current				50			50	nA
I_B/T	Input Bias Current Drift			35			35		$\text{pA}/^{\circ}\text{C}$
V_{CM}	Input Voltage Range	$G = 1$, Other Input Grounded	-14.8		14	-14.8		14	V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, $V_{CM} = -14.8\text{V}$ to 14V $G = 1$ ● $G = 10$ ● $G = 100, 1000$ ●		76 94 98			89 98		dB dB dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range of $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, $R_L = 20\text{k}$, $V_{\text{CM}} = V_{\text{REF}} = 0\text{V}$, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LT1789-1			LT1789-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
PSRR	Power Supply Rejection Ratio	LT1789-1, $V_S = \pm 1.25\text{V}$ to $\pm 16\text{V}$ LT1789-10, $V_S = \pm 1.50\text{V}$ to $\pm 16\text{V}$ $G = 1$ $G = 10$ $G = 100, 1000$	●	90			96		dB
			●	100			102		dB
			●	102					dB
	Minimum Supply Voltage		●			± 1.25		± 1.50	V
I_S	Supply Current		●			160		160	μA
V_O	Output Voltage Swing		●	± 14.15			± 14.15		V
SR	Slew Rate	$V_{\text{OUT}} = \pm 10\text{V}$	●	0.008			0.024		$\text{V}/\mu\text{s}$

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Does not include the effect of the external gain resistor R_G .

Note 3: This parameter is not 100% tested.

Note 4: The LT1789C-1/ LT1789C-10 is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet these extended temperature limits, but is not tested at -40°C and 85°C . The LT1789I-1/ LT1789I-10 is guaranteed to meet the extended temperature limits.

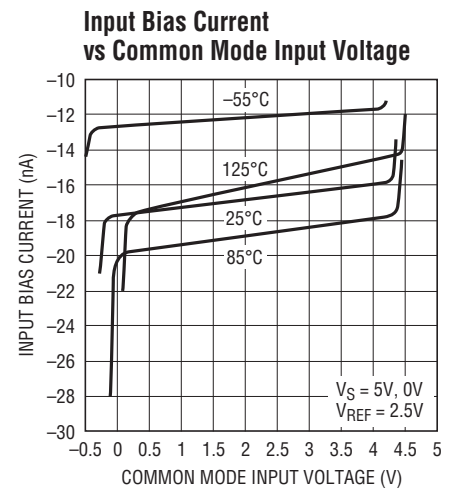
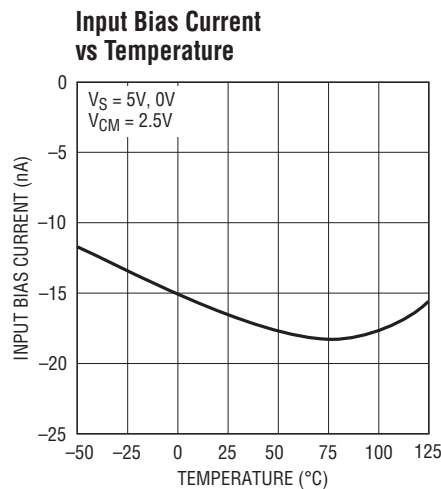
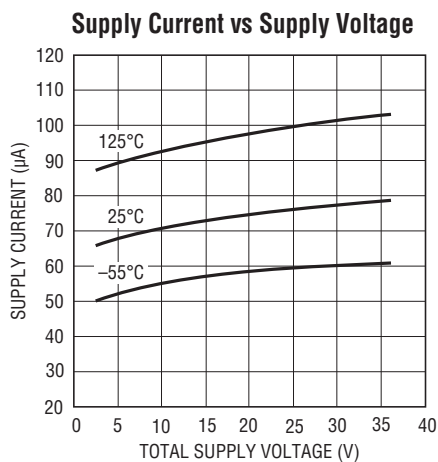
Note 5: Hysteresis in offset voltage is created by package stress that differs depending on whether the IC was previously at a higher or lower temperature. Offset voltage hysteresis is always measured at 25°C , but the IC is cycled to 85°C I-grade (or 70°C C-grade) or -40°C I-grade (0°C C-grade) before successive measurement. 60% of the parts will pass the typical limit on the data sheet.

Note 6: $V_S = 5\text{V}$ limits are guaranteed by correlation to $V_S = 3\text{V}$ and $V_S = \pm 15\text{V}$ tests.

Note 7: $V_S = 3\text{V}$ limits are guaranteed by correlation to $V_S = 5\text{V}$ and $V_S = \pm 15\text{V}$ tests.

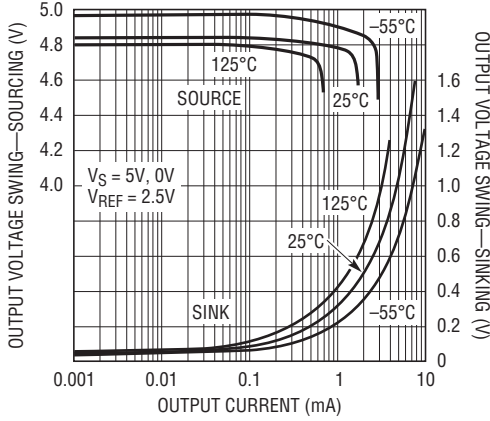
Note 8: This parameter is not tested at $V_S = 3\text{V}$ on the LT1789-10 due to an increase in sensitivity to test system noise. Actual performance is expected to be similar to performance at $V_S = 5\text{V}$.

TYPICAL PERFORMANCE CHARACTERISTICS (LT1789-1, LT1789-10)



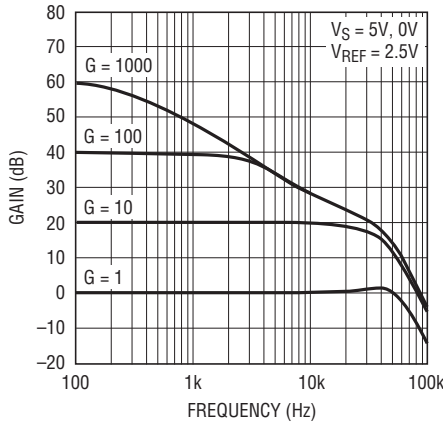
TYPICAL PERFORMANCE CHARACTERISTICS (LT1789-1)

Output Voltage Swing vs Load Current



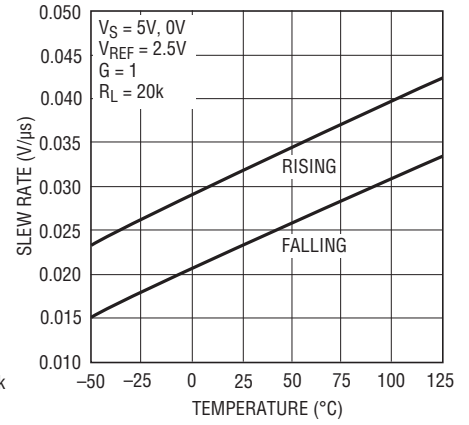
1789 G04

Gain vs Frequency



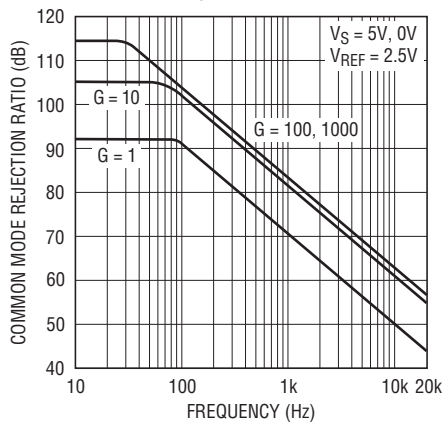
1789 G05

Slew Rate vs Temperature



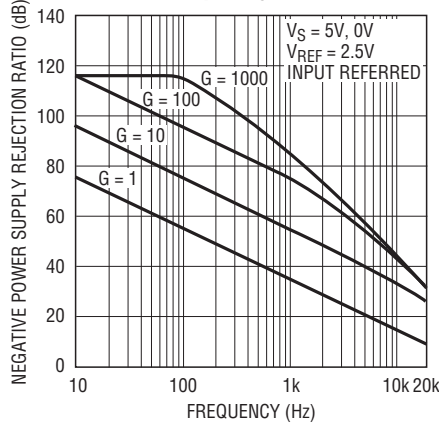
1789 G06

Common Mode Rejection Ratio vs Frequency



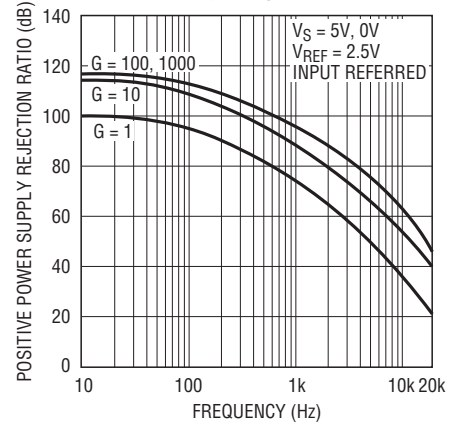
1879 G07

Negative Power Supply Rejection Ratio vs Frequency



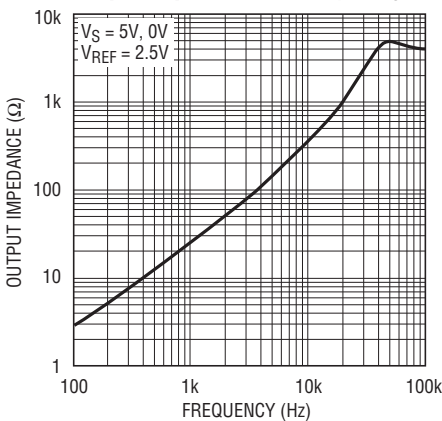
1789 G08

Positive Power Supply Rejection Ratio vs Frequency



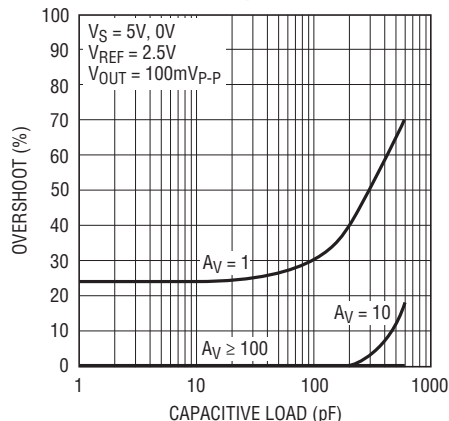
1789 G09

Output Impedance vs Frequency



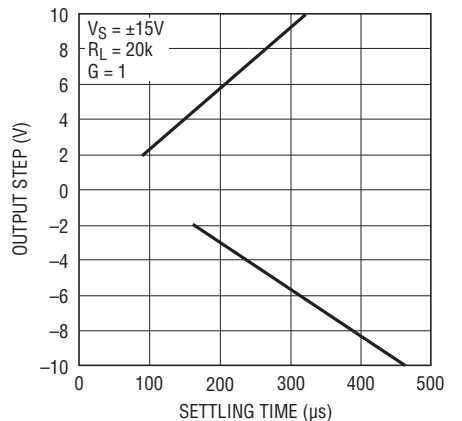
1789 G10

Overshoot vs Capacitive Load



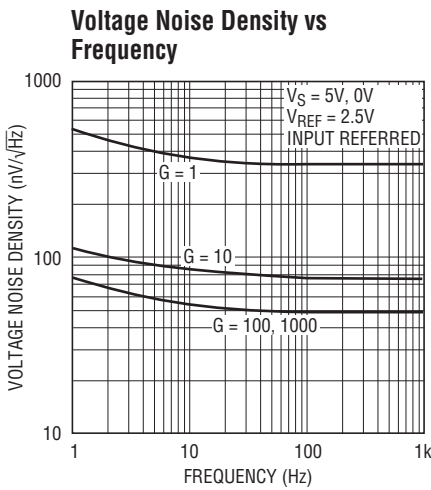
1789 G11

Settling Time to 0.01% vs Output Step

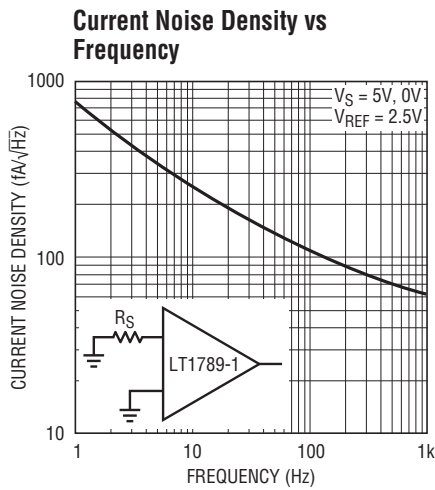


1789 G12

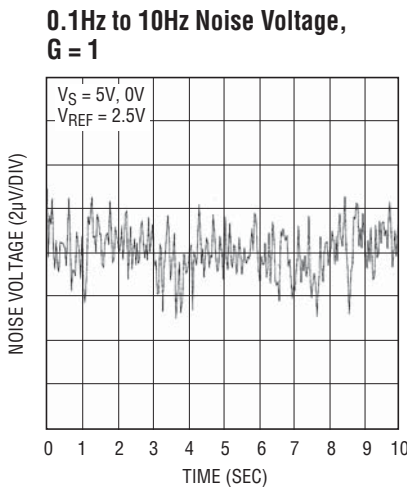
TYPICAL PERFORMANCE CHARACTERISTICS (LT1789-1)



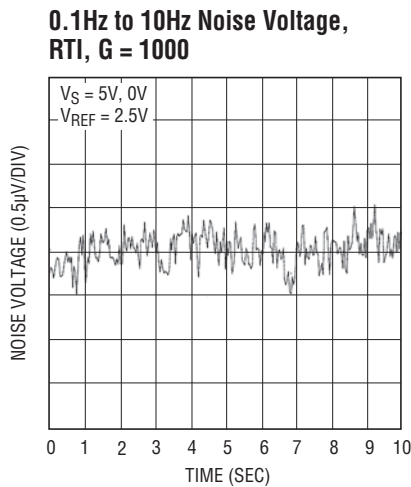
1789 G13



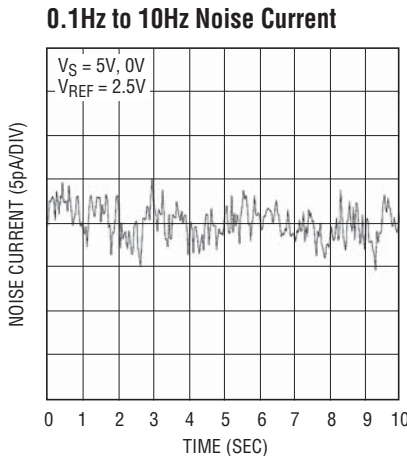
1789 G14



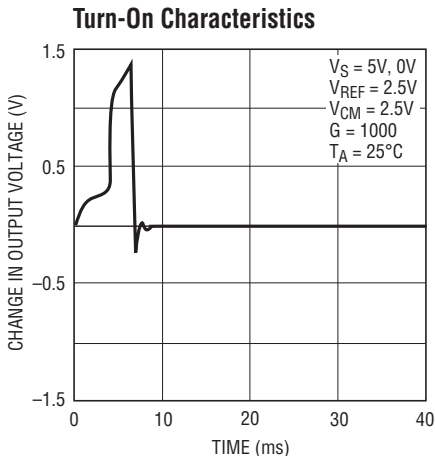
1789 G15



1789 G16



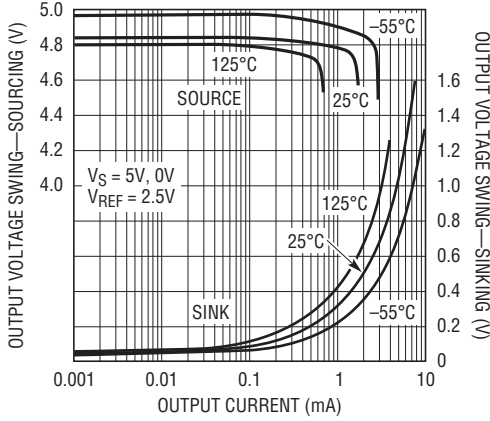
1789 G17



1789 G18

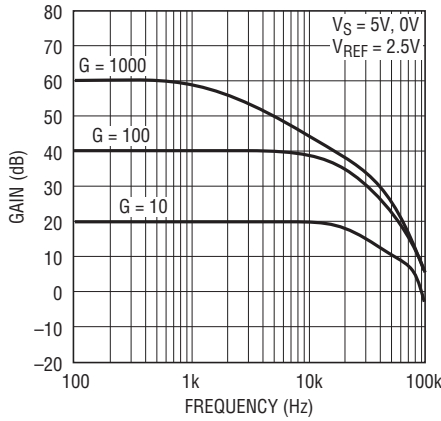
TYPICAL PERFORMANCE CHARACTERISTICS (LT1789-10)

Output Voltage Swing vs Load Current



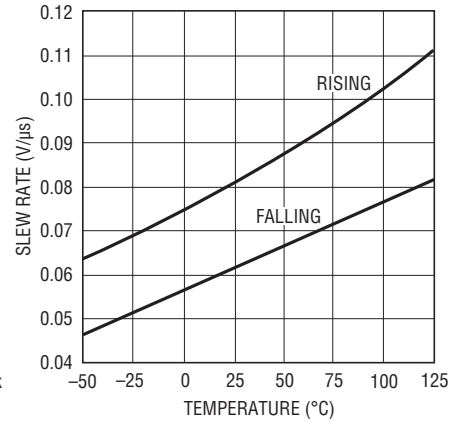
1789 G21

Gain vs Frequency



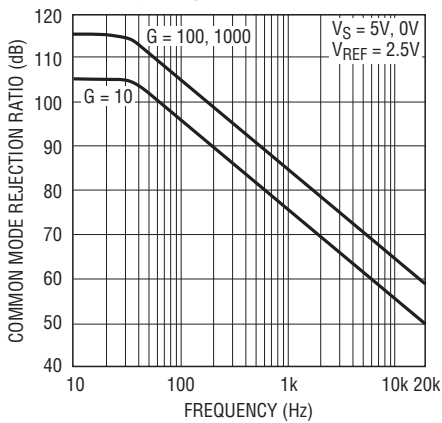
1789 G22

Slew Rate vs Temperature



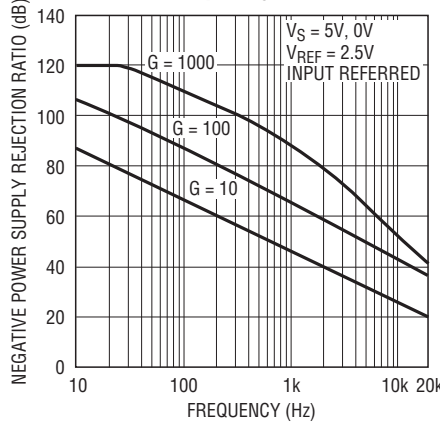
1789 G23

Common Mode Rejection Ratio vs Frequency



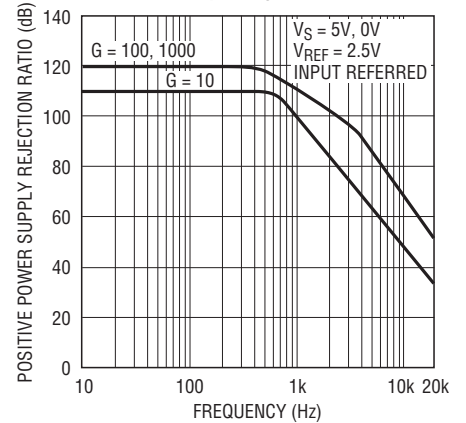
1789 G24

Negative Power Supply Rejection Ratio vs Frequency



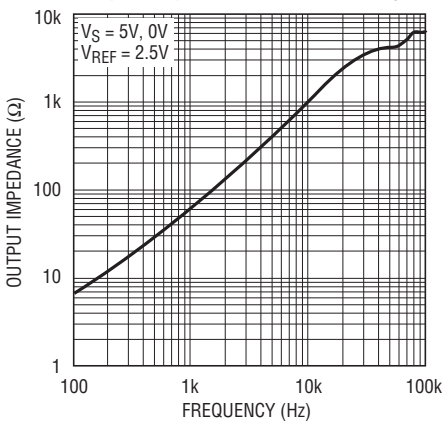
1789 G25

Positive Power Supply Rejection Ratio vs Frequency



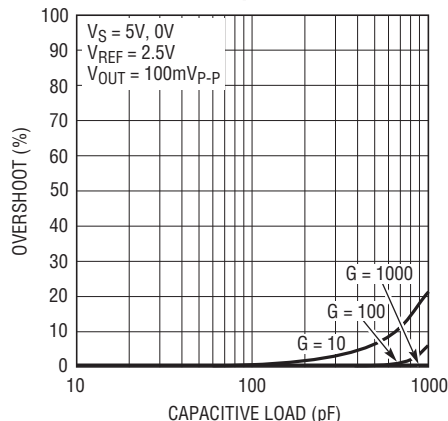
1789 G26

Output Impedance vs Frequency



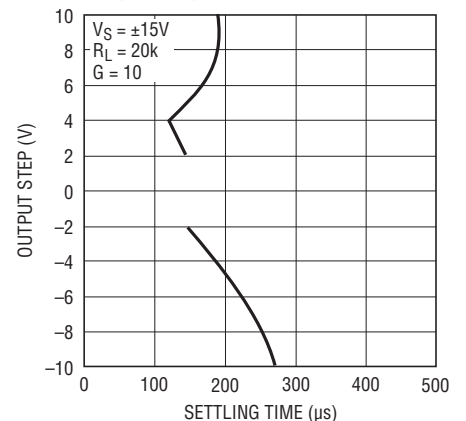
1789 G27

Overshoot vs Capacitive Load



1789 G28

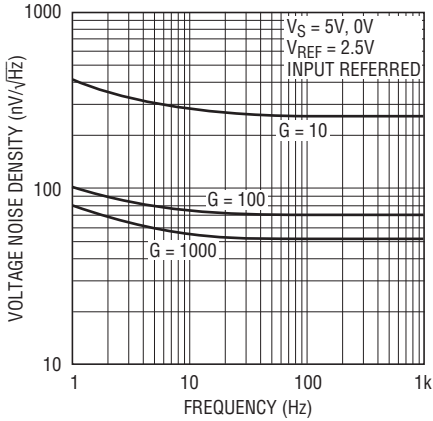
Settling Time to 0.01% vs Output Step



1789 G29

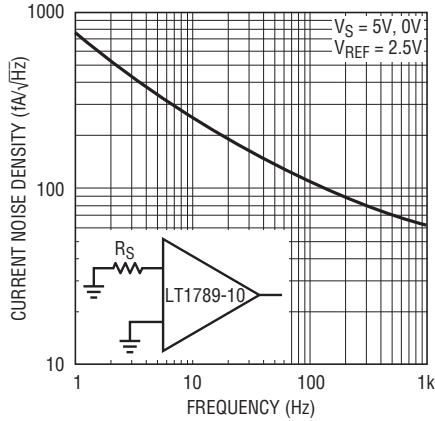
TYPICAL PERFORMANCE CHARACTERISTICS (LT1789-10)

Voltage Noise Density vs Frequency



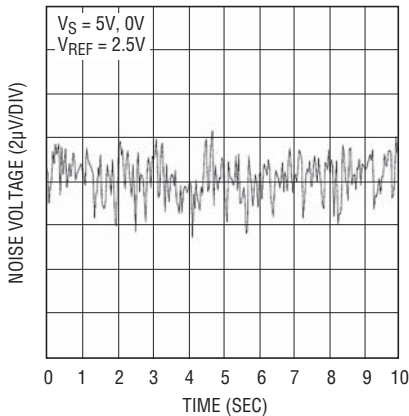
1789 G30

Current Noise Density vs Frequency



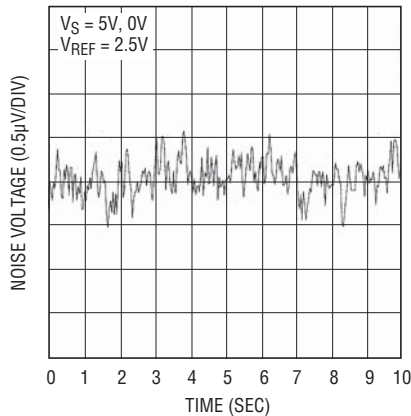
1789 G31

0.1Hz to 10Hz Noise Voltage, RTI, G = 10



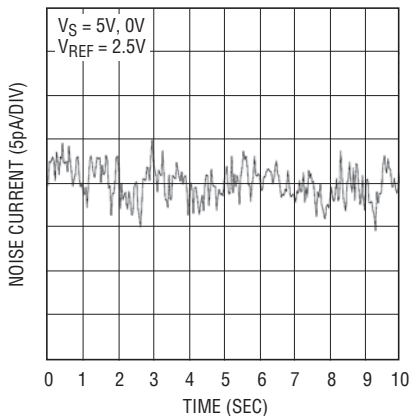
1789 G32

0.1Hz to 10Hz Noise Voltage, RTI, G = 1000



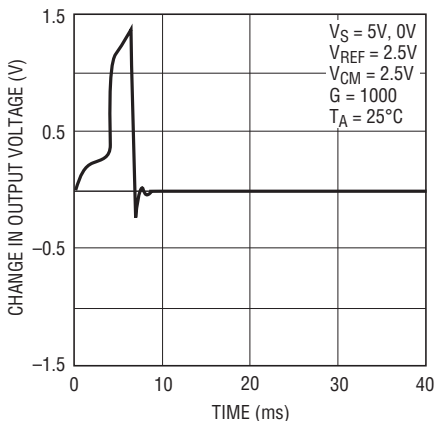
1789 G33

0.1Hz to 10Hz Noise Current



1789 G34

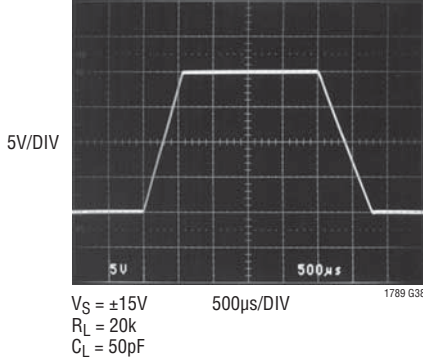
Turn-On Characteristics



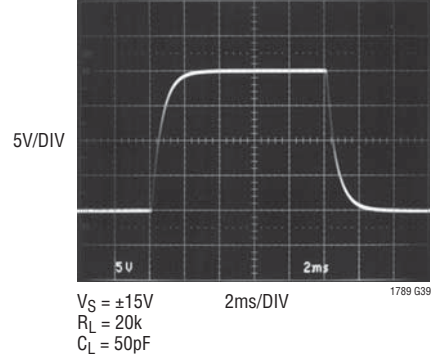
1789 G59

TYPICAL PERFORMANCE CHARACTERISTICS (LT1789-1)

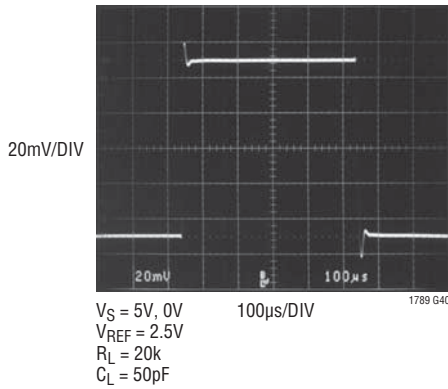
Large-Signal Transient Response
G = 1, 10, 100



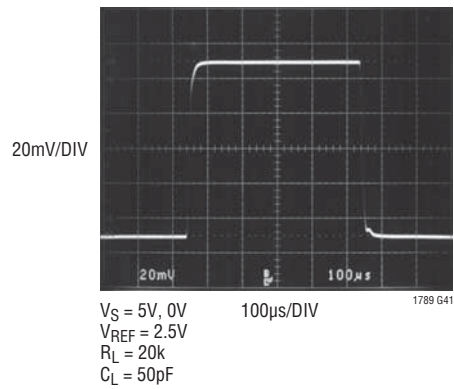
Large-Signal Transient Response
G = 1000



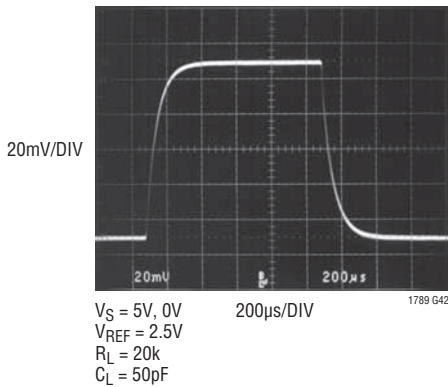
Small-Signal Transient Response
G = 1



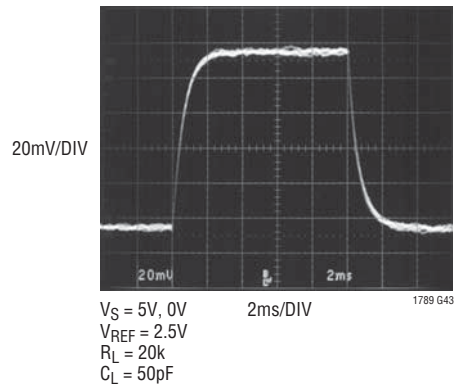
Small-Signal Transient Response
G = 10



Small-Signal Transient Response
G = 100

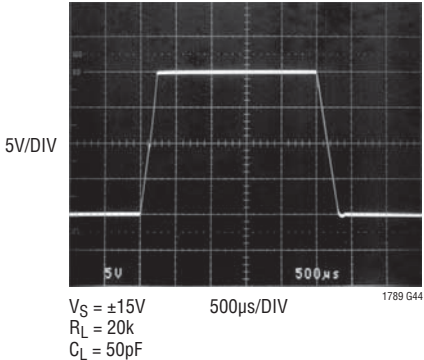


Small-Signal Transient Response
G = 1000

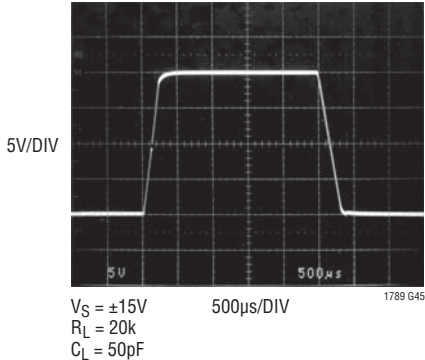


TYPICAL PERFORMANCE CHARACTERISTICS (LT1789-10)

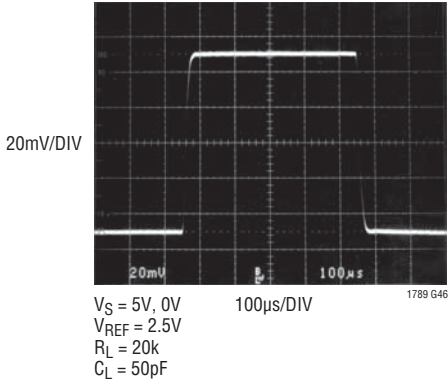
Large-Signal Transient Response
G = 10, 100



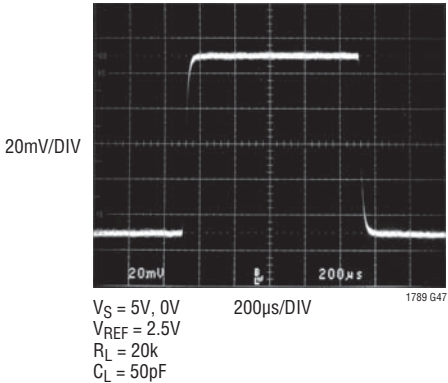
Large-Signal Transient Response
G = 1000



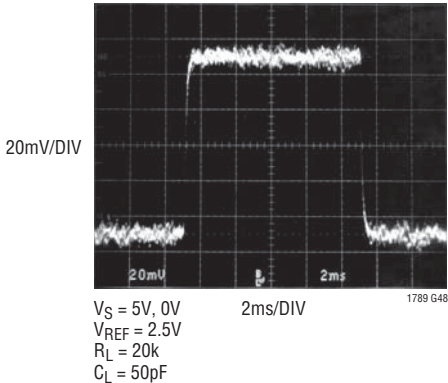
Small-Signal Transient Response
G = 10



Small-Signal Transient Response
G = 100

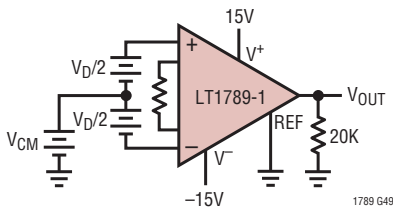
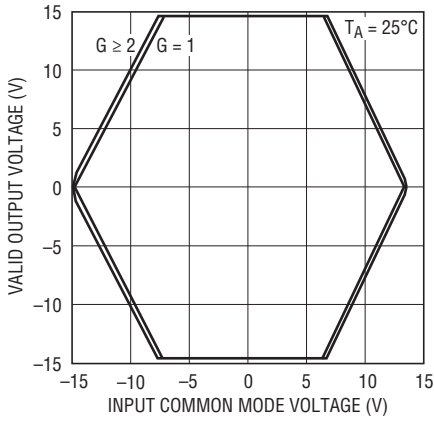


Small-Signal Transient Response
G = 1000

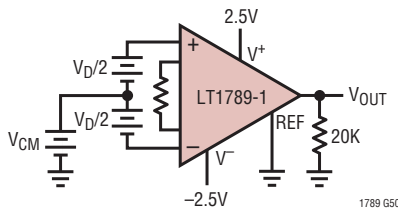
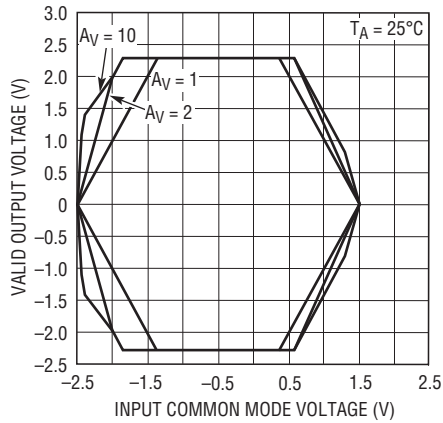


TYPICAL PERFORMANCE CHARACTERISTICS (LT1789-1)

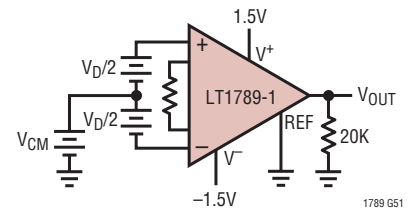
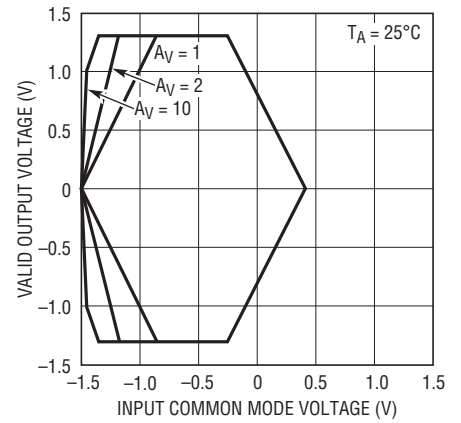
Valid Output Voltage vs Input Common Mode Voltage
 $V_S = \pm 15V$



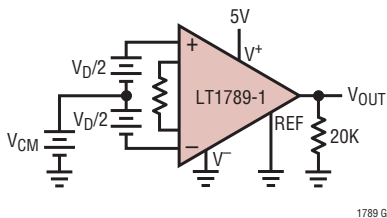
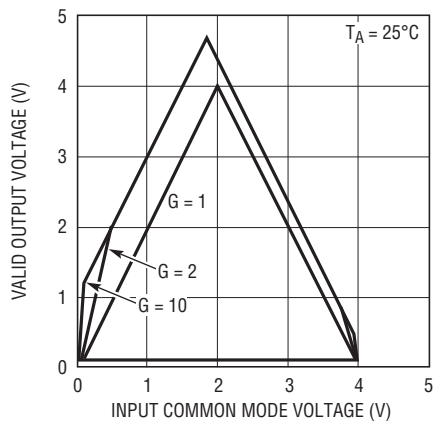
Valid Output Voltage vs Input Common Mode Voltage
 $V_S = \pm 2.5V$



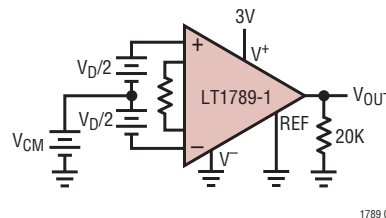
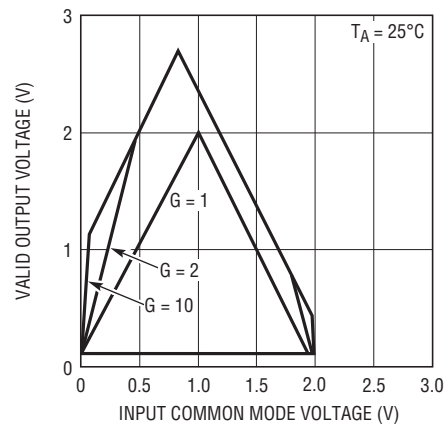
Valid Output Voltage vs Input Common Mode Voltage
 $V_S = \pm 1.5V$



Valid Output Voltage vs Input Common Mode Voltage
 $V_S = 5V$

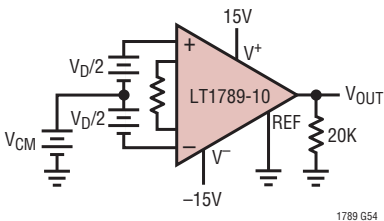
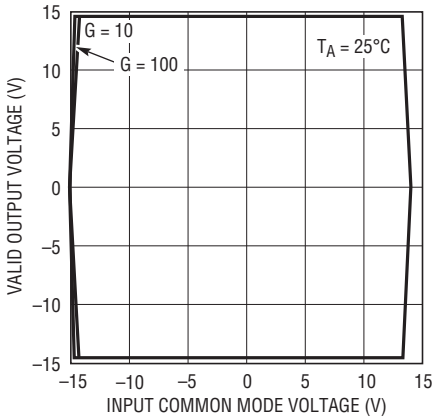


Valid Output Voltage vs Input Common Mode Voltage
 $V_S = 3V$

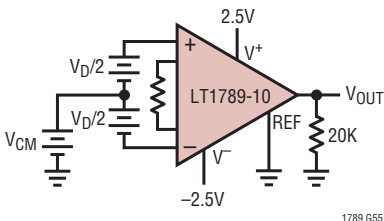
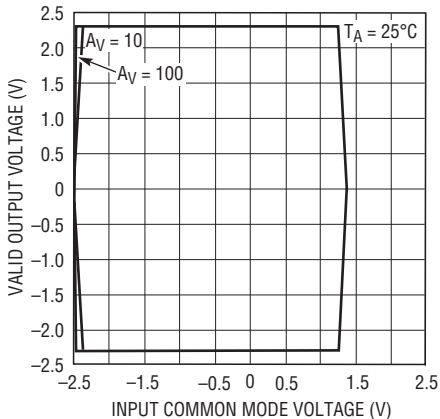


TYPICAL PERFORMANCE CHARACTERISTICS (LT1789-10)

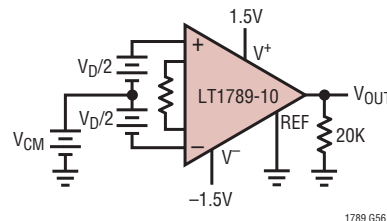
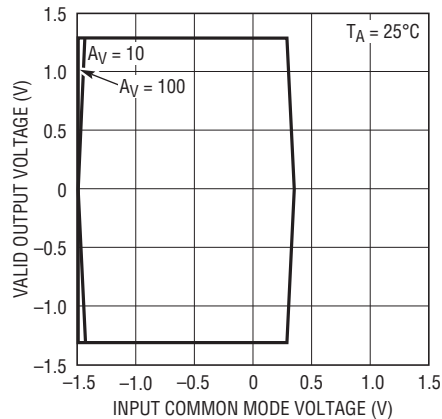
Valid Output Voltage vs Input Common Mode Voltage
 $V_S = \pm 15V$



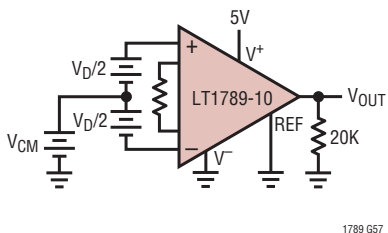
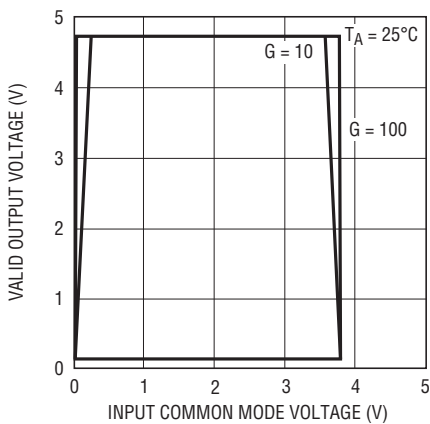
Valid Output Voltage vs Input Common Mode Voltage
 $V_S = \pm 2.5V$



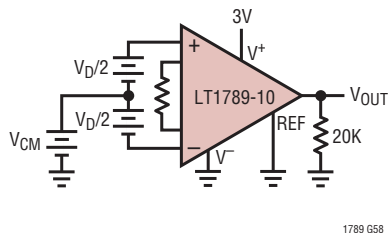
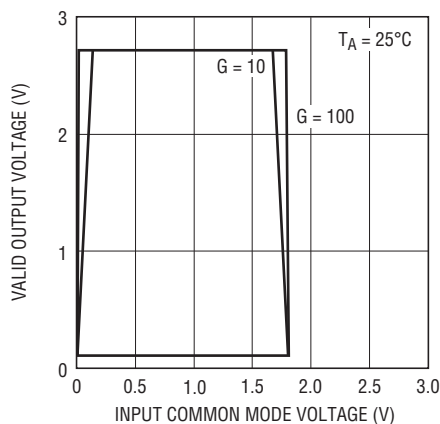
Valid Output Voltage vs Input Common Mode Voltage
 $V_S = \pm 1.5V$



Valid Output Voltage vs Input Common Mode Voltage
 $V_S = 5V$



Valid Output Voltage vs Input Common Mode Voltage
 $V_S = 3V$



BLOCK DIAGRAM

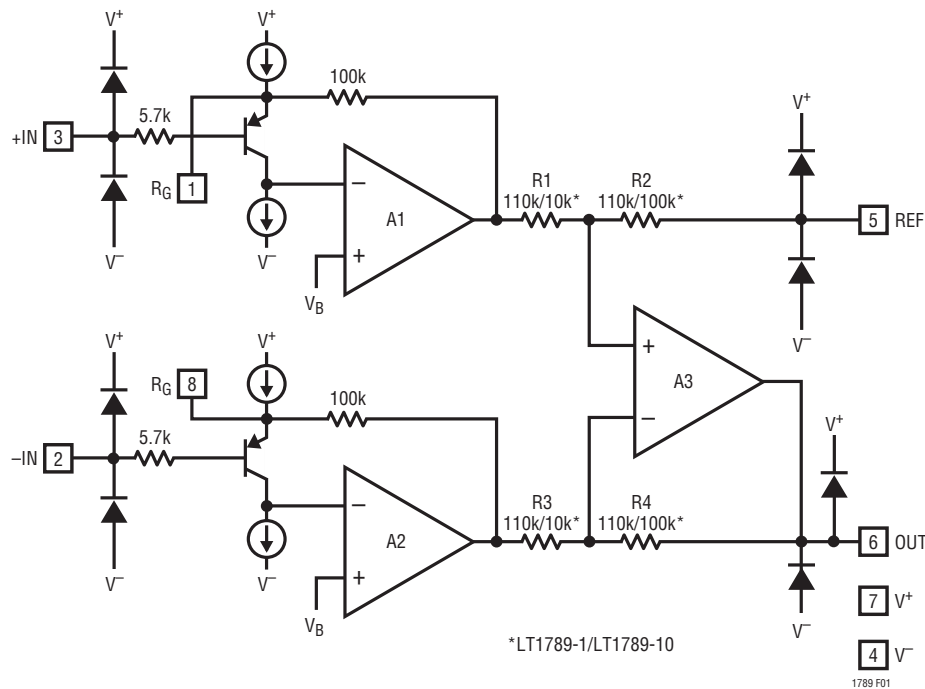


Figure 1. Block Diagram

APPLICATIONS INFORMATION

Setting the Gain

The gain of the LT1789-1 and LT1789-10 is set by the value of resistor R_G , applied across pins 1 and 8. For the LT1789-1, the gain G will be:

$$G = 1 + 200k/R_G$$

and R_G can be calculated from the desired gain by

$$R_G = 200k/(G - 1)$$

For the LT1789-10, the gain G will be

$$G = 10 \cdot (1 + 200k/R_G)$$

and R_G can be calculated from the desired gain by

$$R_G = 200k/(0.1 \cdot G - 1)$$

For the lowest achievable gain, R_G may be set to infinity by leaving Pins 1 and 8 open.

Input and Output Offset Voltage

The offset voltage of the LT1789-1/LT1789-10 has two components: the output offset and the input offset. The total offset voltage referred to the input (RTI) is found by dividing the output offset by the programmed gain (G) and adding it to the input offset. At high gains the input offset voltage dominates, whereas at low gains the output offset voltage dominates. The total offset voltage is:

$$\text{Total input offset voltage (RTI)} = \text{input offset} + (\text{output offset}/G)$$

$$\text{Total output offset voltage (RTO)} = (\text{input offset} \cdot G) + \text{output offset}$$

APPLICATIONS INFORMATION

Reference Terminal

The output voltage of the LT1789-1/LT1789-10 (Pin 6) is referenced to the voltage on the reference terminal (Pin 5). Resistance in series with the REF pin must be minimized for best common mode rejection. For example, a 22Ω resistance from the REF pin to ground will not only increase the gain error by 0.02% but will lower the CMRR to 80dB.

Output Offset Trimming

The LT1789-1/LT1789-10 is laser trimmed for low offset voltage so that no external offset trimming is required for most applications. In the event that the offset needs to be adjusted, the circuit in Figure 2 is an example of an optional offset adjust circuit. The op amp buffer provides a low impedance to the REF pin where resistance must be kept to a minimum for best CMRR and lowest gain error.

Input Bias Current Return Path

The low input bias current of the LT1789-1/LT1789-10 (19nA) and the high input impedance (1.6GΩ) allow the use of high impedance sources without introducing significant offset voltage errors, even when the full common mode range is required. However, a path must be provided for the input bias currents of both inputs when a purely differential signal is being amplified. Without this path the inputs will float high and exceed the input common mode range of the LT1789-1/LT1789-10, resulting in a saturated input stage. Figure 3 shows three examples of an input bias current path. The first example is of a purely differential signal source with a 10kΩ input current path to ground. Since the impedance of the signal source is low, only one resistor is needed. Two matching resistors are needed for higher impedance signal sources as shown in the second example. Balancing the input impedance improves both common mode rejection and DC offset. The need for input resistors is eliminated if a center tap is present as shown in the third example.

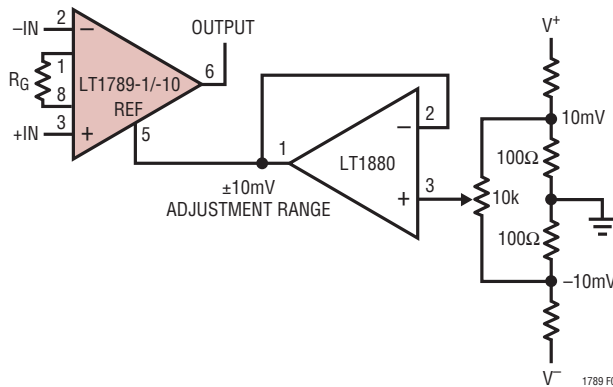


Figure 2. Optional Trimming of Output Offset Voltage

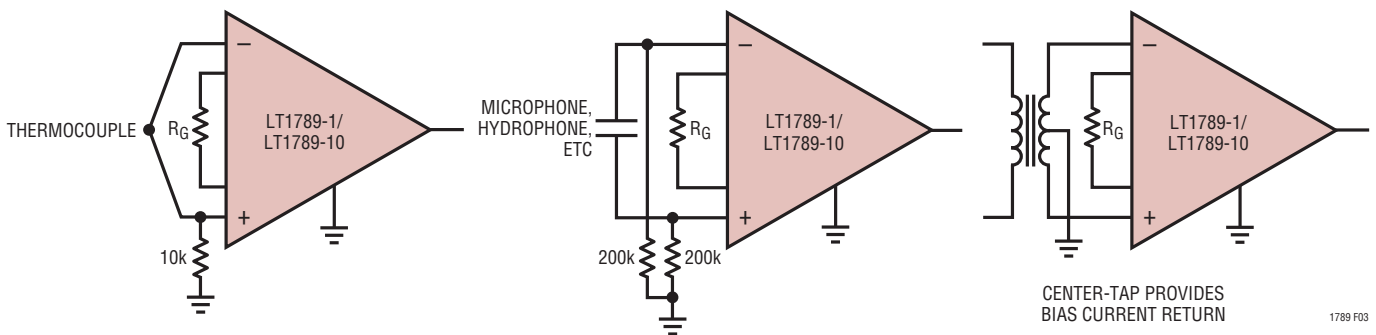


Figure 3. Providing an Input Common Mode Current Path

APPLICATIONS INFORMATION

Output Voltage vs Input Common Mode Voltage

All instrumentation amplifiers have limiting factors that can cause an output to be invalid (the output is not equal to the input differential voltage multiplied by the gain) even though the output appears to be operating in a linear region. Limiting factors such as input voltage range and output swing can be easily measured, however, there are also internal nodes that can limit. These internal nodes cannot be measured externally and can lead to erroneous output readings.

To ensure a valid output for a given input common mode voltage and input differential voltage, the following four limiting factors must be taken into consideration (refer to the block diagram):

- 1) The input voltage ranges of the input amplifiers A1 and A2.
- 2) The output swings of the input amplifiers A1 and A2 (internal nodes).
- 3) The input voltage range of the output amplifier A3 (internal node).
- 4) The output swing of the output amplifier A3.

These limits can be determined using the relationships below.

- 1) The input voltage range limits can be found in the electrical tables.
- 2) The output voltages of the input amplifiers A1 and A2 can be found by the following formulas:

$$V_{OUT\ A1} = (V_D/2)(G)(R1/R2) + V_{CM} + 0.6V$$

$$V_{OUT\ A2} = (-V_D/2)(G)(R1/R2) + V_{CM} + 0.6V$$

Where V_D is the input differential voltage and V_{CM} is the input common mode voltage.

The typical output swing limits for A1 and A2 can be found in the Output Swing vs Load Current typical performance curve, using $R1 + R2$ as the load resistance.

This limitation usually becomes dominant when gain is taken in the input stage and the common mode input voltage is close to either supply rail.

The LT1789-10 is less susceptible to this limiting factor because the gain is taken in the output stage.

- 3) The voltage on the inputs to the output amplifier A3 can be determined by the following formula:

$$V_{IN\ A3} = (V_{OUT\ A1} - V_{REF})(R2/(R1 + R2))$$

The input voltage range of A3 has the same input limits as the LT1789-1. This limiting factor is more prevalent with single supplies, where both the reference voltage and input common mode voltage are near V^+ . This is also more of a concern with the LT1789-10 because the ratio of $R1:R2$ is 1:10 instead of 1:1.

- 4) The output voltage swing limits are also found in the electrical tables.

The Output Voltage vs Input Common Mode Voltage typical performance curves show the regions of operation for the three supply voltages specified.

Single Supply Operation

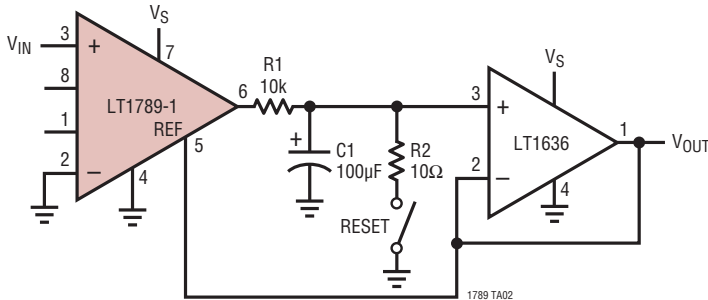
There are usually two types of input signals that need to be processed; differential signals, like the output of a bridge or single ended signals, such as the output from a thermistor. Both signals require special consideration when operating with a single supply.

When processing differential signals, REF (Pin 5) must be brought above the negative supply (Pin 4) to allow the output to process both the positive and negative going input signal. The maximum output operating range is obtained by setting the voltage on the REF pin to half supply. This must be done with a low impedance source to minimize CMRR and gain errors.

For single ended input signals, the REF pin can be at the same potential as the negative supply provided the output of the instrumentation amplifier remains inside the specified operating range. This maximizes the output range, however the smallest input signal that can be processed is limited by the output swing to the negative supply.

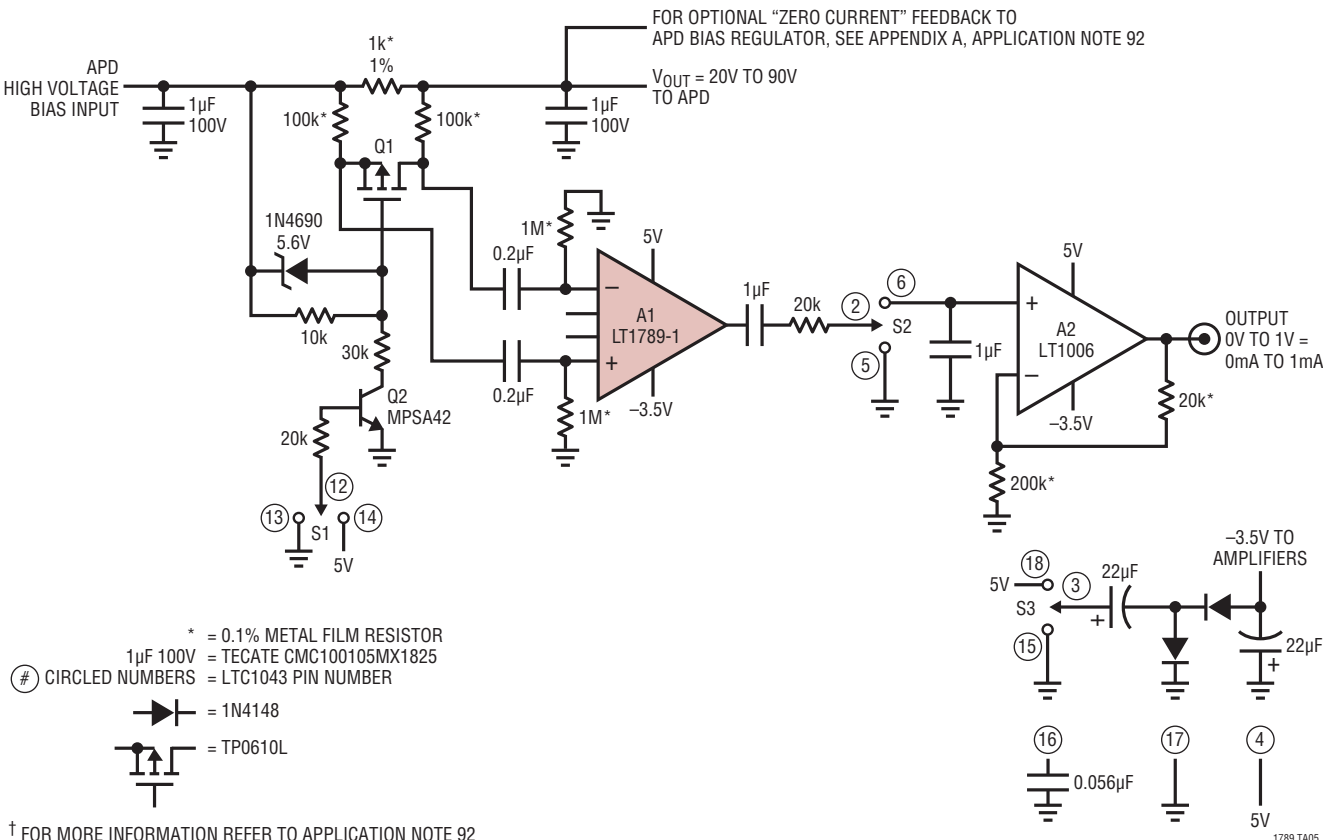
TYPICAL APPLICATIONS

Single Supply Positive Integrator



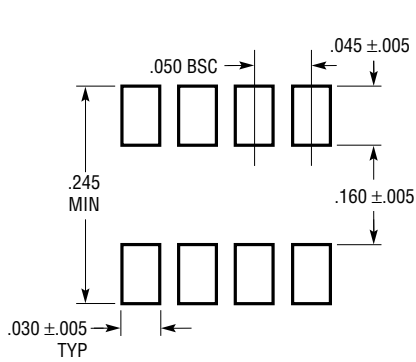
$V_S = 2.7V \text{ TO } 32V$
 TIME CONSTANT = $(R1)(C1) = 1 \text{ SECOND AS SHOWN}$

Avalanche Photo Diode Module Bias Current Monitor

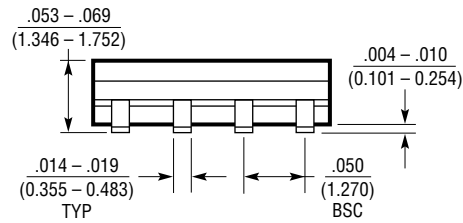
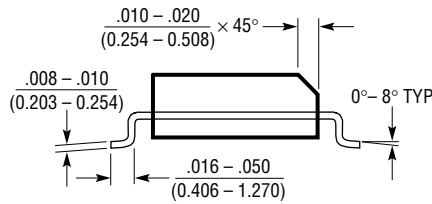
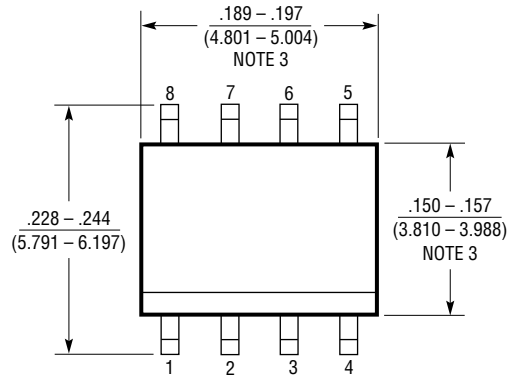


PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
 (Reference LTC DWG # 05-08-1610)



RECOMMENDED SOLDER PAD LAYOUT



- NOTE:
 1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
 2. DRAWING NOT TO SCALE
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED $.006''$ (0.15mm)

S08 0303

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	5/10	Updated Input Noise Current Density Spec	6