Low Noise, Precision, JFET Input Op Amp

FEATURES

- **100% Tested Low Voltage Noise: 6nV/√Hz Max**
- **A Grade 100% Temperature Tested**
- Voltage Gain: 1.2 Million Min
- Offset Voltage Over Temp: 800µV Max
- Gain-Bandwidth Product: 5.6MHz Typ
- Guaranteed Specifications with ±5V Supplies

APPLICATIONS

- Photocurrent Amplifiers
- Hydrophone Amplifiers
- High Sensitivity Piezoelectric Accelerometers
- Low Voltage and Current Noise Instrumentation Amplifier Front Ends
- Two and Three Op Amp Instrumentation Amplifiers
- Active Filters

DESCRIPTION

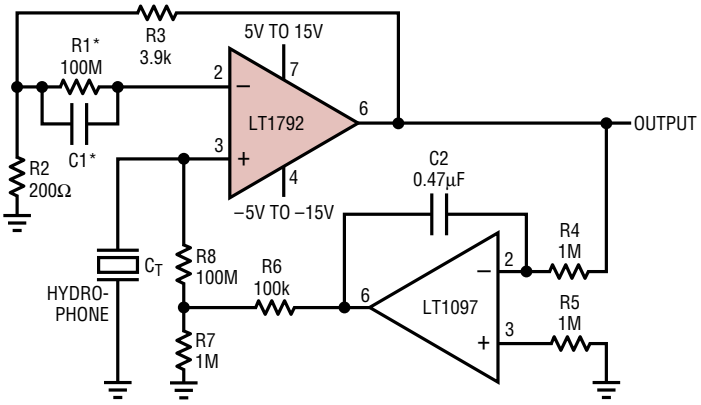
The LT®1792 achieves a new standard of excellence in noise performance for a JFET op amp. The 4.2nV/√Hz voltage noise combined with low current noise and picoampere bias currents make the LT1792 an ideal choice for amplifying low level signals from high impedance capacitive transducers.

The LT1792 is unconditionally stable for gains of 1 or more, even with load capacitances up to 1000pF. Other key features are 600µV V_{OS} and a voltage gain of over 4 million. Each individual amplifier is 100% tested for voltage noise, slew rate and gain bandwidth.

The design of the LT1792 has been optimized to achieve true precision performance with an industry standard pinout in the SO-8 package. Specifications are also provided for ±5V supplies.

TYPICAL APPLICATION

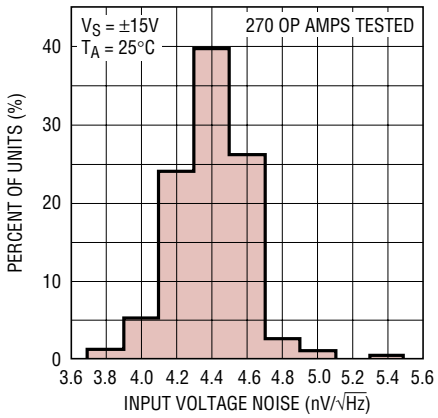
Low Noise Hydrophone Amplifier with DC Servo



DC OUTPUT ≤ 2.5mV FOR T_A < 70°C
OUTPUT VOLTAGE NOISE = 128nV/√Hz AT 1kHz (GAIN = 20)
C1 ≈ C_T ≈ 100pF TO 5000pF; R4C2 > R8C_T; *OPTIONAL

1792 TA01

1kHz Input Noise Voltage Distribution

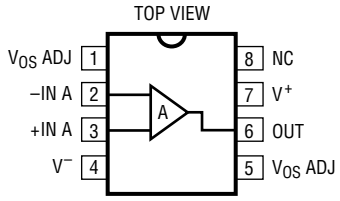


1792 TA02

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±40V
Input Voltage (Equal to Supply Voltage) ..... ±20V
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range
Commercial (Note 8) ..... –40°C to 85°C
Industrial ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

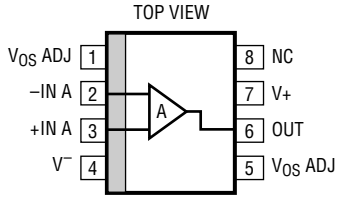


N8 PACKAGE
8-LEAD PDIP

T_{JMAX} = 140°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LT1792ACN8
LT1792CN8
LT1792AIN8
LT1792IN8



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 160°C, θ_{JA} = 190°C/W

ORDER PART NUMBER

LT1792ACS8
LT1792CS8
LT1792AIS8
LT1792IS8

S8 PART MARKING

1792A 1792AI
1792 1792I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS T_A = 25°C, V_S = ±15V, V_{CM} = 0V, unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS (Note 2)	LT1792AC/LT1792AI MIN	LT1792AC/LT1792AI TYP	LT1792AC/LT1792AI MAX	LT1792C/LT1792I MIN	LT1792C/LT1792I TYP	LT1792C/LT1792I MAX	UNITS
V_{OS}	Input Offset Voltage			0.2	0.6		0.2	0.8	mV
		V_S = ±5V		0.4	1.0		0.4	1.3	mV
I_{OS}	Input Offset Current	Warmed Up (Note 3)		100	400		100	400	pA
I_B	Input Bias Current	Warmed Up (Note 3)		300	800		300	800	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		2.4			2.4		μV_{P-P}
	Input Noise Voltage Density	f_O = 10Hz		8.3			8.3		nV/√Hz
		f_O = 1000Hz		4.2	6.0		4.2	6.0	nV/√Hz
i_n	Input Noise Current Density	f_O = 10Hz, f_O = 1000Hz (Note 4)		10			10		fA/√Hz
R_{IN}	Input Resistance								
	Differential Mode			10^{11}			10^{11}		Ω
	Common Mode	V_{CM} = –10V to 8V		10^{11}			10^{11}		Ω
		V_{CM} = 8V to 11V		10^{10}			10^{10}		Ω
C_{IN}	Input Capacitance			14			14		pF
		V_S = ±5V		27			27		pF
V_{CM}	Input Voltage Range (Note 5)		13.0	13.5		13.0	13.5		V
			–10.5	–11.0		–10.5	–11.0		V
CMRR	Common Mode Rejection Ratio	V_{CM} = –10V to 13V	85	105		82	100		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±20V	88	105		83	98		dB

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±15V, V_{CM} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1792AC/LT1792AI MIN	LT1792AC/LT1792AI TYP	LT1792AC/LT1792AI MAX	LT1792C/LT1792I MIN	LT1792C/LT1792I TYP	LT1792C/LT1792I MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	V_O = ±12V, R_L = 10k V_O = ±10V, R_L = 1k	1200 600	4800 4000		1000 500	4500 3000		V/mV V/mV
V_{OUT}	Output Voltage Swing	R_L = 10k R_L = 1k	±13.0 ±12.0	±13.2 ±12.3		±13.0 ±12.0	±13.2 ±12.3		V V
SR	Slew Rate	$R_L \geq$ 2k (Note 7)	2.3	3.4		2.3	3.4		V/µs
GBW	Gain-Bandwidth Product	f_O = 100kHz	4.0	5.6		4.0	5.6		MHz
I_S	Supply Current V_S = ±5V			4.2 4.2	5.20 5.15		4.2 4.2	5.20 5.15	mA mA
	Offset Voltage Adjustment Range	R_{POT} (to V_{EE}) = 10k		10			10		mV

The ● denotes specifications which apply over the temperature range 0°C ≤ T_A ≤ 70°C. V_S = ±15V, V_{CM} = 0V, unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1792AC MIN	LT1792AC TYP	LT1792AC MAX	LT1792C MIN	LT1792C TYP	LT1792C MAX	UNITS
V_{OS}	Input Offset Voltage V_S = ±5V		● ●		0.4 0.6	0.8 1.2		0.8 1.2	2.7 3.2	mV mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 6)	●		4	10		7	40	µV/°C
I_{OS}	Input Offset Current		●		180	500		180	500	pA
I_B	Input Bias Current		●		500	1800		500	1800	pA
V_{CM}	Input Voltage Range		● ●	12.9 –10.0	13.4 –10.8		12.9 –10.0	13.4 –10.8		V V
CMRR	Common Mode Rejection Ratio	V_{CM} = –10V to 12.9V	●	81	104		79	99		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±20V	●	85	99		81	97		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = ±12V, R_L = 10k V_O = ±10V, R_L = 1k	● ●	900 500	3600 2600		800 400	3400 2400		V/mV V/mV
V_{OUT}	Output Voltage Swing	R_L = 10k R_L = 1k	● ●	±12.9 ±11.9	±13.2 ±12.15		±12.9 ±11.9	±13.2 ±12.15		V V
SR	Slew Rate	$R_L \geq$ 2k (Note 7)	●	2.1	3.1		2.1	3.1		V/µs
GBW	Gain-Bandwidth Product	f_O = 100kHz	●	3.2	4.5		3.2	4.5		MHz
I_S	Supply Current V_S = ±5V		● ●		4.2 4.2	5.30 5.25		4.2 4.2	5.30 5.25	mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the temperature range $-40°C \le T_A \le 85°C$. $V_S = \pm 15V$, $V_{CM} = 0V$, unless otherwise noted. (Notes 8, 9)

SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1792AC/LT1792AI MIN	LT1792AC/LT1792AI TYP	LT1792AC/LT1792AI MAX	LT1792C/LT1792I MIN	LT1792C/LT1792I TYP	LT1792C/LT1792I MAX	UNITS
V_{OS}	Input Offset Voltage		●		0.5	1.0		1.2	3.7	mV
		$V_S = \pm 5V$	●		0.8	1.4		1.5	4.2	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 6)	●		4	10		7	40	µV/°C
I_{OS}	Input Offset Current		●		300	800		300	800	pA
I_B	Input Bias Current		●		1200	4000		1200	4000	pA
V_{CM}	Input Voltage Range		●	12.6	13.0		12.6	13.0		V
			●	–10.0	–10.5		–10.0	–10.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -10V$ to 12.6V	●	80	103		78	98		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 20V$	●	83	98		79	96		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 12V$, $R_L = 10k$	●	850	3300		750	3000		V/mV
		$V_O = \pm 10V$, $R_L = 1k$	●	400	2200		300	2000		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k$	●	±12.8	±13.1		±12.8	±13.1		V
		$R_L = 1k$	●	±11.8	±12.1		±11.8	±12.1		V
SR	Slew Rate	$R_L \ge 2k$	●	2.0	3.0		2.0	3.0		V/µs
GBW	Gain-Bandwidth Product	$f_O = 100kHz$	●	2.9	4.3		2.9	4.3		MHz
I_S	Supply Current		●		4.2	5.40		4.2	5.40	mA
		$V_S = \pm 5V$	●		4.2	5.35		4.2	5.35	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers.

Note 3: Warmed-up I_B and I_{OS} readings are extrapolated to a chip temperature of 32°C from 25°C measurements and 32°C characterization data.

Note 4: Current noise is calculated from the formula:

$$i_n = (2qI_B)^{1/2}$$

where $q = 1.6 \cdot 10^{-19}$ coulomb. The noise of source resistors up to 200M swamps the contribution of current noise.

Note 5: Input voltage range functionality is assured by testing offset voltage at the input voltage range limits to a maximum of 2.3mV (A grade), to 2.8mV (C grade).

Note 6: This parameter is not 100% tested.

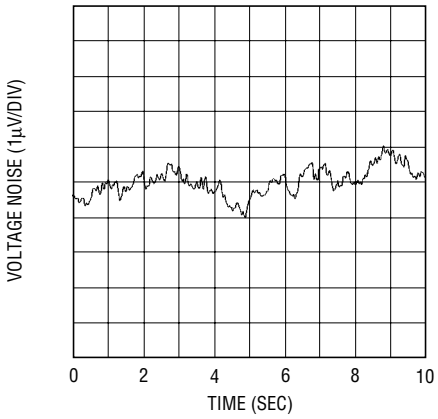
Note 7: Slew rate is measured in $A_V = -1$; input signal is ±7.5V, output measured at ±2.5V.

Note 8: The LT1792AC and LT1792C are guaranteed to meet specified performance from 0°C to 70°C and are designed, characterized and expected to meet these extended temperature limits, but are not tested at –40°C and 85°C. The LT1792I is guaranteed to meet the extended temperature limits. The LT1792AC and LT1792AI grade are 100% temperature tested for the specified temperature range.

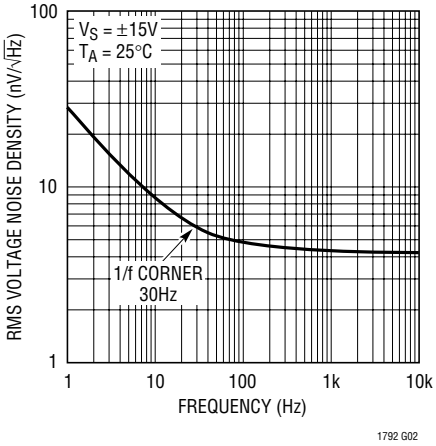
Note 9: The LT1792 is measured in an automated tester in less than one second after application of power. Depending on the package used, power dissipation, heat sinking, and air flow conditions, the fully warmed-up chip temperature can be 10°C to 50°C higher than the ambient temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

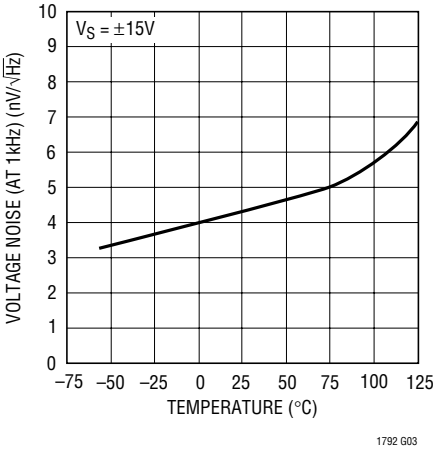
0.1Hz to 10Hz Voltage Noise



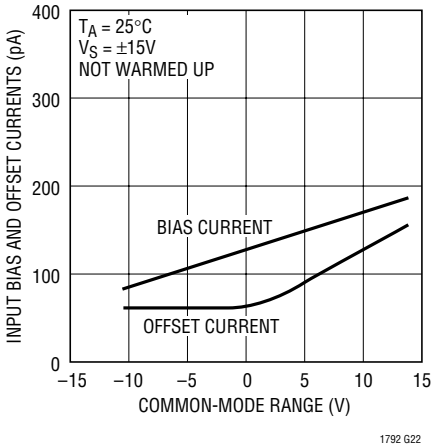
Voltage Noise vs Frequency



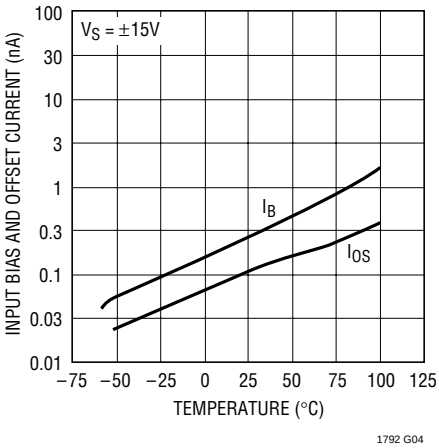
Voltage Noise vs Chip Temperature



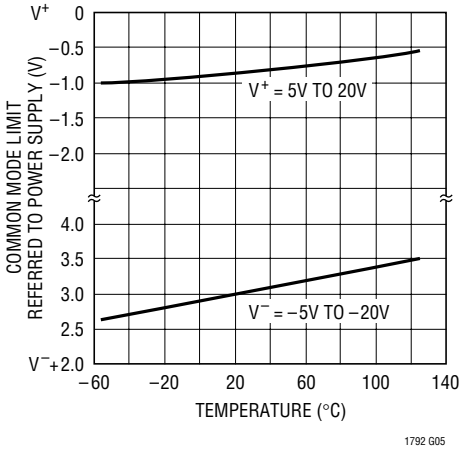
Input Bias and Offset Current Over the Common Mode Range



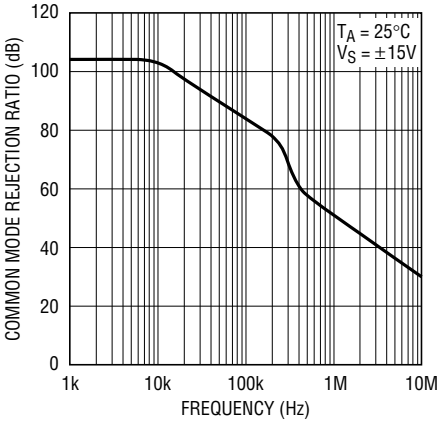
Input Bias and Offset Current vs Chip Temperature



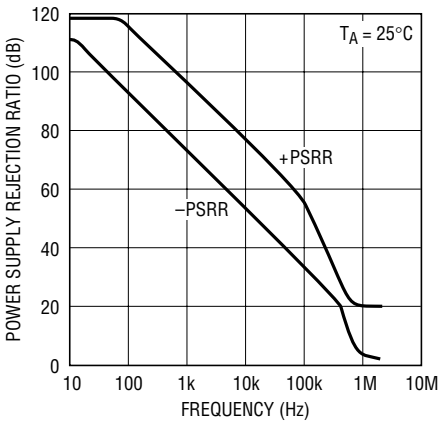
Common Mode Limit vs Temperature



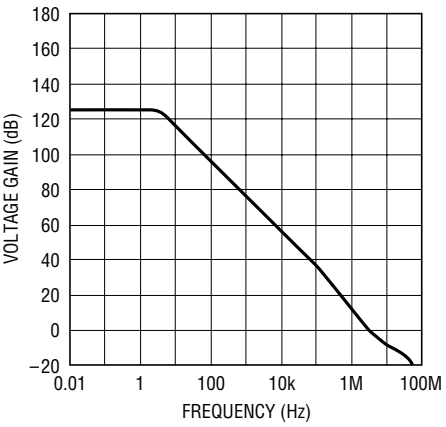
Common Mode Rejection Ratio vs Frequency



Power Supply Rejection Ratio vs Frequency

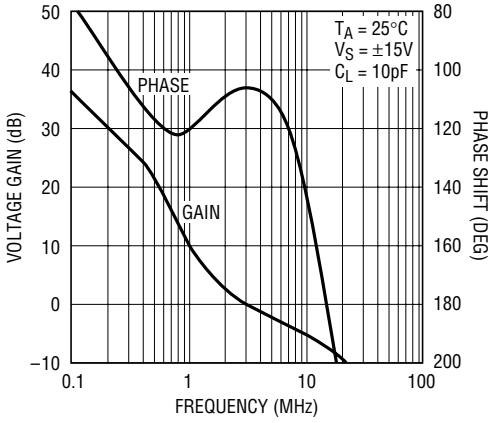


Voltage Gain vs Frequency



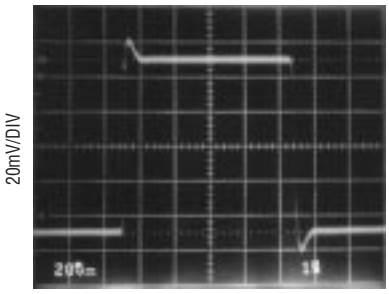
TYPICAL PERFORMANCE CHARACTERISTICS

Gain and Phase Shift vs Frequency



1792 G09

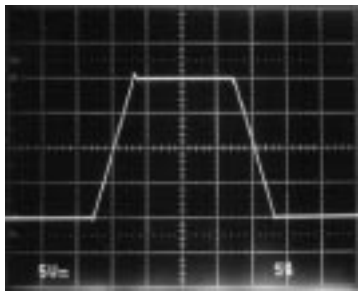
Small-Signal Transient Response



1792 G10

A_V = 1
C_L = 10pF
V_S = ±15V, ±5V
1µs/DIV

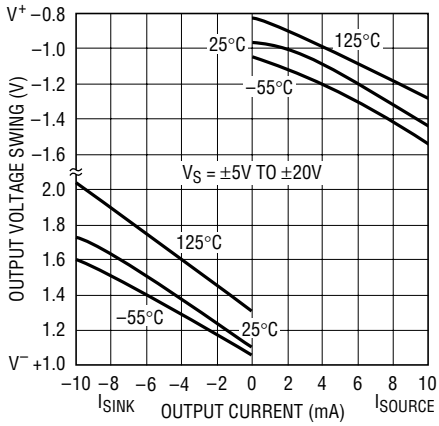
Large-Signal Transient Response



1792 G11

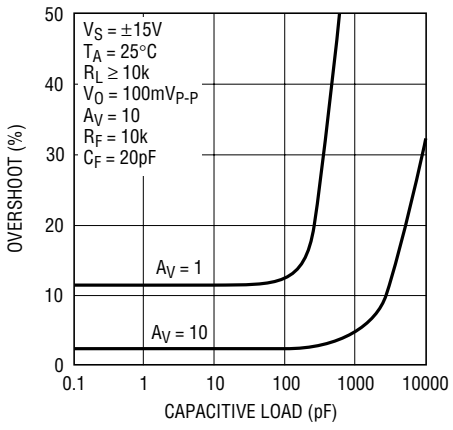
A_V = 1
C_L = 10pF
R_L = 2k
V_S = ±15V
5µs/DIV

Output Voltage Swing vs Load Current



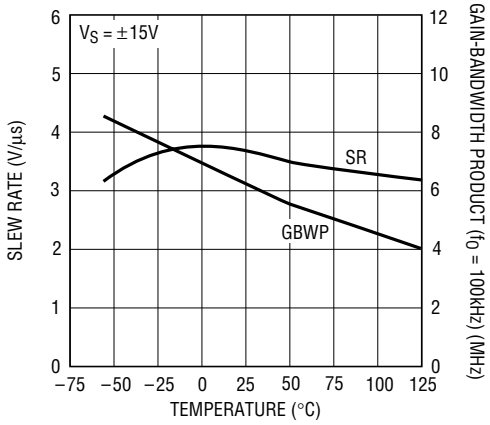
1792 G12

Capacitive Load Handling



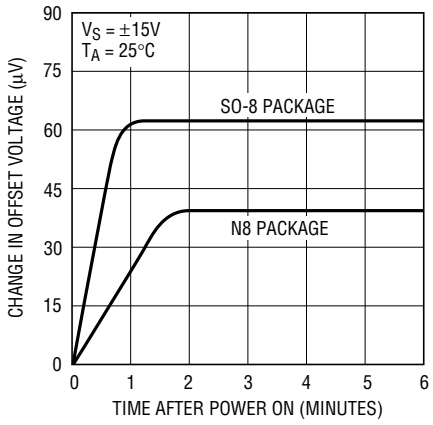
1792 G13

Slew Rate and Gain-Bandwidth Product vs Temperature



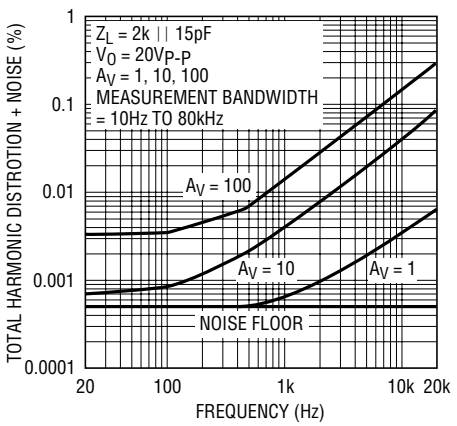
1792 G14

Warm-Up Drift



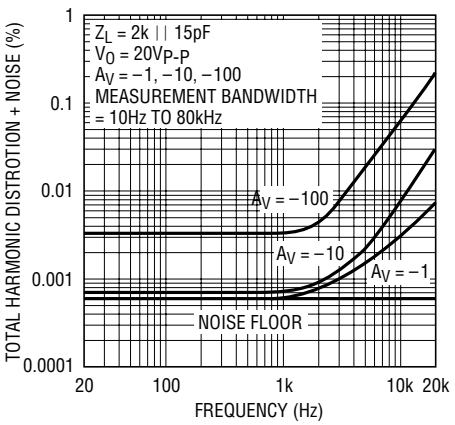
1792 G15

THD and Noise vs Frequency for Noninverting Gain



1792 G16

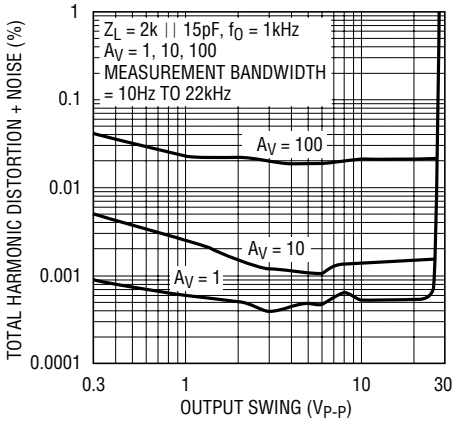
THD and Noise vs Frequency for Inverting Gain



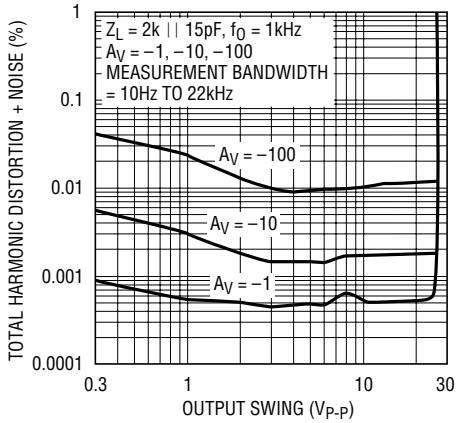
1792 G17

TYPICAL PERFORMANCE CHARACTERISTICS

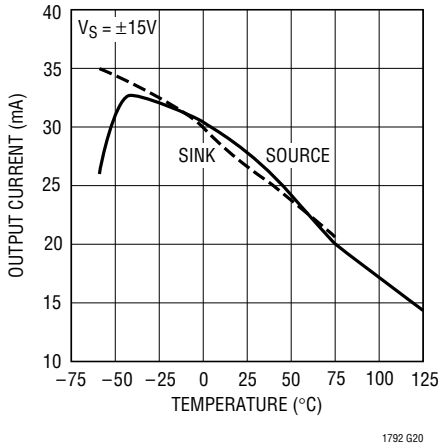
THD and Noise vs Output Amplitude for Noninverting Gain



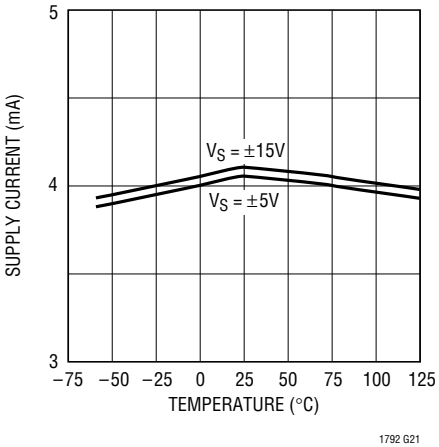
THD and Noise vs Output Amplitude for Inverting Gain



Short-Circuit Output Current vs Temperature



Supply Current vs Temperature



APPLICATIONS INFORMATION

The LT1792 may be inserted directly into OPA124, AD743, AD745, AD645, AD544 and AD820 sockets with improved noise performance. Offset nulling will be compatible with these devices with the wiper of the potentiometer tied to the negative supply (Figure 1a). No appreciable change in offset voltage drift with temperature will occur when the device is nulled with a potentiometer ranging from 10k to 200k. Finer adjustments can be made with resistors in series with the potentiometer (Figure 1b).

Being a low voltage noise JFET op amp, the LT1792 can replace many bipolar op amps that are used in amplifying low level signals from high impedance transducers. The

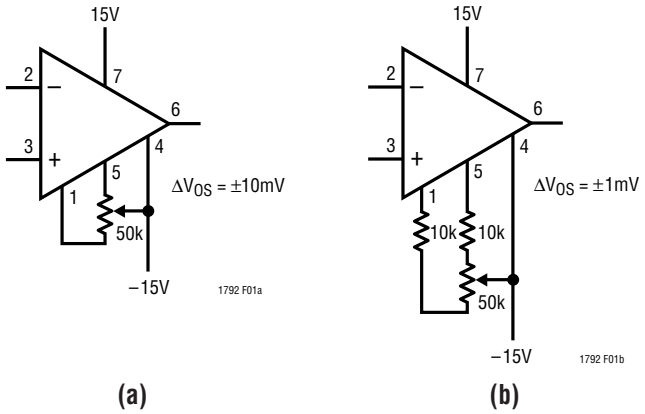


Figure 1

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best bipolar op amps, with higher current noise, will eventually lose out to the LT1792 when transducer impedance increases. The low voltage noise of the LT1792 allows it to surpass most single JFET op amps available. For the best performance versus area available anywhere, the LT1792 is offered in the SO-8 surface mount package with no degradation in performance.

The low voltage and current noise offered by the LT1792 makes it useful in a wide range of applications, especially where high impedance, capacitive transducers are used such as hydrophones, precision accelerometers and photo diodes. The total output noise in such a system is the gain times the RMS sum of the op amp input referred voltage noise, the thermal noise of the transducer, and the op amp bias current noise times the transducer impedance. Figure 2 shows total input voltage noise versus source resistance. In a low source resistance (<5k) application the op amp voltage noise will dominate the total noise. This means the LT1792 will beat out any JFET op amp, only the lowest noise bipolar op amps have the edge at low source resistances. As the source resistance increases from 5k to 50k, the LT1792 will match the best bipolar op amps for noise performance, since the thermal noise of the transducer (4kTR) begins to dominate the total noise. A further increase in source resistance, above 50k, is where the op amp's current noise component ($2qI_B R_{TRANS}$) will eventually dominate the total noise. At these high source resistances, the LT1792 will out perform the lowest noise bipolar op amp due to the inherently low current noise of FET input op amps. Clearly, the LT1792 will extend the range of high impedance transducers that can be used for high signal-to-noise ratios. This makes the LT1792 the best choice for high impedance, capacitive transducers.

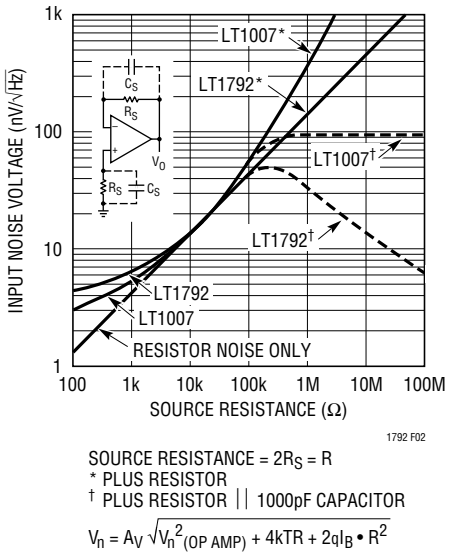


Figure 2. Comparison of LT1792 and LT1007 Total Output 1kHz Voltage Noise Versus Source Resistance

The high input impedance JFET front end makes the LT1792 suitable in applications where very high charge sensitivity is required. Figure 3 illustrates the LT1792 in its inverting and noninverting modes of operation. A charge amplifier is shown in the inverting mode example; here the gain depends on the principal of charge conservation at

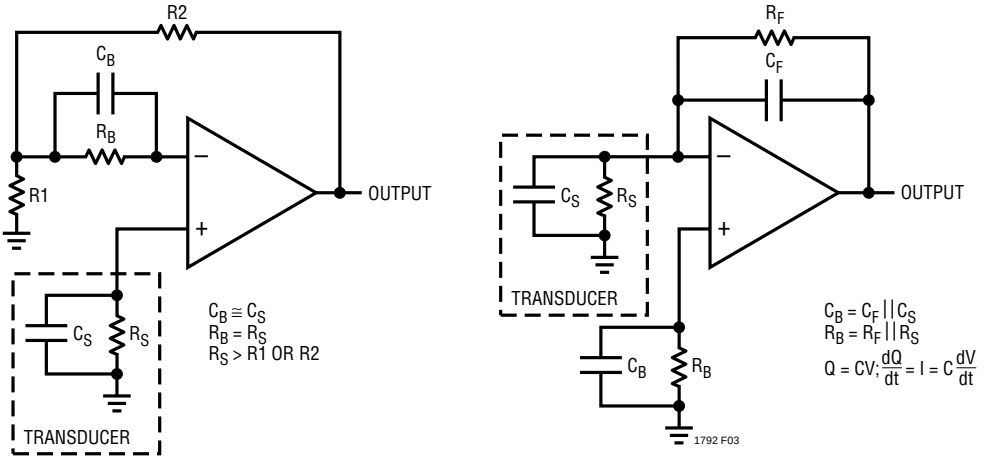


Figure 3. Noninverting and Inverting Gain Configurations

APPLICATIONS INFORMATION

the input of the LT1792. The charge across the transducer capacitance, C_S, is transferred to the feedback capacitor C_F, resulting in a change in voltage, dV, equal to dQ/C_F. The gain therefore is C_F/C_S. For unity gain, the C_F should equal the transducer capacitance plus the input capacitance of the LT1792 and R_F should equal R_S. In the noninverting mode example, the transducer current is converted to a change in voltage by the transducer capacitance; this voltage is then buffered by the LT1792 with a gain of 1 + R1/R2. A DC path is provided by R_S, which is either the transducer impedance or an external resistor. Since R_S is usually several orders of magnitude greater than the parallel combination of R1 and R2, R_B is added to balance the DC offset caused by the noninverting input bias current and R_S. The input bias currents, although small at room temperature, can create significant errors at higher temperature, especially with transducer resistances of up to 100M or more. The optimum value for R_S is determined by equating the thermal noise ($4kTR_S$) to the current noise times R_S, [$(2qI_B) \bullet R_S$], resulting in $R_B = 2V_T/I_B$ (V_T = 26mV at 25°C). A parallel capacitor, C_B, is used to cancel the phase shift caused by the op amp input capacitance and R_B.

Reduced Power Supply Operation

The LT1792 can be operated from ±5V supplies for lower power dissipation resulting in lower I_B and noise at the expense of reduced dynamic range. To illustrate this benefit, let's take the following example:

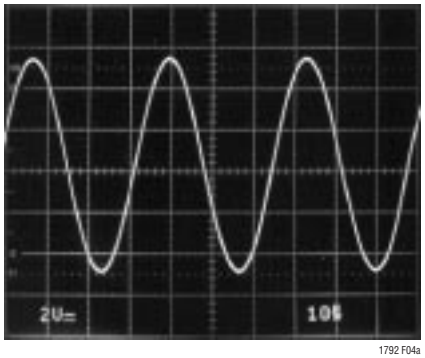
An LT1792CS8 operates at an ambient temperature of 25°C with ±15V supplies, dissipating 159mW of power (typical supply current = 5.3mA). The SO-8 package has a θ_{JA} of 190°C/W, which results in a die temperature increase of 30.2°C or a room temperature die operating temperature of 55.2°C. At ±5V supplies, the die temperature increases by only one third of the previous amount or 10.1°C resulting in a typical die operating temperature of only 35.1°C. A 20 degree reduction of die temperature is achieved at the expense of a 20V reduction in dynamic range.

To take full advantage of a wide input common mode range, the LT1792 was designed to eliminate phase reversal. Referring to the photographs shown in Figure 4, the LT1792 is shown operating in the follower mode (A_V = 1) at ±5V supplies with the input swinging ±5.2V. The output of the LT1792 clips cleanly and recovers with no phase reversal. This has the benefit of preventing lock-up in servo systems and minimizing distortion components.

High Speed Operation

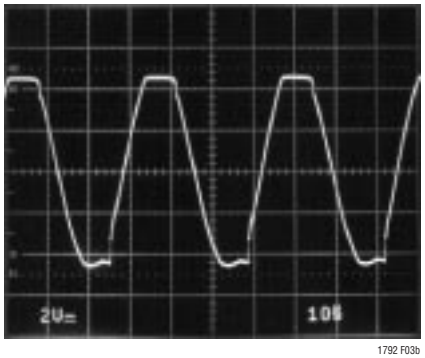
The low noise performance of the LT1792 was achieved by making the input JFET differential pair large to maximize the first stage gain. Increasing the JFET geometry

INPUT: ±5.2V Sine Wave



1792 F04a

LT1792 Output



1792 F03b

Figure 4. Voltage Follower with Input Exceeding the Common Mode Range (V_S = ±5V)

APPLICATIONS INFORMATION

also increases the parasitic gate capacitance, which if left unchecked, can result in increased overshoot and ringing. When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S, C_S), and the amplifier input capacitance (C_{IN} = 27pF). In low gain configurations and with R_S and R_F in the kilohm range (Figure 5), this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S(C_S + C_{IN}) = R_FC_F$, the effect of the feedback pole is completely removed.

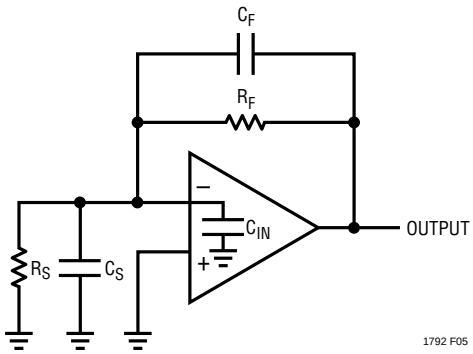
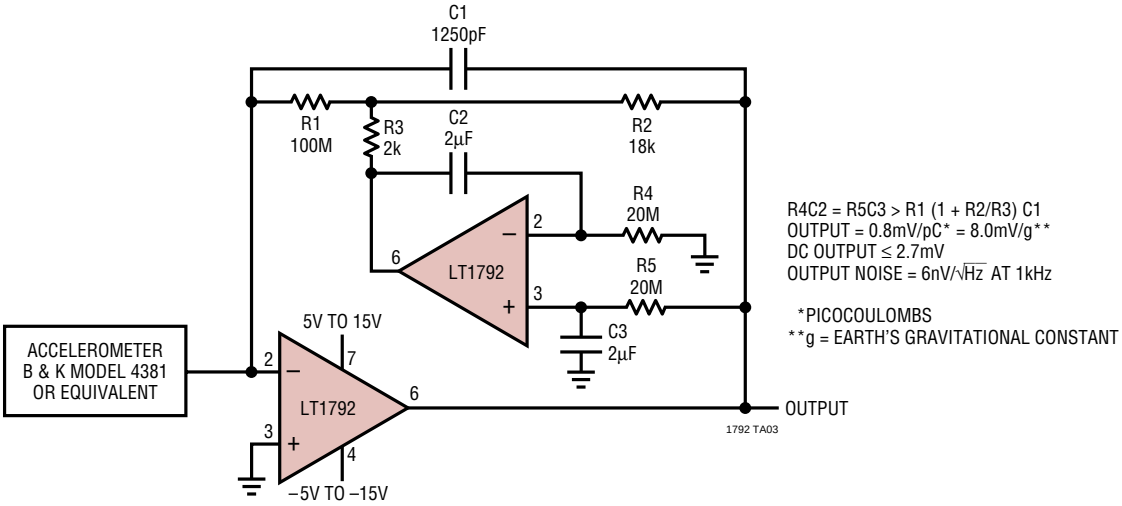


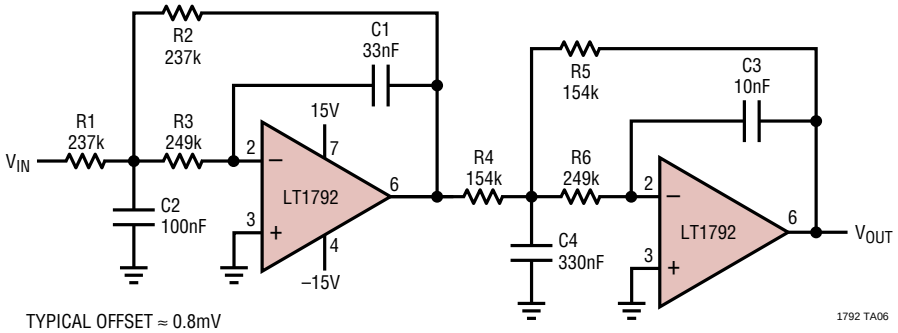
Figure 5

TYPICAL APPLICATIONS

Accelerometer Amplifier with DC Servo



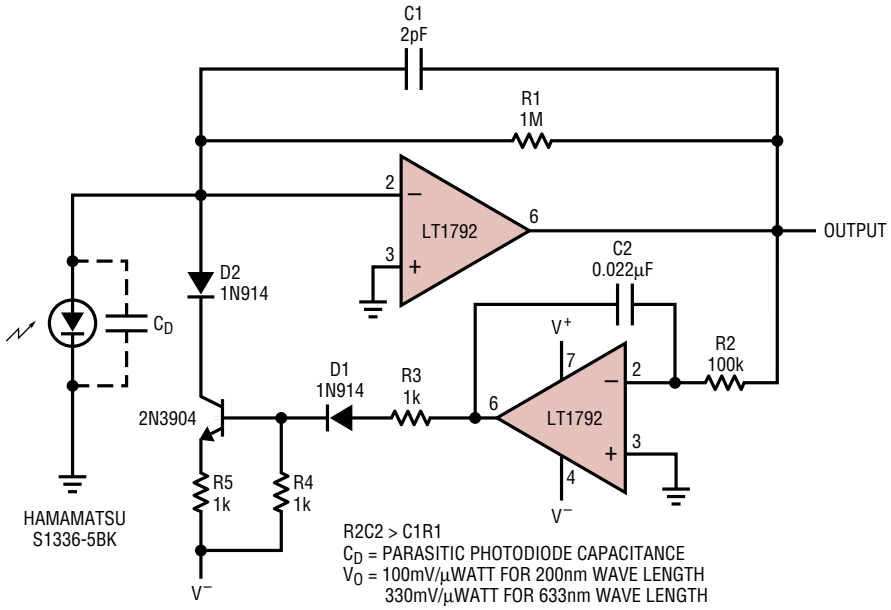
10Hz Fourth Order Chebyshev Lowpass Filter (0.01dB Ripple)



TYPICAL OFFSET ≈ 0.8mV
1% TOLERANCES
FOR V_{IN} = 10V_{P-P}, V_{OUT} = –121dB AT f > 330Hz
= – 6dB AT f = 16.3Hz
LOWER RESISTOR VALUES WILL RESULT IN LOWER THERMAL NOISE AND LARGER CAPACITORS

TYPICAL APPLICATIONS

Low Noise Light Sensor with DC Servo



Paralleling Amplifiers to Reduce Voltage Noise