

Dual/Quad 80MHz, 25V/ μ s Low Power Rail-to-Rail Input and Output Precision Op Amps

FEATURES

- **Gain Bandwidth Product: 80MHz**
- **Input Common Mode Range Includes Both Rails**
- **Output Swings Rail-to-Rail**
- **Low Voltage Operation: Single or Split Supplies 2.3V to 12.6V**
- **Low Quiescent Current: 2mA/Amplifier Max**
- **Input Offset Voltage: 350 μ V Max**
- **Input Bias Current: 250nA Max**
- 3mm \times 3mm \times 0.8mm DFN Package
- Large Output Current: 50mA Typ
- Low Voltage Noise: 8.5nV/ $\sqrt{\text{Hz}}$ Typ
- Slew Rate: 25V/ μ s Typ
- Common Mode Rejection: 105dB Typ
- Power Supply Rejection: 97dB Typ
- Open-Loop Gain: 85V/mV Typ
- Operating Temperature Range: -40°C to 85°C
- LT1801 is Available in 8-Lead SO, MS8 and DFN Packages
- LT1802 is Available in 14-Lead SO Package

APPLICATIONS

- Low Voltage, High Frequency Signal Processing
- Driving A/D Converters
- Rail-to-Rail Buffer Amplifiers
- Active Filters
- Video Line Driver

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DESCRIPTION

The LT[®]1801/LT1802 are dual/quad, low power, high speed rail-to-rail input and output operational amplifiers with excellent DC performance. The LT1801/LT1802 feature reduced supply current, lower input offset voltage, lower input bias current and higher DC gain than other devices with comparable bandwidth.

Typically, the LT1801/LT1802 have an input offset voltage of less than 100 μ V, an input bias current of less than 50nA and an open-loop gain of 85 thousand.

The LT1801/LT1802 have an input range that includes both supply rails and an output that swings within 20mV of either supply rail to maximize the signal dynamic range in low supply applications.

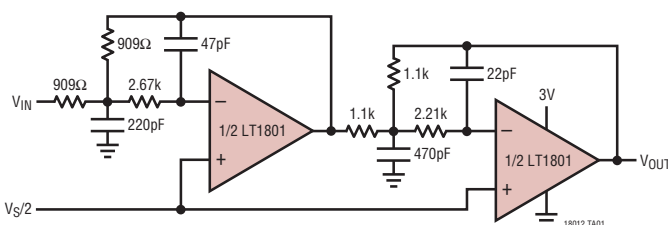
The LT1801/LT1802 maintain their performance for supplies from 2.3V to 12.6V and are specified at 3V, 5V and ± 5 V supplies. The inputs can be driven beyond the supplies without damage or phase reversal of the output.

The LT1801 is available in the MS8, SO-8 and the 3mm \times 3mm \times 0.8mm dual fine pitch leadless package (DFN) with the standard dual op amp pinout. The LT1802 features the standard quad op amp configuration and is available in the 14-pin plastic SO package. The LT1801/LT1802 can be used as plug-in replacements for many op amps to improve input/output range and performance.

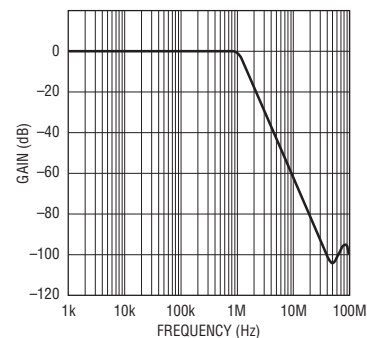
For a single version of these amplifiers, see the LT1800 data sheet.

TYPICAL APPLICATION

3V, 1MHz, 4th Order Butterworth Filter



1MHz Filter Frequency Response



LT1801/LT1802

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V_S^- to V_S^+)	12.6V	Storage Temperature Range	-65°C to 150°C
Input Current (Note 2)	±10mA	Maximum Junction Temperature (DD Package)....	125°C
Output Short-Circuit Duration (Note 3)	Indefinite	Storage Temperature (DD Package)	-65°C to 125°C
Operating Temperature Range (Note 4) ..	-40°C to 85°C	Lead Temperature MSOP, SOIC	
Specified Temperature Range (Note 5)	-40°C to 85°C	(Soldering, 10 sec).....	300°C
Junction Temperature	150°C		

PIN CONFIGURATION

<p>DD PACKAGE 8-LEAD (3mm x 3mm) PLASTIC DFN $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 160^{\circ}\text{C/W}$, (Note 10) EXPOSED PAD INTERNALLY CONNECTED TO V^-. (PCB CONNECTION OPTIONAL)</p>	<p>MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 250^{\circ}\text{C/W}$, (Note 10)</p>
<p>S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 190^{\circ}\text{C/W}$, (Note 10)</p>	<p>S PACKAGE 14-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 160^{\circ}\text{C/W}$, (Note 10)</p>

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	OPERATING TEMPERATURE RANGE
LT1801CDD#PBF	LT1801CDD#TRPBF	LAAM	8-Lead (3mm x 3mm) Plastic DFN	-40°C to 85°C
LT1801IDD#PBF	LT1801IDD#TRPBF	LAAM	8-Lead (3mm x 3mm) Plastic DFN	-40°C to 85°C
LT1801CMS8#PBF	LT1801CMS8#TRPBF	LYR	8-Lead Plastic MSOP	-40°C to 85°C
LT1801IMS8#PBF	LT1801IMS8#TRPBF	LYS	8-Lead Plastic MSOP	-40°C to 85°C
LT1801CS8#PBF	LT1801CS8#TRPBF	1801	8-Lead Plastic SO	-40°C to 85°C
LT1801IS8#PBF	LT1801IS8#TRPBF	1801I	8-Lead Plastic SO	-40°C to 85°C
LT1802CS#PBF	LT1802CS#TRPBF	LT1802CS	14-Lead Plastic SO	-40°C to 85°C
LT1802IS#PBF	LT1802IS#TRPBF	LT1802IS	14-Lead Plastic SO	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}, 0\text{V}$; $V_S = 3\text{V}, 0\text{V}$; $V_{CM} = V_{OUT} = \text{half supply}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = 0\text{V}$		75	350	μV
		$V_{CM} = 0\text{V}$ (MS8)		140	500	μV
		$V_{CM} = 0\text{V}$ (DD)		175	800	μV
		$V_{CM} = V_S$		0.5	3	mV
ΔV_{OS}	Input Offset Shift	$V_{CM} = 0\text{V}$ to $V_S - 1.5\text{V}$		20	185	μV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	$V_{CM} = 0\text{V}$		100	650	μV
		$V_{CM} = 0\text{V}$ (MS8)		150	900	μV
		$V_{CM} = 0\text{V}$ (DD)		280	1200	μV
I_B	Input Bias Current	$V_{CM} = 1\text{V}$		25	250	nA
		$V_{CM} = V_S$		500	1500	nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	$V_{CM} = 1\text{V}$		25	350	nA
		$V_{CM} = V_S$		25	500	nA
I_{OS}	Input Offset Current	$V_{CM} = 1\text{V}$		25	200	nA
		$V_{CM} = V_S$		25	200	nA
	Input Noise Voltage	0.1Hz to 10Hz		1.4		μV_{P-P}
e_n	Input Noise Voltage Density	$f = 10\text{kHz}$		8.5		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 10\text{kHz}$		1		$\text{pA}/\sqrt{\text{Hz}}$
C_{IN}	Input Capacitance			2		pF
A_{VOL}	Large-Signal Voltage Gain	$V_S = 5\text{V}, V_O = 0.5\text{V}$ to $4.5\text{V}, R_L = 1\text{k}$ at $V_S/2$	35	85		V/mV
		$V_S = 5\text{V}, V_O = 1\text{V}$ to $4\text{V}, R_L = 100\Omega$ at $V_S/2$	3.5	8		V/mV
		$V_S = 3\text{V}, V_O = 0.5\text{V}$ to $2.5\text{V}, R_L = 1\text{k}$ at $V_S/2$	30	85		V/mV
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}, V_{CM} = 0\text{V}$ to 3.5V	85	105		dB
		$V_S = 3\text{V}, V_{CM} = 0\text{V}$ to 1.5V	78	97		dB
	CMRR Match (Channel-to-Channel) (Note 9)	$V_S = 5\text{V}, V_{CM} = 0\text{V}$ to 3.5V	79	105		dB
		$V_S = 3\text{V}, V_{CM} = 0\text{V}$ to 1.5V	72	97		dB
	Input Common Mode Range		0		V_S	V
PSRR	Power Supply Rejection Ratio	$V_S = 2.5\text{V}$ to $10\text{V}, V_{CM} = 0\text{V}$	78	97		dB
		$V_S = 2.5\text{V}$ to $10\text{V}, V_{CM} = 0\text{V}$	72	97		dB
	Minimum Supply Voltage (Note 6)			2.3	2.5	V
V_{OL}	Output Voltage Swing Low (Note 7)	No Load		16	60	mV
		$I_{SINK} = 5\text{mA}$		85	200	mV
		$I_{SINK} = 20\text{mA}$		225	500	mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load		18	60	mV
		$I_{SOURCE} = 5\text{mA}$		120	250	mV
		$I_{SOURCE} = 20\text{mA}$		450	800	mV
I_{SC}	Short-Circuit Current	$V_S = 5\text{V}$	20	45		mA
		$V_S = 3\text{V}$	20	40		mA
I_S	Supply Current per Amplifier			1.6	2	mA
GBW	Gain Bandwidth Product	Frequency = 2MHz	40	80		MHz
SR	Slew Rate	$V_S = 5\text{V}, A_V = -1, R_L = 1\text{k}, V_O = 1\text{V}$ to 4V	12.5	25		V/ μs
FPBW	Full Power Bandwidth	$V_S = 5\text{V}, A_V = 1, V_O = 4\text{V}_{P-P}$		2		MHz
HD	Harmonic Distortion	$V_S = 5\text{V}, A_V = 1, R_L = 1\text{k}, V_O = 2\text{V}_{P-P}, f_C = 500\text{kHz}$		-75		dBc
t_S	Settling Time	0.01%, $V_S = 5\text{V}, V_{STEP} = 2\text{V}, A_V = 1, R_L = 1\text{k}$		250		ns
ΔG	Differential Gain (NTSC)	$V_S = 5\text{V}, A_V = 2, R_L = 150\Omega$		0.35		%
$\Delta\theta$	Differential Phase (NTSC)	$V_S = 5\text{V}, A_V = 2, R_L = 150\Omega$		0.4		Deg

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ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the temperature range of $0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$. $V_S = 5\text{V}, 0\text{V}$; $V_S = 3\text{V}, 0\text{V}$; $V_{\text{CM}} = V_{\text{OUT}} = \text{half supply}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{\text{CM}} = 0\text{V}$	●		125	500	μV
		$V_{\text{CM}} = 0\text{V}$ (MS8)	●		140	650	μV
		$V_{\text{CM}} = 0\text{V}$ (DD)	●		290	950	μV
		$V_{\text{CM}} = V_S$	●		0.6	3.5	mV
ΔV_{OS}	Input Offset Shift	$V_{\text{CM}} = 0\text{V}$ to $V_S - 1.5\text{V}$	●		30	275	μV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	$V_{\text{CM}} = 0\text{V}$	●		200	850	μV
		$V_{\text{CM}} = 0\text{V}$ (MS8)	●		200	1250	μV
		$V_{\text{CM}} = 0\text{V}$ (DD)	●		275	1500	μV
$V_{\text{OS TC}}$	Input Offset Voltage Drift (Note 8)		●		1.5	5	$\mu\text{V}/^{\circ}\text{C}$
I_B	Input Bias Current	$V_{\text{CM}} = 1\text{V}$	●		50	300	nA
		$V_{\text{CM}} = V_S - 0.2\text{V}$	●		550	2000	nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	$V_{\text{CM}} = 1\text{V}$	●		25	400	nA
		$V_{\text{CM}} = V_S - 0.2\text{V}$	●		25	600	nA
I_{OS}	Input Offset Current	$V_{\text{CM}} = 1\text{V}$	●		25	300	nA
		$V_{\text{CM}} = V_S - 0.2\text{V}$	●		25	300	nA
A_{VOL}	Large-Signal Voltage Gain	$V_S = 5\text{V}, V_0 = 0.5\text{V}$ to $4.5\text{V}, R_L = 1\text{k}$ at $V_S/2$	●	25	75		V/mV
		$V_S = 5\text{V}, V_0 = 1\text{V}$ to $4\text{V}, R_L = 100\Omega$ at $V_S/2$	●	2.5	6		V/mV
		$V_S = 3\text{V}, V_0 = 0.5\text{V}$ to $2.5\text{V}, R_L = 1\text{k}$ at $V_S/2$	●	20	75		V/mV
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}, V_{\text{CM}} = 0\text{V}$ to 3.5V	●	82	101		dB
		$V_S = 3\text{V}, V_{\text{CM}} = 0\text{V}$ to 1.5V	●	74	93		dB
	CMRR Match (Channel-to-Channel) (Note 9)	$V_S = 5\text{V}, V_{\text{CM}} = 0\text{V}$ to 3.5V	●	76	101		dB
		$V_S = 3\text{V}, V_{\text{CM}} = 0\text{V}$ to 1.5V	●	68	93		dB
	Input Common Mode Range		●	0		V_S	V
PSRR	Power Supply Rejection Ratio	$V_S = 2.5\text{V}$ to $10\text{V}, V_{\text{CM}} = 0\text{V}$	●	74	91		dB
		PSRR Match (Channel-to-Channel) (Note 9)	●	68	91		dB
	Minimum Supply Voltage (Note 6)		●		2.3	2.5	V
V_{OL}	Output Voltage Swing Low (Note 7)	No Load	●		18	80	mV
		$I_{\text{SINK}} = 5\text{mA}$	●		100	225	mV
		$I_{\text{SINK}} = 20\text{mA}$	●		300	600	mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load	●		25	80	mV
		$I_{\text{SOURCE}} = 5\text{mA}$	●		150	300	mV
		$I_{\text{SOURCE}} = 20\text{mA}$	●		600	950	mV
I_{SC}	Short-Circuit Current	$V_S = 5\text{V}$	●	20	40		mA
		$V_S = 3\text{V}$	●	15	30		mA
I_S	Supply Current per Amplifier		●		2	2.8	mA
GBW	Gain Bandwidth Product	Frequency = 2MHz	●	35	75		MHz
SR	Slew Rate	$V_S = 5\text{V}, A_V = -1, R_L = 1\text{k}, V_0 = 1\text{V}$ to 4V	●	11	22		V/ μs

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the temperature range of $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$. $V_S = 5\text{V}, 0\text{V}$; $V_S = 3\text{V}, 0\text{V}$; $V_{CM} = V_{OUT} = \text{half supply}$, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = 0\text{V}$	●	175	700	μV
		$V_{CM} = 0\text{V}$ (MS8)	●	200	850	μV
		$V_{CM} = 0\text{V}$ (DD)	●	320	1150	μV
		$V_{CM} = V_S$	●	0.75	4	mV
ΔV_{OS}	Input Offset Shift	$V_{CM} = 0\text{V}$ to $V_S - 1.5\text{V}$	●	30	300	μV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	$V_{CM} = 0\text{V}$	●	200	1250	μV
		$V_{CM} = 0\text{V}$ (MS8)	●	280	1600	μV
		$V_{CM} = 0\text{V}$ (DD)	●	320	1800	μV
$V_{OS\ TC}$	Input Offset Voltage Drift (Note 8)		●	1.5	5	$\mu\text{V}/^{\circ}\text{C}$
I_B	Input Bias Current	$V_{CM} = V_S - 0.2\text{V}$	●	50	400	nA
			●	600	2250	nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	$V_{CM} = 1\text{V}$	●	25	450	nA
		$V_{CM} = V_S - 0.2\text{V}$	●	25	700	nA
I_{OS}	Input Offset Current	$V_{CM} = 1\text{V}$	●	25	350	nA
		$V_{CM} = V_S - 0.2\text{V}$	●	25	350	nA
A_{VOL}	Large-Signal Voltage Gain	$V_S = 5\text{V}, V_O = 0.5\text{V}$ to $4.5\text{V}, R_L = 1\text{k}$ at $V_S/2$	●	20	65	V/mV
		$V_S = 5\text{V}, V_O = 1.5\text{V}$ to $3.5\text{V}, R_L = 100\Omega$ at $V_S/2$	●	2	6	V/mV
		$V_S = 3\text{V}, V_O = 0.5\text{V}$ to $2.5\text{V}, R_L = 1\text{k}$ at $V_S/2$	●	17.5	65	V/mV
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}, V_{CM} = 0\text{V}$ to 3.5V	●	81	101	dB
		$V_S = 3\text{V}, V_{CM} = 0\text{V}$ to 1.5V	●	73	93	dB
	CMRR Match (Channel-to-Channel) (Note 9)	$V_S = 5\text{V}, V_{CM} = 0\text{V}$ to 3.5V	●	75	101	dB
		$V_S = 3\text{V}, V_{CM} = 0\text{V}$ to 1.5V	●	67	93	dB
	Input Common Mode Range		●	0	V_S	V
PSRR	Power Supply Rejection Ratio	$V_S = 2.5\text{V}$ to $10\text{V}, V_{CM} = 0\text{V}$	●	73	90	dB
			●	67	90	dB
	PSRR Match (Channel-to-Channel) (Note 9)	$V_S = 2.5\text{V}$ to $10\text{V}, V_{CM} = 0\text{V}$	●	67	90	dB
	Minimum Supply Voltage (Note 6)	$V_{CM} = V_O = 0.5\text{V}$	●	2.3	2.5	V
V_{OL}	Output Voltage Swing Low (Note 7)	No Load	●	15	90	mV
		$I_{SINK} = 5\text{mA}$	●	105	250	mV
		$I_{SINK} = 10\text{mA}$	●	170	400	mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load	●	25	90	mV
		$I_{SOURCE} = 5\text{mA}$	●	150	350	mV
		$I_{SOURCE} = 10\text{mA}$	●	300	700	mV
I_{SC}	Short-Circuit Current	$V_S = 5\text{V}$	●	12.5	30	mA
		$V_S = 3\text{V}$	●	12.5	30	mA
I_S	Supply Current per Amplifier		●	2.1	3	mA
GBW	Gain Bandwidth Product	Frequency = 2MHz	●	25	70	MHz
SR	Slew Rate	$V_S = 5\text{V}, A_V = -1, R_L = 1\text{k}, V_O = 1\text{V}$ to 4V	●	9	18	V/ μs

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ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $V_{CM} = 0\text{V}$, $V_{OUT} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V_S^-$		150	600	μV
		$V_{CM} = V_S^-$ (MS8)		180	750	μV
		$V_{CM} = V_S^-$ (DD)		260	1050	μV
		$V_{CM} = V_S^+$		0.7	3.5	mV
ΔV_{OS}	Input Offset Shift	$V_{CM} = V_S^-$ to $V_S^+ - 1.5\text{V}$		30	475	μV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	$V_{CM} = V_S^-$		150	1000	μV
		$V_{CM} = V_S^-$ (MS8)		275	1300	μV
		$V_{CM} = V_S^-$ (DD)		325	1600	μV
I_B	Input Bias Current	$V_{CM} = V_S^- + 1\text{V}$		25	250	nA
		$V_{CM} = V_S^+$		400	1500	nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	$V_{CM} = V_S^- + 1\text{V}$		20	350	nA
		$V_{CM} = V_S^+$		20	500	nA
I_{OS}	Input Offset Current	$V_{CM} = V_S^- + 1\text{V}$		20	250	nA
		$V_{CM} = V_S^+$		20	250	nA
	Input Noise Voltage	0.1Hz to 10Hz		1.4		$\mu\text{V}/\text{p-p}$
e_n	Input Noise Voltage Density	$f = 10\text{kHz}$		8.5		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 10\text{kHz}$		1		$\text{pA}/\sqrt{\text{Hz}}$
C_{IN}	Input Capacitance	$f = 100\text{kHz}$		2		pF
A_{VOL}	Large-Signal Voltage Gain	$V_O = -4\text{V}$ to 4V , $R_L = 1\text{k}$	25	70		V/mV
		$V_O = -2\text{V}$ to 2V , $R_L = 100\Omega$	2.5	7		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = V_S^-$ to 3.5V	85	109		dB
		CMRR Match (Channel-to-Channel) (Note 9)	79	109		dB
		Input Common Mode Range		V_S^-	V_S^+	
PSRR	Power Supply Rejection Ratio	$V_S^+ = 2.5\text{V}$ to 10V , $V_S^- = 0\text{V}$	78	97		dB
		PSRR Match (Channel-to-Channel) (Note 9)	72	97		dB
V_{OL}	Output Voltage Swing Low (Note 7)	No Load		15	70	mV
		$I_{SINK} = 5\text{mA}$		90	200	mV
		$I_{SINK} = 20\text{mA}$		225	500	mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load		20	80	mV
		$I_{SOURCE} = 5\text{mA}$		130	260	mV
		$I_{SOURCE} = 20\text{mA}$		450	850	mV
I_{SC}	Short-Circuit Current		25	50		mA
I_S	Supply Current per Amplifier			1.8	3	mA
GBW	Gain Bandwidth Product	Frequency = 2MHz		70		MHz
FPBW	Full Power Bandwidth	$V_O = 8\text{V}_{\text{p-p}}$		0.9		MHz
SR	Slew Rate	$A_V = -1$, $R_L = 1\text{k}$, $V_O = \pm 4\text{V}$, Measured at $V_O = \pm 2\text{V}$		20		V/ μs
HD	Harmonic Distortion	$A_V = 1$, $R_L = 1\text{k}$, $V_O = 2\text{V}_{\text{p-p}}$, $f_C = 500\text{kHz}$		-75		dBc
t_S	Settling Time	0.01%, $V_{STEP} = 5\text{V}$, $A_V = 1\text{V}$, $R_L = 1\text{k}$		300		ns
ΔG	Differential Gain (NTSC)	$A_V = 2$, $R_L = 150\Omega$		0.35		%
$\Delta\theta$	Differential Phase (NTSC)	$A_V = 2$, $R_L = 150\Omega$		0.2		deg

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the temperature range of 0°C < T_A < 70°C. V_S = ±5V, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	V _{CM} = V _S ⁻	●	200	800	μV
		V _{CM} = V _S ⁻ (MS8)	●	220	1000	μV
		V _{CM} = V _S ⁻ (DD)	●	290	1300	μV
		V _{CM} = V _S ⁺	●	0.75	4	mV
ΔV _{OS}	Input Offset Shift	V _{CM} = V _S ⁻ to V _S ⁺ - 1.5V	●	45	675	μV
V _{OS} TC	Input Offset Voltage Drift (Note 8)	V _{CM} = V _S ⁻	●	1.5	5	μV/°C
		V _{CM} = V _S ⁻ (MS8)	●	240	1500	μV
		V _{CM} = V _S ⁻ (DD)	●	300	1700	μV
I _B	Input Bias Current	V _{CM} = V _S ⁻ + 1V	●	30	300	nA
		V _{CM} = V _S ⁺ - 0.2V	●	450	2000	nA
I _{OS}	Input Bias Current Match (Channel-to-Channel) (Note 9)	V _{CM} = V _S ⁻ + 1V	●	25	400	nA
		V _{CM} = V _S ⁺ - 0.2V	●	25	700	nA
I _{OS}	Input Offset Current	V _{CM} = V _S ⁻ + 1V	●	25	300	nA
		V _{CM} = V _S ⁺ - 0.2V	●	25	300	nA
A _{VOL}	Large-Signal Voltage Gain	V _O = -4V to 4V, R _L = 1k	●	15	55	V/mV
		V _O = -2V to 2V, R _L = 100Ω	●	2	5	V/mV
CMRR	Common Mode Rejection Ratio	V _{CM} = V _S ⁻ to 3.5V	●	82	105	dB
		CMRR Match (Channel-to-Channel) (Note 9)	●	76	105	dB
		Input Common Mode Range	●	V _S ⁻	V _S ⁺	V
PSRR	Power Supply Rejection Ratio	V _S ⁺ = 2.5V to 10V, V _S ⁻ = 0V	●	74	91	dB
		V _S ⁺ = 2.5V to 10V, V _S ⁻ = 0V	●	68	93	dB
V _{OL}	Output Voltage Swing Low (Note 7)	No Load	●	17	80	mV
		I _{SINK} = 5mA	●	105	250	mV
		I _{SINK} = 20mA	●	250	575	mV
V _{OH}	Output Voltage Swing High (Note 7)	No Load	●	25	90	mV
		I _{SOURCE} = 5mA	●	150	310	mV
		I _{SOURCE} = 20mA	●	600	975	mV
I _{SC}	Short-Circuit Current		●	22.5	45	mA
I _S	Supply Current per Amplifier		●	2.4	4	mA
GBW	Gain Bandwidth Product	Frequency = 2MHz	●	70		MHz
SR	Slew Rate	A _V = -1, R _L = 1k, V _O = ±4V, Measured at V _O = ±2V	●	20		V/μs

The ● denotes the specifications which apply over the temperature range of -40°C < T_A < 85°C. V_S = ±5V, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	V _{CM} = V _S ⁻	●	350	1000	μV
		V _{CM} = V _S ⁻ (MS8)	●	350	1200	μV
		V _{CM} = V _S ⁻ (DD)	●	350	1500	μV
		V _{CM} = V _S ⁺	●	0.75	5	mV
ΔV _{OS}	Input Offset Shift	V _{CM} = V _S ⁻ to V _S ⁺ - 1.5V	●	50	750	μV
V _{OS} TC	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V _{CM} = V _S ⁻	●	280	1700	μV
		V _{CM} = V _S ⁻ (MS8)	●	380	1900	μV
		V _{CM} = V _S ⁻ (DD)	●	410	2100	μV

LT1801/LT1802

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range of $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$. $V_S = \pm 5\text{V}$, $V_{\text{CM}} = 0\text{V}$, $V_{\text{OUT}} = 0\text{V}$, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{\text{OS TC}}$	Input Offset Voltage Drift (Note 8)		●	1.5	5	$\mu\text{V}/^{\circ}\text{C}$
I_B	Input Bias Current	$V_{\text{CM}} = V_S^- + 1\text{V}$	●	50	400	nA
		$V_{\text{CM}} = V_S^+ - 0.2\text{V}$	●	450	2250	nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	$V_{\text{CM}} = V_S^- + 1\text{V}$	●	25	450	nA
		$V_{\text{CM}} = V_S^+ - 0.2\text{V}$	●	25	700	nA
I_{OS}	Input Offset Current	$V_{\text{CM}} = V_S^- + 1\text{V}$	●	25	350	nA
		$V_{\text{CM}} = V_S^+ - 0.2\text{V}$	●	25	350	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = -4\text{V to } 4\text{V}, R_L = 1\text{k}$	●	12.5	55	V/mV
		$V_O = -1\text{V to } 1\text{V}, R_L = 100\Omega$	●	2	5	V/mV
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = V_S^- \text{ to } 3.5\text{V}$	●	81	104	dB
	CMRR Match (Channel-to-Channel) (Note 9)	$V_{\text{CM}} = V_S^- \text{ to } 3.5\text{V}$	●	75	104	dB
	Input Common Mode Range		●	V_S^-	V_S^+	V
PSRR	Power Supply Rejection Ratio	$V_S^+ = 2.5\text{V to } 10\text{V}, V_S^- = 0\text{V}$	●	73	90	dB
	PSRR Match (Channel-to-Channel) (Note 9)	$V_S^+ = 2.5\text{V to } 10\text{V}, V_S^- = 0\text{V}$	●	67	90	dB
V_{OL}	Output Voltage Swing Low (Note 7)	No Load	●	20	100	mV
		$I_{\text{SINK}} = 5\text{mA}$	●	110	275	mV
		$I_{\text{SINK}} = 10\text{mA}$	●	180	400	mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load	●	30	110	mV
		$I_{\text{SOURCE}} = 5\text{mA}$	●	150	350	mV
		$I_{\text{SOURCE}} = 10\text{mA}$	●	300	700	mV
I_{SC}	Short-Circuit Current		●	12.5	30	mA
I_S	Supply Current per Amplifier		●	2.6	4.5	mA
GBW	Gain Bandwidth Product	Frequency = 2MHz	●	65		MHz
SR	Slew Rate	$A_V = -1, R_L = 1\text{k}, V_O = \pm 4\text{V}$, Measured at $V_O = \pm 2\text{V}$	●	15		V/ μs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA. It is not 100% tested.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LT1801C/LT1801I and LT1802C/LT1802I are guaranteed functional over the temperature range of -40°C to 85°C .

Note 5: The LT1801C/LT1802C are guaranteed to meet specified performance from 0°C to 70°C . The LT1801C/LT1802C are designed, characterized and expected to meet specified performance from -40°C to 85°C but are not tested or QA sampled at these temperatures. The LT1801I/LT1802I are guaranteed to meet specified performance from -40°C to 85°C .

Note 6: Minimum supply voltage is guaranteed by power supply rejection ratio test.

Note 7: Output voltage swings are measured between the output and power supply rails.

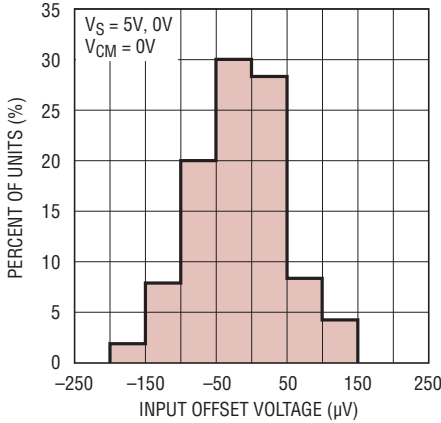
Note 8: This parameter is not 100% tested.

Note 9: Matching parameters are the difference between amplifiers A and D and between B and C on the LT1802; between the two amplifiers on the LT1801.

Note 10: Thermal resistance (θ_{JA}) varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads. If desired, the thermal resistance can be substantially reduced by connecting Pin 4 of the SO-8 and MS8, Pin 11 of the SO-14 or the underside metal of the DD package to a larger metal area (V_S^- trace).

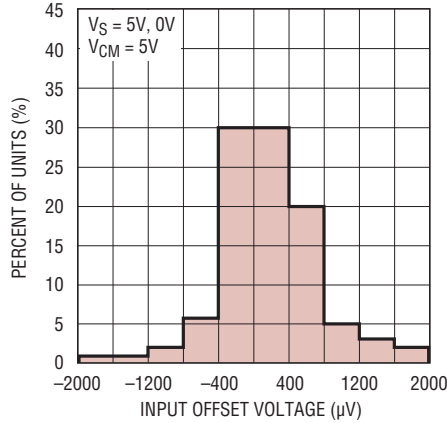
TYPICAL PERFORMANCE CHARACTERISTICS

V_{OS} Distribution, $V_{CM} = 0V$ (PNP Stage)



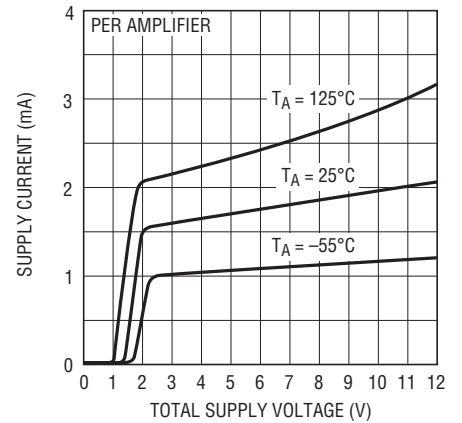
18012 G01

V_{OS} Distribution, $V_{CM} = 5V$ (NPN Stage)



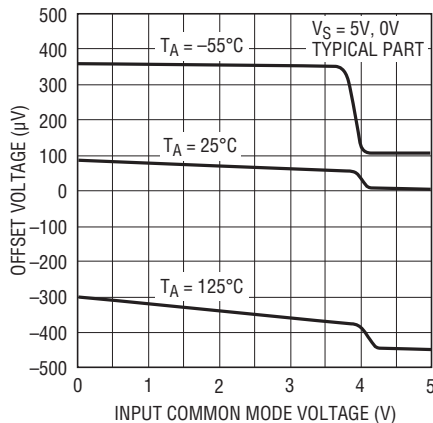
18012 G02

Supply Current vs Supply Voltage



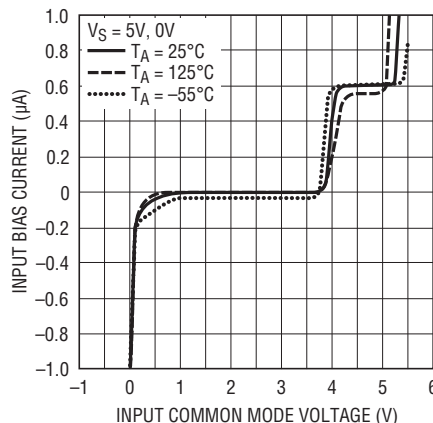
18012 G03

Offset Voltage vs Input Common Mode Voltage



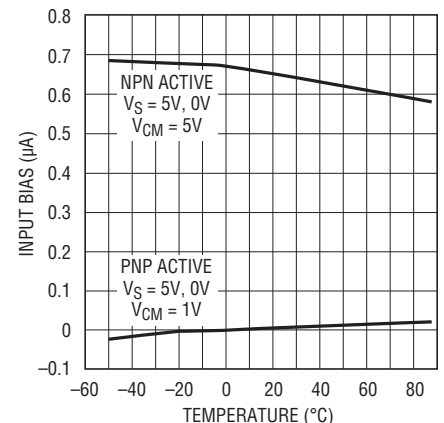
18012 G04

Input Bias Current vs Common Mode Voltage



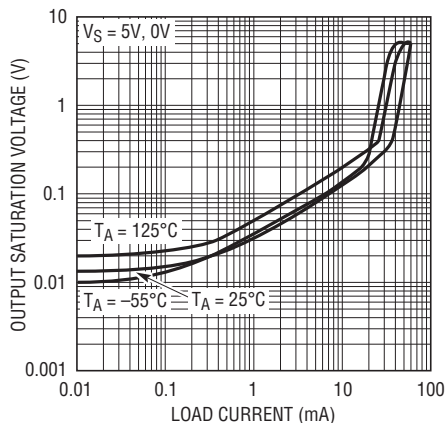
18012 G05

Input Bias Current vs Temperature



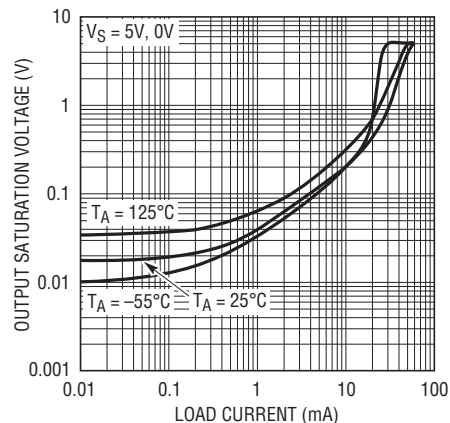
18012 G06

Output Saturation Voltage vs Load Current (Output Low)



18012 G07

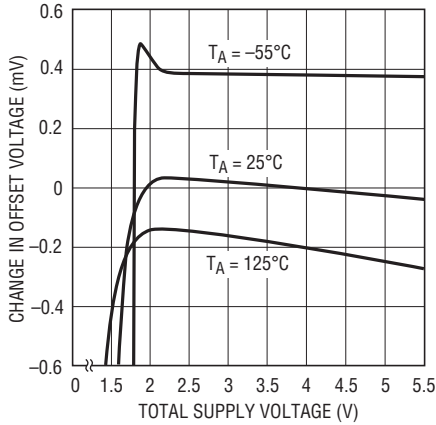
Output Saturation Voltage vs Load Current (Output High)



18012 G08

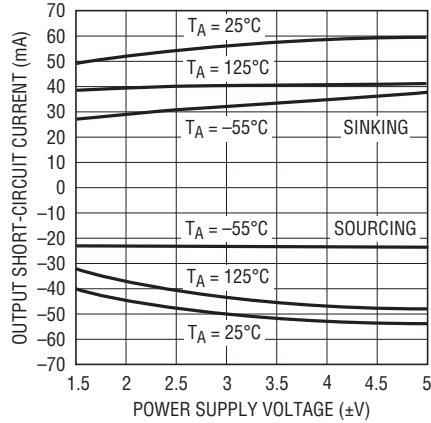
TYPICAL PERFORMANCE CHARACTERISTICS

Minimum Supply Voltage



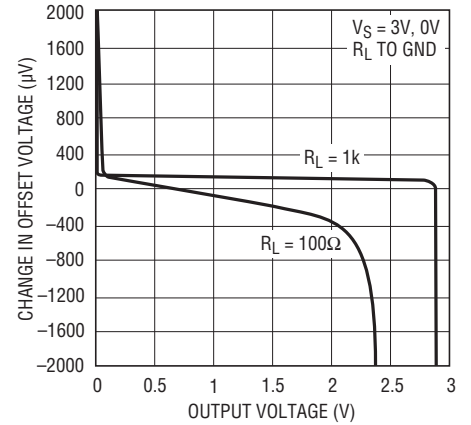
18012 G09

Output Short-Circuit Current vs Power Supply Voltage



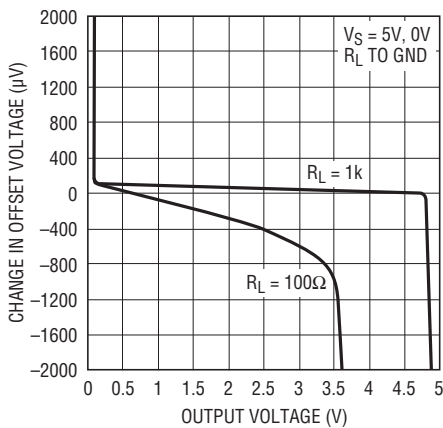
18012 G10

Open-Loop Gain



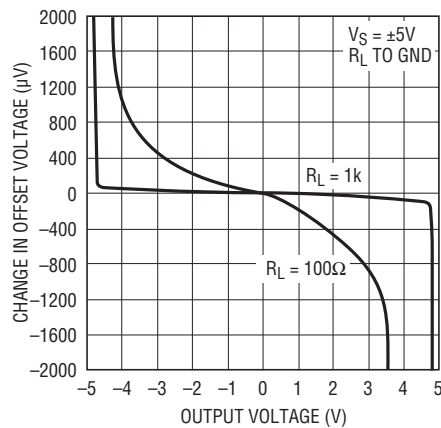
18012 G11

Open-Loop Gain



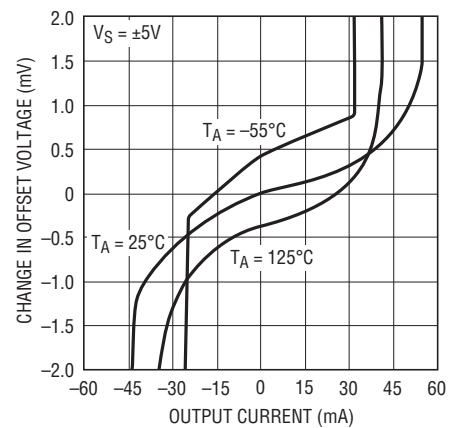
18012 G12

Open-Loop Gain



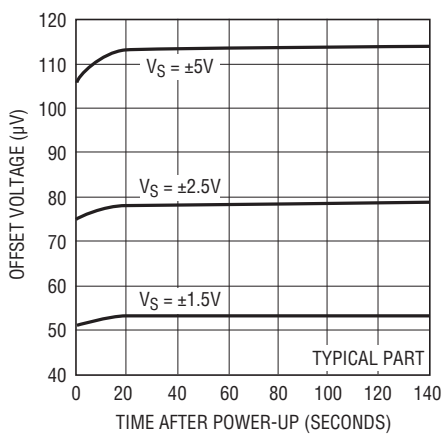
18012 G13

Offset Voltage vs Output Current



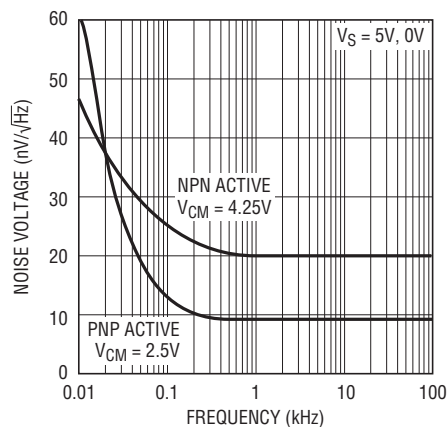
18012 G14

Warm-Up Drift vs Time



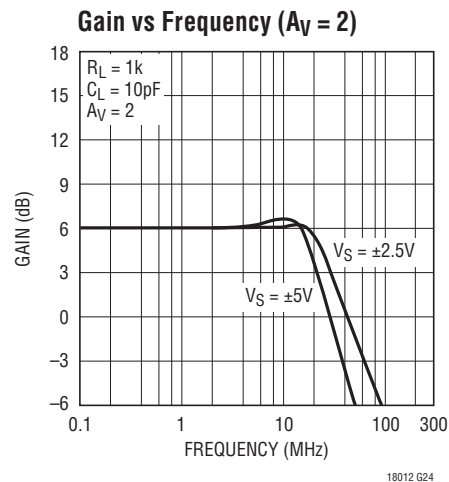
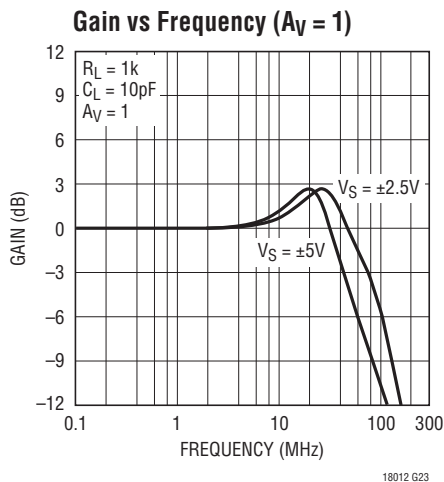
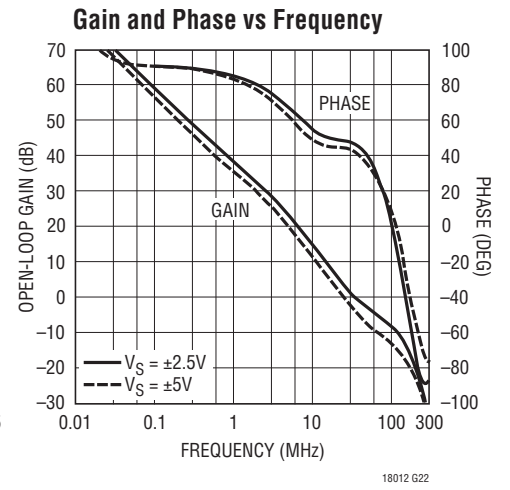
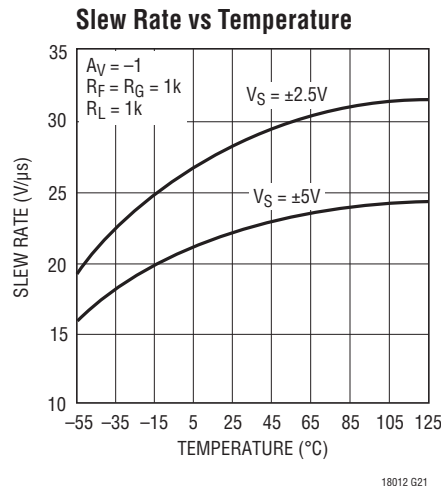
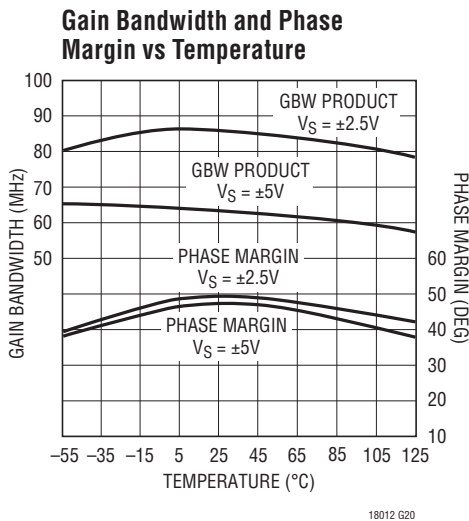
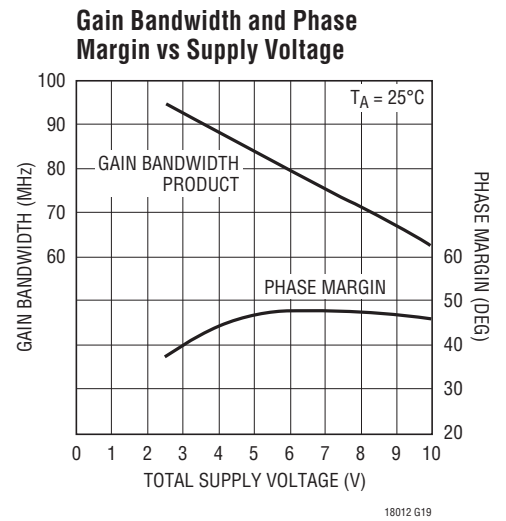
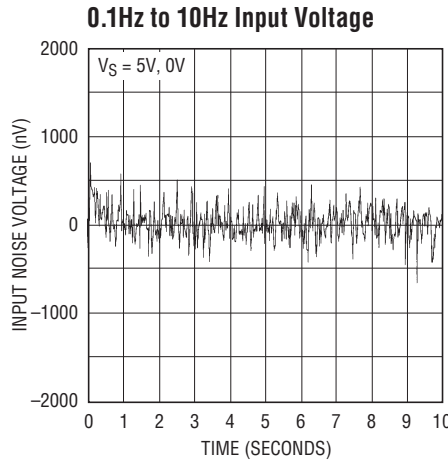
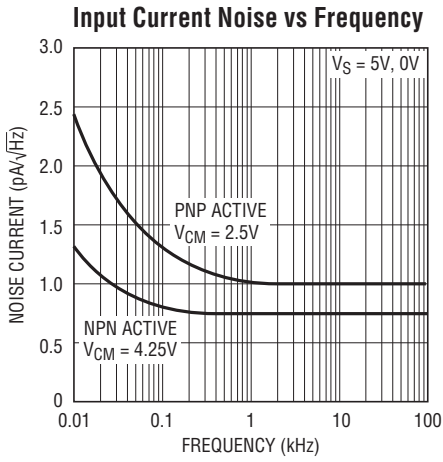
18012 G15

Input Noise Voltage vs Frequency



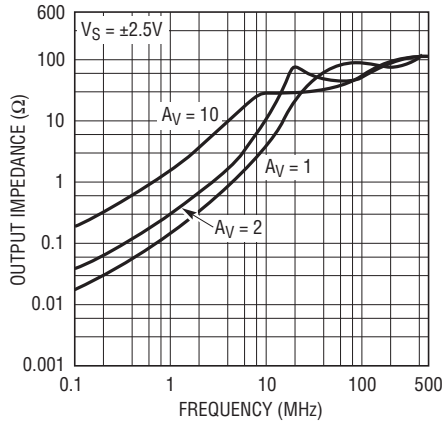
18012 G16

TYPICAL PERFORMANCE CHARACTERISTICS

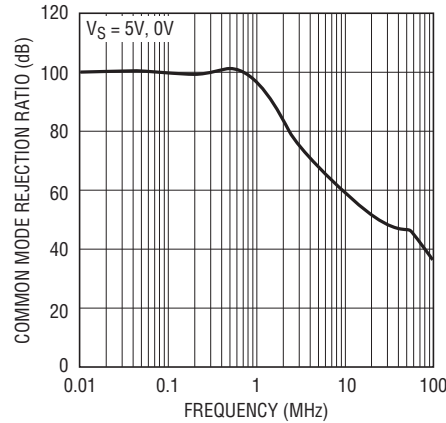


TYPICAL PERFORMANCE CHARACTERISTICS

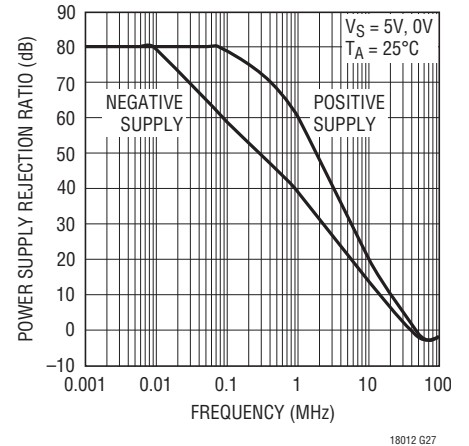
Output Impedance vs Frequency



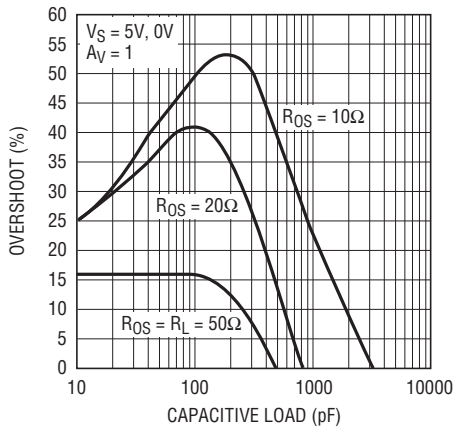
Common Mode Rejection Ratio vs Frequency



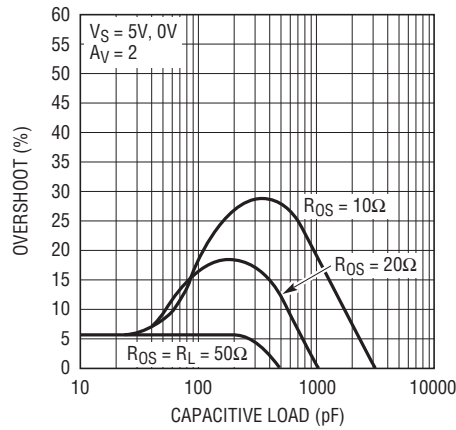
Power Supply Rejection Ratio vs Frequency



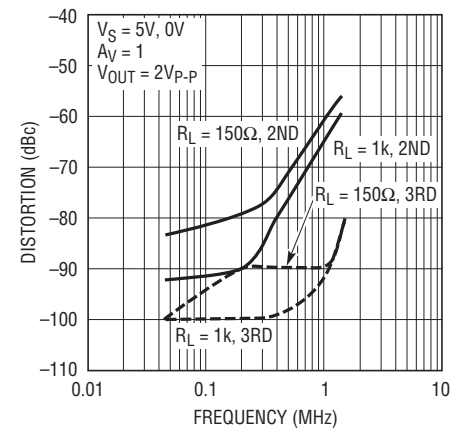
Series Output Resistor vs Capacitive Load



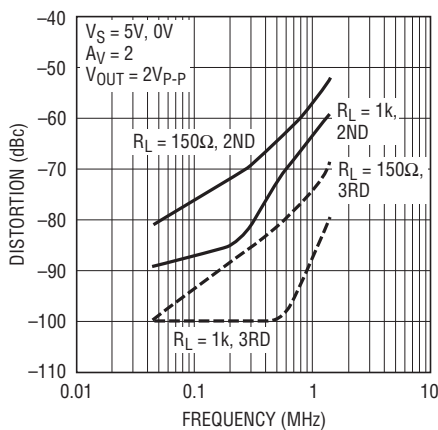
Series Output Resistor vs Capacitive Load



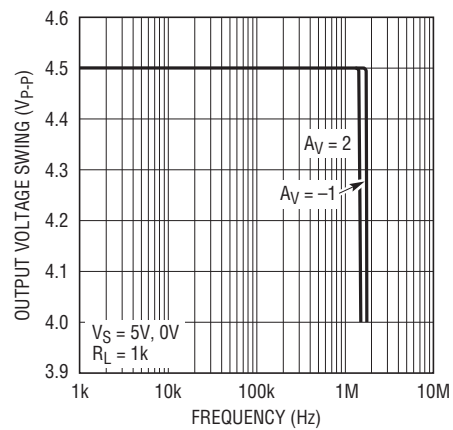
Distortion vs Frequency



Distortion vs Frequency

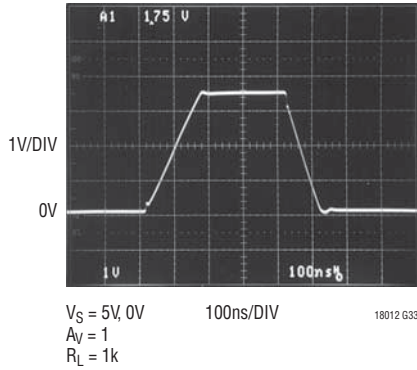


Maximum Undistorted Output Signal vs Frequency

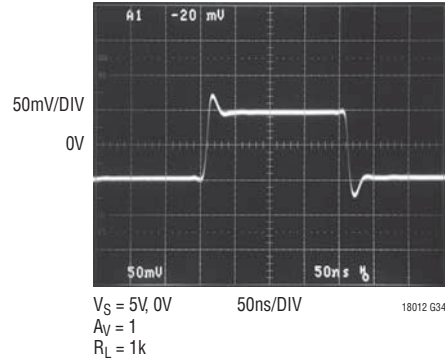


TYPICAL PERFORMANCE CHARACTERISTICS

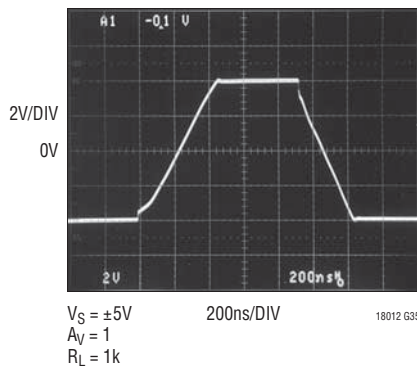
5V Large-Signal Response



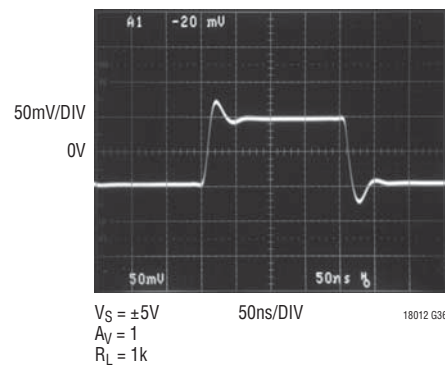
5V Small-Signal Response



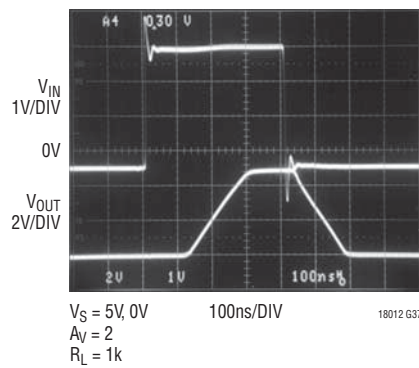
±5V Large-Signal Response



±5V Small-Signal Response



Output Overdriven Recovery



APPLICATIONS INFORMATION

Circuit Description

The LT1801/LT1802 have an input and output signal range that covers from the negative power supply to the positive power supply. Figure 1 depicts a simplified schematic of the amplifier. The input stage is comprised of two differential amplifiers, a PNP stage Q1/Q2 and an NPN stage Q3/Q4 that are active over the different ranges of common mode input voltage. The PNP differential pair is active between the negative supply to approximately 1.2V below the positive supply. As the input voltage moves closer toward the positive supply, the transistor Q5 will steer the tail current I_1 to the current mirror Q6/Q7, activating the NPN differential pair and the PNP pair becomes inactive for the rest of the input common mode range up to the positive supply. Also at the input stage, devices Q17 to Q19 act to cancel the bias current of the PNP input pair. When Q1-Q2 are active, the current in Q16 is controlled to be the same as the current in Q1-Q2, thus the base current of Q16 is nominally equal to the base current of the input devices. The base current of Q16 is then mirrored by devices Q17-Q19 to cancel the base current of the input devices Q1-Q2.

A pair of complementary common emitter stages Q14/Q15 that enable the output to swing from rail to rail constructs the output stage. The capacitors C2 and C3 form the local feedback loops that lower the output impedance at high frequency. These devices are fabricated on Linear Technology's proprietary high speed complementary bipolar process.

Power Dissipation

The LT1801 amplifier is offered in a small package, SO-8, which has a thermal resistance of $190^{\circ}\text{C}/\text{W}$, θ_{JA} . So there is a need to ensure that the die's junction temperature should not exceed 150°C . Junction temperature T_J is calculated from the ambient temperature T_A , power dissipation P_D and thermal resistance θ_{JA} :

$$T_J = T_A + (P_D \cdot \theta_{JA})$$

The power dissipation in the IC is the function of the supply voltage, output voltage and the load resistance. For a given supply voltage, the worst-case power dissipation $P_{D\text{MAX}}$ occurs at the maximum supply current and the

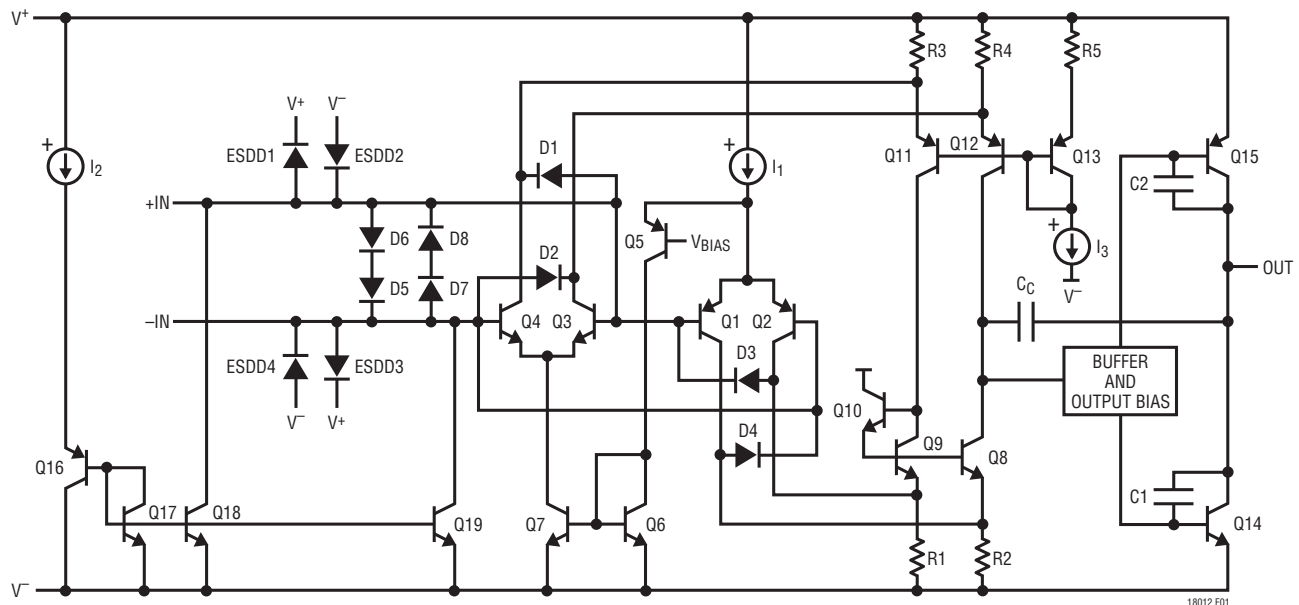


Figure 1. LT1801/LT1802 Simplified Schematic Diagram

APPLICATIONS INFORMATION

output voltage is at half of either supply voltage (or the maximum swing is less than 1/2 supply voltage). P_{DMAX} is given by:

$$P_{DMAX} = (V_S \cdot I_{SMAX}) + (V_S/2)^2/R_L$$

Example: An LT1801 in an SO-8 package operating on $\pm 5V$ supplies and driving a 50Ω load, the worst-case power dissipation is given by:

$$P_{DMAX} = (10 \cdot 4.5mA) + (2.5)^2/50 = 0.045 + 0.125 \\ = 0.17W$$

If both amplifiers are loaded simultaneously, then the total power dissipation is 0.34W.

The maximum ambient temperature that the part is allowed to operate is:

$$T_A = T_J - (P_{DMAX} \cdot 190^\circ C/W) \\ = 150^\circ C - (0.34W \cdot 190^\circ C/W) = 85^\circ C$$

Input Offset Voltage

The offset voltage will change depending upon which input stage is active. The PNP input stage is active from the negative supply rail to 1.2V from the positive supply rail, then the NPN input stage is activated for the remaining input range up to the positive supply rail during which the PNP stage remains inactive. The offset voltage is typically less than $75\mu V$ in the range that the PNP input stage is active.

Input Bias Current

The LT1801/LT1802 employ a patent-pending technique to trim the input bias current to less than 250nA for the input common mode voltage of 0.2V above negative supply rail to 1.2V of the positive rail. The low input offset voltage and low input bias current of the LT1801/LT1802 provide precision performance especially for high source impedance applications.

Output

The LT1801/LT1802 can deliver a large output current, so the short-circuit current limit is set around 50mA to prevent damage to the device. Attention must be paid to keep the junction temperature of the IC below the absolute maximum rating of $150^\circ C$ (refer to the Power Dissipation section) when the output is continuously short circuited. The output of the amplifier has reverse-biased diodes connected to each supply. If the output is forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to several hundred mA and the total supply voltage is less than 12.6V, the absolute maximum rating, no damage will occur to the device.

Overdrive Protection

When the input voltage exceeds the power supplies, two pairs of crossing diodes D1 to D4 will prevent the output from reversing polarity. If the input voltage exceeds either power supply by 700mV, diode D1/D2 or D3/D4 will turn on to keep the output at the proper polarity. For the phase reversal protection to perform properly, the input current must be limited to less than 10mA. If the amplifier is severely overdriven, an external resistor should be used to limit the overdrive current.

The LT1801/LT1802's input stages are also protected against a large differential input voltage of 1.4V or higher by a pair of back-back diodes D5/D8 to prevent the emitter-base breakdown of the input transistors. The current in these diodes should be limited to less than 10mA when they are active. The worst-case differential input voltage usually occurs when the input is driven while the output is shorted to ground in a unity gain configuration. In addition, the amplifier is protected against ESD strikes up to 3kV on all pins by a pair of protection diodes on each pin that are connected to the power supplies as shown in Figure 1.

APPLICATIONS INFORMATION

Capacitive Load

The LT1801/LT1802 are optimized for high bandwidth, low power and precision applications. They can drive a capacitive load of about 75pF in a unity-gain configuration, and more for higher gain. When driving a larger capacitive load, a resistor of 10Ω to 50Ω should be connected between the output and the capacitive load to avoid ringing or oscillation. The feedback should still be taken from the output so that the resistor will isolate the capacitive load to ensure stability. Graphs on capacitive loads indicate the transient response of the amplifier when driving capacitive load with a specified series resistor.

Feedback Components

When feedback resistors are used to set up gain, care must be taken to ensure that the pole formed by the feedback resistors and the total capacitance at the inverting input does not degrade stability. For instance, the LT1801/LT1802 in a noninverting gain of 2, setup with two 5k resistors and a capacitance of 5pF (part plus PC board) will probably oscillate. The pole is formed at 12.7MHz that will reduce phase margin by 57 degrees when the crossover frequency of the amplifier is around 20MHz. A capacitor of 5pF or higher connected across the feedback resistor will eliminate any ringing or oscillation.

TYPICAL APPLICATIONS

Single 3V Supply, 1MHz, 4th Order Butterworth Filter

The circuit shown on the first page of this data sheet makes use of the low voltage operation and the wide bandwidth of the LT1801 to create a DC accurate 1MHz 4th order lowpass filter powered from a 3V supply. The amplifiers are configured in the inverting mode for the lowest distortion and the output can swing rail-to-rail for maximum dynamic range. Also on the first page of this data sheet, the graph displays the frequency response of the filter. Stopband attenuation is greater than 100dB at 50MHz. With a 2.25V_{P-P}, 250kHz input signal, the filter has harmonic distortion products of less than -85dBc. Worst case output offset voltage is less than 6mV.

Fast 1A Current Sense Amplifier

A simple, fast current sense amplifier in Figure 2 is suitable for quickly responding to out-of-range currents. The circuit amplifies the voltage across the 0.1Ω sense resistor by a gain of 20, resulting in a conversion gain of 2V/A. The -3dB bandwidth of the circuit is 4MHz, and the uncertainty due to V_{OS} and I_B is less than 4mA. The minimum output voltage is 60mV, corresponding to 30mA. The large-signal response of the circuit is shown in Figure 3.

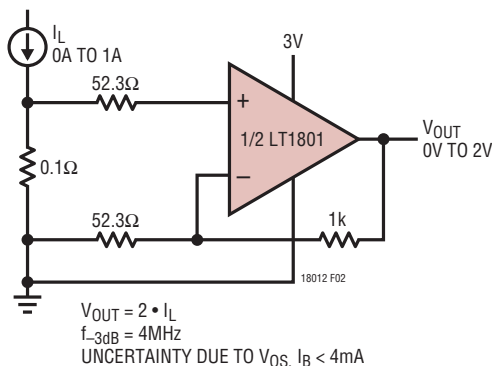


Figure 2. Fast 1A Current Sense

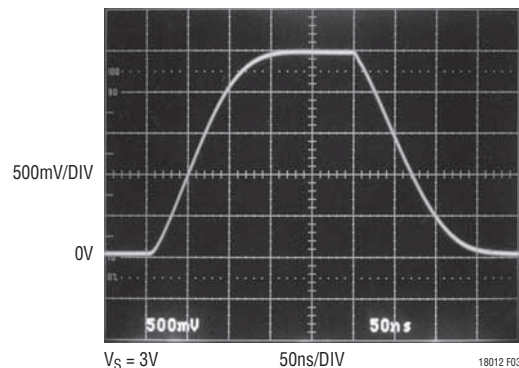


Figure 3. Current Sense Amplifier Large-Signal Response

TYPICAL APPLICATIONS

Single Supply 1A Laser Driver Amplifier

Figure 4 shows the LT1801 used in a 1A laser driver application. One of the reasons the LT1801 is well suited to this control task is that its 2.3V operation ensures that it will be awaked during power-up and operated before the circuit can otherwise cause significant current to flow in the 2.1V threshold laser diode. Driving the noninverting input of the LT1801 to a voltage V_{IN} will control the turning on of the high current NPN transistor, FM6T619 and the laser diode. A current equal to $V_{IN}/R1$ flows through the laser diode. The LT1801 low offset voltage and low input

bias current allows it to control the current that flows through the laser diode precisely. The overall circuit is a 1A per volt V-to-I converter. Frequency compensation components R2 and C1 are selected for fast but zero-overshoot time domain response to avoid overcurrent conditions in the laser. The time domain response of this circuit, measured at R1 and given a 500mV 230ns input pulse, is shown in Figure 5. While the circuit is capable of 1A operation, the laser diode and the transistor are thermally limited due to power dissipation, so they must be operated at low duty cycles.

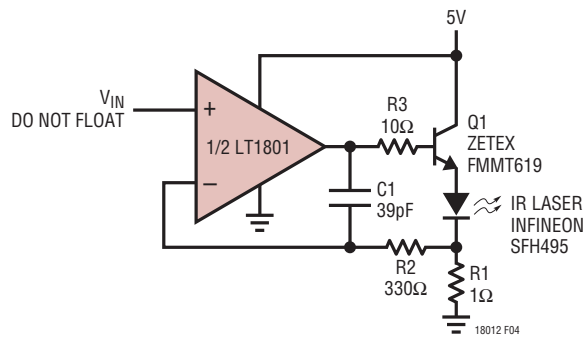


Figure 4. Single Supply 1A Laser Driver Amplifier

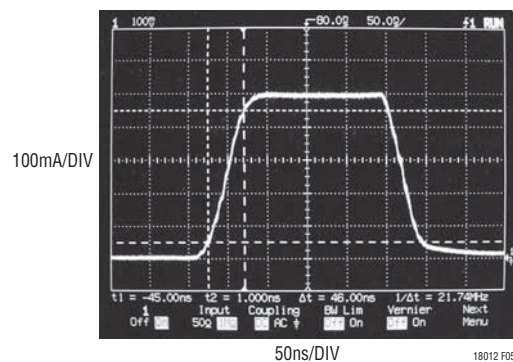
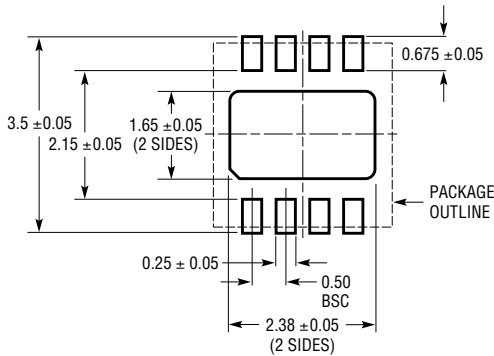


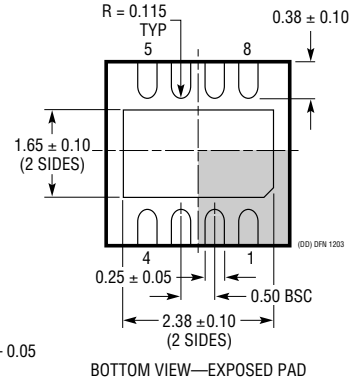
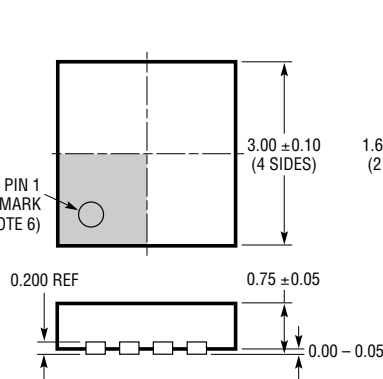
Figure 5. 500mA Pulse Response

PACKAGE DESCRIPTION

DD Package 8-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1698)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



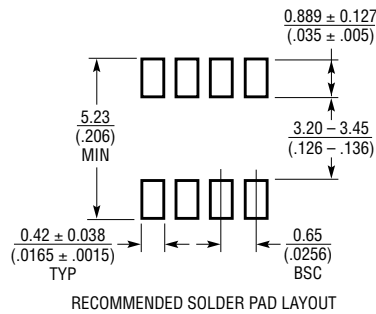
BOTTOM VIEW—EXPOSED PAD

NOTE:

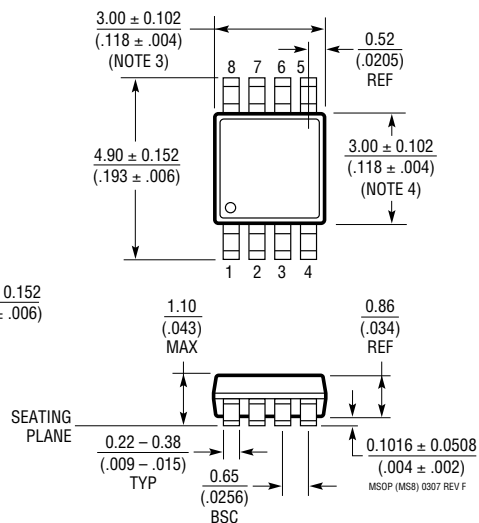
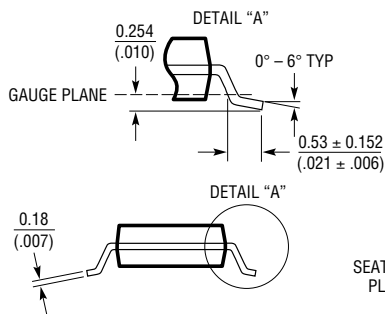
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE MO-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

MS8 Package 8-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1660 Rev F)



RECOMMENDED SOLDER PAD LAYOUT

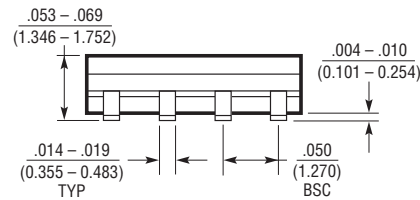
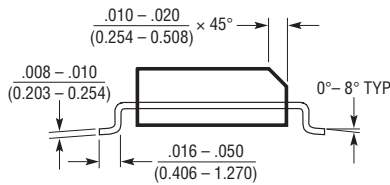
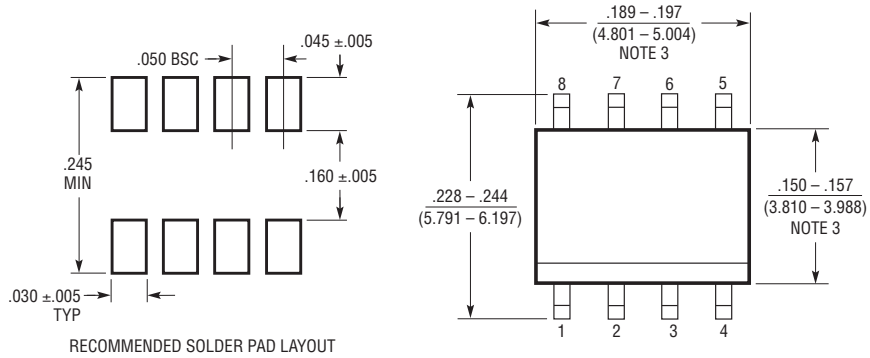


NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

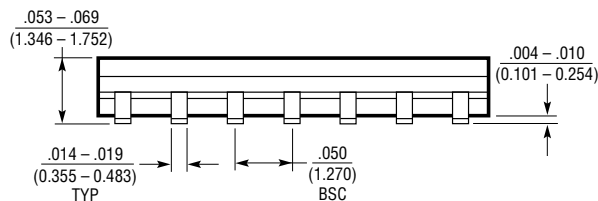
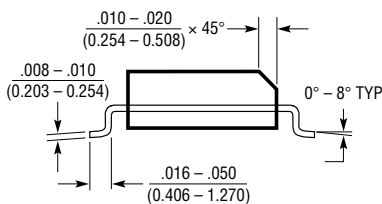
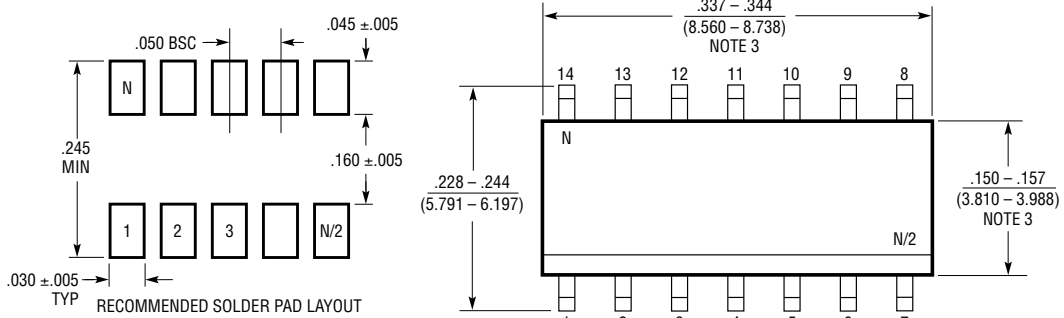
S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S08 0303

S Package 14-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S14 0502