Single/Dual/Quad 100V/µs, 85MHz, Rail-to-Rail Input and Output Op Amps

FEATURES

- **Slew Rate: 100V/µs**
- **Gain Bandwidth Product: 85MHz**
- **Input Common Mode Range Includes Both Rails**
- **Output Swings Rail-to-Rail**
- **Low Quiescent Current: 3mA Max per Amplifier**
- Large Output Current: 42mA
- Voltage Noise: 21nV/√Hz
- Power Supply Rejection: 90dB
- Open-Loop Gain: 60V/mV
- Operating Temperature Range: –40°C to 85°C
- Single Available in the 8-Pin SO and 5-Pin Low Profile (1mm) SOT-23 (ThinSOT™) Package
- Dual Available in 8-Lead DFN and SO Packages
- Quad Available in the 14-Pin Narrow SO Package

APPLICATIONS

- Low Voltage, High Frequency Signal Processing
- Driving A/D Converters
- Rail-to-Rail Buffer Amplifiers
- Active Filters
- Video Line Driver

DESCRIPTION

The LT®1803/LT1804/LT1805 are single/dual/quad, low power, high speed rail-to-rail input and output operational amplifiers with excellent DC performance. The LT1803/LT1804/LT1805 feature reduced supply current, lower input offset voltage, lower input bias current and higher DC gain than other devices with comparable bandwidth and slew rate.

Typically, the LT1803/LT1804/LT1805 have an input offset voltage of 350µV, an input bias current of 125nA and an open-loop gain of 60V/mV.

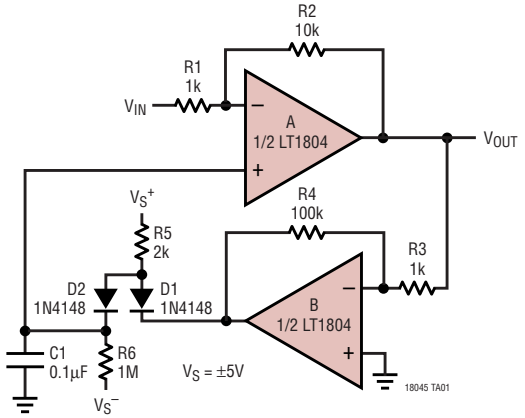
The LT1803/LT1804/LT1805 have an input range that includes both supply rails and an output that swings within 20mV of either supply rail to maximize the signal dynamic range in low supply applications.

The LT1803/LT1804/LT1805 are specified at 3V, 5V and ±5V supplies and typically maintain their performance for supplies from 2.3V to 12.6V. The inputs can be driven beyond the supplies without damage or phase reversal of the output.

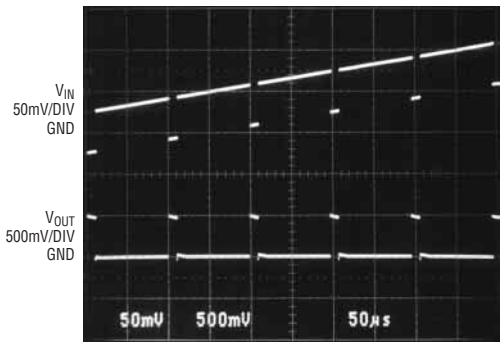
The LT1803 is available in the 8-pin SO package with the standard op amp pinout and in the 5-pin SOT-23 package. The LT1804 is available in 8-pin DFN and SO packages with the standard op amp pinouts. The LT1805 features the standard quad op amp configuration and is available in a 14-pin plastic SO package.

TYPICAL APPLICATION

Inverting DC Restore



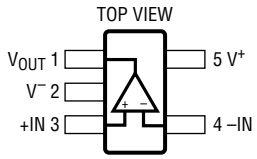
Inverting DC Restore Circuit Response



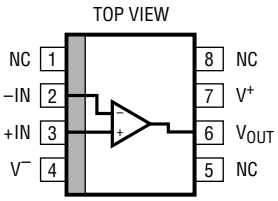
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 12.6V
Input Current (Note 2) ..... ±10mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4) .. –40°C to 85°C
Specified Temperature Range (Note 5) ... –40°C to 85°C
Maximum Junction Temperature ..... 150°C
Maximum Junction Temperature (DD Package) .. 125°C
Storage Temperature Range ..... –65°C to 150°C
Storage Temperature Range
(DD Package) ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

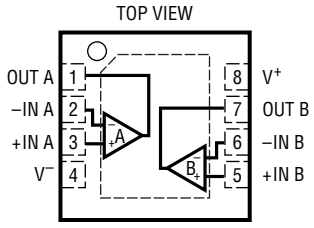


S5 PACKAGE
5-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 250°C/W

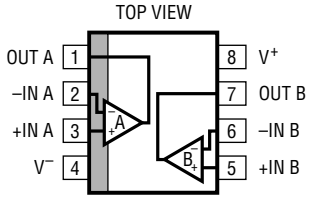


S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 190°C/W

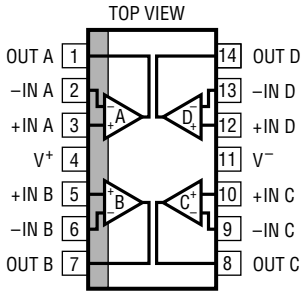
ORDER PART NUMBER	S5 PART MARKING*	ORDER PART NUMBER	S8 PART MARKING
LT1803CS5 LT1803IS5	LTAFN	LT1803CS8 LT1803IS8	1803 1803I



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 160°C/W
UNDERSIDE METAL INTERNALLY CONNECTED TO V^-
(PCB CONNECTION OPTIONAL)



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 190°C/W



S PACKAGE
14-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 160°C/W

ORDER PART NUMBER	DD PART MARKING*	ORDER PART NUMBER	S8 PART MARKING	ORDER PART NUMBER
LT1804CDD LT1804IDD	LADJ	LT1804CS8 LT1804IS8	1804 1804I	LT1805CS LT1805IS

Consult LTC Marketing for parts specified with wider operating temperature ranges.
*The temperature grades are identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 0V V_{CM} = 0V (DD Package) V_{CM} = 0V (SOT-23 Package) V_{CM} = V_S		0.35 1.00 1.00 1.50	2 3 5 8	mV mV mV mV
ΔV_{OS}	Input Offset Shift	V_{CM} = 0V to V_S – 2V		0.125	0.50	mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = 0V V_{CM} = 0V (DD Package)		0.5 1.0	3.5 5.0	mV mV
I_B	Input Bias Current	V_{CM} = 1V V_{CM} = V_S		125 3	750 5.5	nA µA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = 1V V_{CM} = V_S		100 100	1250 1500	nA nA
I_{OS}	Input Offset Current	V_{CM} = 1V V_{CM} = V_S		100 50	1000 1000	nA nA
	Input Noise Voltage	0.1Hz to 10Hz		4		μV_{P-P}
e_n	Input Noise Voltage Density	f = 10kHz		21		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz		2.5		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			2		pF
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to V_S/2 V_S = 5V, V_O = 1V to 4V, R_L = 100Ω to V_S/2 V_S = 3V, V_O = 0.5V to 2.5V, R_L = 1k to V_S/2	20 2 15	60 4.5 45		V/mV V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 0V to 3V V_S = 3V, V_{CM} = 0V to 1V	75 66	96 90		dB dB
	CMRR Match (Channel-to-Channel) (Note 9)	V_S = 5V, V_{CM} = 0V to 3V V_S = 3V, V_{CM} = 0V to 1V	69 60	91 85		dB dB
	Input Common Mode Range		0		V_S	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	68	90		dB
	PSRR Match (Channel-to-Channel) (Note 9)	V_S = 2.5V to 10V, V_{CM} = 0V	62	90		dB
	Minimum Supply Voltage (Note 6)			2.3	2.5	V
V_{OL}	Output Voltage Swing Low (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 15mA		17 80 180	60 150 300	mV mV mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 15mA		17 125 350	60 250 600	mV mV mV
I_{SC}	Short-Circuit Current (Note 3)	V_S = 5V V_S = 3V	20 18	42 34		mA mA
I_S	Supply Current per Amplifier			2.7	3	mA
GBW	Gain Bandwidth Product	V_S = 5V, Frequency = 2MHz, R_L = 1k to 2.5V	50	85		MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k to V_S/2, V_O = 0.5V to 4.5V Measured at V_O = 1.5V, 3.5V	65	100		V/µs
FPBW	Full Power Bandwidth (Note 10)	V_S = 5V, A_V = –1, V_O = 0.5V to 4.5V, R_L = 1k to V_S/2		8		MHz
HD	Harmonic Distortion	V_S = 5V, A_V = 1, R_L = 1k, V_O = $2V_{P-P}$, f_C = 1MHz		–75		dBc
t_S	Settling Time	0.01%, V_S = 5V, V_{STEP} = 2V, A_V = 1, R_L = 1k		350		ns
ΔG	Differential Gain (NTSC)	V_S = 5V, A_V = 2, R_L = 150Ω		0.15		%
Δθ	Differential Phase (NTSC)	V_S = 5V, A_V = 2, R_L = 150Ω		1		Deg

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the 0°C ≤ T_A ≤ 70°C temperature range. V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 0V	●		0.50	3.5	mV
		V_{CM} = 0V (DD Package)	●		1.25	5	mV
		V_{CM} = 0V (SOT-23 Package)	●		1.25	6	mV
		V_{CM} = V_S	●		1.60	8.5	mV
ΔV_{OS}	Input Offset Shift	V_{CM} = 0V to V_S – 2V	●		0.05	0.8	mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = 0V	●		0.75	5.5	mV
		V_{CM} = 0V (DD Package)	●		1.50	7.5	mV
V_{OS} TC	Input Offset Voltage Drift (Note 8)		●		10	35	µV/°C
I_B	Input Bias Current	V_{CM} = 1V	●		150	1100	nA
		V_{CM} = V_S – 0.2V	●		3.2	6	µA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = 1V	●		120	1500	nA
		V_{CM} = V_S – 0.2V	●		120	1800	nA
I_{OS}	Input Offset Current	V_{CM} = 1V	●		100	1400	nA
		V_{CM} = V_S – 0.2V	●		50	1400	nA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to V_S/2	●	15	50		V/mV
		V_S = 5V, V_O = 1V to 4V, R_L = 100Ω to V_S/2	●	1.4	3.7		V/mV
		V_S = 3V, V_O = 0.5V to 2.5V, R_L=1k to V_S/2	●	10	40		V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 0V to 3V	●	71	95		dB
		V_S = 3V, V_{CM} = 0V to 1V	●	61	90		dB
	CMRR Match (Channel-to-Channel) (Note 9)	V_S = 5V, V_{CM} = 0V to 3V	●	65	90		dB
		V_S = 3V, V_{CM} = 0V to 1V	●	55	85		dB
	Input Common Mode Range		●	0		V_S	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	●	65	87		dB
	PSRR Match (Channel-to-Channel) (Note 9)	V_S = 2.5V to 10V, V_{CM} = 0V	●	59	87		dB
	Minimum Supply Voltage (Note 6)		●		2.3	2.5	V
V_{OL}	Output Voltage Swing Low (Note 7)	No Load	●		19	80	mV
		I_{SINK} = 5mA	●		100	225	mV
		I_{SINK} = 15mA	●		200	450	mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load	●		19	80	mV
		I_{SOURCE} = 5mA	●		150	350	mV
		I_{SOURCE} = 15mA	●		450	900	mV
I_{SC}	Short-Circuit Current (Note 3)	V_S = 5V	●	17	40		mA
		V_S = 3V	●	15	28		mA
I_S	Supply Current per Amplifier		●		3	3.75	mA
GBW	Gain Bandwidth Product	V_S = 5V, Frequency = 2MHz, R_L = 1k to 2.5V	●	45	82		MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k to V_S/2, V_O = 0.5V to 4.5V Measured at V_O = 1.5V, 3.5V	●	45	93		V/µs

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the $-40°C \le T_A \le 85°C$ temperature range. V_S = 5V, 0V; V_S = 3V, 0V; $V_{CM} = V_{OUT}$ = half supply unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 0V	●		0.7	4	mV
		V_{CM} = 0V (DD Package)	●		1.5	6.5	mV
		V_{CM} = 0V (SOT-23 Package)	●		1.5	7	mV
		$V_{CM} = V_S$	●		1.7	9	mV
ΔV_{OS}	Input Offset Shift	V_{CM} = 0V to V_S – 2V	●		0.125	1.00	mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = 0V	●		1	6.5	mV
		V_{CM} = 0V (DD Package)	●		2	9	mV
V_{OS} TC	Input Offset Voltage Drift (Note 8)		●		10	35	µV/°C
I_B	Input Bias Current	V_{CM} = 1V	●		200	1500	nA
		$V_{CM} = V_S$ – 0.2V	●		3.4	6.5	µA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = 1V	●		150	2000	nA
		$V_{CM} = V_S$ – 0.2V	●		150	2200	nA
I_{OS}	Input Offset Current	V_{CM} = 1V	●		100	1600	nA
		$V_{CM} = V_S$ – 0.2V	●		50	1600	nA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to $V_S/2$	●	12	48		V/mV
		V_S = 5V, V_O = 1.5V to 3.5V, R_L = 100Ω to $V_S/2$	●	1.3	4.8		V/mV
		V_S = 3V, V_O = 0.5V to 2.5V, R_L=1k to $V_S/2$	●	8	35		V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 0V to 3V	●	69	95		dB
		V_S = 3V, V_{CM} = 0V to 1V	●	60	90		dB
	CMRR Match (Channel-to-Channel) (Note 9)	V_S = 5V, V_{CM} = 0V to 3V	●	63	90		dB
		V_S = 3V, V_{CM} = 0V to 1V	●	54	85		dB
	Input Common Mode Range		●	0		V_S	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	●	64	86		dB
	PSRR Match (Channel-to-Channel) (Note 9)	V_S = 2.5V to 10V, V_{CM} = 0V	●	58	86		dB
	Minimum Supply Voltage (Note 6)		●		2.3	2.5	V
V_{OL}	Output Voltage Swing Low (Note 7)	No Load	●		20	90	mV
		I_{SINK} = 5mA	●		100	250	mV
		I_{SINK} = 10mA	●		170	350	mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load	●		20	90	mV
		I_{SOURCE} = 5mA	●		170	400	mV
		I_{SOURCE} = 10mA	●		300	600	mV
I_{SC}	Short-Circuit Current (Note 3)	V_S = 5V	●	12	35		mA
		V_S = 3V	●	11	27		mA
I_S	Supply Current per Amplifier		●		3.1	4.25	mA
GBW	Gain Bandwidth Product	V_S = 5V, Frequency = 2MHz, R_L = 1k to 2.5V	●	40	77		MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k to $V_S/2$, V_O = 0.5V to 4.5V Measured at V_O = 1.5V, 3.5V	●	30	70		V/µs

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±5V, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = –5V V_{CM} = –5V (DD Package) V_{CM} = –5V (SOT-23 Package) V_{CM} = 5V		0.35 1.50 1.50 1.50	2.5 3.5 6 8	mV mV mV mV
ΔV_{OS}	Input Offset Shift	V_{CM} = –5V to 3V		0.3	1	mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = –5V V_{CM} = –5V (DD Package)		0.5 1	4 5.5	mV mV
I_B	Input Bias Current	V_{CM} = –4V V_{CM} = 5V		125 2.5	750 5.5	nA µA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = –4V V_{CM} = 5V		150 150	1250 1500	nA nA
I_{OS}	Input Offset Current	V_{CM} = –4V V_{CM} = 5V		100 50	1000 1000	nA nA
	Input Noise Voltage	0.1Hz to 10Hz		4		μV_{P-P}
e_n	Input Noise Voltage Density	f = 10kHz		21		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz		2.5		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance	f = 100kHz		2		pF
A_{VOL}	Large-Signal Voltage Gain	V_O = –4V to 4V, R_L = 1k V_O = –1.5V to 1.5V, R_L = 100Ω	20 2	55 5		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = –5V to 3V	78	96		dB
	CMRR Match (Channel-to-Channel) (Note 9)	V_{CM} = –5V to 3V	72	96		dB
	Input Common Mode Range		V_S^-		V_S^+	V
PSRR	Power Supply Rejection Ratio	V_S^+ = 2.5V to 10V, V_S^- = 0V, V_{OUT} = V_S^+/2	68	90		dB
	PSRR Match (Channel-to-Channel) (Note 9)	V_S^+ = 2.5V to 10V, V_S^- = 0V, V_{OUT} = V_S^+/2	62	90		dB
V_{OL}	Output Voltage Swing Low (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 15mA		17 85 200	60 150 300	mV mV mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 15mA		17 125 350	60 250 600	mV mV mV
I_{SC}	Short-Circuit Current (Note 3)		25	50		mA
I_S	Supply Current per Amplifier			2.5	3	mA
GBW	Gain Bandwidth Product	Frequency = 2MHz, R_L = 1k		83		MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = ±4V Measured at V_O = ±2V		88		V/µs
FPBW	Full Power Bandwidth (Note 10)	V_O = $8V_{P-P}$, A_V = –1, R_L = 1k		4		MHz
HD	Harmonic Distortion	A_V = 1, R_L = 1k, V_O = $2V_{P-P}$, f_C = 1MHz		–75		dBc
t_S	Settling Time	0.01%, V_{STEP} = 5V, A_V = 1, R_L = 1k		500		ns
ΔG	Differential Gain (NTSC)	A_V = 2, R_L = 150Ω		0.75		%
$\Delta\theta$	Differential Phase (NTSC)	A_V = 2, R_L = 150Ω		0.8		Deg

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the 0°C ≤ T_A ≤ 70°C temperature range. V_S = ±5V, V_{CM} = 0V, V_{OUT} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = –5V	●		0.5	3.5	mV
		V_{CM} = –5V (DD Package)	●		1.5	5	mV
		V_{CM} = –5V (SOT-23 Package)	●		1.5	7	mV
		V_{CM} = 5V	●		1.4	8.5	mV
ΔV_{OS}	Input Offset Shift	V_{CM} = –5V to 3V	●		0.35	1.5	mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = –5V	●		0.75	5.5	mV
		V_{CM} = –5V (DD Package)	●		1.50	7.5	mV
V_{OS} TC	Input Offset Voltage Drift (Note 8)		●		10	35	µV/°C
I_B	Input Bias Current	V_{CM} = –4V	●		175	1000	nA
		V_{CM} = 4.8V	●		2.5	6	µA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = –4V	●		175	1500	nA
		V_{CM} = 4.8V	●		175	1800	nA
I_{OS}	Input Offset Current	V_{CM} = –4V	●		100	1400	nA
		V_{CM} = 4.8V	●		50	1400	nA
A_{VOL}	Large-Signal Voltage Gain	V_O = –4V to 4V, R_L = 1k	●	15	47		V/mV
		V_O = –1.5V to 1.5V, R_L = 100Ω	●	1.5	4.5		V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = –5V to 3V	●	74	95		dB
	CMRR Match (Channel-to-Channel) (Note 9)	V_{CM} = –5V to 3V	●	68	95		dB
	Input Common Mode Range		●	V_S^-		V_S^+	V
PSRR	Power Supply Rejection Ratio	V_S^+ = 2.5V to 10V, V_S^- = 0V, V_{OUT} = V_S^+/2	●	65	87		dB
	PSRR Match (Channel-to-Channel) (Note 9)	V_S^+ = 2.5V to 10V, V_S^- = 0V, V_{OUT} = V_S^+/2	●	59	87		dB
V_{OL}	Output Voltage Swing Low (Note 7)	No Load	●		19	80	mV
		I_{SINK} = 5mA	●		100	225	mV
		I_{SINK} = 15mA	●		220	475	mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load	●		19	80	mV
		I_{SOURCE} = 5mA	●		150	350	mV
		I_{SOURCE} = 15mA	●		460	900	mV
I_{SC}	Short-Circuit Current (Note 3)		●	20	46		mA
I_S	Supply Current per Amplifier		●		2.8	3.75	mA
GBW	Gain Bandwidth Product	Frequency = 2MHz, R_L = 1k	●		80		MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = ±4V, Measured at V_O = ±2V	●		84		V/µs

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the –40°C ≤ T_A ≤ 85°C temperature range. V_S = ±5V, V_{CM} = 0V, V_{OUT} = 0V unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = –5V	●		1	4.0	mV
		V_{CM} = –5V (DD Package)	●		2	6.5	mV
		V_{CM} = –5V (SOT-23 Package)	●		2	8	mV
		V_{CM} = 5V	●		2	9	mV
ΔV_{OS}	Input Offset Shift	V_{CM} = –5V to 3V	●		0.4	1.7	mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = –5V	●		1	6.5	mV
		V_{CM} = –5V (DD Package)	●		2	9.0	mV
V_{OS} TC	Input Offset Voltage Drift (Note 8)		●		10	35	µV/°C
I_B	Input Bias Current	V_{CM} = –4V	●		250	1200	nA
		V_{CM} = 4.8V	●		2.5	6.5	µA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = –4V	●		200	2000	nA
		V_{CM} = 4.8V	●		250	2200	nA
I_{OS}	Input Offset Current	V_{CM} = –4V	●		100	1600	nA
		V_{CM} = 4.8V	●		50	1600	nA
A_{VOL}	Large-Signal Voltage Gain	V_O = –4V to 4V, R_L = 1k	●	12	45		V/mV
		V_O = –1V to 1V, R_L = 100Ω	●	1.4	5.3		V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = –5V to 3V	●	73	95		dB
	CMRR Match (Channel-to-Channel) (Note 9)	V_{CM} = –5V to 3V	●	67	95		dB
	Input Common Mode Range		●	V_S^-		V_S^+	V
PSRR	Power Supply Rejection Ratio	V_S^+ = 2.5V to 10V, V_S^- = 0V, V_{OUT} = V_S^+/2	●	64	86		dB
	PSRR Match (Channel-to-Channel) (Note 9)	V_S^+ = 2.5V to 10V, V_S^- = 0V, V_{OUT} = V_S^+/2	●	58	86		dB
V_{OL}	Output Voltage Swing Low (Note 7)	No Load	●		20	90	mV
		I_{SINK} = 5mA	●		110	250	mV
		I_{SINK} = 10mA	●		170	350	mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load	●		20	90	mV
		I_{SOURCE} = 5mA	●		170	400	mV
		I_{SOURCE} = 10mA	●		300	600	mV
I_{SC}	Short-Circuit Current (Note 3)		●	12.5	34		mA
I_S	Supply Current per Amplifier		●		2.9	4.25	mA
GBW	Gain Bandwidth Product	Frequency = 2MHz, R_L = 1k	●		75		MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = ±4V, Measured at V_O = ±2V	●		65		V/µs

Note 1: Absolute Maximium Ratings are those values beyond which the life of the device may be impaired.

Note 2: The inputs are protected by back-to-back diodes and by ESD diodes to supply rails. If the differential input voltage exceeds 1.4V, or if an input is driven beyond the supply rails, the input current should be limited to less than 10mA. This parameter is not tested; however it is guaranteed by characterization.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LT1803C/LT1803I, LT1804C/LT1804I and LT1805C/LT1805I are guaranteed functional over the temperature range of –40°C and 85°C.

Note 5: The LT1803C/LT1804C/LT1805C are guaranteed to meet specified performance from 0°C to 70°C. The LT1803C/LT1804C/LT1805C are designed, characterized and expected to meet specified performance from –40°C to 85°C but are not tested or QA sampled at these temperatures. The LT1803I/LT1804I/LT1805I are guaranteed to meet specified performance from –40°C to 85°C.

Note 6: Minimum supply voltage is guaranteed by power supply rejection ratio test.

Note 7: Output voltage swings are measured between the output and power supply rails.

Note 8: This parameter is not 100% tested.

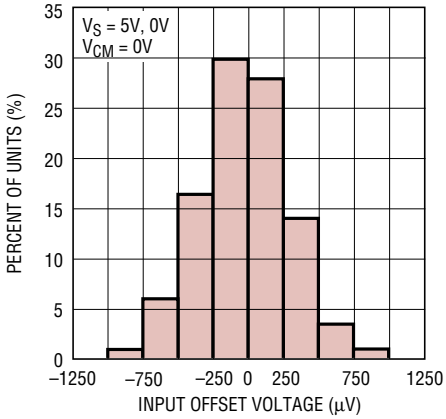
Note 9: Matching parameters are the difference between amplifiers A and D and between B and C on the LT1805; between the two amplifiers on the LT1804.

Note 10: Full power bandwidth is based on slew rate:

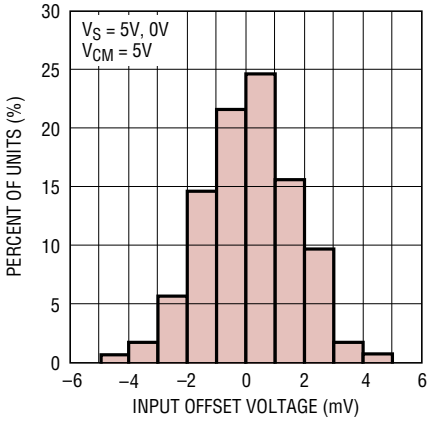
$FPBW = SR/2\pi V_P$

TYPICAL PERFORMANCE CHARACTERISTICS

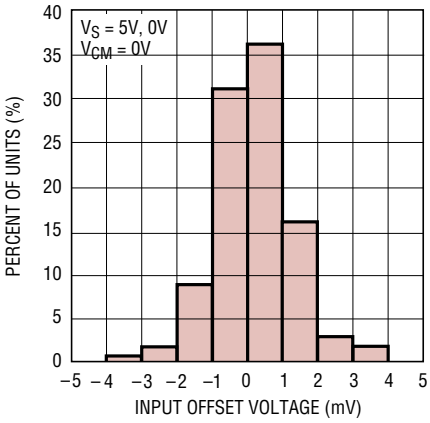
V_{OS} Distribution, V_{CM} = 0V (SO-8, PNP Stage)



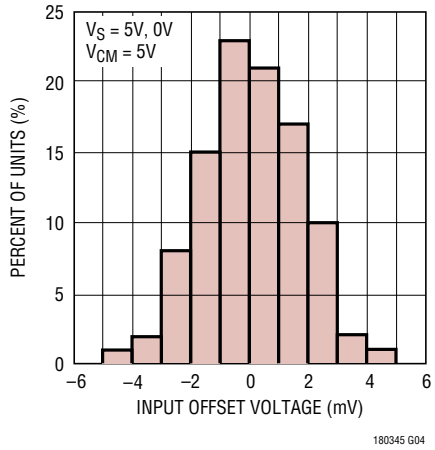
V_{OS} Distribution, V_{CM} = 5V (SO-8, NPN Stage)



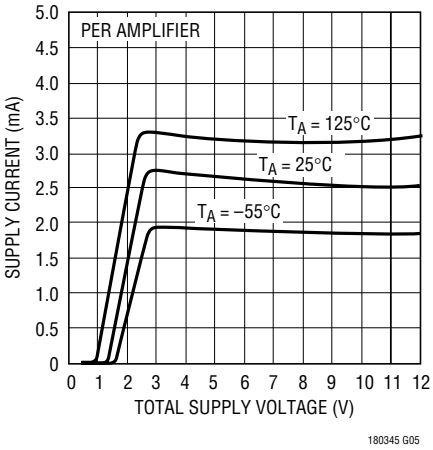
V_{OS} Distribution, V_{CM} = 0V (SOT-23, PNP Stage)



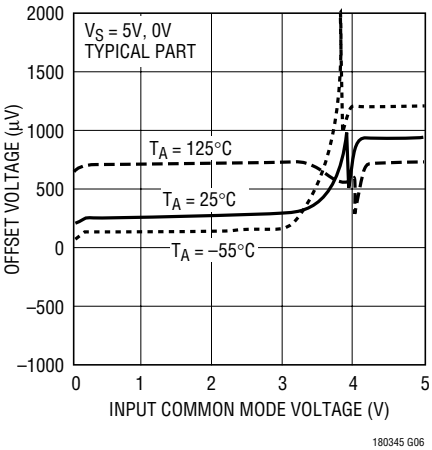
V_{OS} Distribution, V_{CM} = 5V (SOT-23, NPN Stage)



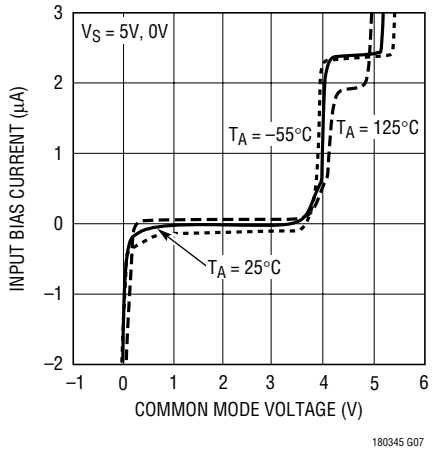
Supply Current vs Supply Voltage



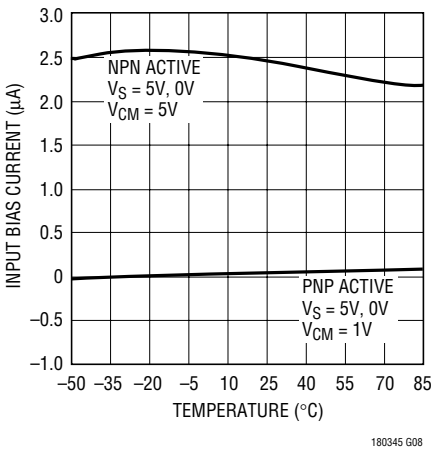
Offset Voltage vs Input Common Mode Voltage



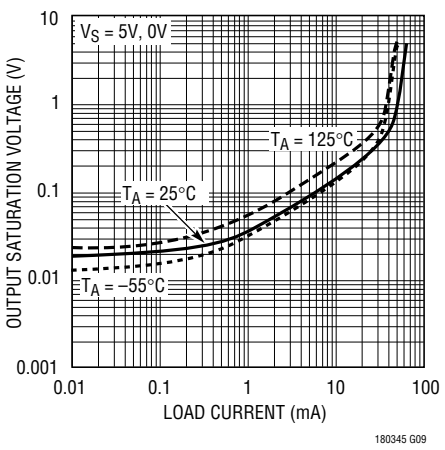
Input Bias Current vs Common Mode Voltage



Input Bias Current vs Temperature

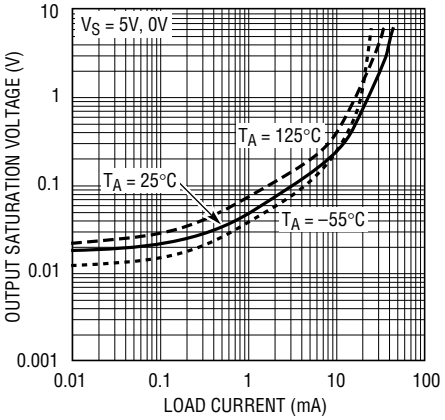


Output Saturation Voltage vs Load Current (Output Low)



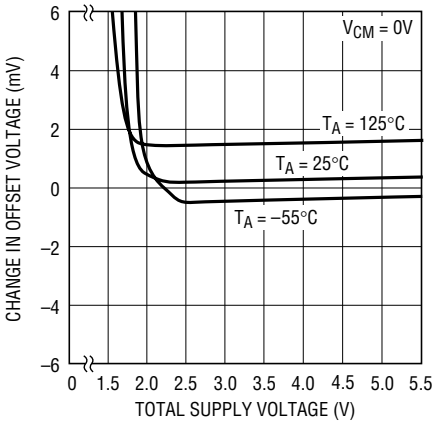
TYPICAL PERFORMANCE CHARACTERISTICS

Output Saturation Voltage vs Load Current (Output High)



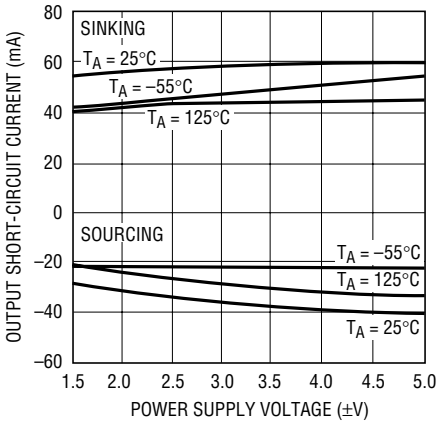
180345 G10

Minimum Supply Voltage



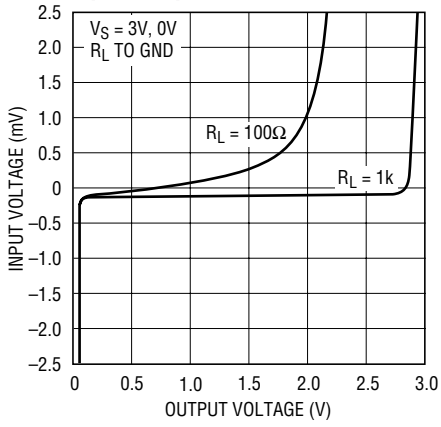
180345 G11

Output Short-Circuit Current vs Power Supply Voltage



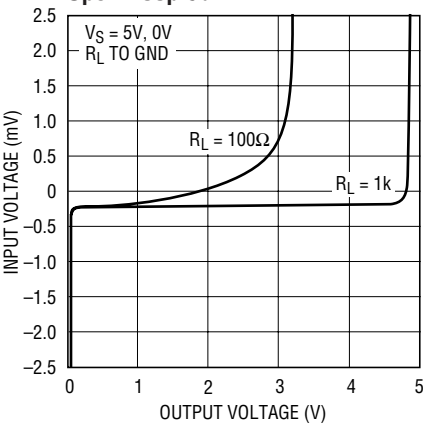
180345 G12

Open-Loop Gain



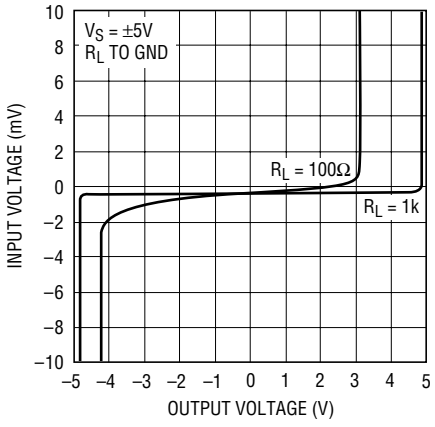
180345 G13

Open-Loop Gain



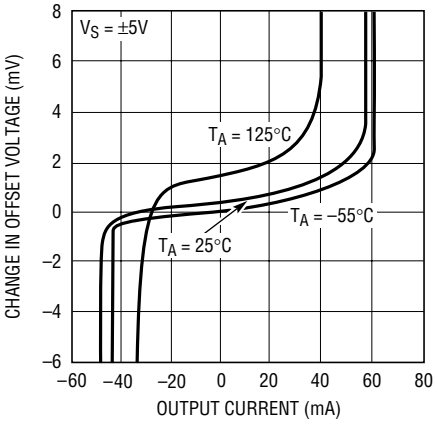
180345 G14

Open-Loop Gain



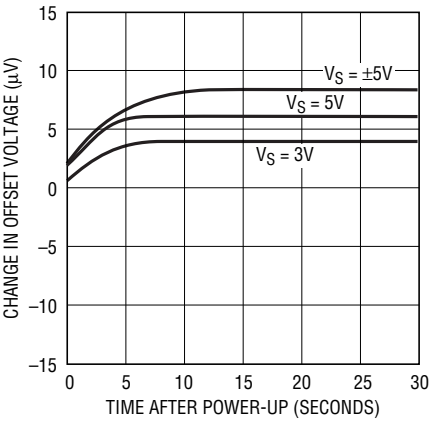
180345 G15

Offset Voltage Change vs Output Current



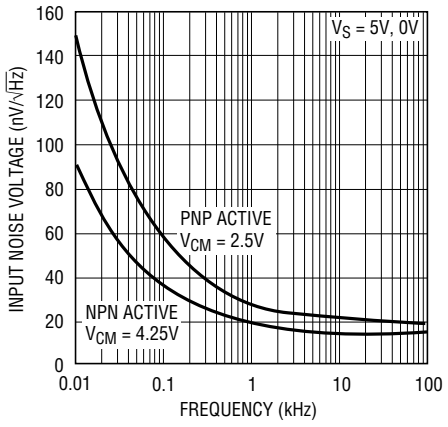
180345 G16

Warm-Up Drift vs Time (LT1804S8)



180345 G17

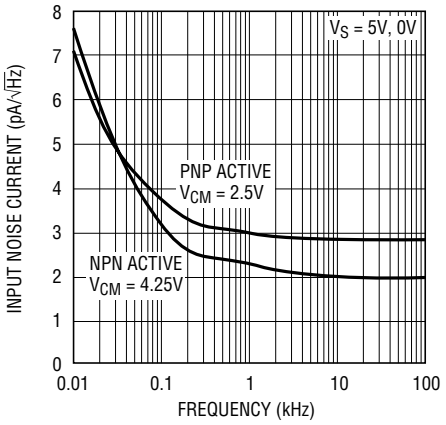
Input Noise Voltage vs Frequency



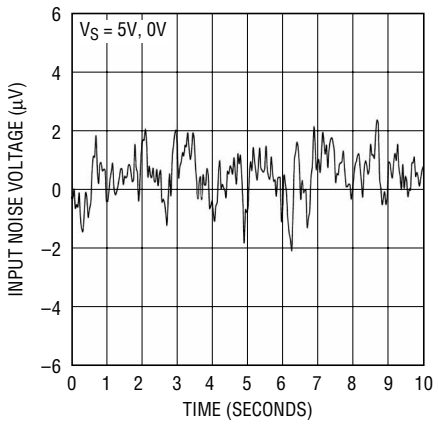
180345 G18

TYPICAL PERFORMANCE CHARACTERISTICS

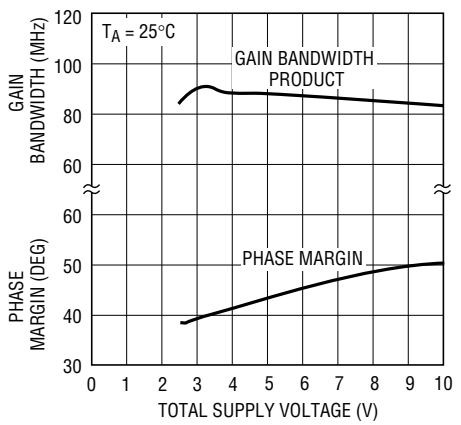
Input Current Noise vs Frequency



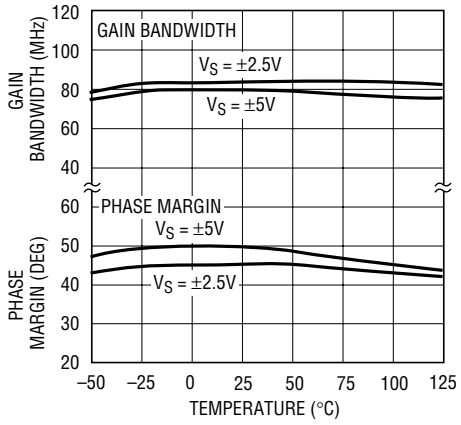
0.1Hz to 10Hz Voltage Noise



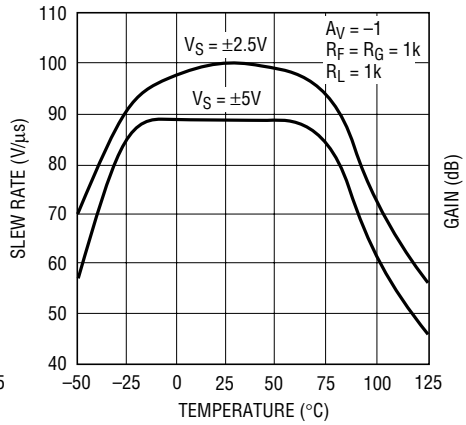
Gain Bandwidth and Phase Margin vs Supply Voltage



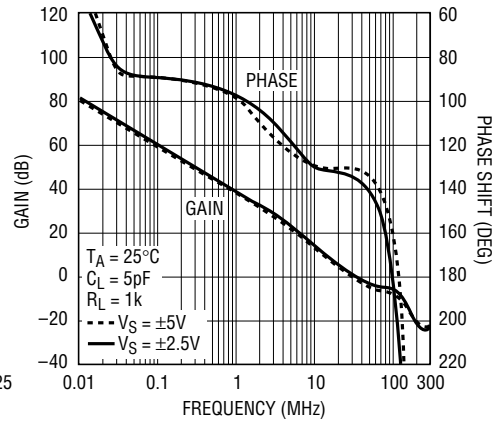
Gain Bandwidth and Phase Margin vs Temperature



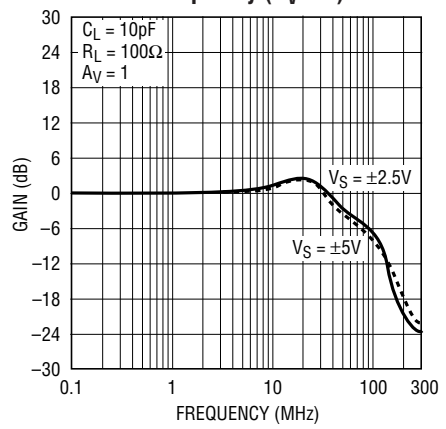
Slew Rate vs Temperature



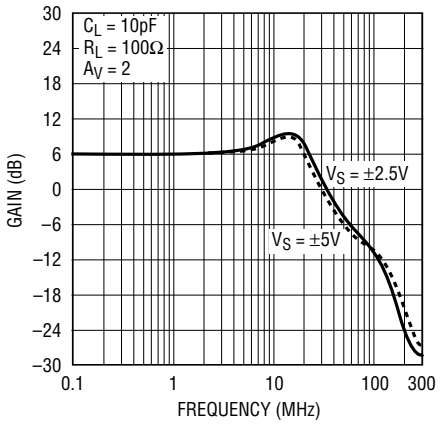
Gain and Phase vs Frequency



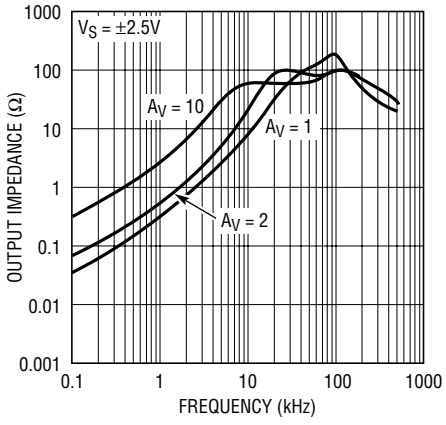
Gain vs Frequency (A_V = 1)



Gain vs Frequency (A_V = 2)

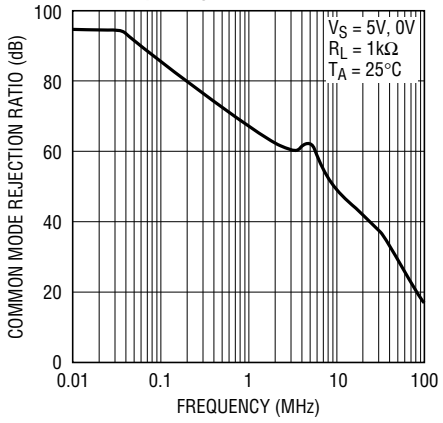


Output Impedance vs Frequency

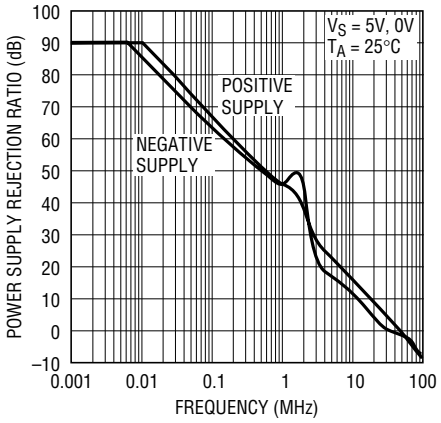


TYPICAL PERFORMANCE CHARACTERISTICS

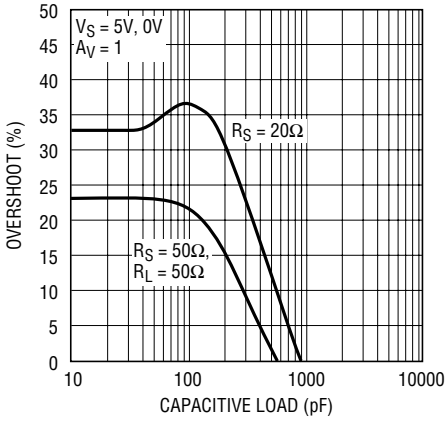
Common Mode Rejection Ratio vs Frequency



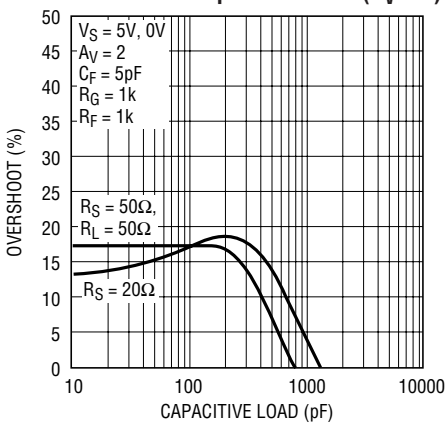
Power Supply Rejection Ratio vs Frequency



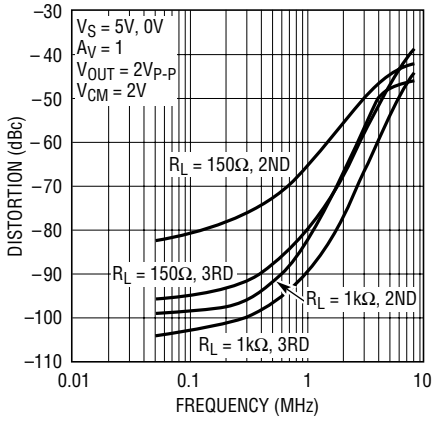
Overshoot and Series Output Resistor vs Capacitive Load (A_V = 1)



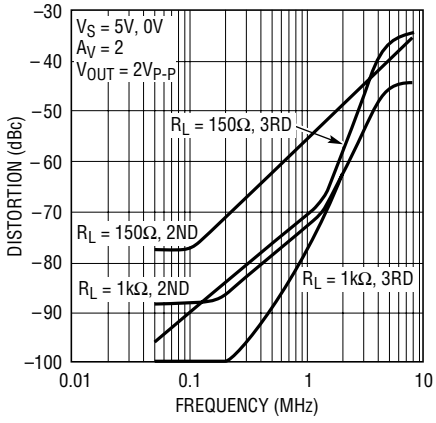
Overshoot and Series Output Resistor vs Capacitive Load (A_V = 2)



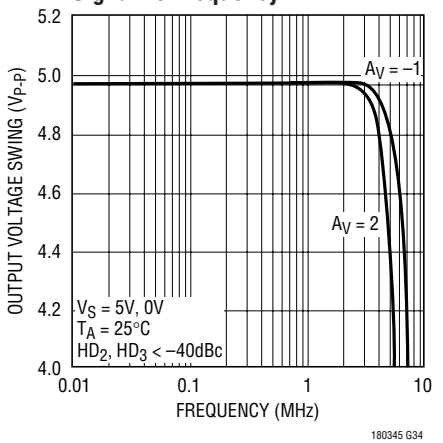
Distortion vs Frequency (A_V = 1)



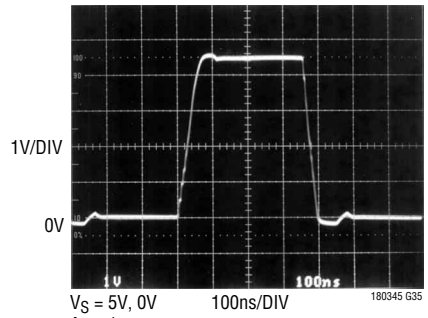
Distortion vs Frequency (A_V = 2)



Maximum Undistorted Output Signal vs Frequency

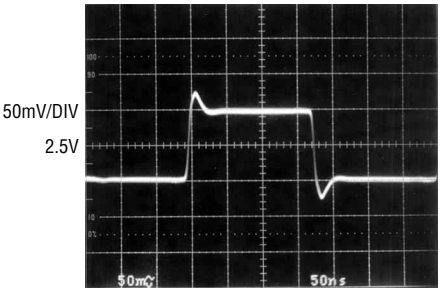


5V Large-Signal Response



VS = 5V, 0V
AV = 1
RL = 1k
100ns/DIV

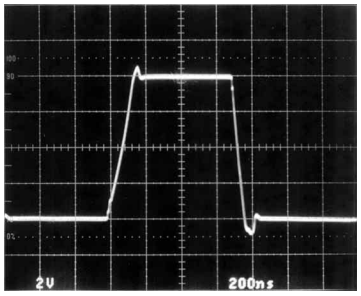
5V Small-Signal Response



VS = 5V, 0V
AV = 1
RL = 1k
50ns/DIV

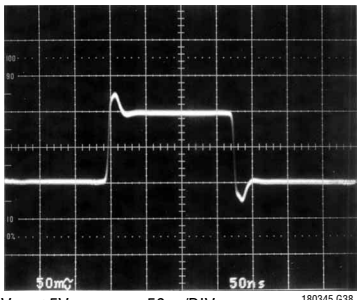
TYPICAL PERFORMANCE CHARACTERISTICS

±5V Large-Signal Response



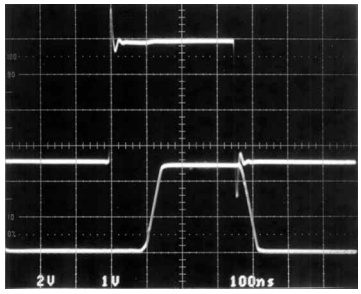
V_S = ±5V
A_V = 1
R_L = 1k
200ns/DIV
180345 G37

±5V Small-Signal Response



V_S = ±5V
A_V = 1
R_L = 1k
50ns/DIV
180345 G38

Output Overdrive Recovery



V_S = 5V, 0V
A_V = 2
R_L = 1k
100ns/DIV
180345 G39

APPLICATIONS INFORMATION

Circuit Description

The LT1803/LT1804/LT1805 have input and output signal ranges from the negative power supply to the positive power supply. Figure 1 depicts a simplified schematic of one amplifier. The input stage is comprised of two differential amplifiers, a PNP stage Q1/Q2 and an NPN stage Q3/Q4 that are active over the different ranges of the common mode input voltage. The PNP differential pair is active between the negative supply and approximately 1.3V below the positive supply. As the input voltage moves toward the positive supply, the transistor Q5 will steer the tail current I_1 to the current mirror Q6/Q7 activating the NPN differential pair. The PNP pair becomes inactive for the rest of the input common mode range up to the positive supply. Also at the input stage, devices Q18 and Q19 act to cancel the bias current of the PNP input pair. When Q1 and Q2 are active, the current in Q16 is controlled to be the same as the current in Q1 and Q2; therefore, the base current of Q16 is nominally equal to the base current of the input devices. The base current of Q16 is then mirrored by devices Q17 through Q19 to cancel the base current of the input devices Q1 and Q2.

A pair of complementary common emitter stages Q14/Q15 that enable the output to swing from rail-to-rail constructs the output stage. The capacitors C1 and C2 form the local feedback loops that lower the output impedance at high frequency. The LT1803/LT1804/LT1805 are fabricated on Linear Technology's proprietary high speed complementary bipolar process.

Power Dissipation

There is a need to ensure that the die's junction temperature does not exceed 150°C. Junction temperature T_J is calculated from the ambient temperature T_A, power dissipation P_D and thermal resistance θ_{JA}:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

The power dissipated in the IC is a function of the supply voltage, amplifier current, output voltage and output current. For a given supply voltage, the worst-case power dissipation, P_{DMAX}, occurs when the output current and voltage drop in the amplifier product is maximized. For example, if the amplifier is sourcing a constant current then the P_{DMAX} occurs when the output voltage is at about V_S^-. On the other hand, for a given load resistance to ground, the P_{DMAX} will occur when the output voltage is at half of either supply voltage. P_{DMAX} for a given resistance to ground is given by:

$$P_{DMAX} = (V_S^+ - V_S^-)\, I_{SMAX} + (V_S/2)^2/R_L$$

Example: An LT1804 in an SO-8 package operating on ±5V supplies and driving a 100Ω load to ground, the P_{DMAX} per amplifier is given by:

$$P_{DMAX} = (10 \bullet 3.25mA) + (2.5)^2/100 = 0.0425 + 0.0625 = 0.095W$$

I_{SMAX} is approximated for a typical part from the Supply Currrent vs Supply Voltage graph.

APPLICATIONS INFORMATION

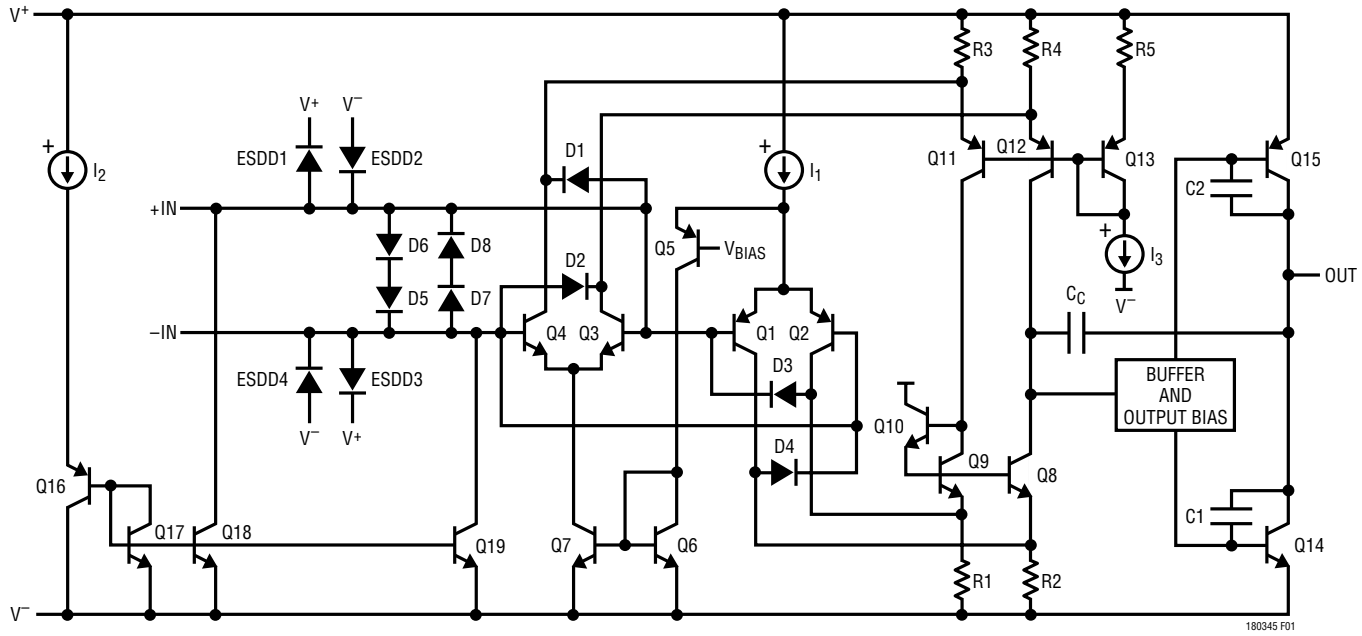


Figure 1. LT1803/LT1804/LT1805 Simplified Schematic Diagram

If both amplifiers are loaded simultaneously, then the total power dissipation is 0.19W.

The maximum ambient temperature that the part is allowed to operate is:

$$T_A = T_J – (P_{DMAX} \bullet 190°C/W)$$

$$= 150°C – (0.190W \bullet 190°C/W) = 113.9°C$$

Similar calculations can be carried out for specific packages and conditions.

Also worth noting, the DD package includes a low θ_{JA} underside metal which is internally connected to $V_S^–$. If the underside metal is properly soldered to a PCB, the θ_{JA} of the part will be close to 50°C/W. This θ_{JA} is significantly less than leaving the underside metal unattached and can be useful for certain applications.

Input Offset Voltage

The input offset voltage will change greatly based upon which input stage is active. The PNP input stage is active from the negative supply voltage to about 1.3V below the positive supply rail, then the NPN input stage is activated for the remaining input range up to the positive supply rail during which the PNP stage remains inactive. The offset voltage is typically less than 1000µV in the range the PNP input stage is active.

Input Bias Current

The LT1803/LT1804/LT1805 employ a patent-pending technique to reduce the input bias current to less than 1µA for the input common mode voltage range of 0.2V above the negative supply rail to 1.75V below the positive rail. The low input offset voltage and low input bias current provide precision performance in high source impedance applications.

Output

The LT1803/LT1804/LT1805 can deliver a large output current, so the short-circuit current limit is set around 50mA to prevent damage to the device. Attention must be paid to keep the junction temperature of the IC below the absolute maximum rating of 150°C (refer to the Power Dissipation section) when the output is continuously short circuited. The output of the amplifier has reverse-biased diodes connected to each supply. If the output is forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to less than 100mA and the total supply voltage is less than

APPLICATIONS INFORMATION

12.6V, the absolute maximum rating, no damage will occur to the device.

Overdrive Protection

When the input voltage exceeds the power supplies, two pairs of crossing diodes D1 through D4 will prevent the output from reversing polarity. If the input voltage exceeds either power supply by 700mV, diode D1/D2 or D3/D4 will turn on to keep the output at the proper polarity. For the phase reversal protection to perform properly, the input current must be limited to less than 10mA. If the amplifier is severely overdriven, an external resistor should be used to limit the overdrive current.

The LT1803/LT1804/LT1805's input stages are also protected against a large differential input voltage of 1.4V or higher by a pair of back-to-back diodes D5 through D8 to prevent the emitter-base breakdown of the input transistors. The current in these diodes should be limited to less than 10mA when they are active. The worst-case differential input voltage usually occurs when the input is driven while the output is shorted to ground in a unity gain configuration. In addition, the amplifier is protected against ESD strikes up to 3kV on all pins by a pair of protection diodes on each pin that is connected to the power supplies as shown in Figure 1.

Capacitive Load

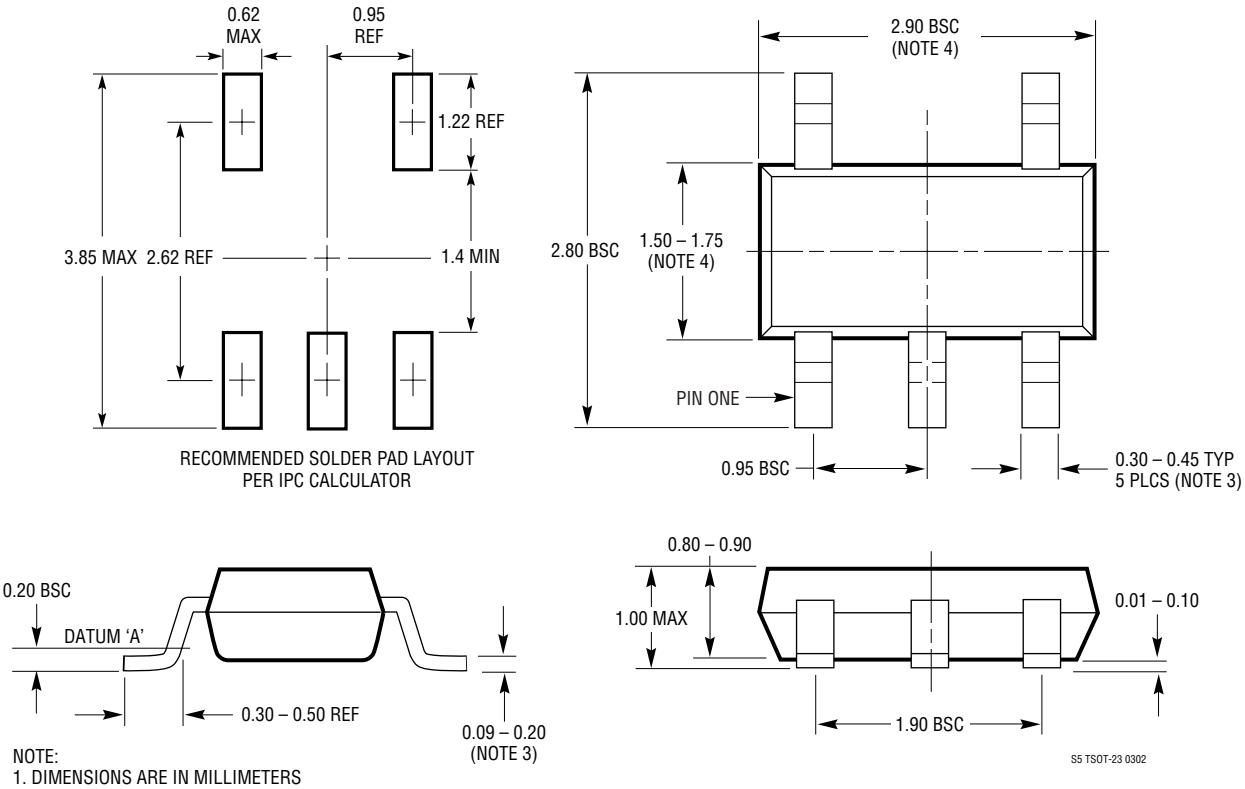
The LT1803/LT1804/LT1805 are optimized for wide bandwidth, low power and precision applications. They can drive a capacitive load of about 20pF in a unity-gain configuration, and more for higher gain. When driving a larger capacitive load, a resistor of 10Ω to 50Ω should be connected between the output and the capacitive load to avoid ringing or oscillation. The feedback should still be taken from the output so that the resistor will isolate the capacitive load to ensure stability. Graphs on capacitive load indicate the transient response of the amplifier when driving a capacitive load with a specified resistor.

Feedback Components

When feedback resistors are used to set up gain, care must be taken to ensure that the pole formed by the feedback resistors and the total capacitance at the inverting input does not degrade stability. For instance, the LT1803/LT1804/LT1805 in a noninverting gain of 2 setup with two 5k resistors and a capacitance of 5pF (part plus PC board) will probably oscillate. The pole formed at 12.7MHz, reduces phase margin by about 58 degrees when the crossover frequency of the amplifier is around 20MHz. A capacitor of 5pF or higher connected across the feedback resistor will eliminate any ringing or oscillation.

PACKAGE DESCRIPTION

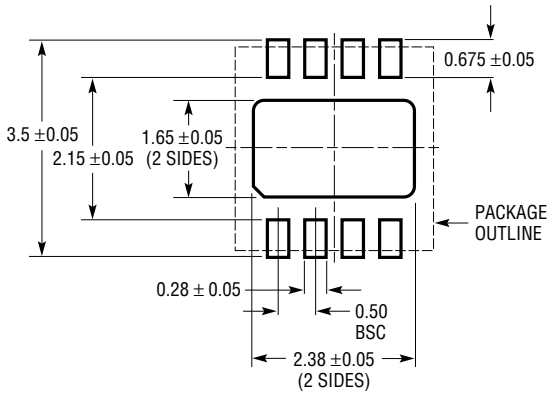
S5 Package
5-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1635)



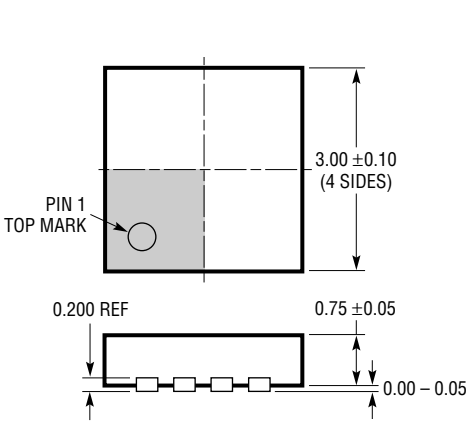
NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

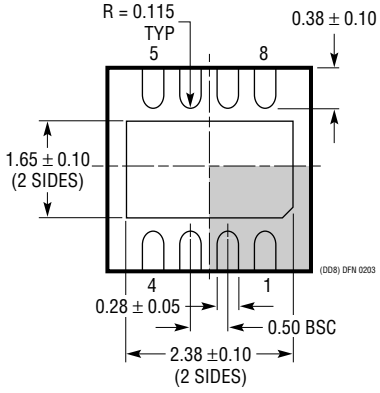
PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



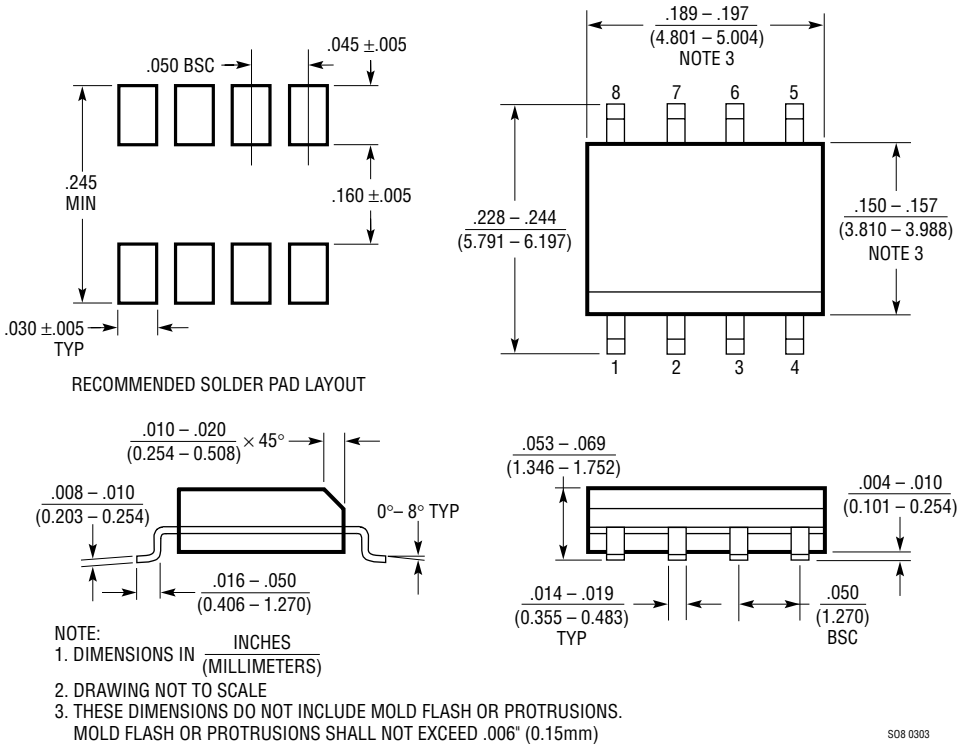


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. EXPOSED PAD SHALL BE SOLDER PLATED

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

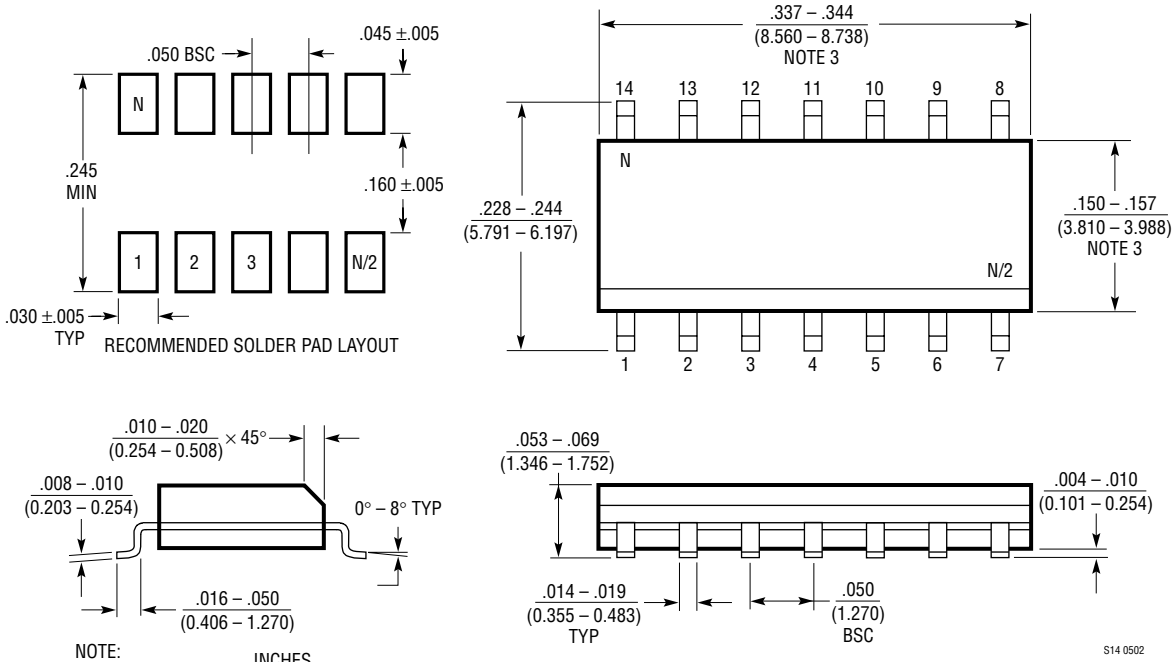


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S08 0303

PACKAGE DESCRIPTION

S Package
14-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)