

Dual and Quad Rail-to-Rail Output, Picoamp Input Precision Op Amps

FEATURES

- **Offset Voltage: 50 μ V Maximum (LT1881A)**
- **Input Bias Current: 200pA Maximum (LT1881A)**
- **Offset Voltage Drift: 0.8 μ V/ $^{\circ}$ C Maximum**
- **Rail-to-Rail Output Swing**
- **Supply Range: 2.7V to 36V**
- Operates with Single or Split Supplies
- Open-Loop Voltage Gain: 1 Million Minimum
- 1mA Maximum Supply Current Per Amplifier
- Stable at $A_V = 1$, $C_L = 1000\text{pF}$
- Standard Pinouts
- Wide Operating Temperature Range:
 -55 $^{\circ}$ C to 125 $^{\circ}$ C (LT1882)

APPLICATIONS

- Thermocouple Amplifiers
- Bridge Transducer Conditioners
- Instrumentation Amplifiers
- Battery-Powered Systems
- Photo Current Amplifiers

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DESCRIPTION

The LT[®]1881 and LT1882 op amps bring high accuracy input performance to amplifiers with rail-to-rail output swing. Input bias currents and capacitive load driving capabilities are superior to the similar LT1884 and LT1885 amplifiers, at the cost of a slight loss in speed. Input offset voltage is trimmed to less than 50 μ V and the low drift maintains this accuracy over the operating temperature range. Input bias currents are an ultralow 200pA maximum.

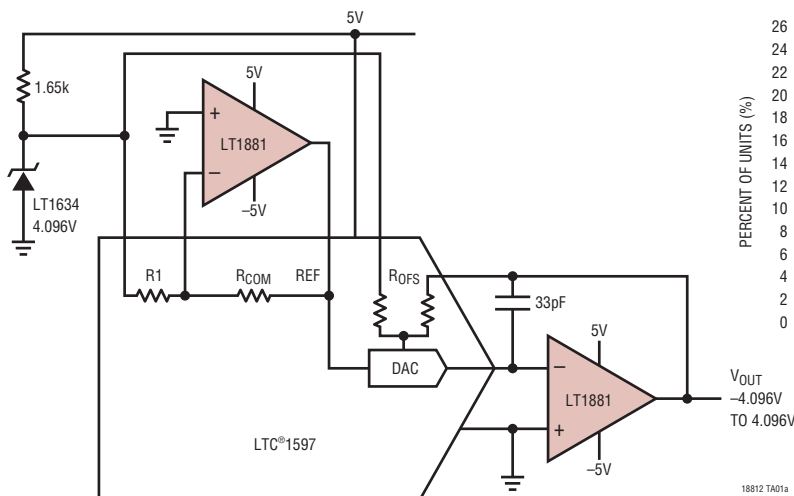
The amplifiers work on any total power supply voltage between 2.7V and 36V (fully specified from 5V to ± 15 V). Output voltage swings to within 40mV of the negative supply and 220mV of the positive supply make these amplifiers good choices for low voltage single supply operation.

Capacitive loads up to 1000pF can be driven directly in unity-gain follower applications.

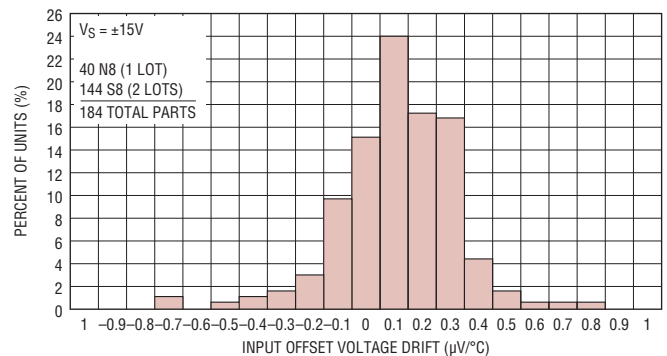
The dual LT1881 and LT1881A are available with standard pinouts in S8 and PDIP packages. The quad LT1882 is in a 14-pin SO package. For a higher speed device with similar DC specifications, see the LT1884/LT1885.

TYPICAL APPLICATION

16-Bit Voltage Output DAC on ± 5 V Supply



TC V_{OS} Distribution, Industrial Grade



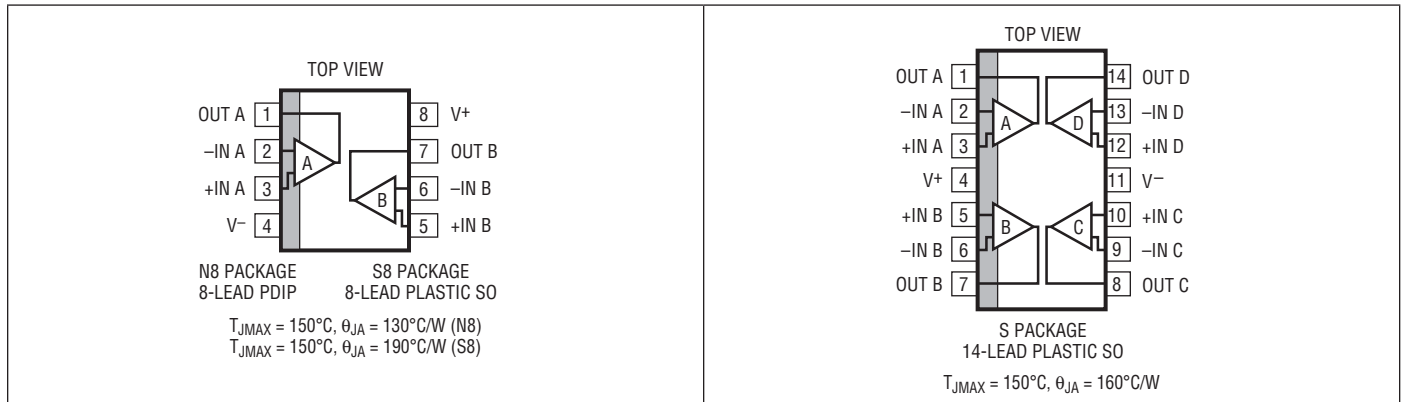
LT1881/LT1882

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+ to V^-).....	40V
Differential Input Voltage (Note 2).....	$\pm 10V$
Input Voltage.....	V^+ to V^-
Input Current (Note 2).....	$\pm 10mA$
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range (Note 4)	
LT1881C/LT1882C.....	$-40^\circ C$ to $85^\circ C$
LT1881I/LT1882I.....	$-40^\circ C$ to $85^\circ C$
LT1882H	$-40^\circ C$ to $125^\circ C$
LT1882MP.....	$-55^\circ C$ to $125^\circ C$

Specified Temperature Range (Note 5)	
LT1881C/LT1882C.....	$-40^\circ C$ to $85^\circ C$
LT1881I/LT1882I	$-40^\circ C$ to $85^\circ C$
LT1882H	$-40^\circ C$ to $125^\circ C$
LT1882MP.....	$-55^\circ C$ to $125^\circ C$
Maximum Junction Temperature.....	$150^\circ C$
Storage Temperature Range.....	$-65^\circ C$ to $150^\circ C$
Lead Temperature (Soldering, 10 sec)	$300^\circ C$

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1881CN8#PBF	LT1881CN8#TRPBF	LT1881CN8	8-Lead PDIP	$0^\circ C$ to $70^\circ C$
LT1881IN8#PBF	LT1881IN8#TRPBF	LT1881IN8	8-Lead PDIP	$-40^\circ C$ to $85^\circ C$
LT1881CS8#PBF	LT1881CS8#TRPBF	1881	8-Lead Plastic SO	$0^\circ C$ to $70^\circ C$
LT1881IS8#PBF	LT1881IS8#TRPBF	1881I	8-Lead Plastic SO	$-40^\circ C$ to $85^\circ C$
LT1881ACN8#PBF	LT1881ACN8#TRPBF	LT1881ACN8	8-Lead PDIP	$0^\circ C$ to $70^\circ C$
LT1881AIN8#PBF	LT1881AIN8#TRPBF	LT1881AIN8	8-Lead PDIP	$-40^\circ C$ to $85^\circ C$
LT1881ACS8#PBF	LT1881ACS8#TRPBF	1881A	8-Lead Plastic SO	$0^\circ C$ to $70^\circ C$
LT1881AIS8#PBF	LT1881AIS8#TRPBF	1881AI	8-Lead Plastic SO	$-40^\circ C$ to $85^\circ C$
LT1882CS#PBF	LT1882CS#TRPBF	LT1882CS	14-Lead Plastic SO	$0^\circ C$ to $70^\circ C$
LT1882IS#PBF	LT1882IS#TRPBF	LT1882IS	14-Lead Plastic SO	$-40^\circ C$ to $85^\circ C$
LT1882HS#PBF	LT1882HS#TRPBF	LT1882HS	14-Lead Plastic SO	$-40^\circ C$ to $125^\circ C$
LT1882MPS#PBF	LT1882MPS#TRPBF	LT1882MPS	14-Lead Plastic SO	$-55^\circ C$ to $125^\circ C$

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

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ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Single supply operation $V_S = 5\text{V}, 0\text{V}$; $V_{CM} = V_S/2$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	C/I Grades			H/MP Grades			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage (LT1881A)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$ $-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●	25	50				μV μV μV
	Input Offset Voltage (LT1881/LT1882)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$ $-40^\circ\text{C} < T_A < 85^\circ\text{C}$ $-40^\circ\text{C} < T_A < 125^\circ\text{C}$ $-55^\circ\text{C} < T_A < 125^\circ\text{C}$	● ● ● ●	30	80 125 150	30	80	300 300	μV μV μV μV μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 6)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$ $-40^\circ\text{C} < T_A < 85^\circ\text{C}$	● ●	0.3	0.8				$\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/^\circ\text{C}$
		$-40^\circ\text{C} < T_A < 125^\circ\text{C}$ $-55^\circ\text{C} < T_A < 125^\circ\text{C}$	● ●			0.3	0.8	0.3	$\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/^\circ\text{C}$
$\Delta V_{OS}/\Delta \text{TIME}$	Long-Term Input Offset Voltage Stability			0.3		0.3			$\mu\text{V}/\text{month}$
I_{OS}	Input Offset Current (LT1881A)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$ $-40^\circ\text{C} < T_A < 85^\circ\text{C}$	● ●	100	200 250 300				pA pA pA
	Input Offset Current (LT1881/LT1882)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$ $-40^\circ\text{C} < T_A < 85^\circ\text{C}$ $-40^\circ\text{C} < T_A < 125^\circ\text{C}$ $-55^\circ\text{C} < T_A < 125^\circ\text{C}$	● ● ● ●	150	500 600 700	150	500	2000 2000	pA pA pA pA pA
I_B	Input Bias Current (LT1881A)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$ $-40^\circ\text{C} < T_A < 85^\circ\text{C}$	● ●	100	200 250 300				pA pA pA
	Input Bias Current (LT1881/LT1882)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$ $-40^\circ\text{C} < T_A < 85^\circ\text{C}$ $-40^\circ\text{C} < T_A < 125^\circ\text{C}$ $-55^\circ\text{C} < T_A < 125^\circ\text{C}$	● ● ● ●	150	500 600 700	150	500	3000 3000	pA pA pA pA pA
	Input Noise Voltage	0.1Hz to 10Hz		0.5		0.5			$\mu\text{V}_{\text{p-p}}$
e_n	Input Noise Voltage Density	$f = 1\text{kHz}$		14		14			$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 1\text{kHz}$		0.03		0.03			$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	Differential Mode	●	20		20			$\text{M}\Omega$
		Common Mode	●	100		100			$\text{G}\Omega$
C_{IN}	Input Capacitance		●	2		2			pF
V_{CM}	Input Voltage Range		●	$V^- + 1.0$ $V^- + 1.2$	$V^+ - 1.0$ $V^+ - 1.2$	$V^- + 1.0$ $V^- + 1.2$	$V^+ - 1.0$ $V^+ - 1.2$		V V
CMRR	Common Mode Rejection Ratio	$1\text{V} < V_{CM} < 4\text{V}$	●	106	128	106	128		dB
		$1.2\text{V} < V_{CM} < 3.8\text{V}$	●	104		102			dB
PSRR	Power Supply Rejection Ratio	$V^- = 0\text{V}, V_{CM} = 1.5\text{V}$	●						dB
		$0^\circ\text{C} < T_A < 85^\circ\text{C}, 2.7\text{V} < V^+ < 32\text{V}$	●	106		106			dB
		$0^\circ\text{C} < T_A < 125^\circ\text{C}, 2.7\text{V} < V^+ < 32\text{V}$	●						dB
		$T_A = -40^\circ\text{C}, 3\text{V} < V^+ < 32\text{V}$ $T_A = -55^\circ\text{C}, 3\text{V} < V^+ < 32\text{V}$	● ●	106		106			dB dB
	Minimum Operating Supply Voltage		●	2.4	2.7	2.4	2.7		V

LT1881/LT1882

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Single supply operation $V_S = 5\text{V}, 0\text{V}$; $V_{\text{CM}} = V_S/2$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	C/I Grades			H/MP Grades			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
A_{VOL}	Large-Signal Voltage Gain	$R_L = 10\text{k}; 1\text{V} < V_{\text{OUT}} < 4\text{V}$	●	500 350	1600		500 300	1600	V/mV V/mV	
		$R_L = 2\text{k}; 1\text{V} < V_{\text{OUT}} < 4\text{V}$	●	300 250	800		300 200	800	V/mV V/mV	
		$R_L = 1\text{k}; 1\text{V} < V_{\text{OUT}} < 4\text{V}$	●	250 200	400		250 150	400	V/mV V/mV	
V_{OL}	Output Voltage Swing Low	No Load	●		20	40		20	50	mV
		$I_{\text{SINK}} = 100\mu\text{A}$	●		25	50		25	60	mV
		$I_{\text{SINK}} = 1\text{mA}$	●		70	150		70	200	mV
		$I_{\text{SINK}} = 5\text{mA}$	●		270	600		270	750	mV
V_{OH}	Output Voltage Swing High (Referred to V^+)	No Load	●		120	220		120	300	mV
		$I_{\text{SINK}} = 100\mu\text{A}$	●		130	230		130	325	mV
		$I_{\text{SINK}} = 1\text{mA}$	●		180	300		180	450	mV
		$I_{\text{SINK}} = 5\text{mA}$	●		360	600		360	800	mV
I_S	Supply Current Per Amplifier	$V_S = 3\text{V}, 0\text{V}$	●	0.45	0.65	0.85 1.2	0.45	0.65	0.85 1.5	mA mA
		$V_S = 5\text{V}, 0\text{V}$	●	0.5	0.65	0.9 1.4	0.5	0.65	0.9 1.7	mA mA
		$V_S = 12\text{V}, 0\text{V}$	●	0.5	0.70	1.0 1.5	0.5	0.70	1.0 1.8	mA mA
I_{SC}	Short-Circuit Current	V_{OUT} Short to GND	●	15	30		10	30		mA
		V_{OUT} Short to V^+	●	15	30		10	30		mA
GBW	Gain Bandwidth Product	$f = 20\text{kHz}$		0.35	1.0		0.35	1.0		MHz
	Channel Separation	$f = 1\text{kHz}$			120			120		dB
t_S	Settling Time	0.01%, $V_{\text{OUT}} = 1.5\text{V}$ to 3.5V , $A_V = -1$, $R_L = 2\text{k}$			30			30		μs
SR^+	Slew Rate Positive	$A_V = -1$	●	0.15 0.12	0.35		0.15 0.1	0.35		V/ μs V/ μs
SR^-	Slew Rate Negative	$A_V = -1$	●	0.11 0.08	0.18		0.11 0.06	0.18		V/ μs V/ μs
FPBW	Full-Power Bandwidth	$V_{\text{OUT}} = 4V_{\text{P-P}}$ (Note 10)	●	8.75 6.35	14		8.75 4.75	14		kHz kHz
		Offset Voltage Match (LT1881A)	(Note 7) $0^\circ\text{C} < T_A < 70^\circ\text{C}$ $-40^\circ\text{C} < T_A < 85^\circ\text{C}$	● ●		30 70 125 160				
ΔV_{OS}	Offset Voltage Match (LT1881/LT1882)	(Note 7) $0^\circ\text{C} < T_A < 70^\circ\text{C}$ $-40^\circ\text{C} < T_A < 85^\circ\text{C}$	● ●		35 125 175 235			35 125		μV μV μV μV
		$-40^\circ\text{C} < T_A < 125^\circ\text{C}$	●					385		μV
		$-55^\circ\text{C} < T_A < 125^\circ\text{C}$	●					385		μV
		Offset Voltage Match Drift	(Notes 6, 7)	●		0.4	1.2		0.4	1.2
ΔI_{B^+}	Noninverting Bias Current Match (LT1881A)	(Note 7) $0^\circ\text{C} < T_A < 70^\circ\text{C}$	●		200	300				pA
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●			400				pA
			●			500				pA

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Single supply operation $V_S = 5\text{V}, 0\text{V}$; $V_{CM} = V_S/2$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	C/I Grades			H/MP Grades			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ΔI_{B+}	Noninverting Bias Current Match (LT1881/LT1882)	(Note 7)		250	700		250	700	pA
		$0^\circ\text{C} < T_A < 70^\circ\text{C}$	●						pA
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●						pA
		$-40^\circ\text{C} < T_A < 125^\circ\text{C}$	●					2000	pA
		$-55^\circ\text{C} < T_A < 125^\circ\text{C}$	●					2000	pA
ΔCMRR	Common Mode Rejection Ratio Match	(Notes 7, 9)	●	102	125		100	125	dB
ΔPSRR	Power Supply Rejection Match (Notes 7, 9)	$V^- = 0\text{V}, V_{CM} = 1.5\text{V}$							
		$0^\circ\text{C} < T_A < 85^\circ\text{C}, 2.7\text{V} < V^+ < 32\text{V}$	●	104	126				dB
		$0^\circ\text{C} < T_A < 125^\circ\text{C}, 2.7\text{V} < V^+ < 32\text{V}$	●				102	126	dB
		$T_A = -40^\circ\text{C}, 3\text{V} < V^+ < 32\text{V}$		104	126				dB
	$T_A = -55^\circ\text{C}, 3\text{V} < V^+ < 32\text{V}$					102	126	dB	

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Split supply operation $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	C/I Grades			H/MP Grades			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage (LT1881A)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$	●	25	50				μV
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●		85				μV
						110			μV
V_{OS}	Input Offset Voltage (LT1881/LT1882)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$	●	30	80		30	80	μV
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●		125				μV
		$-40^\circ\text{C} < T_A < 125^\circ\text{C}$	●					300	μV
		$-55^\circ\text{C} < T_A < 125^\circ\text{C}$	●					300	μV
									μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 6)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$	●	0.3	0.8				$\mu\text{V}/^\circ\text{C}$
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●	0.3	0.8				$\mu\text{V}/^\circ\text{C}$
		$-40^\circ\text{C} < T_A < 125^\circ\text{C}$	●				0.3	0.8	$\mu\text{V}/^\circ\text{C}$
		$-55^\circ\text{C} < T_A < 125^\circ\text{C}$	●				0.3	0.8	$\mu\text{V}/^\circ\text{C}$
$\Delta V_{OS}/\Delta\text{TIME}$	Long-Term Input Offset Voltage Stability			0.3		0.3		$\mu\text{V}/\text{month}$	
I_{OS}	Input Offset Current (LT1881A)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$	●	100	200				pA
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●		250				pA
						300			pA
I_{OS}	Input Offset Current (LT1881/LT1882)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$	●	150	500		150	500	pA
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●		600				pA
		$-40^\circ\text{C} < T_A < 125^\circ\text{C}$	●					2000	pA
		$-55^\circ\text{C} < T_A < 125^\circ\text{C}$	●					2000	pA
									pA
I_B	Input Bias Current (LT1881A)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$	●	100	200				pA
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●		250				pA
						300			pA
I_B	Input Bias Current (LT1881/LT1882)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$	●	150	500		150	500	pA
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●		600				pA
		$-40^\circ\text{C} < T_A < 125^\circ\text{C}$	●					3000	pA
		$-55^\circ\text{C} < T_A < 125^\circ\text{C}$	●					3000	pA
									pA

LT1881/LT1882

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SYMBOL	PARAMETER	CONDITIONS	C/I Grades			H/MP Grades			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Input Noise Voltage	0.1Hz to 10Hz		0.5		0.5		$\mu\text{V}_{\text{P-P}}$	
e_n	Input Noise Voltage Density	$f = 1\text{kHz}$		14		14		$\text{nV}/\sqrt{\text{Hz}}$	
i_n	Input Noise Current Density	$f = 1\text{kHz}$		0.03		0.03		$\text{pA}/\sqrt{\text{Hz}}$	
R_{IN}	Input Resistance	Differential Mode Common Mode	● ●	20 100		20 100		$\text{M}\Omega$ $\text{G}\Omega$	
C_{IN}	Input Capacitance		●	2		2		pF	
V_{CM}	Input Voltage Range		●	$V^- + 1.0$ $V^- + 1.2$	$V^+ - 1.0$ $V^+ - 1.2$	$V^- + 1.0$ $V^- + 1.2$	$V^+ - 1.0$ $V^+ - 1.2$	V V	
CMRR	Common Mode Rejection Ratio	$-13.5\text{V} < V_{\text{CM}} < 13.5\text{V}$	●	114	130	110	130	dB	
+PSRR	Positive Power Supply Rejection Ratio	$V^- = -15\text{V}$, $V_{\text{CM}} = 0\text{V}$; $1.5\text{V} < V^+ < 18\text{V}$	●	110	132	108	132	dB	
-PSRR	Negative Power Supply Rejection Ratio	$V^+ = 15\text{V}$, $V_{\text{CM}} = 0\text{V}$; $-1.5\text{V} < V^- < -18\text{V}$	●	106	132	104	132	dB	
	Minimum Operating Supply Voltage		●	± 1.2	± 1.35	± 1.2	± 1.35	V	
A_{VOL}	Large-Signal Voltage Gain	$R_L = 10\text{k}$; $-13.5\text{V} < V_{\text{OUT}} < 13.5\text{V}$	●	1000 700	1600	1000 500	1600	V/mV V/mV	
		$R_L = 2\text{k}$; $-13.5\text{V} < V_{\text{OUT}} < 4\text{V}$	●	175 125	420	175 110	420	V/mV V/mV	
		$R_L = 1\text{k}$; $1\text{V} < V_{\text{OUT}} < 4\text{V}$	●	90 65	230	90 7	230	V/mV V/mV	
V_{OL}	Output Voltage Swing Low (Referred to V_{EE})	No Load $I_{\text{SINK}} = 100\mu\text{A}$ $I_{\text{SINK}} = 1\text{mA}$ $I_{\text{SINK}} = 5\text{mA}$	● ● ● ●	20 25 70 270	40 50 150 600	20 25 70 270	50 60 200 750	mV mV mV mV	
V_{OH}	Output Voltage Swing High (Referred to V_{CC})	No Load $I_{\text{SOURCE}} = 100\mu\text{A}$ $I_{\text{SOURCE}} = 1\text{mA}$ $I_{\text{SOURCE}} = 5\text{mA}$	● ● ● ●	120 130 180 360	220 230 300 600	120 130 180 360	300 325 450 800	mV mV mV mV	
I_S	Supply Current Per Amplifier	$V_S = \pm 15\text{V}$	●	0.5	0.85 1.1 1.6	0.5	0.85 1.1 2.0	mA mA	
I_{SC}	Short-Circuit Current	V_{OUT} Short to V^- V_{OUT} Short to V^+	● ●	20 15	40 40	20 10	40 40	mA mA mA mA	
GBW	Gain Bandwidth Product	$f = 20\text{kHz}$		0.4	0.85	0.4	0.85	MHz	
	Channel Separation	$f = 1\text{kHz}$		120		120		dB	
t_S	Settling Time	0.01%, $V_{\text{OUT}} = -5\text{V}$ to 5V , $A_V = -1$, $R_L = 2\text{k}$		30		30		μs	
SR^+	Slew Rate Positive	$A_V = -1$	●	0.21 0.18	0.4	0.21 0.15	0.4	$\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$	
SR^-	Slew Rate Negative	$A_V = -1$	●	0.13 0.1	0.20	0.11 0.07	0.20	$\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$	

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Split supply operation $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	C/I Grades			H/MP Grades			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
FPBW	Full-Power Bandwidth	$V_{OUT} = 28V_{P-P}$ (Note 10)	● 1.47 1.13	2.25		1.47 0.79	2.25		kHz kHz
ΔV_{OS}	Offset Voltage Match (LT1881A)	(Note 7)	●	35	70				μV
		$0^\circ\text{C} < T_A < 70^\circ\text{C}$	●		125				μV
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●		160				μV
	Offset Voltage Match (LT1881/LT1882)	(Note 7)	●	42	125	42	125		μV
		$0^\circ\text{C} < T_A < 70^\circ\text{C}$	●		175				μV
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●		235				μV
		$-40^\circ\text{C} < T_A < 125^\circ\text{C}$	●					435	μV
		$-55^\circ\text{C} < T_A < 125^\circ\text{C}$	●					435	μV
	Offset Voltage Match Drift	(Notes 6, 7)	●	0.4	1.1	0.4	1.1		$\mu\text{V}/^\circ\text{C}$
ΔI_{B+}	Noninverting Bias Current Match (LT1881A)	(Note 7)	●	200	300				pA
		$0^\circ\text{C} < T_A < 70^\circ\text{C}$	●		400				pA
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●		500				pA
ΔI_{B+}	Noninverting Bias Current Match (LT1881/LT1882)	(Note 7)	●	250	700	250	700		pA
		$0^\circ\text{C} < T_A < 70^\circ\text{C}$	●		900				pA
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●		1000				pA
		$-40^\circ\text{C} < T_A < 125^\circ\text{C}$	●					2000	pA
		$-55^\circ\text{C} < T_A < 125^\circ\text{C}$	●					2000	pA
ΔCMRR	Common Mode Rejection Match	(Notes 7, 9)	●	110	125	106	125		dB
$\Delta+\text{PSRR}$	Positive Power Supply Rejection Ratio Match	$V^- = -15\text{V}$, $V_{CM} = 0\text{V}$, $1.5\text{V} < V^+ < 18\text{V}$, (Notes 7, 9)	●	108	130	108	130		dB
$\Delta-\text{PSRR}$	Negative Power Supply Rejection Ratio Match	$V^+ = 15\text{V}$, $V_{CM} = 0\text{V}$, $-1.5\text{V} < V^- < -18\text{V}$, (Notes 7, 9)	●	104	130	104	130		dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by internal resistors and back-to-back diodes. If the differential input voltage exceeds $\pm 0.7\text{V}$, the input current should be limited externally to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum.

Note 4: The LT1881C/LT1882C and LT1881I/LT1882I are guaranteed functional over the operating temperature range of -40°C to 85°C . The LT1882H is guaranteed functional over the operating temperature range -40°C to 125°C . The LT1882MP is guaranteed functional over the operating temperature range -55°C to 125°C .

Note 5: The LT1881C/LT1882C are guaranteed to meet specified performance from 0°C to 70°C . The LT1881C/LT1882C are designed, characterized and expected to meet specified performance from -40°C to 85°C but are not tested or QA sampled at these temperatures. The LT1881I/LT1882I are guaranteed to meet specified performance from -40°C to 85°C . The LT1882H is guaranteed to meet specified performance from -40°C to 125°C . The LT1882MP is guaranteed to meet specified performance from -55°C to 125°C .

Note 6: This parameter is not 100% tested.

Note 7: Matching parameters are the difference between amplifiers A and B in the LT1881; and between amplifiers A and D and B and C in the LT1882.

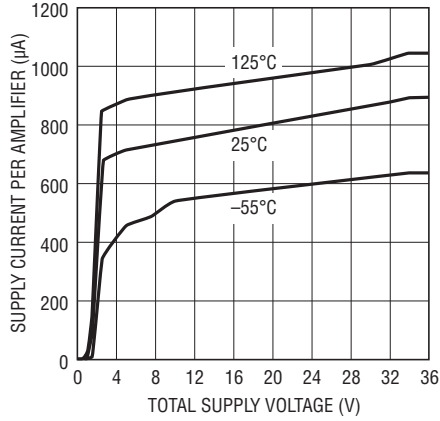
Note 8: This parameter is the difference between the two noninverting input bias currents.

Note 9: ΔCMRR and ΔPSRR are defined as follows: CMRR and PSRR are measured in $\mu\text{V}/\text{V}$ on each amplifier. The difference is calculated in $\mu\text{V}/\text{V}$ and then converted to dB.

Note 10: Full power bandwidth is calculated from the slew rate: $\text{FPBW} = \text{SR}/2\pi V_P$.

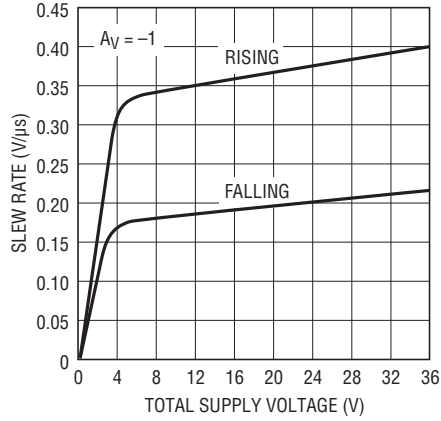
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current per Amplifier vs Supply Voltage



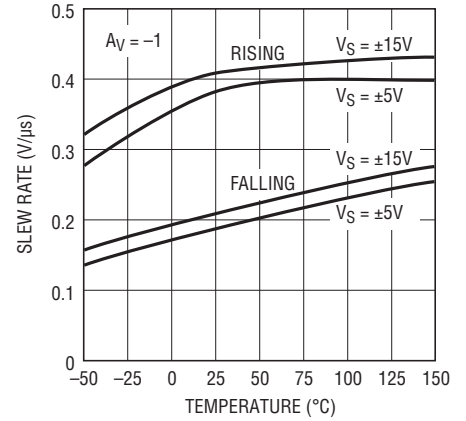
18812 G01

Slew Rate vs Supply Voltage



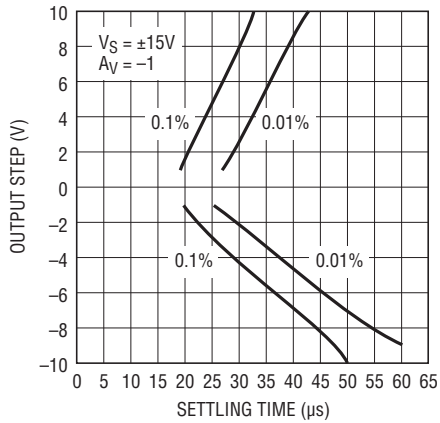
18812 G02

Slew Rate vs Temperature



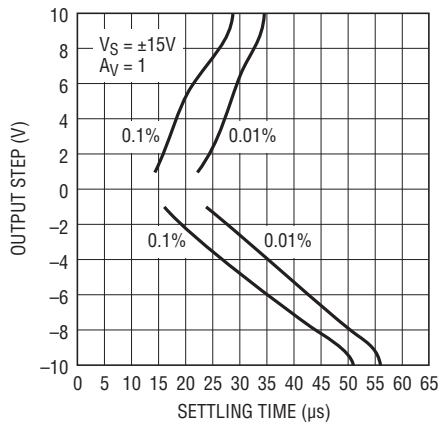
18812 G03

Settling Time vs Output Step



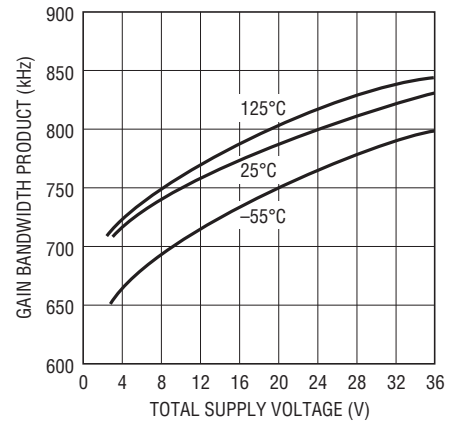
18812 G04

Settling Time vs Output Step



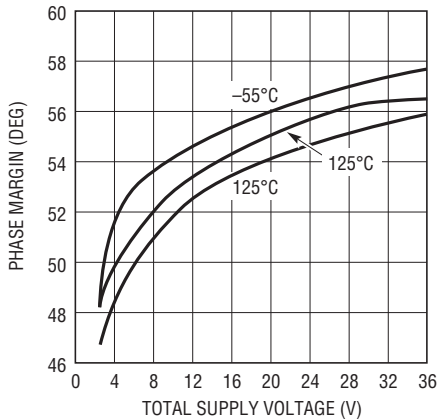
18812 G05

Gain Bandwidth Product vs Supply Voltage



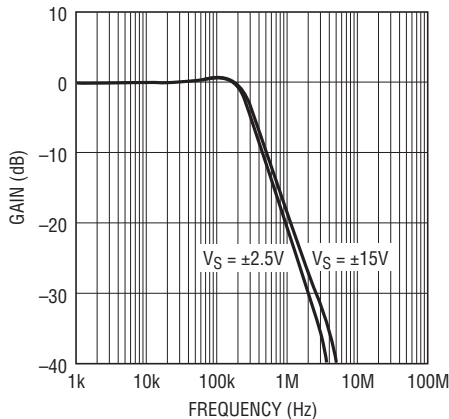
18812 G06

Phase Margin vs Supply Voltage



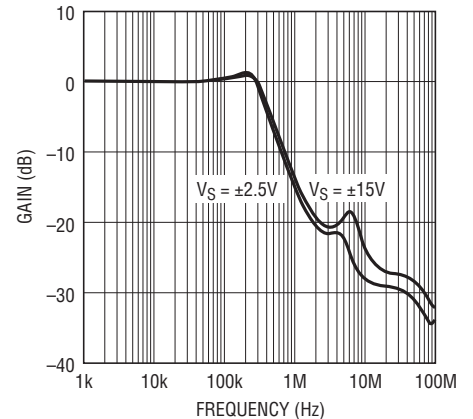
18812 G07

Gain vs Frequency, Av = -1



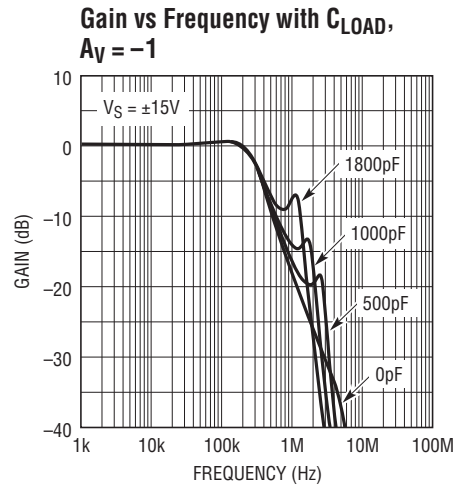
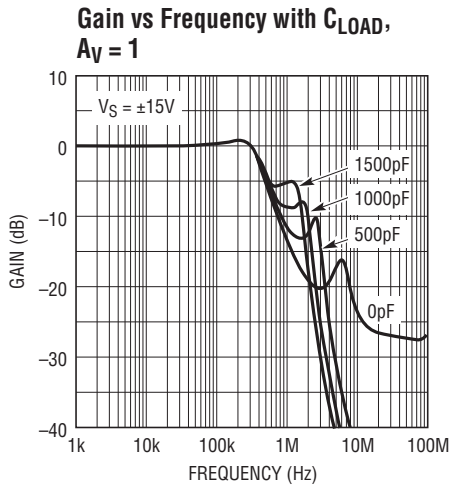
18812 G08

Gain vs Frequency, Av = 1

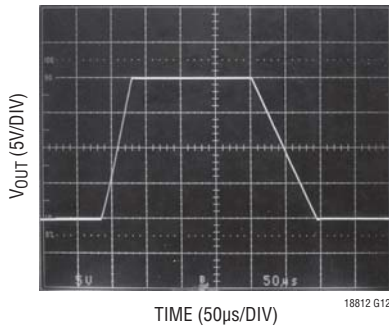


18812 G09

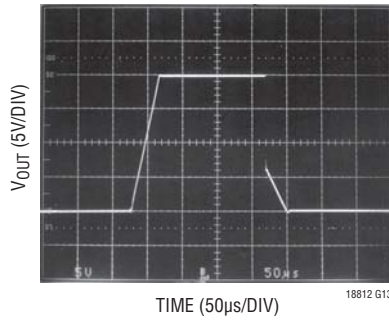
TYPICAL PERFORMANCE CHARACTERISTICS



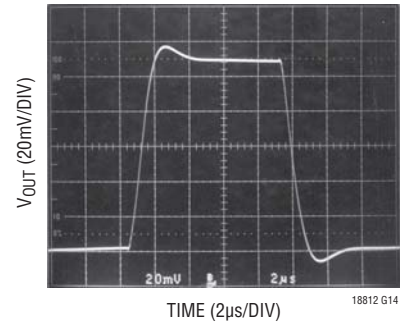
Large Signal Response, $A_V = -1$



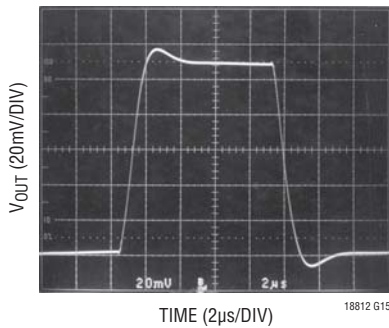
Large Signal Response, $A_V = 1$



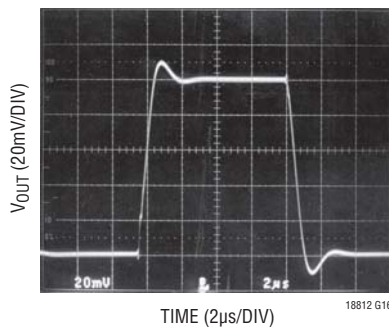
Small Signal Response, $A_V = -1$, No Load



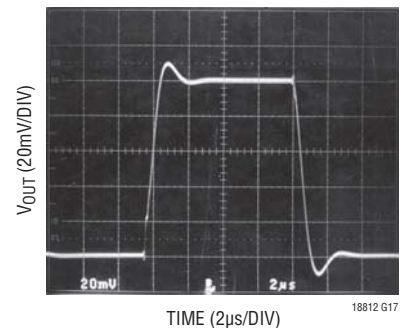
Small Signal Response, $A_V = -1$, $C_L = 1000pF$



Small Signal Response, $A_V = 1$, $R_L = 2k$

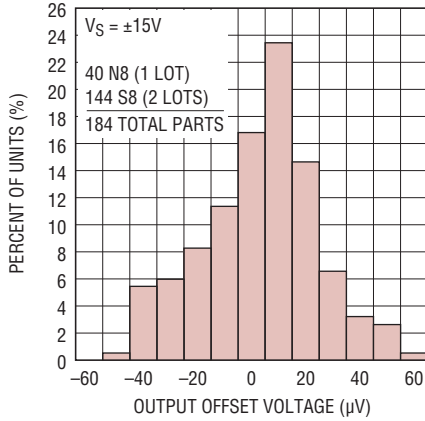


Small Signal Response, $A_V = 1$, $C_L = 500pF$



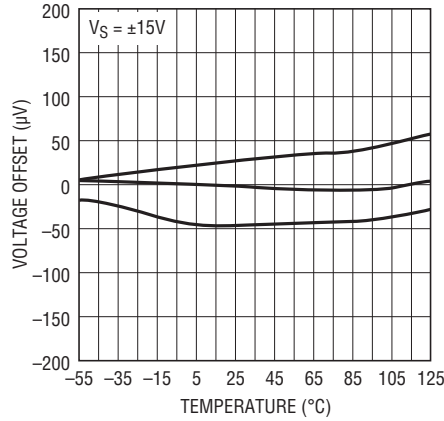
TYPICAL PERFORMANCE CHARACTERISTICS

V_{OS} Distribution, $T_A = 25^\circ\text{C}$



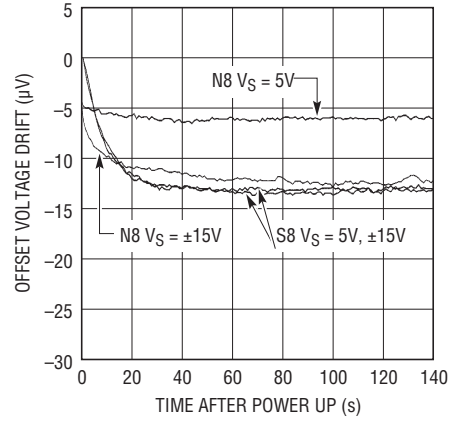
18812 G18

Voltage Offset vs Temperature



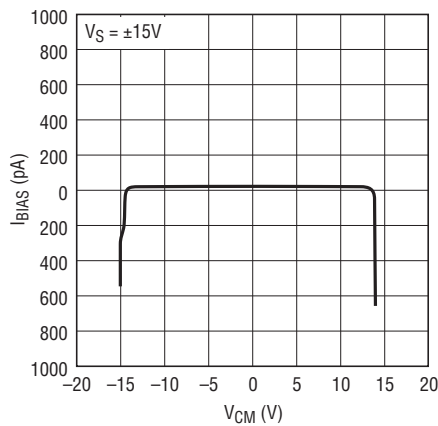
18812 G19

Warm-Up Drift vs Time



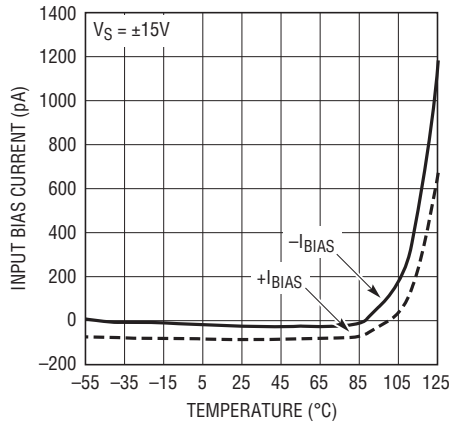
18812 G20

Input Bias Current vs Common Mode Voltage



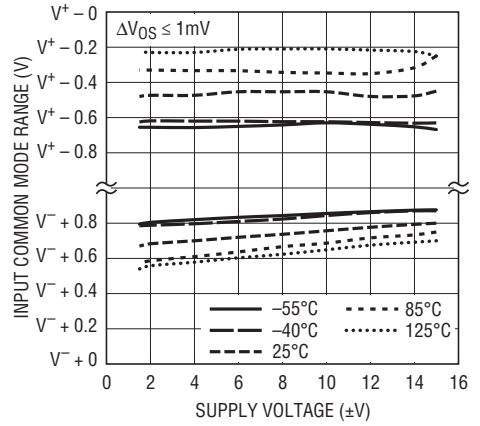
18812 G21

Input Bias Current vs Temperature



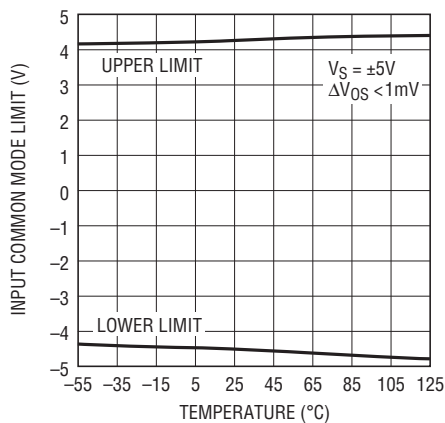
18812 G22

Input Common Mode Range vs Supply Voltage



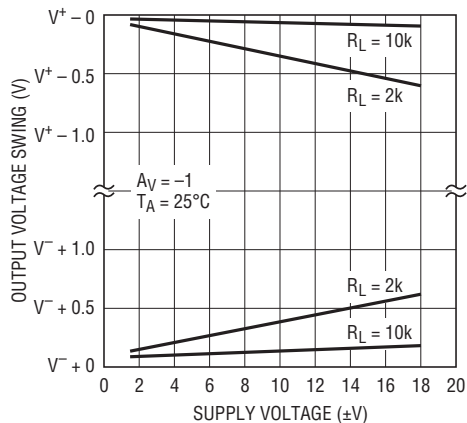
18812 G23

Input Common Mode Range vs Temperature



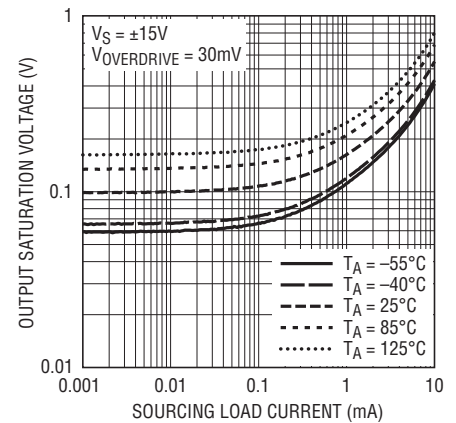
18812 G24

Output Voltage Swing vs Supply Voltage



18812 G25

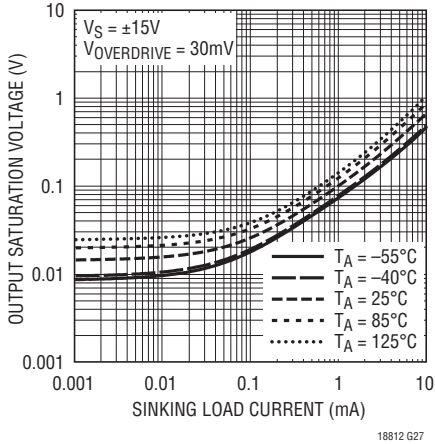
Output Saturation Voltage vs Load Current (Output High)



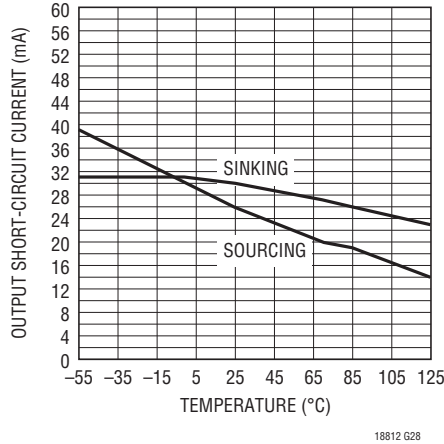
18812 G26

TYPICAL PERFORMANCE CHARACTERISTICS

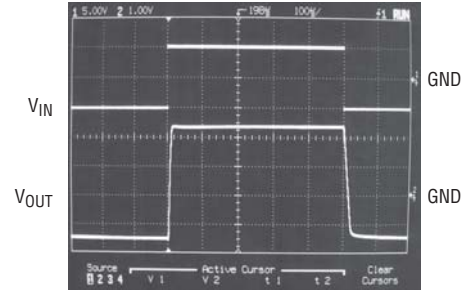
Output Saturation Voltage vs Load Current (Output Low)



Output Short-Circuit Current vs Temperature

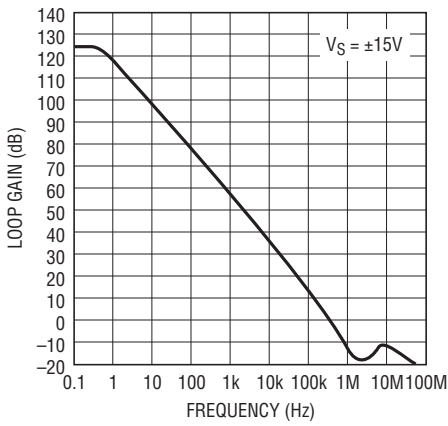


Output Voltage vs Large Input Voltage

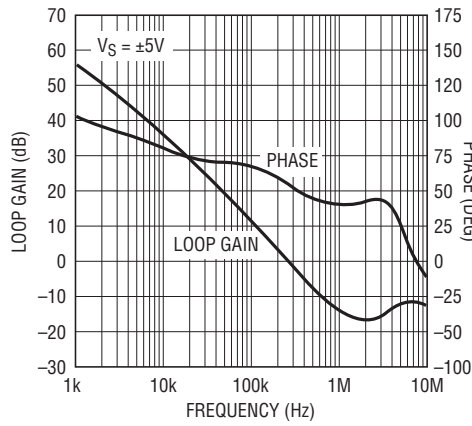


$A_V = 1$
 $V_S = \pm 2.5V$
 $V_{IN} = \pm 5V$
 $R_{IN} = 10k$

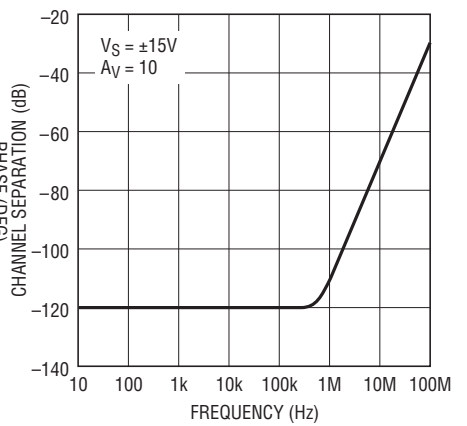
Open-Loop Gain vs Frequency



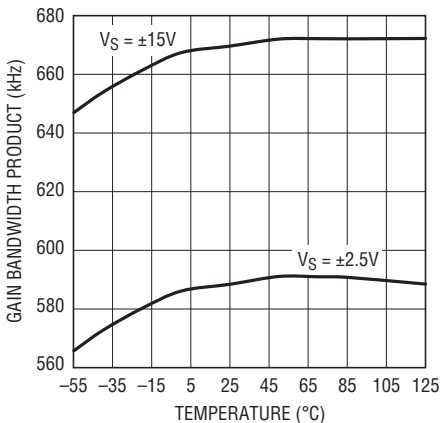
Open-Loop Gain and Phase vs Frequency



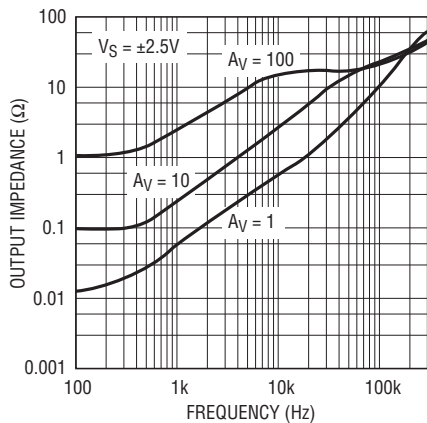
Channel Separation vs Frequency



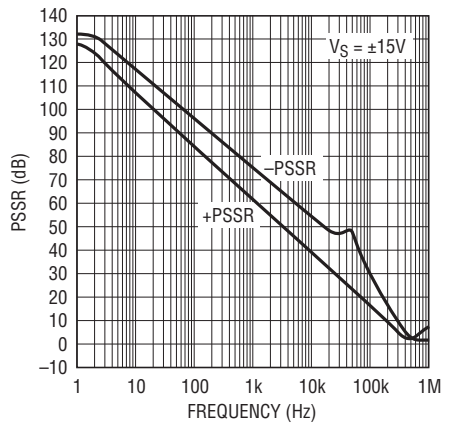
Gain Bandwidth Product vs Temperature



Output Impedance vs Frequency

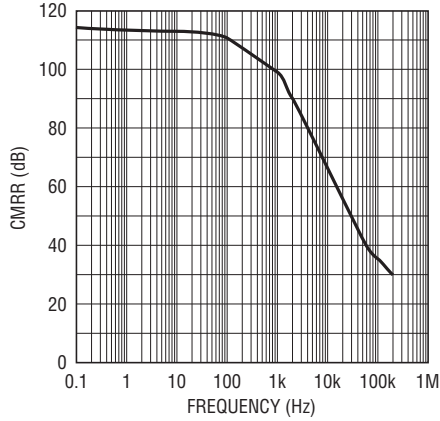


PSRR vs Frequency

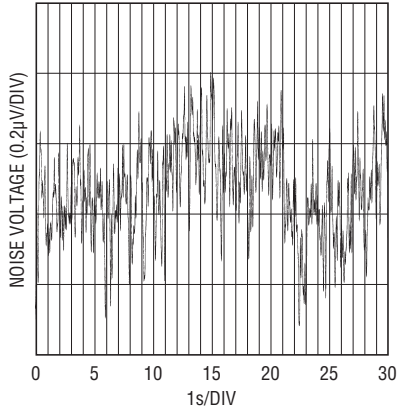


TYPICAL PERFORMANCE CHARACTERISTICS

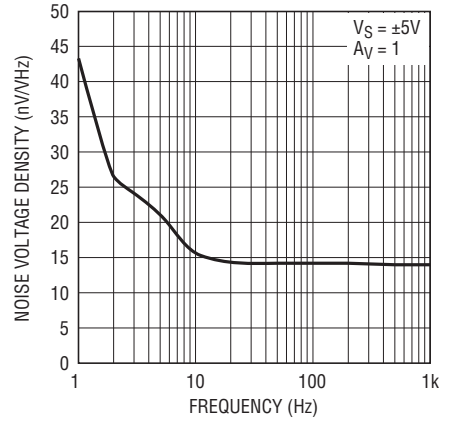
Common Mode Rejection Ratio vs Frequency



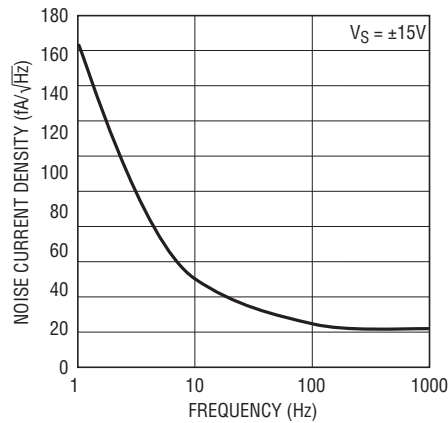
0.1Hz to 10Hz Noise



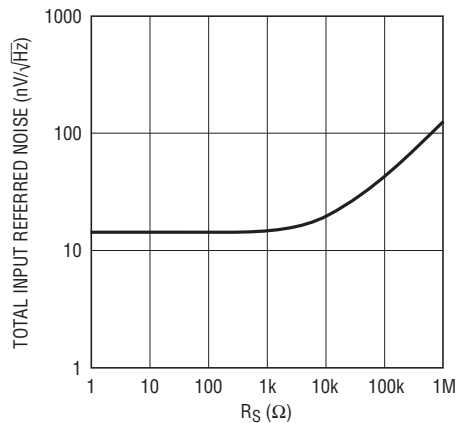
Noise Voltage vs Frequency



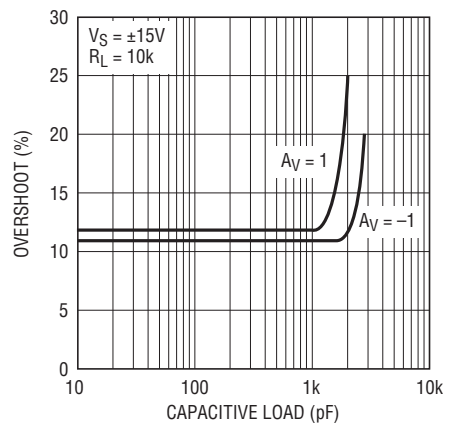
Noise Current Density vs Frequency



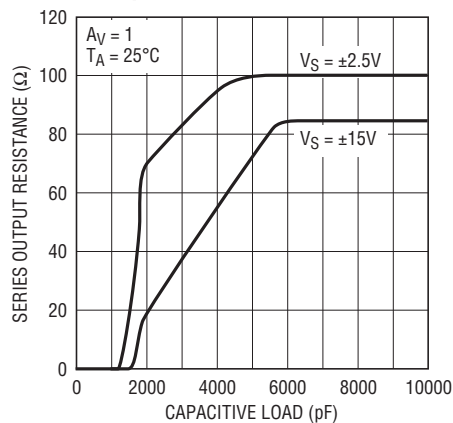
Total Noise vs Source Resistance



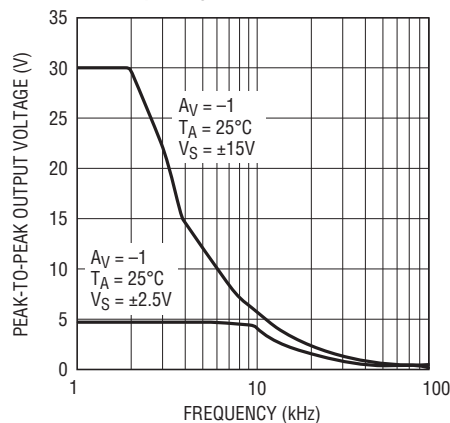
Overshoot vs Capacitive Load



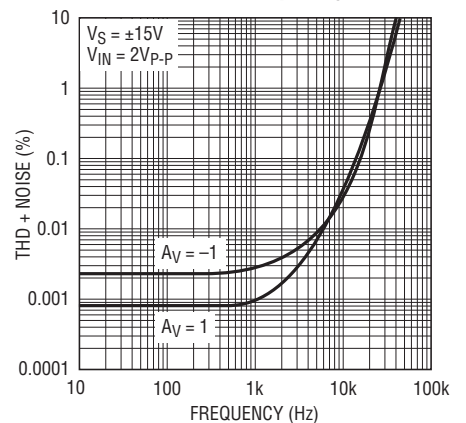
Series Output Resistance vs Capacitive Load



Undistorted Output Swing vs Frequency

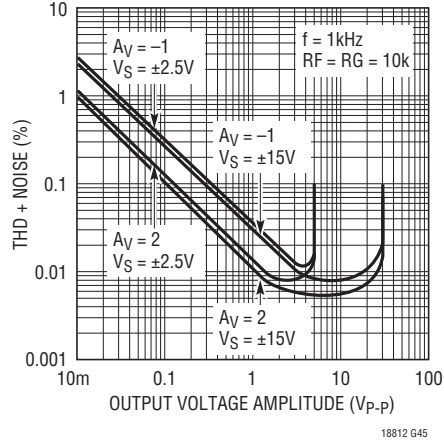


THD + Noise vs Frequency

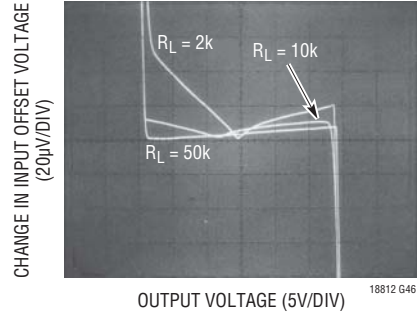


TYPICAL PERFORMANCE CHARACTERISTICS

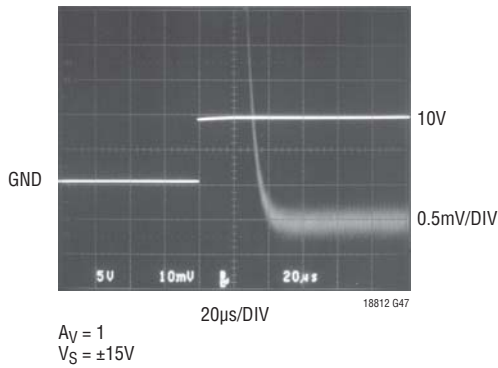
Total Harmonic Distortion + Noise vs Output Voltage Amplitude



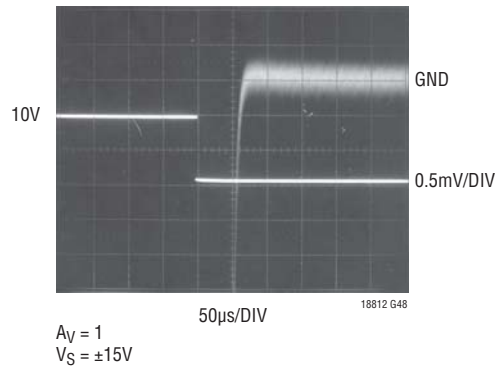
Open-Loop Gain



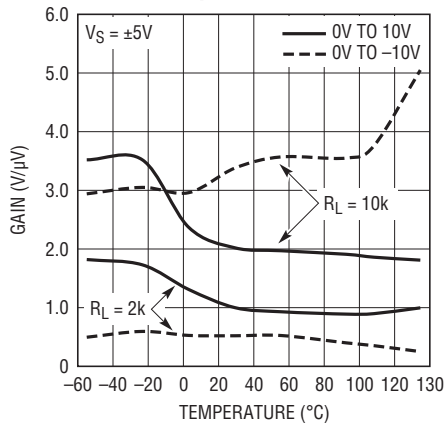
Settling Time/Output Step 0.01%



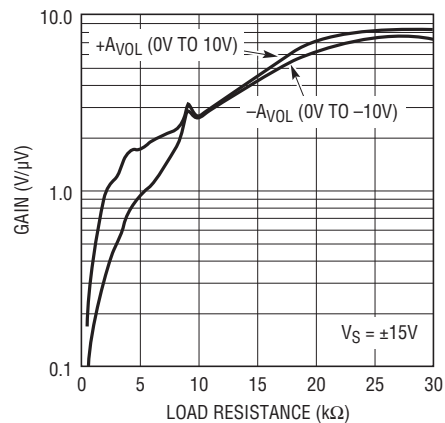
Settling Time/Output Step 0.01%



Gain vs Temperature



Gain vs Load Resistance



APPLICATIONS INFORMATION

The LT1881 dual and LT1882 quad op amps feature exceptional input precision with rail-to-rail output swing. The amplifiers are similar to the LT1884 and LT1885 devices. The LT1881 and LT1882 offer superior capacitive load driving capabilities over the LT1884 and LT1885 in low voltage gain configurations. Offset voltages are trimmed to less than $50\mu\text{V}$ and input bias currents are less than 200pA on the “A” grade devices. Obtaining beneficial advantage of these precision input characteristics depends upon proper applications circuit design and board layout.

Preserving Input Precision

Preserving the input voltage accuracy of the LT1881/LT1882 requires that the applications circuit and PC board layout do not introduce errors comparable to or greater than the $30\mu\text{V}$ offset. Temperature differentials across the input connections can generate thermocouple voltages of 10's of microvolts. PC board layouts should keep connections to the amplifier's input pins close together and away from heat dissipating components. Air currents across the board can also generate temperature differentials.

The extremely low input bias currents, 150pA , allow high accuracy to be maintained with high impedance sources and feedback networks. The LT1881/LT1882's low input bias currents are obtained by using a cancellation circuit on-chip. This causes the resulting $I_{\text{BIAS}+}$ and $I_{\text{BIAS}-}$ to be uncorrelated, as implied by the I_{OS} specification being greater than the I_{BIAS} . The user should not try to balance the input resistances in each input lead, as is commonly recommended with most amplifiers. The impedance at either input should be kept as small as possible to minimize total circuit error.

PC board layout is important to insure that leakage currents do not corrupt the low I_{BIAS} of the amplifier. In high precision, high impedance circuits, the input pins should be surrounded by a guard ring of PC board interconnect, with the guard driven to the same common mode voltage as the amplifier inputs.

Input Common Mode Range

The LT1881 and LT1882 outputs are able to swing nearly to each power supply rail, but the input stage is limited to operating between $V^- + 1\text{V}$ and $V^+ - 1\text{V}$. Exceeding this common mode range will cause the gain to drop to zero; however, no phase reversal will occur.

Input Protection

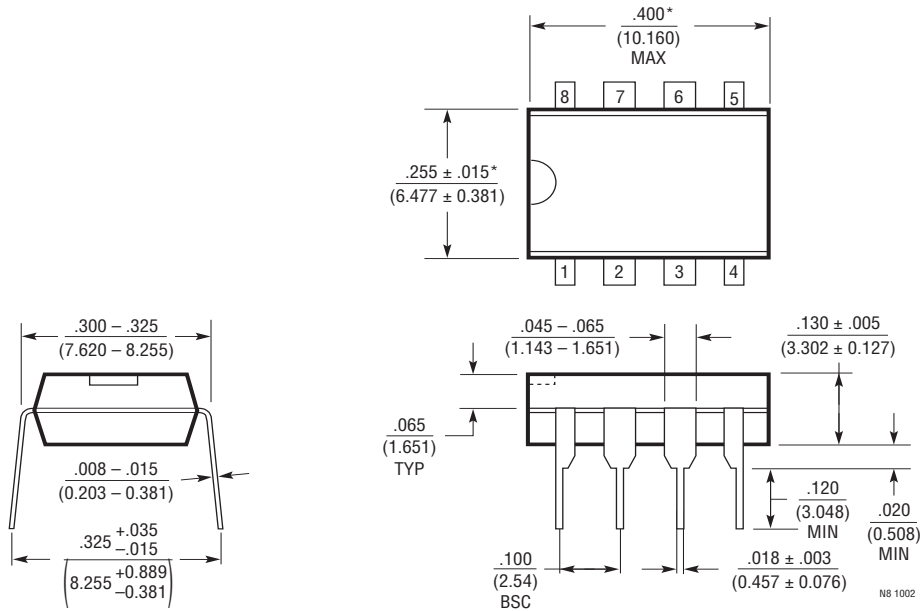
The inverting and noninverting input pins of the LT1881 and LT1882 have limited on-chip protection. ESD protection is provided to prevent damage during handling. The input transistors have voltage clamping and limiting resistors to protect against input differentials up to 10V . Short transients above this level will also be tolerated. If the input pins can see a sustained differential voltage above 10V , external limiting resistors should be used to prevent damage to the amplifier. A 1k resistor in each input lead will provide protection against a 30V differential voltage.

Capacitive Loads

The LT1881 and LT1882 can drive capacitive loads up to 1000pF in unity-gain. The capacitive load driving increases as the amplifier is used in higher gain configurations. Capacitive load driving may be increased by decoupling the capacitance from the output with a small resistance.

PACKAGE DESCRIPTION

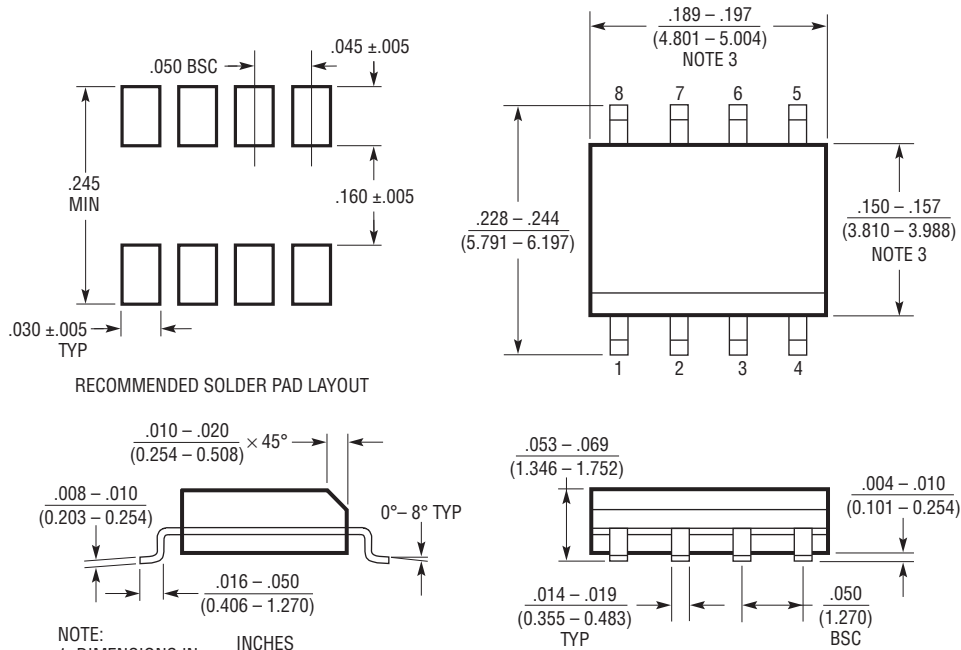
N8 Package
8-Lead PDIP (Narrow 0.300)
 (LTC DWG # 05-08-1510)



NOTE:
 1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
 *THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
 (LTC DWG # 05-08-1610)

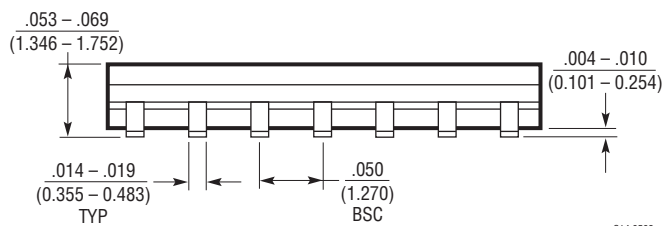
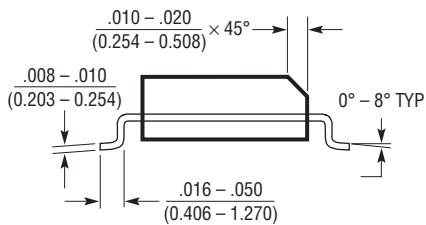
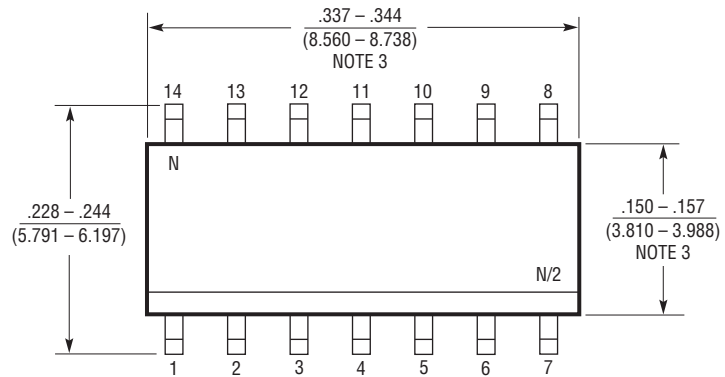
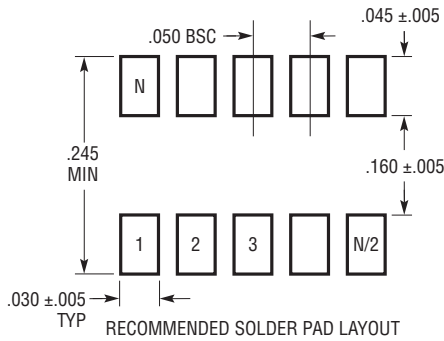


- NOTE:
 1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
 2. DRAWING NOT TO SCALE
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED $.006''$ (0.15mm)

S08 0303

PACKAGE DESCRIPTION

S Package 14-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



- NOTE:
 1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
 2. DRAWING NOT TO SCALE
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S14 0502