# Dual 700MHz, 200mA Operational Amplifier

## FEATURES

- **700MHz Gain Bandwidth**
- **±200mA Minimum $I_{OUT}$**
- **Low Distortion: –72dBc at 1MHz, $4V_{P-P}$, 25Ω, $A_V$ = 2**
- Stable in $A_V \geq 10$, Simple Compensation for $A_V < 10$
- ±4.3V Minimum Output Swing, $V_S$ = ±6V, $R_L$ = 25Ω
- 7mA Supply Current per Amplifier
- 200V/µs Slew Rate
- Stable with 1000pF Load
- 6nV/√Hz Input Noise Voltage
- 2pA/√Hz Input Noise Current
- 4mV Maximum Input Offset Voltage
- 4µA Maximum Input Bias Current
- 400nA Maximum Input Offset Current
- ±4.5V Minimum Input CMR, $V_S$ = ±6V
- Specified at ±6V, ±2.5V

## APPLICATIONS

- DSL Modems
- xDSL PCI Cards
- USB Modems
- Line Drivers

## DESCRIPTION

The LT®1886 is a 200mA minimum output current dual op amp with outstanding distortion performance. The amplifiers are gain-of-ten stable, but can be easily compensated for lower gains. The LT1886 features balanced, high impedance inputs with 4µA maximum input bias current, and 4mV maximum input offset voltage. Single supply applications are easy to implement and have lower total noise than current feedback amplifier implementations.

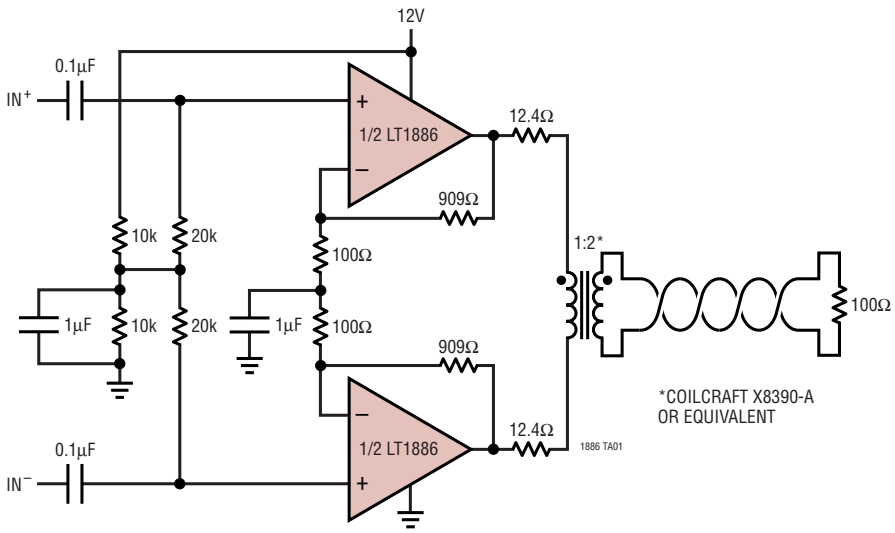
The output drives a 25Ω load to ±4.3V with ±6V supplies. On ±2.5V supplies the output swings ±1.5V with a 100Ω load. The amplifier is stable with a 1000pF capacitive load which makes it useful in buffer and cable driver applications.

The LT1886 is manufactured on Linear Technology's advanced low voltage complementary bipolar process and is available in a thermally enhanced SO-8 package.

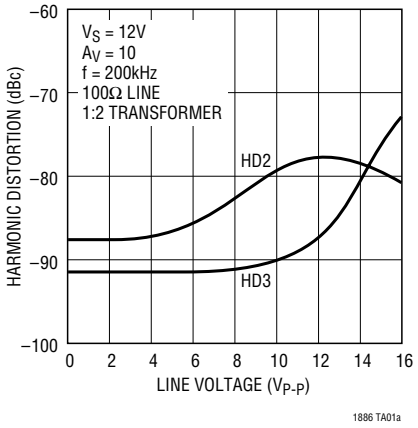


## TYPICAL APPLICATION

**Single 12V Supply ADSL Modem Line Driver**




**ADSL Modem Line Driver Distortion**

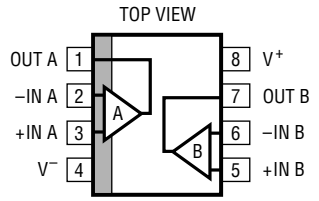


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Total Supply Voltage ($V^+$ to $V^-$) ..... 13.2V
Input Current (Note 2) ..... ±10mA
Input Voltage (Note 2) ..... $\pm V_S$
Maximum Continuous Output Current (Note 3)
DC ..... ±100mA
AC ..... ±300mA
Operating Temperature Range (Note 10) –40°C to 85°C
Specified Temperature Range (Note 9) .. –40°C to 85°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

## PACKAGE/ORDER INFORMATION




S8 PACKAGE
8-LEAD PLASTIC SO

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 80°C/W (Note 4)

| ORDER PART NUMBER |
|---|
| LT1886CS8 |
| **S8 PART MARKING** |
| 1886 |

Consult factory for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = ±6V, $V_{CM}$ = 0V, pulse power tested unless otherwise noted. (Note 9)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | (Note 5) | <br>● | | 1 | 4<br>5 | mV<br>mV |
| | Input Offset Voltage Drift | (Note 8) | ● | | 3 | 17 | µV/°C |
| $I_{OS}$ | Input Offset Current | | <br>● | | 150 | 400<br>600 | nA<br>nA |
| $I_B$ | Input Bias Current | | <br>● | | 1.5 | 4<br>6 | µA<br>µA |
| $e_n$ | Input Noise Voltage | f = 10kHz | | | 6 | | nV/√Hz |
| $i_n$ | Input Noise Current | f = 10kHz | | | 2 | | pA/√Hz |
| $R_{IN}$ | Input Resistance | $V_{CM}$ = ±4.5V<br>Differential | | 5 | 10<br>35 | | MΩ<br>kΩ |
| $C_{IN}$ | Input Capacitance | | | | 2 | | pF |
| | Input Voltage Range (Positive)<br>Input Voltage Range (Negative) | | ●<br>● | 4.5 | 5.9<br>–5.2 | <br>–4.5 | V<br>V |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ = ±4.5V | ● | 77 | 98 | | dB |
| | Minimum Supply Voltage | Guaranteed by PSRR | ● | | | ±2 | V |
| PSRR | Power Supply Rejection Ratio | $V_S$ = ±2V to ±6.5V | <br>● | 80<br>78 | 86 | | dB<br>dB |
| $A_{VOL}$ | Large-Signal Voltage Gain | $V_{OUT}$ = ±4V, $R_L$ = 100Ω | <br>● | 5.0<br>4.5 | 12 | | V/mV<br>V/mV |
| | | $V_{OUT}$ = ±4V, $R_L$ = 25Ω | <br>● | 4.5<br>4.0 | 12 | | V/mV<br>V/mV |
| $V_{OUT}$ | Output Swing | $R_L$ = 100Ω, 10mV Overdrive | <br>● | 4.85<br>4.70 | 5 | | ±V<br>±V |
| | | $R_L$ = 25Ω, 10mV Overdrive | <br>● | 4.30<br>4.10 | 4.6 | | ±V<br>±V |
| | | $I_{OUT}$ = 200mA, 10mV Overdrive | <br>● | 4.30<br>4.10 | 4.5 | | ±V<br>±V |
| $I_{SC}$ | Short-Circuit Current (Sourcing)<br>Short-Circuit Current (Sinking) | (Note 3) | | | 800<br>500 | | mA<br>mA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = ±6V, $V_{CM}$ = 0V, pulse power tested unless otherwise noted. (Note 9)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| SR | Slew Rate | $A_V$ = –10 (Note 6) | <br>● | 133<br>110 | 200 | | V/µs<br>V/µs |
| | Full Power Bandwidth | 4V Peak (Note 7) | | | 8 | | MHz |
| GBW | Gain Bandwidth | f = 1MHz | | | 700 | | MHz |
| $t_r$, $t_f$ | Rise Time, Fall Time | $A_V$ = 10, 10% to 90% of 0.1V, $R_L$ = 100Ω | | | 4 | | ns |
| | Overshoot | $A_V$ = 10, 0.1V, $R_L$ = 100Ω | | | 1 | | % |
| | Propagation Delay | $A_V$ = 10, 50% $V_{IN}$ to 50% $V_{OUT}$, 0.1V, $R_L$ = 100Ω | | | 2.5 | | ns |
| $t_S$ | Settling Time | 6V Step, 0.1% | | | 50 | | ns |
| | Harmonic Distortion | HD2, $A_V$ = 10, $2V_{P-P}$, f = 1MHz, $R_L$ = 100Ω/25Ω<br>HD3, $A_V$ = 10, $2V_{P-P}$, f = 1MHz, $R_L$ = 100Ω/25Ω | | | –75/–63<br>–85/–71 | | dBc<br>dBc |
| IMD | Intermodulation Distortion | $A_V$ = 10, f = 0.9MHz, 1MHz, 14dBm, $R_L$ = 100Ω/25Ω | | | –81/–80 | | dBc |
| $R_{OUT}$ | Output Resistance | $A_V$ = 10, f = 1MHz | | | 0.1 | | Ω |
| | Channel Separation | $V_{OUT}$ = ±4V, $R_L$ = 25Ω | <br>● | 82<br>80 | 92 | | dB<br>dB |
| $I_S$ | Supply Current | Per Amplifier | <br>● | | 7 | 8.25<br>8.50 | mA<br>mA |

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = ±2.5V, $V_{CM}$ = 0V, pulse power tested unless otherwise noted. (Note 9)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | (Note 5) | <br>● | | 1.5 | 5<br>6 | mV<br>mV |
| | Input Offset Voltage Drift | (Note 8) | ● | | 5 | 17 | µV/°C |
| $I_{OS}$ | Input Offset Current | | <br>● | | 100 | 350<br>550 | nA<br>nA |
| $I_B$ | Input Bias Current | | <br>● | | 1.2 | 3.5<br>5.5 | µA<br>µA |
| $e_n$ | Input Noise Voltage | f = 10kHz | | | 6 | | nV/√Hz |
| $i_n$ | Input Noise Current | f = 10kHz | | | 2 | | pA/√Hz |
| $R_{IN}$ | Input Resistance | $V_{CM}$ = ±1V<br>Differential | | 10 | 20<br>50 | | MΩ<br>kΩ |
| $C_{IN}$ | Input Capacitance | | | | 2 | | pF |
| | Input Voltage Range (Positive)<br>Input Voltage Range (Negative) | | ●<br>● | 1 | 2.4<br>–1.7 | <br>–1 | V<br>V |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ = ±1V | ● | 75 | 91 | | dB |
| $A_{VOL}$ | Large-Signal Voltage Gain | $V_{OUT}$ = ±1V, $R_L$ = 100Ω | <br>● | 5.0<br>4.5 | 10 | | V/mV<br>V/mV |
| | | $V_{OUT}$ = ±1V, $R_L$ = 25Ω | <br>● | 4.5<br>4.0 | 10 | | V/mV<br>V/mV |
| $V_{OUT}$ | Output Swing | $R_L$ = 100Ω, 10mV Overdrive | <br>● | 1.50<br>1.40 | 1.65 | | ±V<br>±V |
| | | $R_L$ = 25Ω, 10mV Overdrive | <br>● | 1.35<br>1.25 | 1.50 | | ±V<br>±V |
| | | $I_{OUT}$ = 200mA, 10mV Overdrive | <br>● | 0.87<br>0.80 | 1 | | ±V<br>±V |

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_S$ = ±2.5V, $V_{CM}$ = 0V, pulse power tested unless otherwise noted. (Note 9)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $I_{SC}$ | Short-Circuit Current (Sourcing)<br>Short-Circuit Current (Sinking) | (Note 3) | | | 600<br>400 | | mA<br>mA |
| SR | Slew Rate | $A_V$ = –10 (Note 6) | <br>● | 66<br>60 | 100 | | V/µs<br>V/µs |
| | Full Power Bandwidth | 1V Peak (Note 7) | | | 16 | | MHz |
| GBW | Gain Bandwidth | f = 1MHz | | | 530 | | MHz |
| $t_r$, $t_f$ | Rise Time, Fall Time | $A_V$ = 10, 10% to 90% of 0.1V, $R_L$ = 100Ω | | | 7 | | ns |
| | Overshoot | $A_V$ = 10, 0.1V, $R_L$ = 100Ω | | | 5 | | % |
| | Propagation Delay | $A_V$ = 10, 50% $V_{IN}$ to 50% $V_{OUT}$, 0.1V, $R_L$ = 100Ω | | | 5 | | ns |
| | Harmonic Distortion | HD2, $A_V$ = 10, $2V_{P-P}$, f = 1MHz, $R_L$ = 100Ω/25Ω<br>HD3, $A_V$ = 10, $2V_{P-P}$, f = 1MHz, $R_L$ = 100Ω/25Ω | | | –75/–64<br>–80/–66 | | dBc<br>dBc |
| IMD | Intermodulation Distortion | $A_V$ = 10, f = 0.9MHz, 1MHz, 5dBm, $R_L$ = 100Ω/25Ω | | | –77/–85 | | dBc |
| $R_{OUT}$ | Output Resistance | $A_V$ = 10, f = 1MHz | | | 0.2 | | Ω |
| | Channel Separation | $V_{OUT}$ = ±1V, $R_L$ = 25Ω | <br>● | 82<br>80 | 92 | | dB<br>dB |
| $I_S$ | Supply Current | Per Amplifier | <br>● | | 5 | 5.75<br>6.25 | mA<br>mA |

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** The inputs are protected by back-to-back diodes. If the differential input voltage exceeds 0.7V, the input current should be limited to less than 10mA.

**Note 3:** A heat sink may be required to keep the junction temperature below absolute maximum.

**Note 4:** Thermal resistance varies depending upon the amount of PC board metal attached to the device. $\theta_{JA}$ is specified for a 2500mm$^2$ test board covered with 2 oz copper on both sides.

**Note 5:** Input offset voltage is exclusive of warm-up drift.

**Note 6:** Slew rate is measured between ±2V on a ±4V output with ±6V supplies, and between ±1V on a ±1.5V output with ±2.5V supplies.

**Note 7:** Full power bandwidth is calculated from the slew rate: FPBW = SR/2π$V_P$.

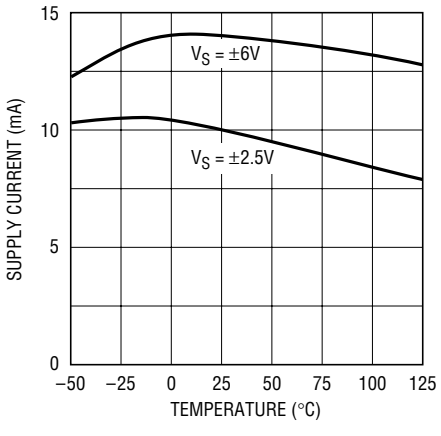
**Note 8:** This parameter is not 100% tested.

**Note 9:** The LT1886C is guaranteed to meet specified performance from 0°C to 70°C. The LT1886C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. For guaranteed I-grade parts, consult the factory.

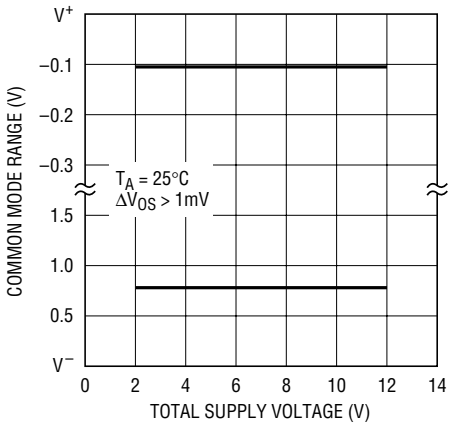
**Note 10:** The LT1886C is guaranteed functional over the operating temperature range of –40°C to 85°C.

## TYPICAL PERFORMANCE CHARACTERISTICS

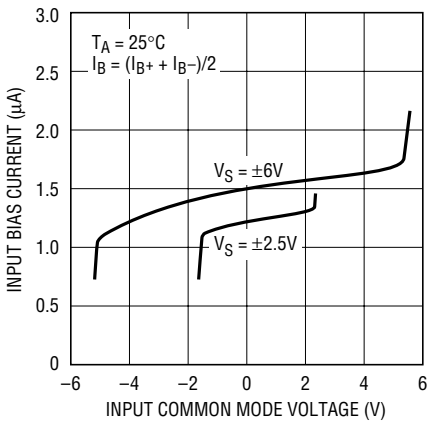
**Supply Current vs Temperature**




**Input Common Mode Range vs Supply Voltage**

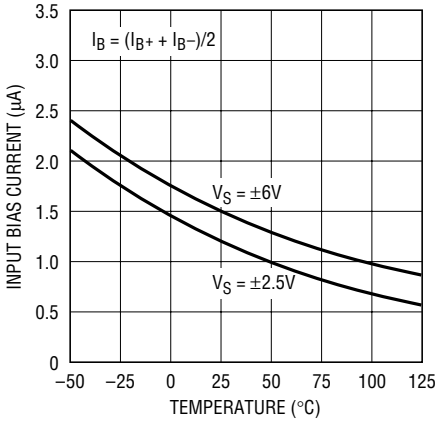



**Input Bias Current vs Input Common Mode Voltage**



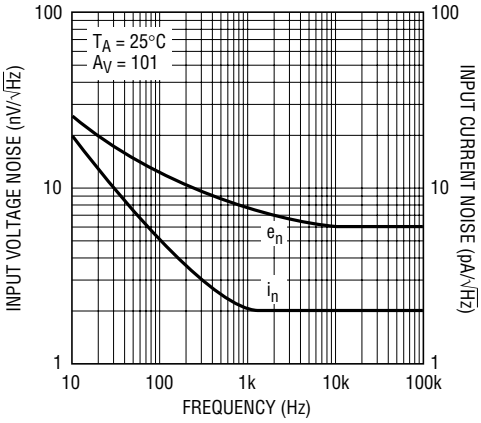
# TYPICAL PERFORMANCE CHARACTERISTICS

### Input Bias Current vs Temperature



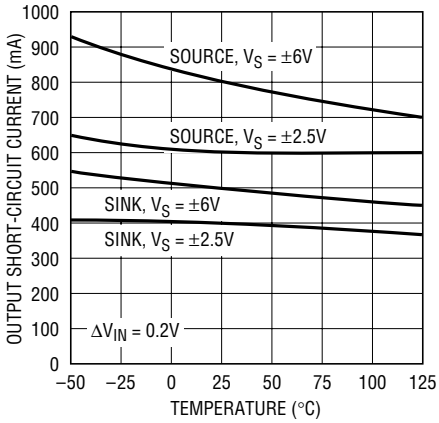

1886 G04

### Input Noise Spectral Density



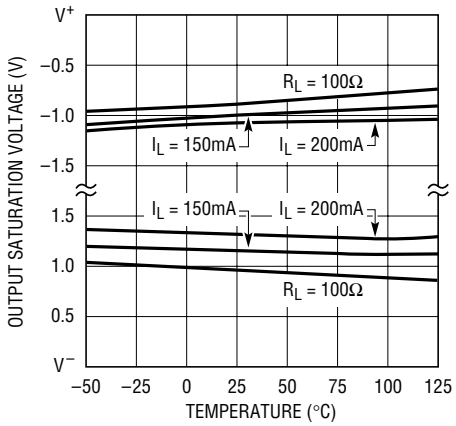

1886 G05

### Output Short-Circuit Current vs Temperature



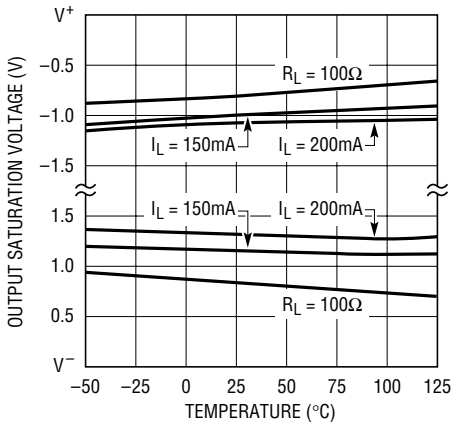

1886 G06

### Output Saturation Voltage vs Temperature, $V_S = \pm 6V$



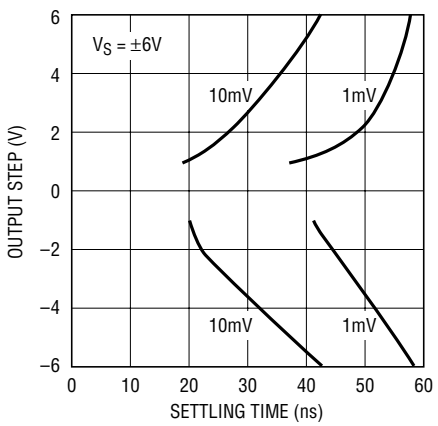

1886 G07

### Output Saturation Voltage vs Temperature, $V_S = \pm 2.5V$



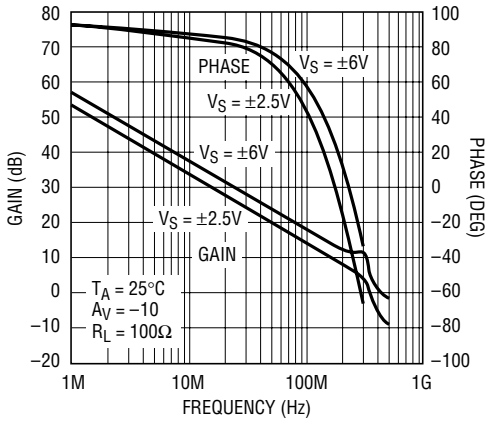

1886 G08

### Settling Time vs Output Step



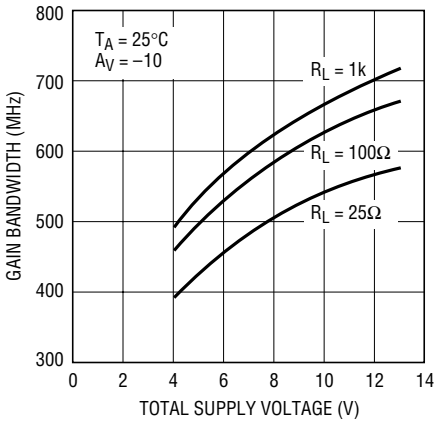

1886 G09

### Gain and Phase vs Frequency



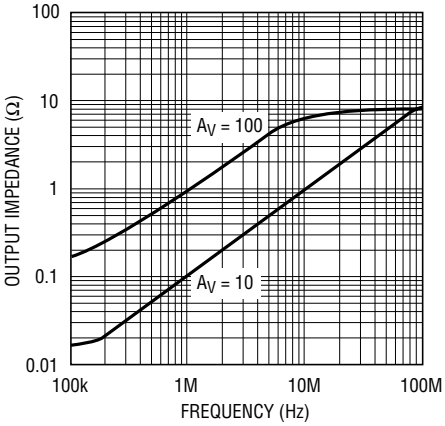

1886 G10

### Gain Bandwidth vs Supply Voltage




1886 G11

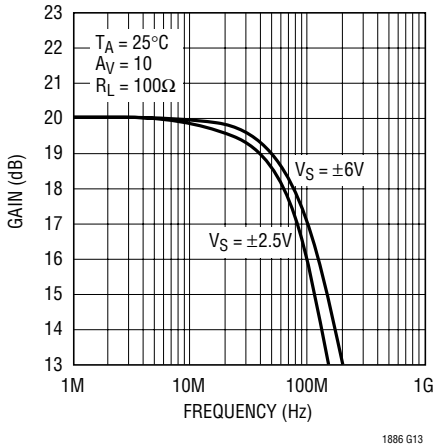
### Output Impedance vs Frequency



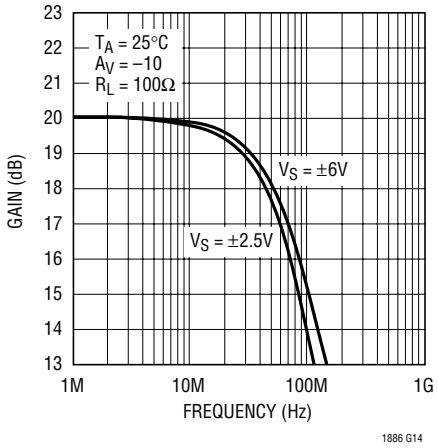

1886 G12

# TYPICAL PERFORMANCE CHARACTERISTICS

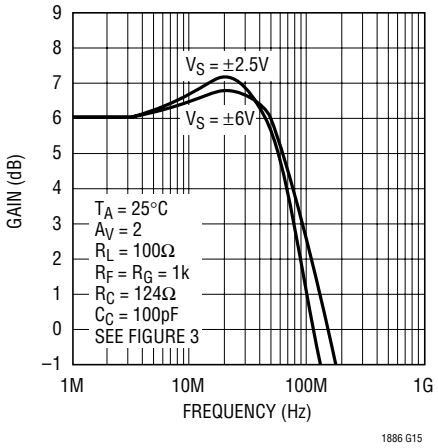
### Frequency Response vs Supply Voltage, $A_V = 10$



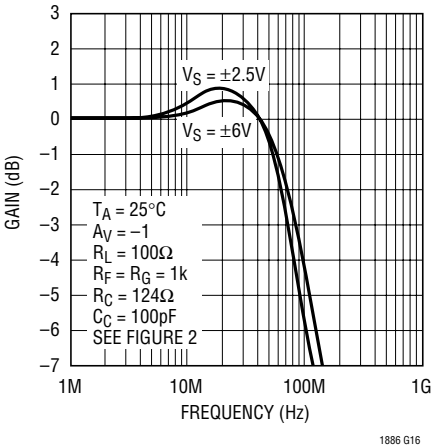

### Frequency Response vs Supply Voltage, $A_V = -10$



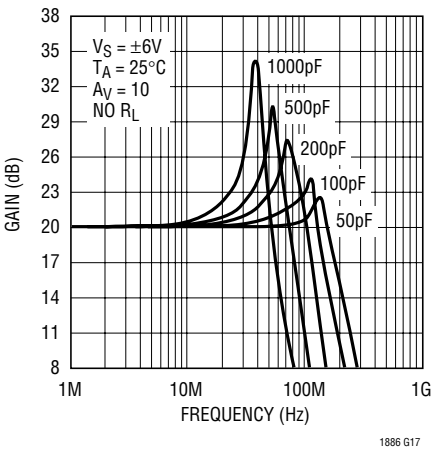

### Frequency Response vs Supply Voltage, $A_V = 2$



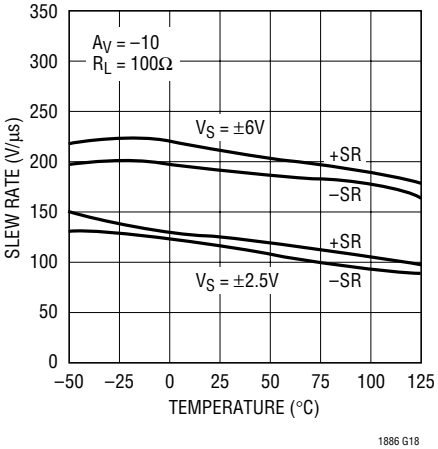

### Frequency Response vs Supply Voltage, $A_V = -1$



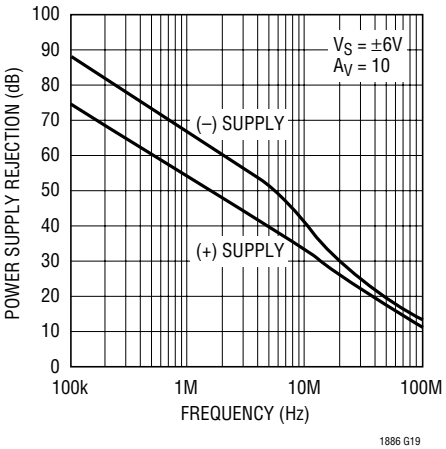

### Frequency Response vs Capacitive Load



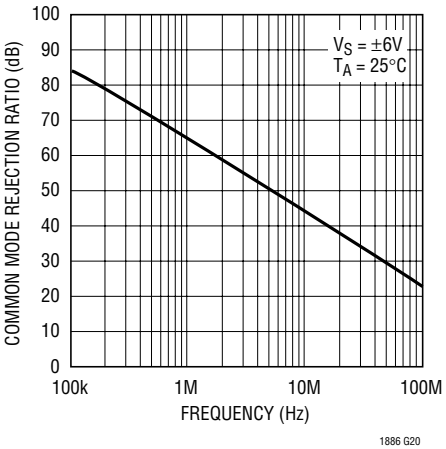

### Slew Rate vs Temperature



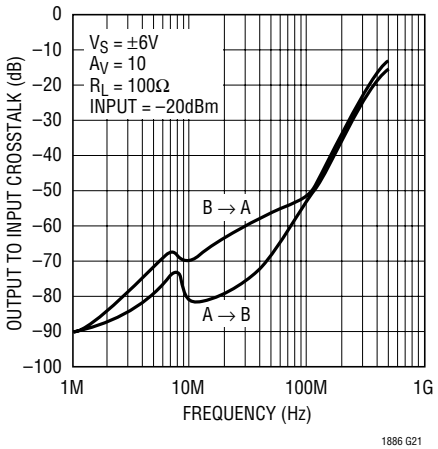

### Power Supply Rejection vs Frequency




### Common Mode Rejection Ratio vs Frequency

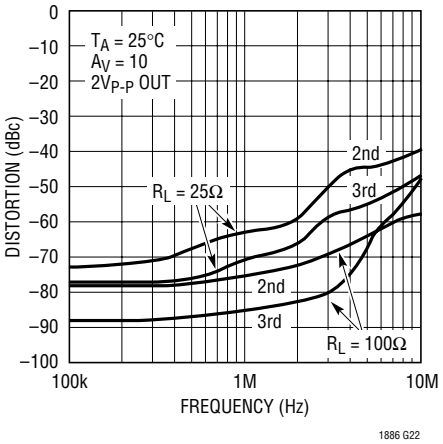



### Amplifier Crosstalk vs Frequency



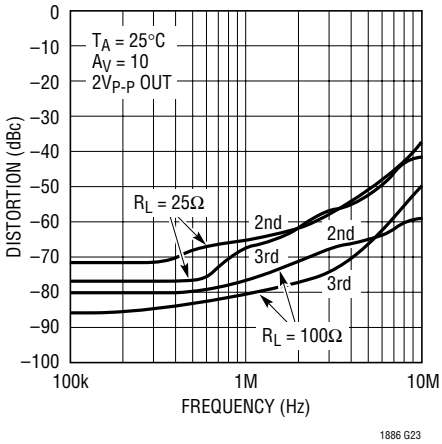
# TYPICAL PERFORMANCE CHARACTERISTICS

### Harmonic Distortion vs Frequency, $A_V = 10$, $V_S = \pm 6V$



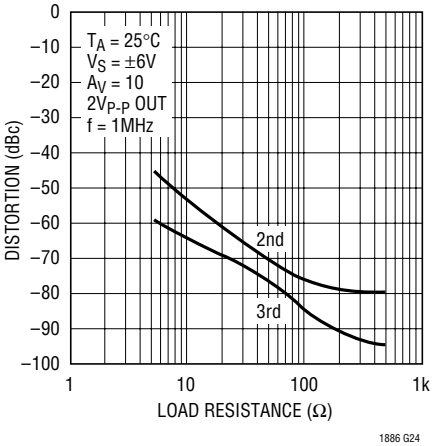

1886 G22

### Harmonic Distortion vs Frequency, $A_V = 10$, $V_S = \pm 2.5V$



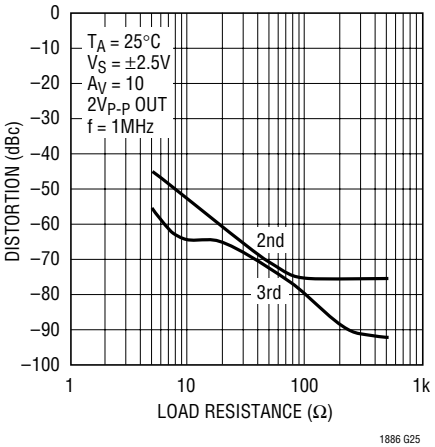

1886 G23

### Harmonic Distortion vs Resistive Load



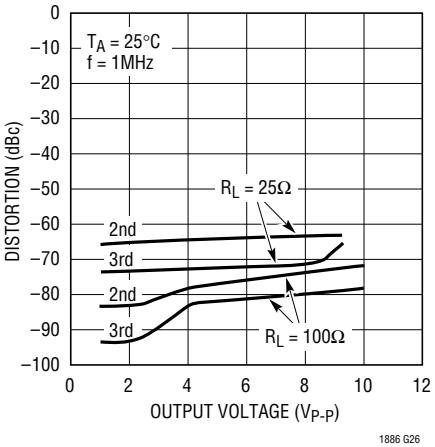

1886 G24

### Harmonic Distortion vs Resistive Load



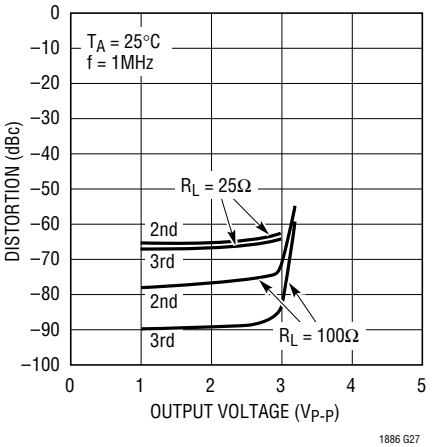

1886 G25

### Harmonic Distortion vs Output Swing, $A_V = 10$, $V_S = \pm 6V$



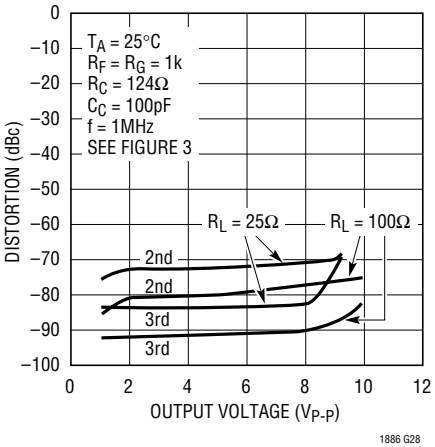

1886 G26

### Harmonic Distortion vs Output Swing, $A_V = 10$, $V_S = \pm 2.5V$



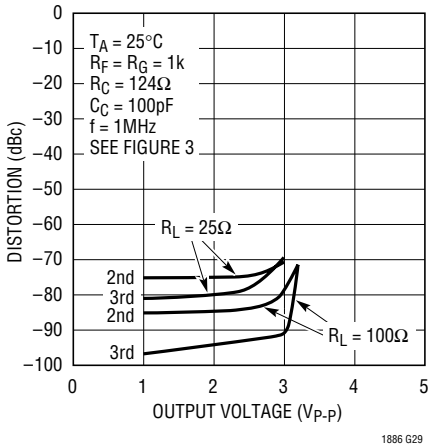

1886 G27

### Harmonic Distortion vs Output Swing, $A_V = 2$, $V_S = \pm 6V$



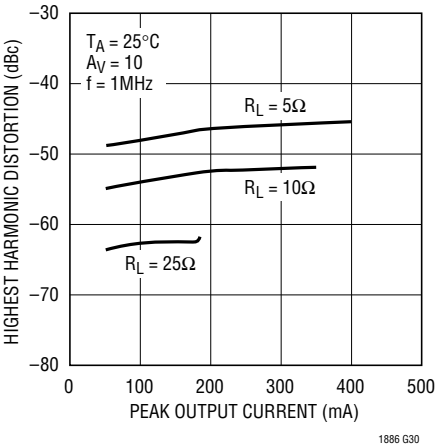

1886 G28

### Harmonic Distortion vs Output Swing, $A_V = 2$, $V_S = \pm 2.5V$




1886 G29

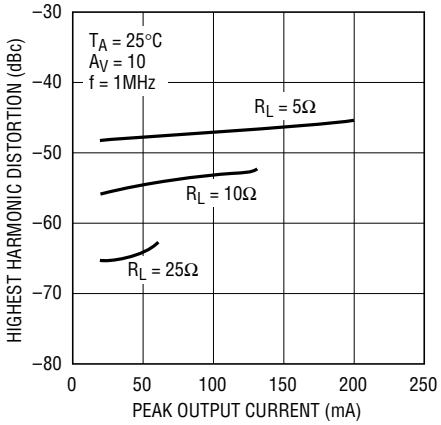
### Harmonic Distortion vs Output Current, $V_S = \pm 6V$




1886 G30

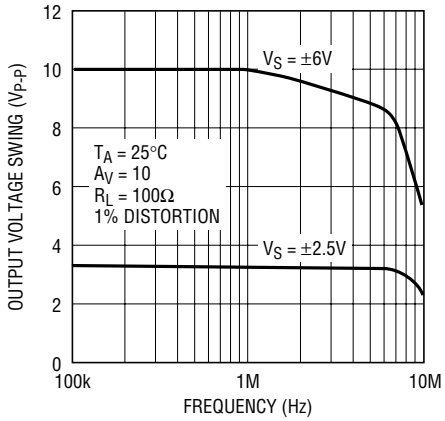
## TYPICAL PERFORMANCE CHARACTERISTICS

**Harmonic Distortion vs Output Current, $V_S = \pm 2.5V$**



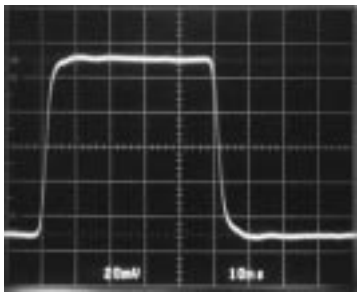

1886 G30

**Undistorted Output Swing vs Frequency**



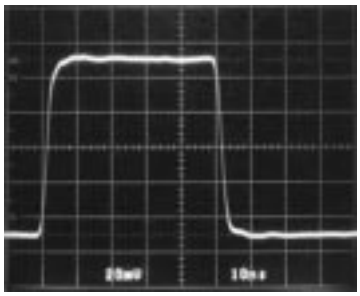

1886 G32

**Small-Signal Transient, $A_V = 10$**



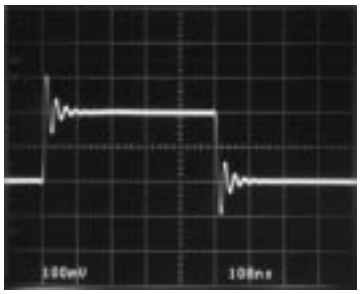
1886 G33

**Small-Signal Transient, $A_V = -10$**



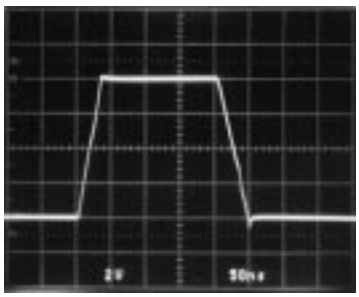
1886 G34

**Small-Signal Transient, $A_V = 10$, $C_L = 1000pF$**



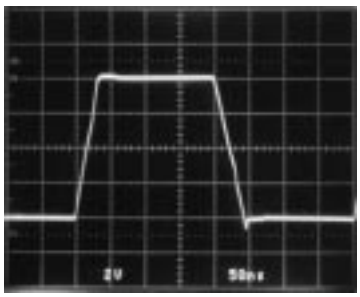
1886 G35

**Large-Signal Transient, $A_V = 10$**



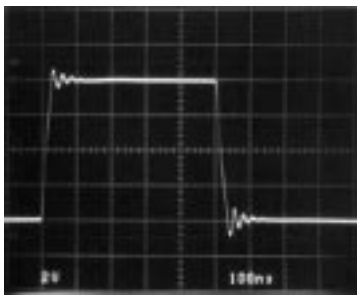
1886 G36

**Large-Signal Transient, $A_V = -10$**



1886 G37

**Large-Signal Transient, $A_V = 10$, $C_L = 1000pF$**



1886 G38

## APPLICATIONS INFORMATION

### Input Considerations

The inputs of the LT1886 are an NPN differential pair protected by back-to-back diodes (see the Simplified Schematic). There are no series protection resistors onboard which would degrade the input voltage noise. If the inputs can have a voltage difference of more than 0.7V, the input current should be limited to less than 10mA with external resistance (usually the feedback resistor or source resistor). Each input also has two ESD clamp diodes—one to each supply. If an input drive exceeds the supply, limit the current with an external resistor to less than 10mA.

The LT1886 design is a true operational amplifier with high impedance inputs and low input bias currents. The input offset current is a factor of ten lower than the input bias current. To minimize offsets due to input bias currents, match the equivalent DC resistance seen by both inputs. The low input noise current can significantly reduce total noise compared to a current feedback amplifier, especially for higher source resistances.

### Layout and Passive Components

With a gain bandwidth product of 700MHz the LT1886 requires attention to detail in order to extract maximum performance. Use a ground plane, short lead lengths and a combination of RF-quality supply bypass capacitors (i.e., 470pF and 0.1µF). As the primary applications have high drive current, use low ESR supply bypass capacitors (1µF to 10µF). For best distortion performance with high drive current a capacitor with the shortest possible trace lengths should be placed between Pins 4 and 8. The optimum location for this capacitor is on the back side of the PC board. The DSL driver demo board (DC304) for this part uses a Taiyo Yuden 10µF ceramic (TMK432BJ106MM).

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause frequency peaking. In general, use feedback resistors of 1kΩ or less.

### Thermal Issues

The LT1886 enhanced $\theta_{JA}$ SO-8 package has the $V^-$ pin fused to the lead frame. This thermal connection increases the efficiency of the PC board as a heat sink. The PCB material can be very effective at transmitting heat between the pad area attached to the $V^-$ pin and a ground or power plane layer. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by the device. Table 1 lists the thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on 3/32" FR-4 board with 2oz copper. This data can be used as a rough guideline in estimating thermal resistance. The thermal resistance for each application will be affected by thermal interactions with other components as well as board size and shape.

**Table 1. Fused 8-Lead SO Package**

| COPPER AREA (2oz) | | TOTAL | |
|---|---|---|---|
| TOPSIDE | BACKSIDE | COPPER AREA | θJA |
| 2500 sq. mm | 2500 sq. mm | 5000 sq. mm | 80°C/W |
| 1000 sq. mm | 2500 sq. mm | 3500 sq. mm | 92°C/W |
| 600 sq. mm | 2500 sq. mm | 3100 sq. mm | 96°C/W |
| 180 sq. mm | 2500 sq. mm | 2680 sq. mm | 98°C/W |
| 180 sq. mm | 1000 sq. mm | 1180 sq. mm | 112°C/W |
| 180 sq. mm | 600 sq. mm | 780 sq. mm | 116°C/W |
| 180 sq. mm | 300 sq. mm | 480 sq. mm | 118°C/W |
| 180 sq. mm | 100 sq. mm | 280 sq. mm | 120°C/W |
| 180 sq. mm | 0 sq. mm | 180 sq. mm | 122°C/W |

### Calculating Junction Temperature

The junction temperature can be calculated from the equation:

$$T_J = (P_D)(\theta_{JA}) + T_A$$

$T_J$ = Junction Temperature

$T_A$ = Ambient Temperature

$P_D$ = Device Dissipation

$\theta_{JA}$ = Thermal Resistance (Junction-to-Ambient)

As an example, calculate the junction temperature for the circuit in Figure 1 assuming an 85°C ambient temperature.

The device dissipation can be found by measuring the supply currents, calculating the total dissipation and then subtracting the dissipation in the load.

## APPLICATIONS INFORMATION

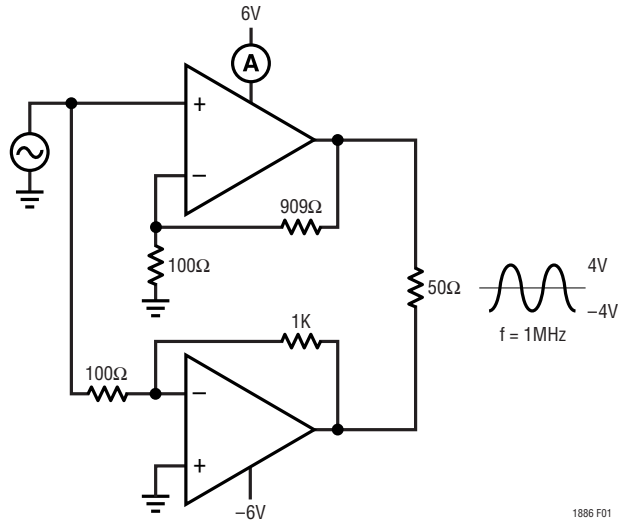



**Figure 1. Thermal Calculation Example**

The dissipation for the amplifiers is:

$$P_D = (63.5mA)(12V) – (4V/\sqrt{2})^2/(50) = 0.6W$$

The total package power dissipation is 0.6W. When a 2500 sq. mm PC board with 2oz copper on top and bottom is used, the thermal resistance is 80°C/W. The junction temperature $T_J$ is:

$$T_J = (0.6W)(80°C/W) + 85°C = 133°C$$

The maximum junction temperature for the LT1886 is 150°C so the heat sinking capability of the board is adequate for the application.

If the copper area on the PC board is reduced to 180 sq. mm the thermal resistance increases to 122°C/W and the junction temperature becomes:

$$T_J = (0.6W)(122°C/W) + 85°C = 158°C$$

which is above the maximum junction temperature indicating that the heat sinking capability of the board is inadequate and should be increased.

### Capacitive Loading

The LT1886 is stable with a 1000pF capacitive load. The photo of the small-signal response with 1000pF load in a gain of 10 shows 50% overshoot. The photo of the large-signal response with a 1000pF load shows that the output slew rate is not limited by the short-circuit current. The Typical Performance Curve of Frequency Response vs Capacitive Load shows the peaking for various capacitive loads.

This stability is useful in the case of directly driving a coaxial cable or twisted pair that is inadvertently unterminated. For best pulse fidelity, however, a termination resistor of value equal to the characteristic impedance of the cable or twisted pair (i.e., 50Ω/75Ω/100Ω/135Ω) should be placed in series with the output. The other end of the cable or twisted pair should be terminated with the same value resistor to ground.

### Compensation

The LT1886 is stable in a gain 10 or higher for any supply and resistive load. It is easily compensated for lower gains with a single resistor or a resistor plus a capacitor. Figure 2 shows that for inverting gains, a resistor from the inverting node to AC ground guarantees stability if the parallel combination of $R_C$ and $R_G$ is less than or equal to $R_F/9$. For lowest distortion and DC output offset, a series capacitor, $C_C$, can be used to reduce the noise gain at lower frequencies. The break frequency produced by $R_C$ and $C_C$ should be less than 15MHz to minimize peaking. The Typical Curve of Frequency Response vs Supply Voltage, $A_V$ = –1 shows less than 1dB of peaking for a break frequency of 12.8MHz.

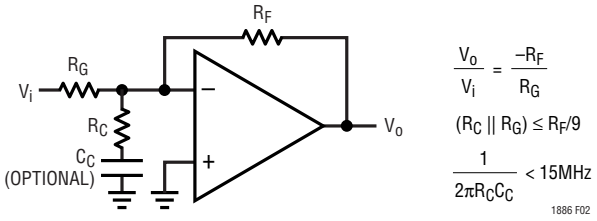



**Figure 2. Compensation for Inverting Gains**

Figure 3 shows compensation in the noninverting configuration. The $R_C$, $C_C$ network acts similarly to the inverting case. The input impedance is not reduced because the network is bootstrapped. This network can also be placed between the inverting input and an AC ground.

Another compensation scheme for noninverting circuits is shown in Figure 4. The circuit is unity gain at low frequency and a gain of 1 + $R_F/R_G$ at high frequency. The DC output offset is reduced by a factor of ten. The techniques of

## APPLICATIONS INFORMATION

Figures 3 and 4 can be combined as shown in Figure 5. The gain is unity at low frequencies, $1 + R_F/R_G$ at mid-band and for stability, a gain of 10 or greater at high frequencies.

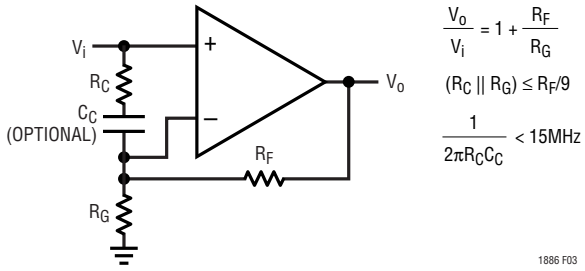



**Figure 3. Compensation for Noninverting Gains**

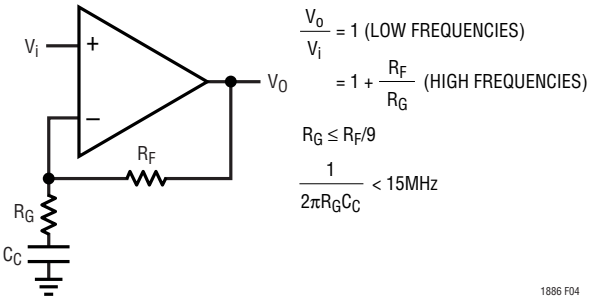



**Figure 4. Alternate Noninverting Compensation**

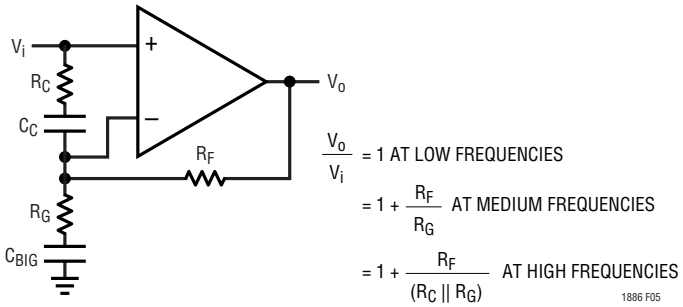



**Figure 5. Combination Compensation**

### Output Loading

The LT1886 output stage is very wide bandwidth and able to source and sink large currents. Reactive loading, even isolated with a back-termination resistor, can cause ringing at frequencies of hundreds of MHz. For this reason, any design should be evaluated over a wide range of output conditions. To reduce the effects of reactive loading, an optional snubber network consisting of a series RC across the load can provide a resistive load at high frequency. Another option is to filter the drive to the load. If a back-termination resistor is used, a capacitor to ground at the load can eliminate ringing.

### Line Driving Back-Termination

The standard method of cable or line back-termination is shown in Figure 6. The cable/line is terminated in its characteristic impedance (50Ω, 75Ω, 100Ω, 135Ω, etc.). A back-termination resistor also equal to to the chararacteristic impedance should be used for maximum pulse fidelity of outgoing signals, and to terminate the line for incoming signals in a full-duplex application. There are three main drawbacks to this approach. First, the power dissipated in the load and back-termination resistors is equal so half of the power delivered by the amplifier is wasted in the termination resistor. Second, the signal is halved so the gain of the amplifer must be doubled to have the same overall gain to the load. The increase in gain increases noise and decreases bandwidth (which can also increase distortion). Third, the output swing of the amplifier is doubled which can limit the power it can deliver to the load for a given power supply voltage.

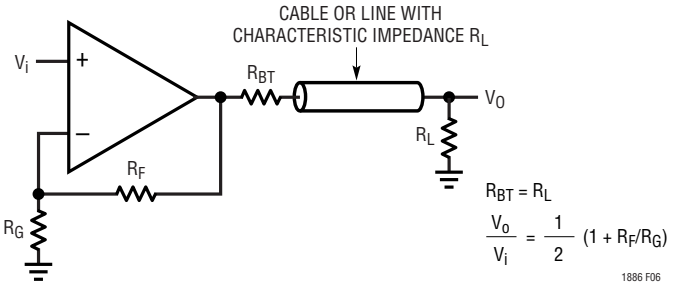



**Figure 6. Standard Cable/Line Back-Termination**

An alternate method of back-termination is shown in Figure 7. Positive feedback increases the effective back-termination resistance so $R_{BT}$ can be reduced by a factor of n. To analyze this circuit, first ground the input. As $R_{BT} = R_L/n$, and assuming $R_{P2} >> R_L$ we require that:

$V_a = V_o\ (1 - 1/n)$ to increase the effective value of $R_{BT}$ by n.

$V_p = V_o\ (1 - 1/n)/(1 + R_F/R_G)$

$V_o = V_p\ (1 + R_{P2}/R_{P1})$

Eliminating Vp, we get the following:

$(1 + R_{P2}/R_{P1}) = (1 + R_F/R_G)/(1 - 1/n)$

## APPLICATIONS INFORMATION

For example, reducing $R_{BT}$ by a factor of n = 4, and with an amplifer gain of $(1 + R_F/R_G) = 10$ requires that $R_{P2}/R_{P1} = 12.3$.

Note that the overall gain is increased:

$$\frac{V_o}{V_i} = \frac{R_{P2}/(R_{P2}+R_{P1})}{\left[(1+1/n)/(1+R_F/R_G)\right]-\left[R_{P1}/(R_{P2}+R_{P1})\right]}$$

A simpler method of using positive feedback to reduce the back-termination is shown in Figure 8. In this case, the drivers are driven differentially and provide complementary outputs. Grounding the inputs, we see there is inverting gain of $-R_F/R_P$ from $-V_o$ to $V_a$

$$V_a = V_o\ (R_F/R_P)$$

and assuming $R_P >> R_L$, we require

$$V_a = V_o\ (1 - 1/n)$$

solving

$$R_F/R_P = 1 - 1/n$$

So to reduce the back-termination by a factor of 3 choose $R_F/R_P = 2/3$. Note that the overall gain is increased to:

$$V_o/V_i = (1 + R_F/R_G + R_F/R_P)/[2(1 - R_F/R_P)]$$

### ADSL Driver Requirements

The LT1886 is an ideal choice for ADSL upstream (CPE) modems. The key advantages are: ±200mA output drive with only 1.7V worst-case total supply voltage headroom, high bandwidth, which helps achieve low distortion, low quiescent supply current of 7mA per amplifier and a space-saving, thermally enhanced SO-8 package.

An ADSL remote terminal driver must deliver an average power of 13dBm (20mW) into a 100Ω line. This corresponds to $1.41V_{RMS}$ into the line. The DMT-ADSL peak-to-average ratio of 5.33 implies voltage peaks of 7.53V into the line. Using a differential drive configuration and transformer coupling with standard back-termination, a transformer ratio of 1:2 is well suited. This is shown on the front page of this data sheet along with the distortion performance vs line voltage at 200kHz, which is beyond ADSL requirements. Note that the distortion is better than –73dBc for all swings up to $16V_{P-P}$ into the line. The gain of this circuit from the differential inputs to the line voltage is 10. Lower gains are easy to implement using the compensation techniques of Figure 5. Table 2 shows the drive requirements for this standard circuit.

The above design is an excellent choice for desktop applications and draws typically 550mW of power. For portable applications, power savings can be achieved by reducing the back-termination resistor using positive feedback as shown in Figure 9. The overall gain of this circuit is also 10, but the power consumption has been reduced to 350mW, a savings of 36% over the previous design. Note that the reduction of the back-termination resistor has allowed use of a 1:1 transformer ratio.

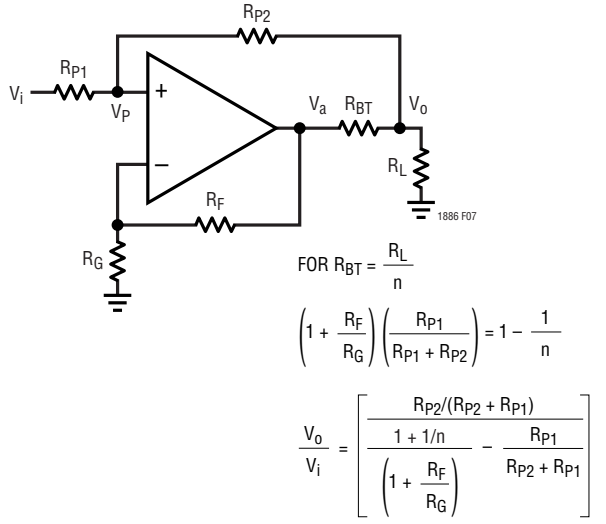



Figure 7. Back-Termination Using Positive Feedback

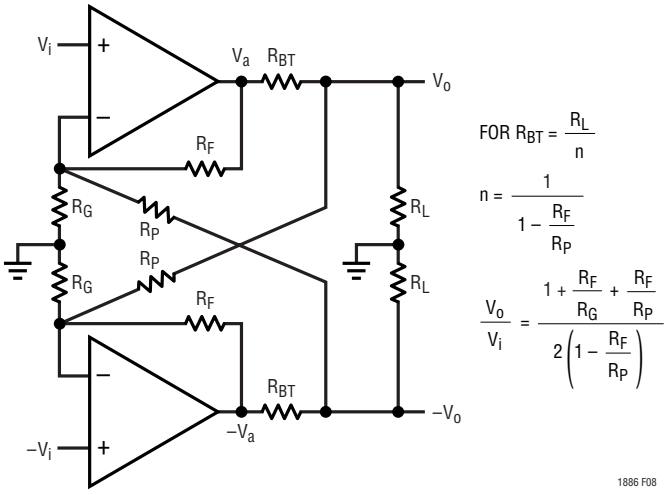



Figure 8. Back-Termination Using Differential Positive Feedback

## APPLICATIONS INFORMATION

**Table 2. ADSL Upstream Driver Designs**

| | STANDARD | LOW POWER |
|---|---|---|
| Line Impedance | 100Ω | 100Ω |
| Line Power | 13dBm | 13dBm |
| Peak-to-Average Ratio | 5.33 | 5.33 |
| Transformer Turns Ratio | 2 | 1 |
| Reflected Impedance | 25Ω | 100Ω |
| Back-Termination Resistors | 12.5Ω | 8.35Ω |
| Transformer Insertion Loss | 1dB | 0.5dB |
| Average Amplifier Swing | $0.79V_{RMS}$ | $0.87V_{RMS}$ |
| Average Amplifier Current | $31.7mA_{RMS}$ | $15mA_{RMS}$ |
| Peak Amplifier Swing | 4.21V Peak | 4.65V Peak |
| Peak Amplifier Current | 169mA Peak | 80mA Peak |
| Total Average Power Consumption | 550mW | 350mW |
| Supply Voltage | Single 12V | Single 12V |

Table 2 compares the two approaches. It may seem that the low power design is a clear choice, but there are further system issues to consider. In addition to driving the line, the amplifiers provide back-termination for signals that are received simultaneously from the line. In order to reject the drive signal, a receiver circuit is used such as shown in Figure 10. Taking advantage of the differential nature of the signals, the receiver can subtract out the drive signal and amplify the received signal. This method works well for standard back-termination. If the back-termination resistors are reduced by positive feedback, a portion of the received signal also appears at the amplifier outputs. The result is that the received signal is attenuated by the same amount as the reduction in the back-termination resistor. Taking into account the different transformer turns ratios, the received signal of the low power design will be one third of the standard design received signal. The reduced signal has system implications for the sensitivity of the receiver. The power reduction may, or may not, be an acceptable system tradeoff for a given design.

### Demo Board

Demo board DC304 has been created to provide a versatile platform for a line driver/receiver design. (Figure 11 shows a complete schematic.) The board is set up for either single or dual supply designs with Jumpers 1–4. The LT1886 is set up for differential, noninverting gain of 3. Each amp is configured as in Figure 5 for maximum flexibility. The amplifiers drive a 1:2 transformer through back-termination resistors that can be reduced with optional positive feedback. The secondary of the transformer can be isolated from the primary with Jumper 5.

A differential receiver is included using the LT1813, a dual 100MHz, 750V/μs operational amplifier. The receiver gain from the transformer secondary is 2, and the drive signals are rejected by approximately a factor of 14dB. Other optional components include filter capacitors and an RC snubber network at the transformer primary.

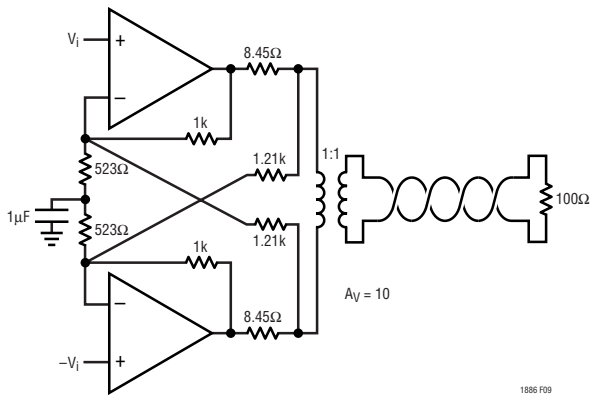



**Figure 9. Power Saving ADSL Modem Driver**

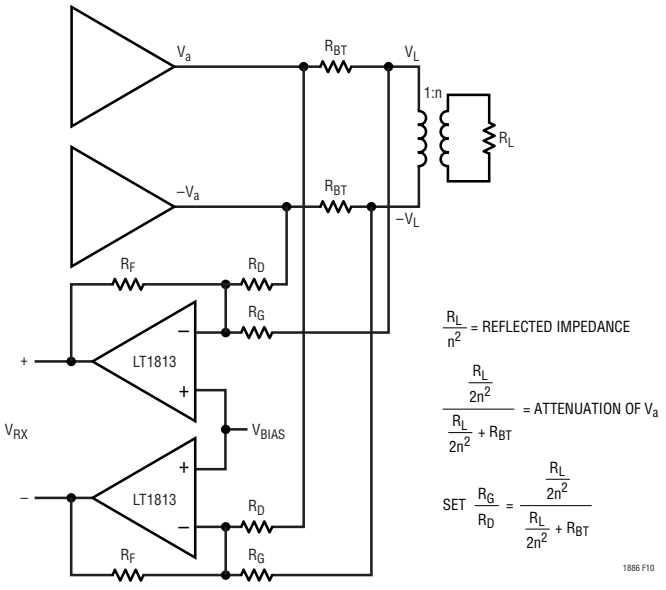



**Figure 10. Receiver Configuration**

## APPLICATIONS INFORMATION

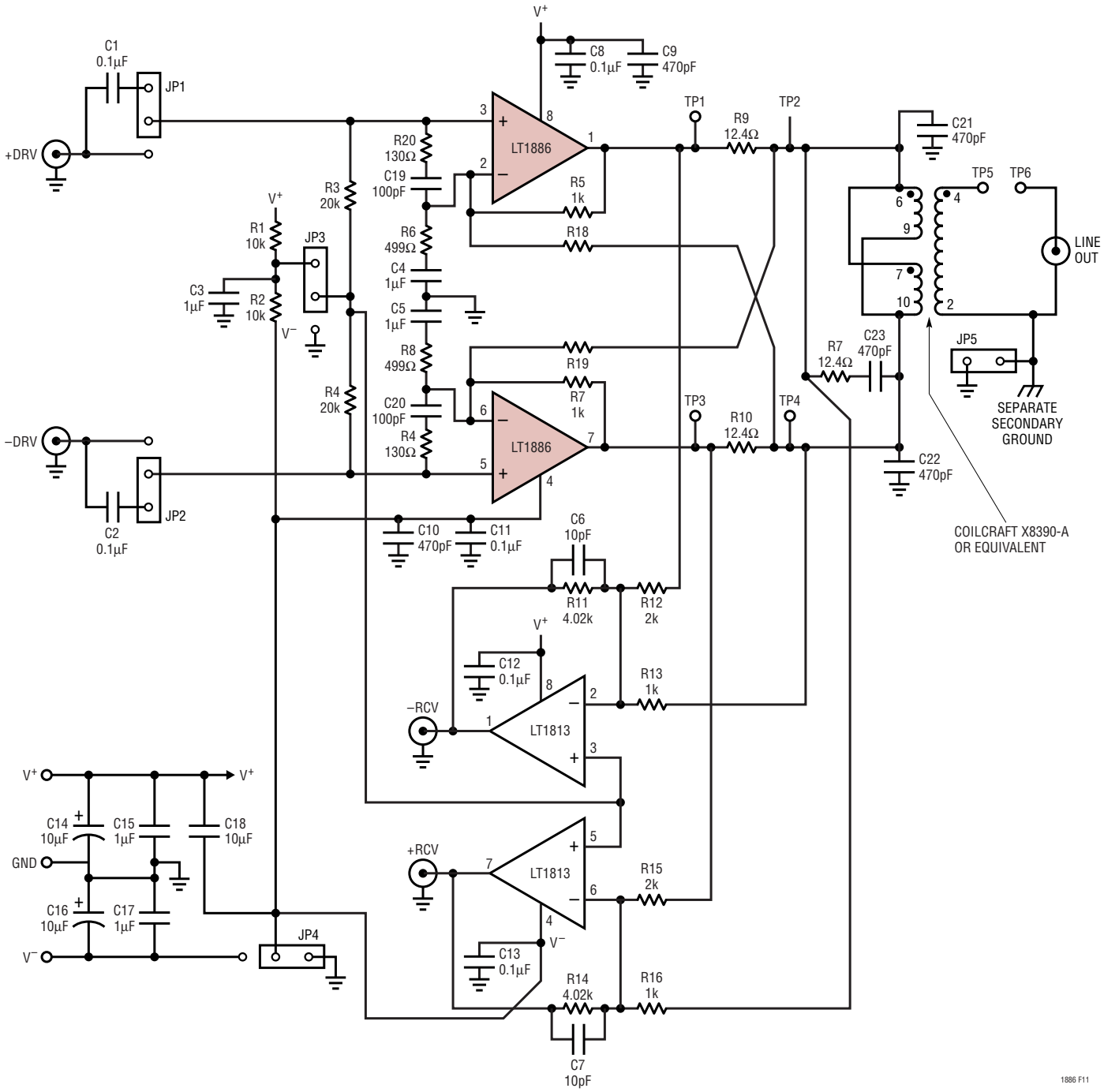
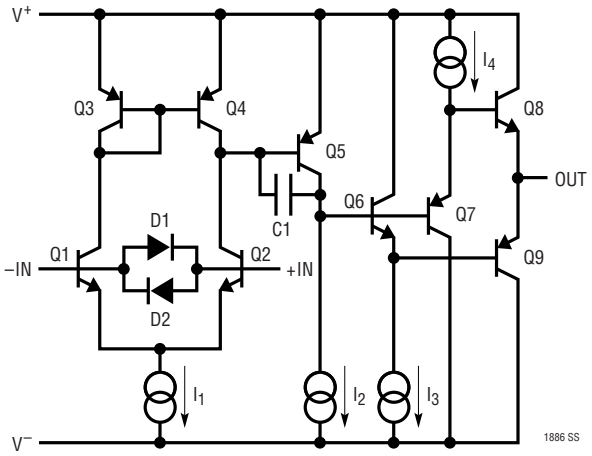



**Figure 11. LT1886, LT1813 DSL Demo Board (DC304)**

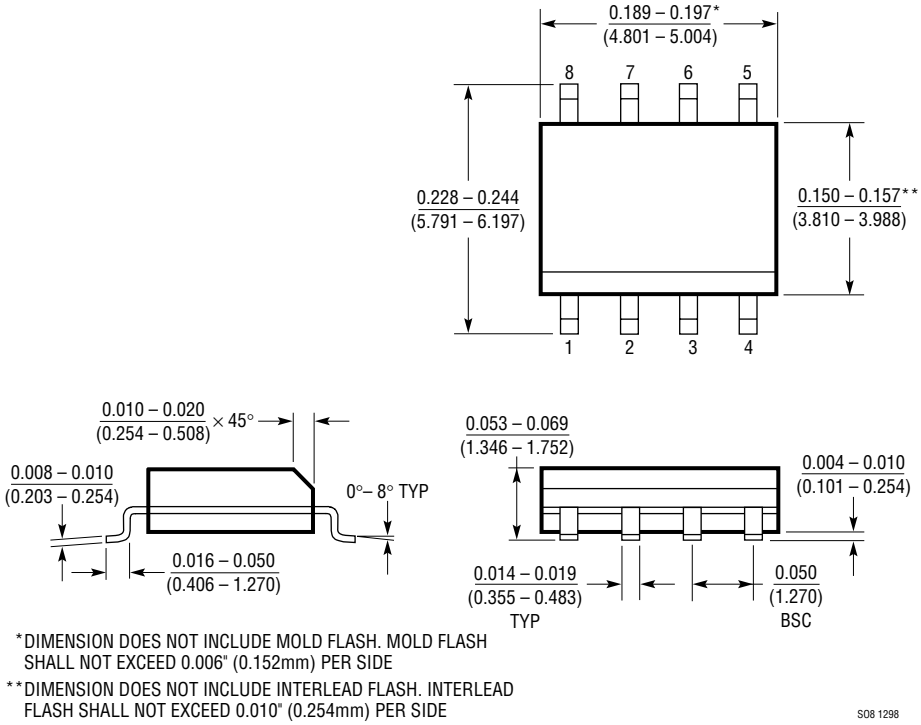
## SIMPLIFIED SCHEMATIC




## PACKAGE DESCRIPTION

**Dimensions in inches (millimeters) unless otherwise noted.**

**S8 Package**
**8-Lead Plastic Small Outline (Narrow 0.150)**
(LTC DWG # 05-08-1610)




*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 1298