Precision, Wide Voltage Range, Gain Selectable Funnel Amplifier

FEATURES

- Precision Attenuation: Gain = 0.1, 0.2, 0.25
- ±255V Common Mode Voltage Range
- 105dB Minimum CMRR (Gain = 0.1)
- 0.006% (60ppm) Maximum Gain Error
- 1ppm/°C Maximum Gain Error Drift
- 2ppm Maximum Gain Nonlinearity
- Wide Supply Voltage Range: 3.3V to 50V
- Rail-to-Rail Output
- 350µA Supply Current
- 80µV Maximum Op Amp Offset Voltage
- 1MHz –3dB Bandwidth (Gain = 0.1)
- Low Power Shutdown: 20µA
- Space-Saving MSOP and DFN Packages

APPLICATIONS

- High Voltage to Low Voltage Level Translation
- ADC Driver
- Bidirectional Wide Common Mode Range Voltage and Current Sensing
- Industrial Data-Acquisition Front-Ends
- Replacement for Isolation Circuits
- Differential to Single-Ended Conversion

DESCRIPTION

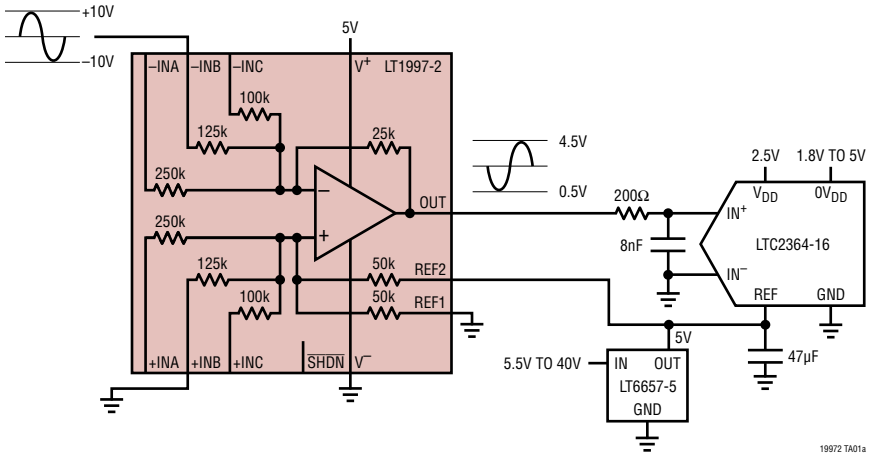
The LT®1997-2 is an attenuating (funnel) difference amplifier that can be used to translate large differential signals to the low voltage range compatible with ADCs. It combines a precision operational amplifier with highly-matched resistors to form a one-chip solution to attenuate and level shift voltages accurately using no external components. It comes with three standard pin-selectable gain options (0.1, 0.2 and 0.25), which can be further combined to form gains from 0.0455 to 0.55 (attenuations of 1.82 to 22) with accuracy of 0.006% (60ppm). The LT1997-2 also works across a very wide input common-mode voltage range (±255V), enabling robust operation in demanding industrial environments. Its excellent resistor matching results in a common mode rejection ratio of greater than 105dB.

The resistors maintain their excellent matching over temperature; the matching temperature coefficient is guaranteed less than 1ppm/°C. The resistors are extremely linear with voltage, resulting in a gain nonlinearity of less than 2ppm.

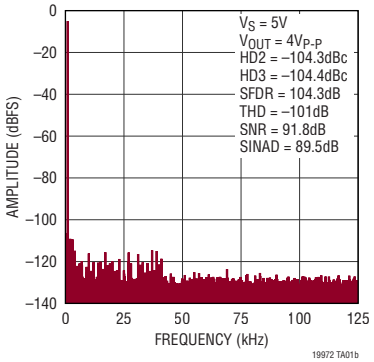
The LT1997-2 is fully specified at 5V and ±15V supplies and from –40°C to 125°C. The device is available in space saving 16-lead MSOP and 4mm × 4mm DFN14 packages.

TYPICAL APPLICATION

Interfacing a 20V$_{P-P}$ Ground-Referenced Input Signal to a 5V ADC



LT1997-2 Driving LTC2364-16, ADC, f_{IN} = 1kHz, 32768-Point FFT



Rev 0

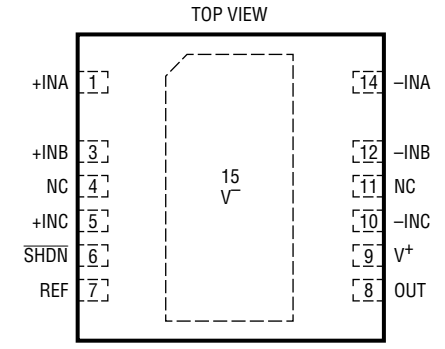
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages (V^+ to V^-).....60V
+INA, –INA, +INB, –INB,
+INC, –INC (Note 2).....V^- ±270V
REF, REF1, REF2..... (V^- + 60V) to (V^- – 0.3V)
$\overline{SHDN}$..... (V^+ + 0.3V) to (V^- – 0.3V)
Output Current (Continuous) (Note 6).....50mA
Output Short-Circuit Duration
(Note 3) .....Thermally Limited

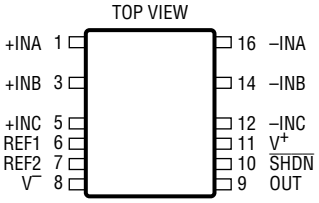
Temperature Range (Notes 4, 5)
LT1997I-2.....–40 to 85°C
LT1997H-2 .....–40 to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range .....–65 to 150°C
MSOP Lead Temperature (Soldering, 10 sec).....300°C

PIN CONFIGURATION



DF PACKAGE
14(12)-LEAD (4mm × 4mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 45°C/W , θ_{JC} = 3°C/W
EXPOSED PAD (PIN 15) IS V^-, MUST BE SOLDERED TO PCB



MS PACKAGE
VARIATION: MS16 (12)
16-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1997IDF-2#PBF	LT1997IDF-2#TRPBF	19972	14-Lead (4mm × 4mm) Plastic DFN	–40°C to 85°C
LT1997HDF-2#PBF	LT1997HDF-2#TRPBF	19972	14-Lead (4mm × 4mm) Plastic DFN	–40°C to 125°C
LT1997IMS-2#PBF	LT1997IMS-2#TRPBF	19972	16-Lead Plastic MSOP	–40°C to 85°C
LT1997HMS-2#PBF	LT1997HMS-2#TRPBF	19972	16-Lead Plastic MSOP	–40°C to 125°C

*The temperature grade is identified by a label on the shipping container. Consult ADI Marketing for parts specified with wider operating temperature ranges. Parts ending with PBF are RoHS and WEEE compliant.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, –40°C < T_A < 85°C for I-grade parts, –40°C < T_A < 125°C for H-grade parts, otherwise specifications are at T_A = 25°C. Difference Amplifier Configuration, V^+ = 15V, V^- = –15V, V_{CM} = V_{OUT} = V_{REF} = V_{REF1} = V_{REF2} = 0V. V_{CMOP} is the common mode voltage of the internal op amp.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔG	Gain Error	V_{OUT} = ±2.8V G = 0.1	 ●		±0.001	±0.006 ±0.008	% %
		V_{OUT} = ±5.6V G = 0.2	 ●		±0.001	±0.006 ±0.008	% %
		V_{OUT} = ±7V G = 0.25	 ●		±0.001	±0.006 ±0.008	% %
ΔG/ΔT	Gain Drift vs Temperature (Note 6)	V_{OUT} = ±7V	●		±0.2	±1	ppm/°C
GNL	Gain Nonlinearity	V_{OUT} = ±7V	 ●		±1	±2 ±3	ppm ppm
V_{OS}	Op Amp Offset Voltage (Note 9)	V^- < V_{CMOP} < V^+ – 1.75V	 ●		±20	±80 ±200	µV µV
$ΔV_{OS}/ΔT$	Op Amp Offset Voltage Drift (Note 6)	V^- < V_{CMOP} < V^+ – 1.75V	●		±0.5	±1.5	µV/°C
I_B	Op Amp Input Bias Current	V^- + 0.25V < V_{CMOP} < V^+ – 1.75V	 ●	–5 –15	±2	5 15	nA nA
I_{OS}	Op Amp Input Offset Current	V^- + 0.25V < V_{CMOP} < V^+ – 1.75V	 ●	–3 –10	±0.5	3 10	nA nA
R_{IN}	Input Impedance (Note 8)	Common Mode					
		G = 0.1	●	115	137.5	160	kΩ
		G = 0.2	●	63	75	87	kΩ
		G = 0.25	●	52	62.5	73	kΩ
		Differential					
		G = 0.1	●	420	500	580	kΩ
		G = 0.2	●	210	250	290	kΩ
		G = 0.25	●	168	200	232	kΩ
CMRR	Common Mode Rejection Ratio, Referred to Output, MS16 Package	G = 0.1, V_{CM} = ±28V	 ●	105 103	120		dB dB
		G = 0.2, V_{CM} = ±28V	 ●	101 99	118		dB dB
		G = 0.25, V_{CM} = ±28V	 ●	101 98	118		dB dB
CMRR	Common Mode Rejection Ratio, Referred to Output, DF14 Package	G = 0.1, V_{CM} = ±28V	 ●	103 101	118		dB dB
		G = 0.1, V_{CM} = ±255V, V_S = ±25V	 ●	103 101	118		dB dB
		G = 0.2, V_{CM} = ±28V	 ●	99 97	116		dB dB
		G = 0.2, V_{CM} = ±140V, V_S = ±25V	 ●	99 97	116		dB dB
		G = 0.25, V_{CM} = ±28V	 ●	99 97	116		dB dB
		G = 0.25, V_{CM} = ±115V, V_S = ±25V	 ●	99 97	116		dB dB
V_{CM}	Input Voltage Range (Note 7)	+INA/–INA +INB/–INB +INC/–INC	● ● ●	–255 –140 –115		255 140 115	V V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, –40°C < T_A < 85°C for I-grade parts, –40°C < T_A < 125°C for H-grade parts, otherwise specifications are at T_A = 25°C. Difference Amplifier Configuration, V^+ = 15V, V^- = –15V, V_{CM} = V_{OUT} = V_{REF} = V_{REF1} = V_{REF2} = 0V. V_{CMOP} is the common mode voltage of the internal op amp.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔR/R	Reference Divider Matching Error $\frac{\Delta R}{R} = \frac{R_{REF1} - R_{REF2}}{\left(\frac{R_{REF1} + R_{REF2}}{2}\right)}$	Available in MS16 Package Only	 ●		±0.002	±0.009 ±0.011	% %
PSRR	Power Supply Rejection Ratio (Note 9)	V_S = ±1.65V to ±25V, V_{CM} = V_{OUT} = Mid-Supply	●	114	124		dB
e_{ni}	Output Noise Voltage Density	f = 1kHz G = 0.1 G = 0.2 G = 0.25			 37 39 40		 nV/√Hz nV/√Hz nV/√Hz
	Output Noise Voltage	f = 0.1Hz to 10Hz G = 0.1 G = 0.2 G = 0.25			 0.9 0.95 1		 μV_{P-P} μV_{P-P} μV_{P-P}
V_{OL}	Output Voltage Swing Low (Referred to V^-)	No Load I_{SINK} = 5mA	● ●		50 280	150 500	mV mV
V_{OH}	Output Voltage Swing High (Referred to V^+)	No Load I_{SOURCE} = 5mA	● ●		50 450	150 900	mV mV
I_{SC}	Short-Circuit Output Current	50Ω to V^+ 50Ω to V^-	● ●	10 10	30 32		mA mA
SR	Slew Rate	ΔV_{OUT} = ±7V	●	0.45	0.75		V/µs
BW	Small Signal –3dB Bandwidth	G = 0.1 G = 0.2 G = 0.25			1 1.2 1.1		MHz MHz MHz
t_S	Settling Time	G = 0.1 0.1%, ΔV_{OUT} = 10V 0.01%, ΔV_{OUT} = 10V			 15 19		 µs µs
		G = 0.2 0.1%, ΔV_{OUT} = 10V 0.01%, ΔV_{OUT} = 10V			 16.9 20.6		 µs µs
		G = 0.25 0.1%, ΔV_{OUT} = 10V 0.01%, ΔV_{OUT} = 10V			 17.1 20.9		 µs µs
V_S	Supply Voltage		 ●	3 3.3		50 50	V V
t_{ON}	Turn-On Time				16		µs
V_{IL}	$\overline{SHDN}$ Input Logic Low (Referred to V^+)		●			–2.5	V
V_{IH}	$\overline{SHDN}$ Input Logic High (Referred to V^+)		●	–1.2			V
I_{SHDN}	$\overline{SHDN}$ Pin Current		●		–10	–15	µA
I_S	Supply Current	Active, $V_{\overline{SHDN}} \geq V^+ - 1.2V$ Active, $V_{\overline{SHDN}} \geq V^+ - 1.2V$ Shutdown, $V_{\overline{SHDN}} \leq V^+ - 2.5V$ Shutdown, $V_{\overline{SHDN}} \leq V^+ - 2.5V$	 ● ●		350 20 	400 600 25 70	µA µA µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, –40°C < T_A < 85°C for I-grade parts, –40°C < T_A < 125°C for H-grade parts, otherwise specifications are at T_A = 25°C. Difference Amplifier Configuration, V^+ = 5V, V^- = 0V, V_{CM} = V_{OUT} = V_{REF} = V_{REF1} = V_{REF2} = Mid-Supply. V_{CMOP} is the common mode voltage of the internal op amp.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔG	Gain Error	V_{OUT} = 1V to 4V G = 0.1	 ●		±0.001	±0.006 ±0.008	% %
		G = 0.2	 ●		±0.001	±0.006 ±0.008	% %
		G = 0.25	 ●		±0.001	±0.006 ±0.008	% %
ΔG/ΔT	Gain Drift vs Temperature (Note 6)	V_{OUT} = 1V to 4V	●		±0.2	±1	ppm/°C
GNL	Gain Nonlinearity	V_{OUT} = 1V to 4V			±1		ppm
V_{OS}	Op Amp Offset Voltage (Note 9)	V^- < V_{CMOP} < V^+ – 1.75V	 ●		±20	±80 ±200	μV μV
$\Delta V_{OS}/\Delta T$	Op Amp Offset Voltage Drift (Note 6)	V^- < V_{CMOP} < V^+ – 1.75V	●		±0.5	±1.5	μV/°C
I_B	Op Amp Input Bias Current	V^- + 0.25V < V_{CMOP} < V^+ – 1.75V	 ●	–5 –15	±2	5 15	nA nA
I_{OS}	Op Amp Input Offset Current	V^- + 0.25V < V_{CMOP} < V^+ – 1.75V	 ●	–3 –10	±0.5	3 10	nA nA
R_{IN}	Input Impedance (Note 8)	Common Mode					
		G = 0.1	●	115	137.5	160	kΩ
		G = 0.2	●	63	75	87	kΩ
		G = 0.25	●	52	62.5	73	kΩ
		Differential					
		G = 0.1	●	420	500	580	kΩ
		G = 0.2	●	210	250	290	kΩ
		G = 0.25	●	168	200	232	kΩ
CMRR	Common Mode Rejection Ratio, Referred to Output, MS16 Package	G = 0.1, V_{CM} = –25V to 10.75V	 ●	104 102	120		dB dB
		G = 0.2, V_{CM} = –12.5V to 7V	 ●	100 98	118		dB dB
		G = 0.25, V_{CM} = –10V to 6.25V	 ●	100 98	118		dB dB
CMRR	Common Mode Rejection Ratio, Referred to Output, DF14 Package	G = 0.1, V_{CM} = –25V to 10.75V	 ●	102 100	118		dB dB
		G = 0.2, V_{CM} = –12.5V to 7V	 ●	98 96	116		dB dB
		G = 0.25, V_{CM} = –10V to 6.25V	 ●	98 96	116		dB dB
ΔR/R	Reference Divider Matching Error $\frac{\Delta R}{R} = \frac{R_{REF1} - R_{REF2}}{\left(\frac{R_{REF1} + R_{REF2}}{2}\right)}$	Available in MS16 Package Only	 ●		±0.002	±0.009 ±0.011	% %
PSRR	Power Supply Rejection Ratio (Note 9)	V_S = ±1.65V to ±25V, V_{CM} = V_{OUT} = Mid-Supply	●	114	124		dB
e_{ni}	Output Noise Voltage Density	f = 1kHz					
		G = 0.1			37		nV/√Hz
		G = 0.2			39		nV/√Hz
		G = 0.25			40		nV/√Hz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, –40°C < T_A < 85°C for I-grade parts, –40°C < T_A < 125°C for H-grade parts, otherwise specifications are at T_A = 25°C. Difference Amplifier Configuration, V^+ = 5V, V^- = 0V, V_{CM} = V_{OUT} = V_{REF} = V_{REF1} = V_{REF2} = Mid-Supply. V_{CMOP} is the common mode voltage of the internal op amp.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Output Noise Voltage	f = 0.1Hz to 10Hz G = 0.1 G = 0.2 G = 0.25			 0.9 0.95 1		 μV_{P-P} μV_{P-P} μV_{P-P}
V_{OL}	Output Voltage Swing Low (Referred to V^-)	No Load I_{SINK} = 5mA	● ●		15 280	50 500	mV mV
V_{OH}	Output Voltage Swing High (Referred to V^+)	No Load I_{SOURCE} = 5mA	● ●		15 450	50 800	mV mV
I_{SC}	Short-Circuit Output Current	50Ω to V^+ 50Ω to V^-	● ●	10 10	30 28		mA mA
SR	Slew Rate	ΔV_{OUT} = 3V	●	0.45	0.75		V/µs
BW	Small signal –3dB Bandwidth	G = 0.1 G = 0.2 G = 0.25			1 1.2 1.1		MHz MHz MHz
t_S	Settling Time	G = 0.1 0.1%, ΔV_{OUT} = 2V 0.01%, ΔV_{OUT} = 2V			 7.5 11.7		 µs µs
		G = 0.2 0.1%, ΔV_{OUT} = 2V 0.01%, ΔV_{OUT} = 2V			 8.8 13.1		 µs µs
		G = 0.25 0.1%, ΔV_{OUT} = 2V 0.01%, ΔV_{OUT} = 2V			 8.7 12.7		 µs µs
V_S	Supply Voltage		 ●	3 3.3		50 50	V V
t_{ON}	Turn-On Time				22		µs
V_{IL}	$\overline{SHDN}$ Input Logic Low (Referred to V^+)		●			–2.5	V
V_{IH}	$\overline{SHDN}$ Input Logic High (Referred to V^+)		●	–1.2			V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current		●		–10	–15	µA
I_S	Supply Current	Active, $V_{\overline{SHDN}} \geq V^+ - 1.2V$ Active, $V_{\overline{SHDN}} \geq V^+ - 1.2V$ Shutdown, $V_{\overline{SHDN}} \leq V^+ - 2.5V$ Shutdown, $V_{\overline{SHDN}} \leq V^+ - 2.5V$	 ● ●		330 15 	370 525 20 40	µA µA µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: See Common Mode Voltage Range in the Applications Information section of this data sheet for other considerations when taking +INA/–INA/+INB/–INB/+INC/–INC pins to ±270V.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum. This depends on the power supply, input voltages and the output current.

Note 4: The LT1997I-2 is guaranteed functional over the operating temperature range of –40°C to 85°C. The LT1997H-2 is guaranteed functional over the operating temperature range of –40°C to 125°C.

Note 5: The LT1997I-2 is guaranteed to meet specified performance from –40°C to 85°C. The LT1997H-2 is guaranteed to meet specified performance from –40°C to 125°C.

Note 6: This parameter is not 100% tested.

Note 7: The input voltage range is guaranteed by the ±25V CMRR tests. The Input Voltage Range numbers specified in the table guarantee that the internal op amp operates in its normal operating region. The Input voltage range can be higher if the internal op amp operates in its Over-The-Top® operating region. See Common Mode Voltage Range in the Applications Information section to determine the valid input voltage range under various operating conditions.

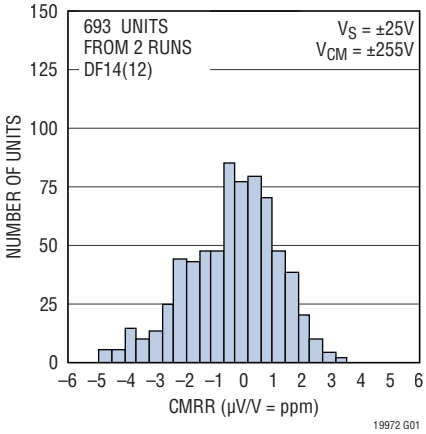
Note 8: Input impedance is tested by a combination of direct measurements and correlation to the CMRR and gain error tests.

Note 9: Offset voltage, offset voltage drift and PSRR are defined as referred to the internal op amp. The following shows the calculation of output offset: In the case of balanced source resistance, $V_{OS,OUT}$ = (V_{OS} • NOISEGAIN) + (I_{OS} • 25k) + (I_B • 25k • (1– R_P/R_N)) where R_P and R_N are the total resistance at the op amp positive and negative terminal, respectively.

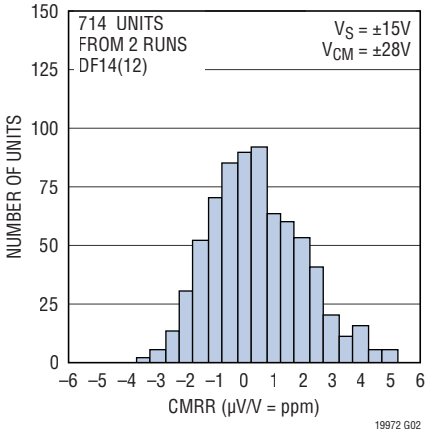
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, Difference Amplifier configuration, unless otherwise noted.

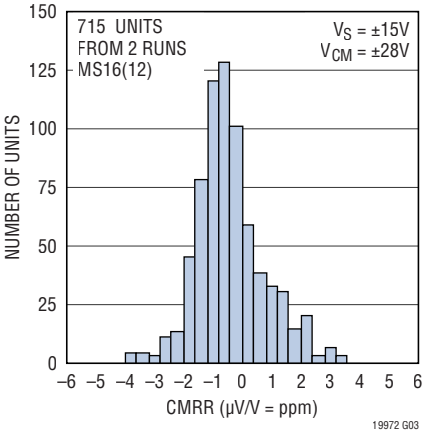
Typical Distribution of CMRR, Referred to Output (G = 0.1)



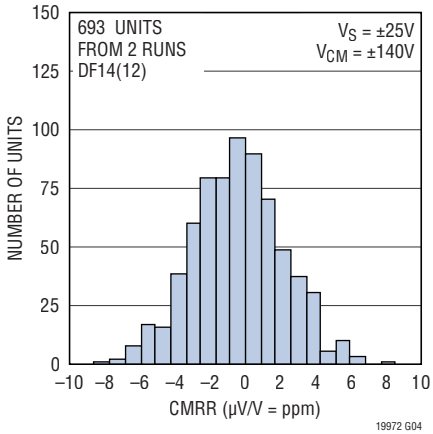
Typical Distribution of CMRR, Referred to Output (G = 0.1)



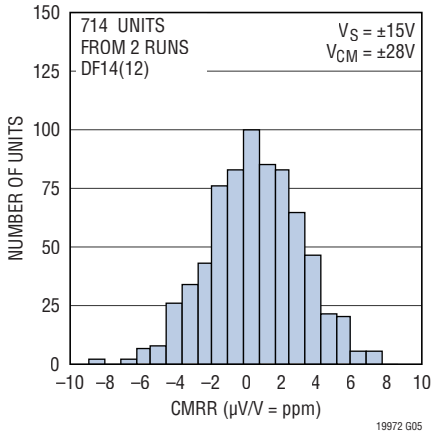
Typical Distribution of CMRR, Referred to Output (G = 0.1)



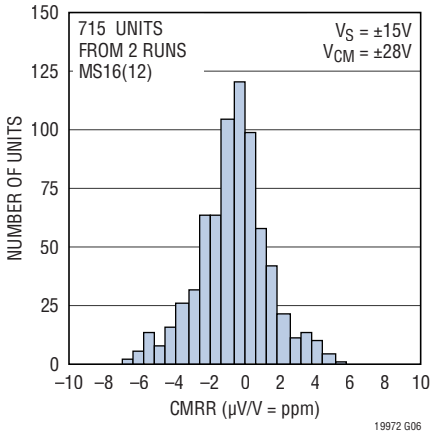
Typical Distribution of CMRR, Referred to Output (G = 0.2)



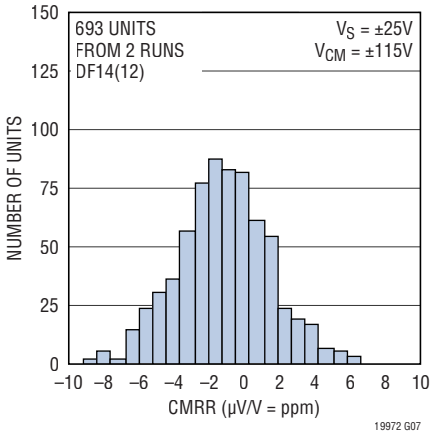
Typical Distribution of CMRR, Referred to Output (G = 0.2)



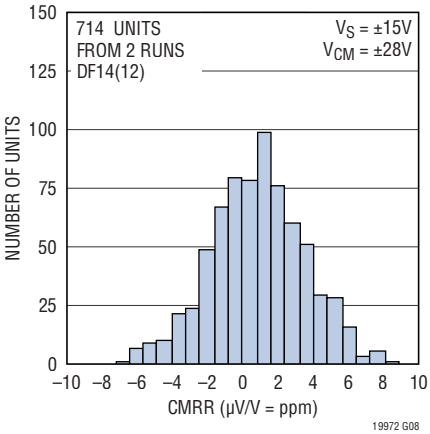
Typical Distribution of CMRR, Referred to Output (G = 0.2)



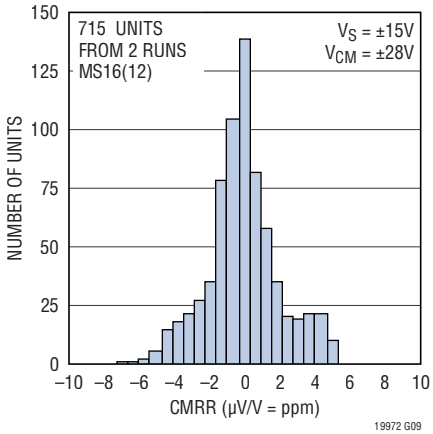
Typical Distribution of CMRR, Referred to Output (G = 0.25)



Typical Distribution of CMRR, Referred to Output (G = 0.25)



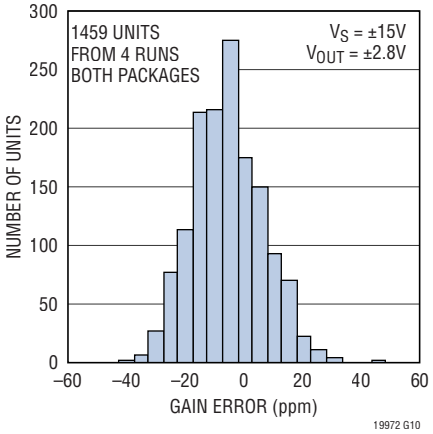
Typical Distribution of CMRR, Referred to Output (G = 0.25)



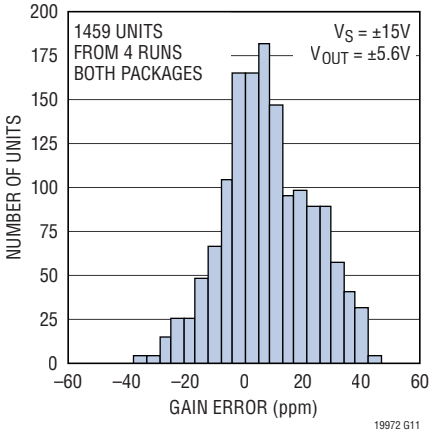
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, Difference Amplifier configuration, unless otherwise noted.

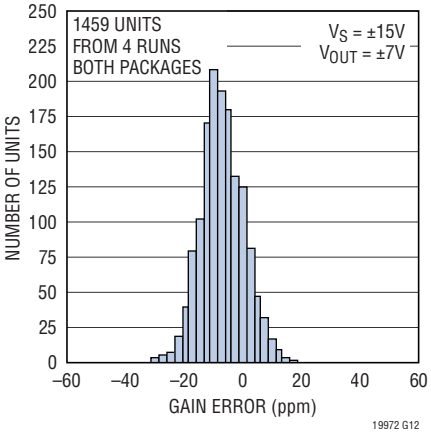
Typical Distribution of Gain Error (G = 0.1)



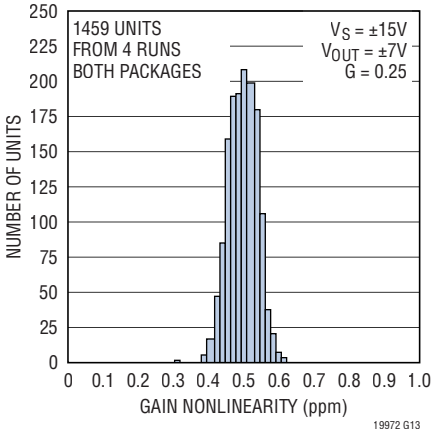
Typical Distribution of Gain Error (G = 0.2)



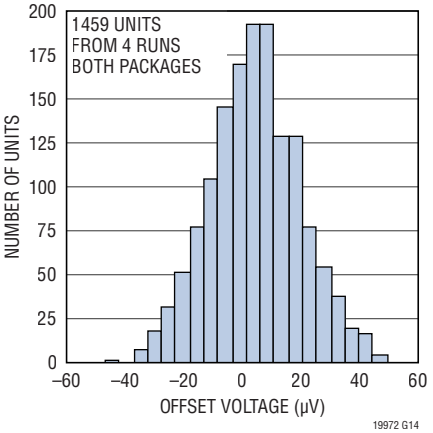
Typical Distribution of Gain Error (G = 0.25)



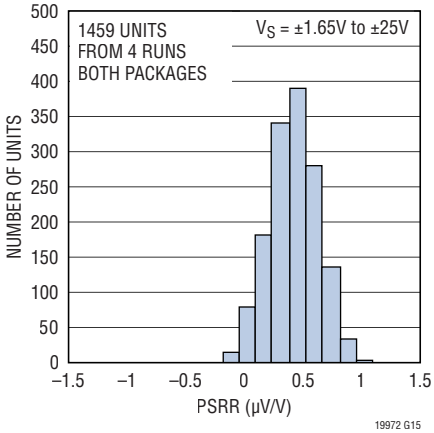
Typical Distribution of Gain Nonlinearity



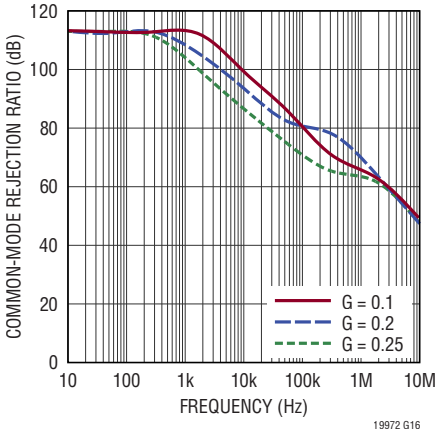
Typical Distribution of Op Amp Offset Voltage



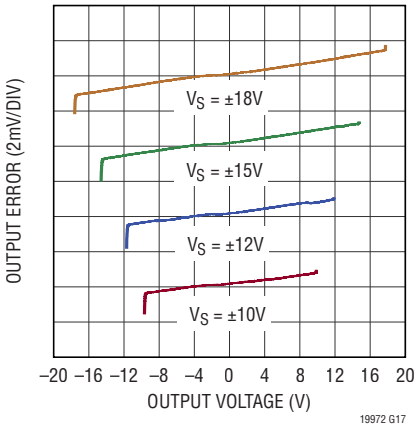
Typical Distribution of Op Amp PSRR



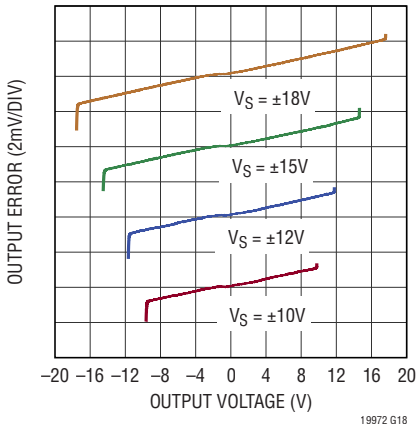
CMRR vs Frequency, Referred to Output



Typical Gain Error for R_L = 10kΩ, (G = 0.25) (Curves Offset for Clarity)



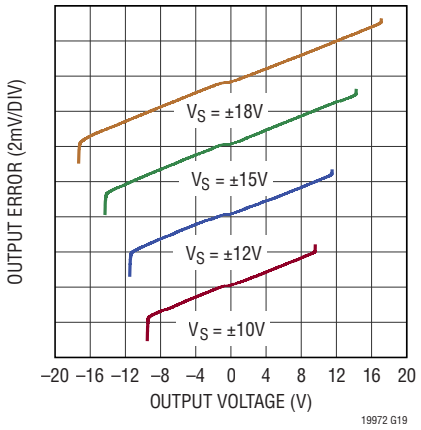
Typical Gain Error for R_L = 5kΩ, (G = 0.25) (Curves Offset for Clarity)



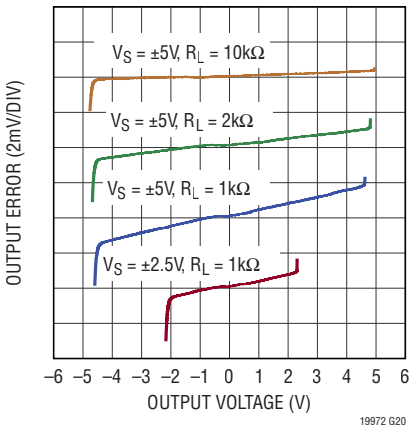
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, Difference Amplifier configuration, unless otherwise noted.

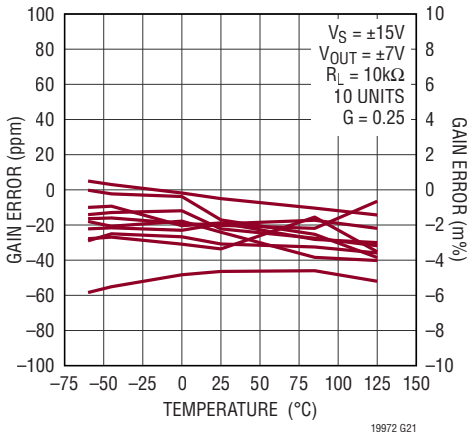
Typical Gain Error for R_L = 2kΩ (G = 0.25) (Curves Offset for Clarity)



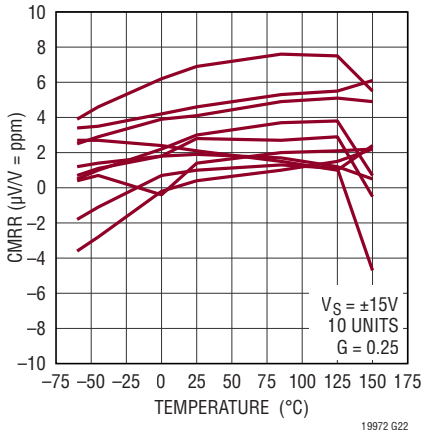
Typical Gain Error for Low Supply Voltages (G = 0.25) (Curves Offset for Clarity)



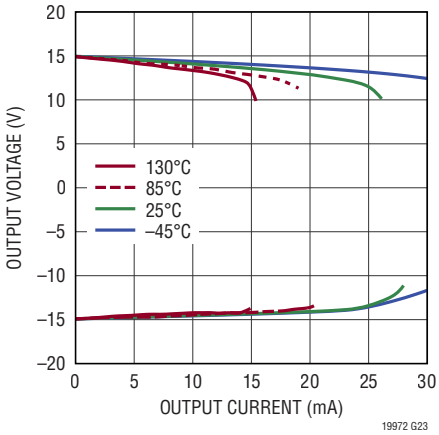
Gain Error vs Temperature



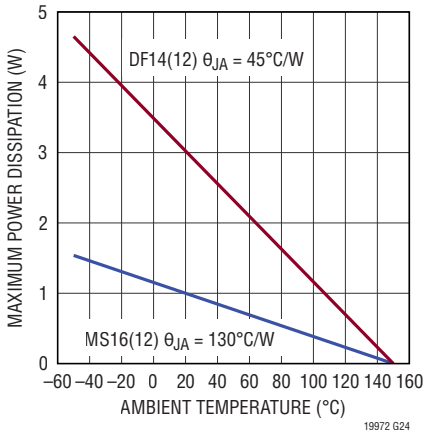
CMRR vs Temperature, Referred to Output



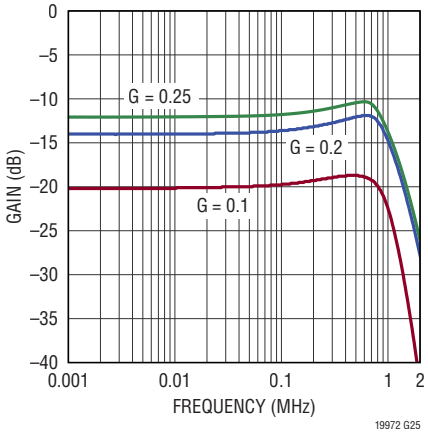
Output Voltage vs Load Current



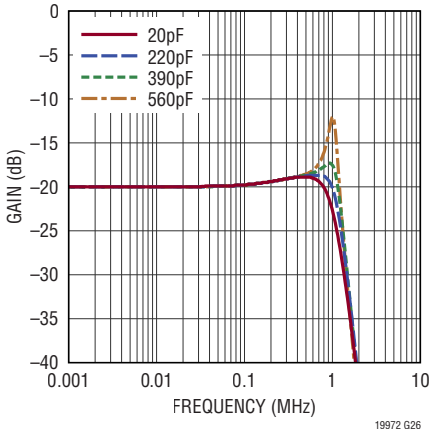
Maximum Power Dissipation vs Temperature



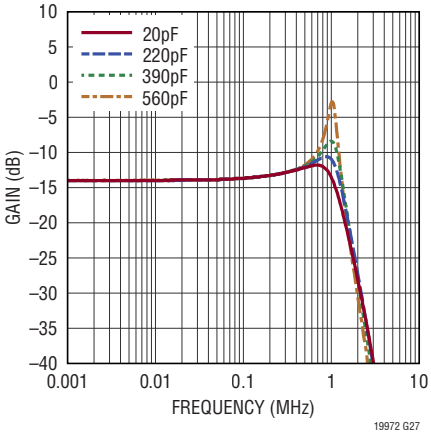
Gain vs Frequency



Frequency Response vs Capacitive Load (G = 0.1)



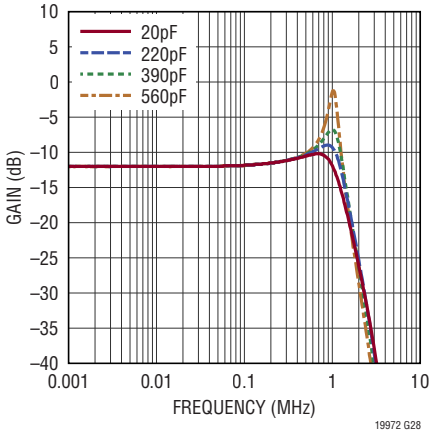
Frequency Response vs Capacitive Load (G = 0.2)



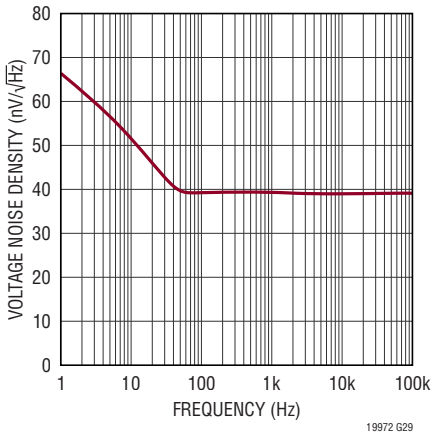
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, Difference Amplifier configuration, unless otherwise noted.

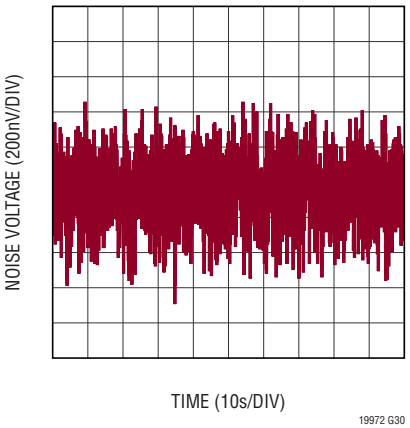
Frequency Response vs Capacitive Load (G = 0.25)



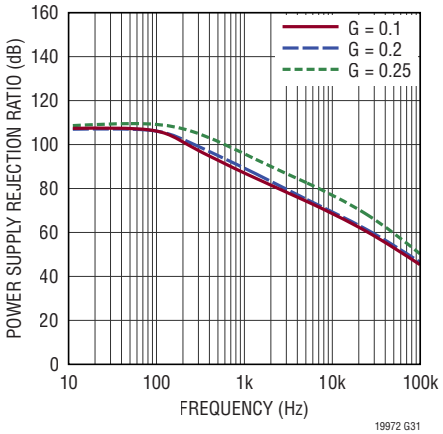
Output Noise Density vs Frequency (G = 0.25)



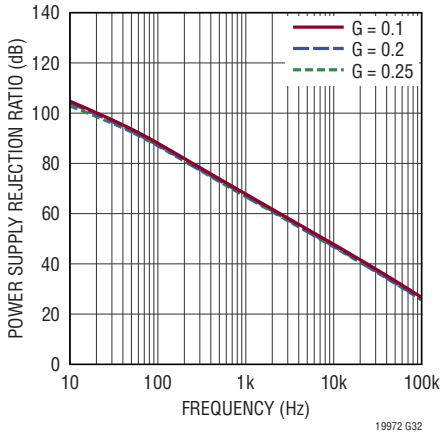
Output 0.1Hz to 10Hz Noise (G = 0.25)



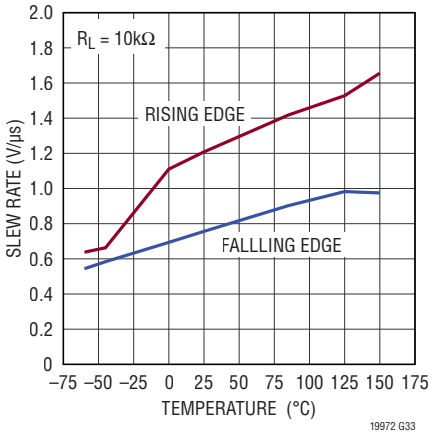
Positive PSRR vs Frequency



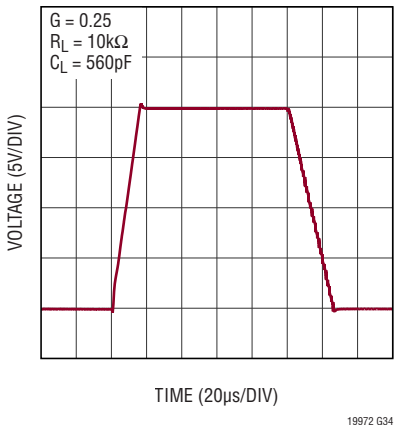
Negative PSRR vs Frequency



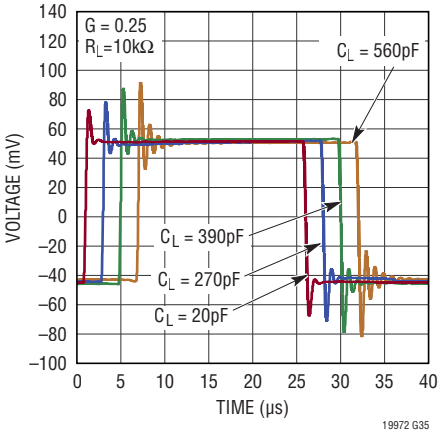
Slew Rate vs Temperature



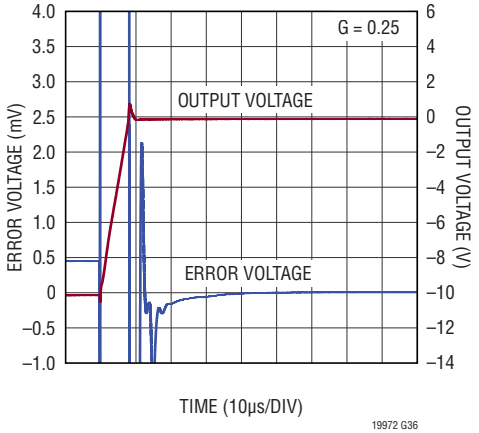
Large-Signal Step Response



Small-Signal Step Response



Settling Time

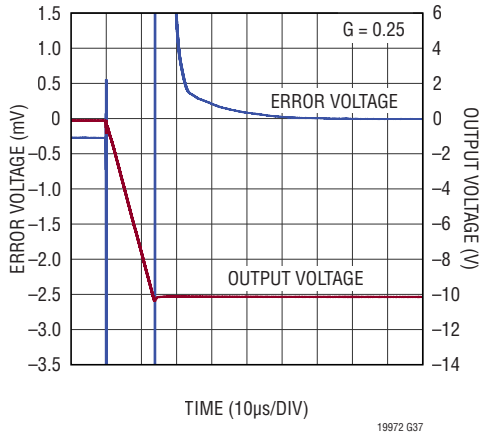


Rev 0

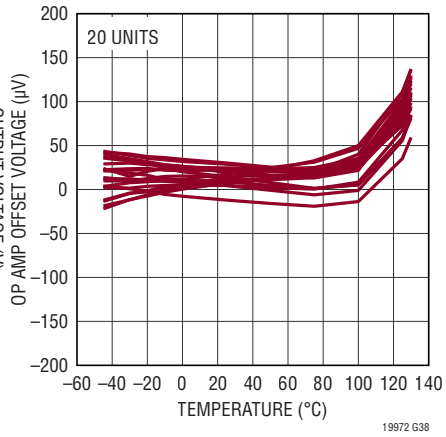
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, Difference Amplifier configuration, unless otherwise noted.

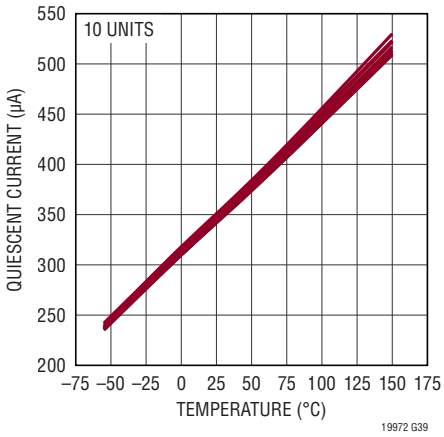
Settling Time



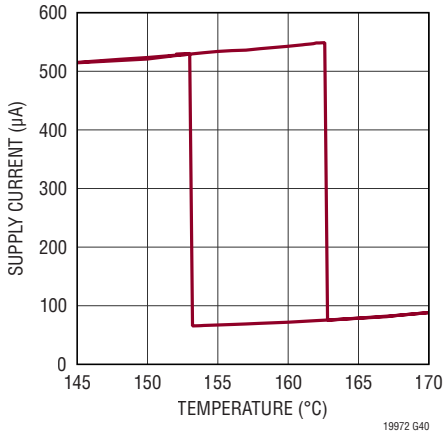
Op Amp Offset Voltage vs Temperature



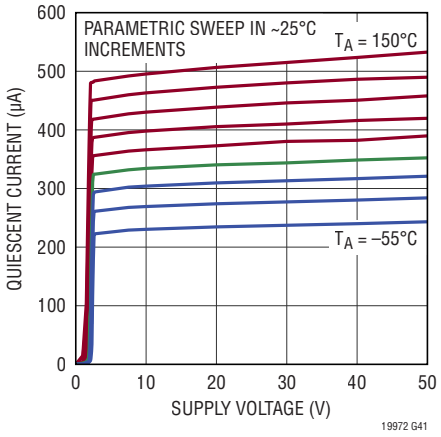
Quiescent Current vs Temperature



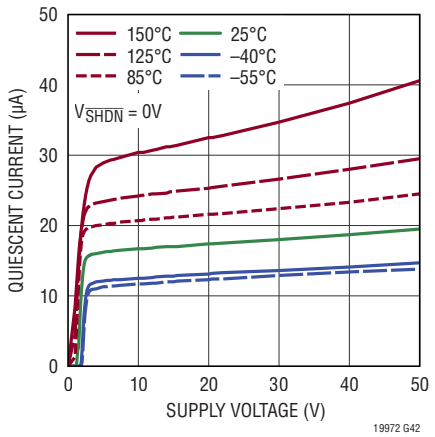
Thermal Shutdown vs Hysteresis



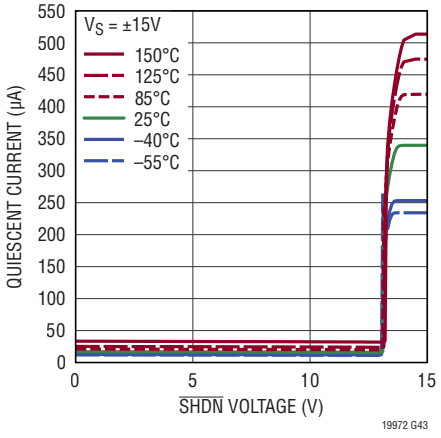
Quiescent Current vs Supply Voltage



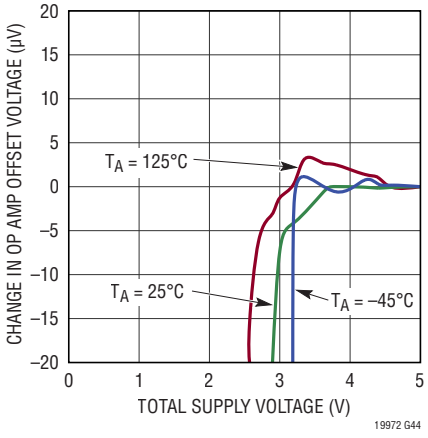
Shutdown Quiescent Current vs Supply Voltage



Quiescent Current vs $\overline{SHDN}$ Voltage



Minimum Supply Voltage



PIN FUNCTIONS (DFN/MSOP)

V^+ (Pin 9/Pin 11): Positive Supply Pin.

V^- (EXPOSED PAD Pin 15/Pin 8): Negative Supply Pin.

OUT (Pin 8/Pin 9): Output Pin.

+INA (Pin 1/Pin 1): Noninverting Gain-of-0.1 Input Pin. Connects a 250k internal resistor to the internal op amp's noninverting input.

+INB (Pin 3/Pin 3): Noninverting Gain-of-0.2 Input Pin. Connects a 125k internal resistor to the internal op amp's noninverting input.

+INC (Pin 5/Pin 5): Noninverting Gain-of-0.25 Input Pin. Connects a 100k internal resistor to the internal op amp's noninverting input.

–INA (Pin 14/Pin 16): Inverting Gain-of-0.1 input Pin. Connects a 250k internal resistor to the internal op amp's inverting input.

–INB (Pin 12/Pin 14): Inverting Gain-of-0.2 input Pin. Connects a 125k internal resistor to the internal op amp's inverting input.

–INC (Pin 10/Pin 12): Inverting Gain-of-0.25 input Pin. Connects a 100k internal resistor to the internal op amp's inverting input.

REF (Pin 7/NA): Reference Input Pin. Sets the output level when the difference between the inputs is zero.

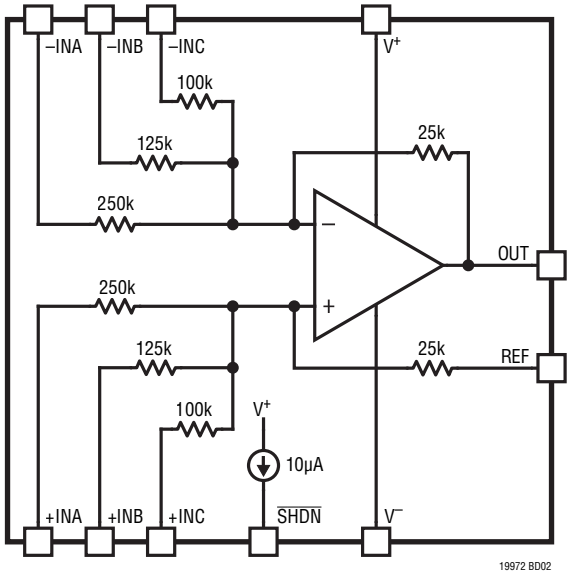
REF1 (NA/Pin 6): Reference 1 Input Pin. With REF2, sets the output level when the difference between the inputs is zero.

REF2 (NA/Pin 7): Reference 2 Input Pin. With REF1, sets the output level when the difference between the inputs is zero.

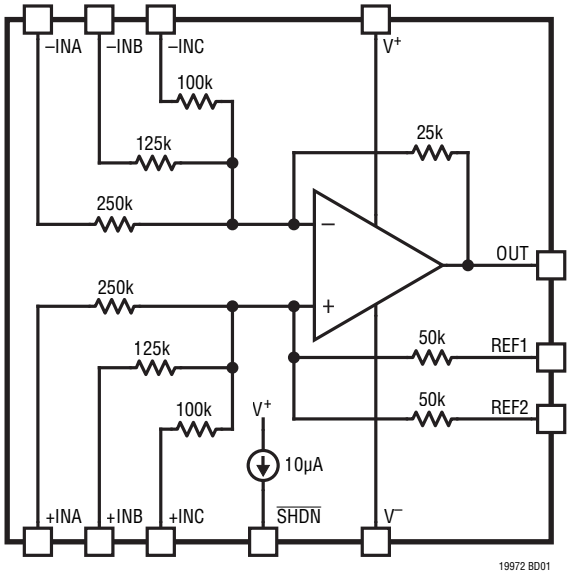
$\overline{\text{SHDN}}$ (Pin 6/Pin 10): Shutdown Pin. Amplifier is active when this pin is tied to V^+ or left floating. Pulling the pin more than 2.5V below V^+ causes the amplifier to enter a low power state.

BLOCK DIAGRAM

DFN



MSOP



APPLICATIONS INFORMATION

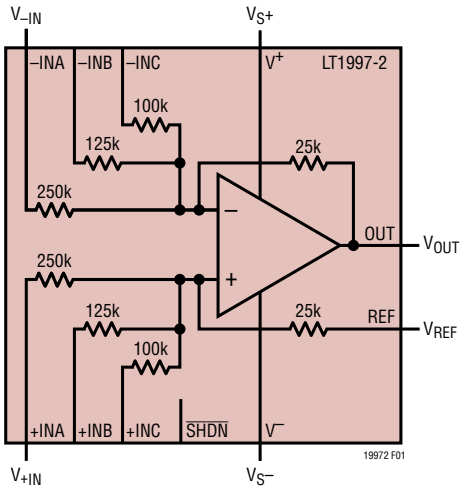


Figure 1. Difference Amplifier with Dual-Supply Operation (Gain = 0.1)

Introduction

The LT1997-2 is a precision, high voltage funnel amplifier combined with a highly-matched resistor network. It can easily be configured into many different gain circuits without adding external components, as it will be shown in this data sheet. The LT1997-2 provides the resistors and op amp together in a small package in order to save board space and reduce complexity. Highly accurate measurement circuits can be easily constructed with the LT1997-2. The circuits can be tailored to specific measurement applications.

Common Mode Voltage Range

The common mode voltage range of the LT1997-2 is set by the voltage range allowed on the LT1997-2's input pins and by the input voltage range of the internal op amp.

The internal op amp of LT1997-2 has 2 operating regions:

a) if the common-mode voltage at the inputs of the internal op amp (V_{CMOP}) is between V^- and $V^+ – 1.75V$, the op amp operates in its normal region;

b) If V_{CMOP} is between $V^+ – 1.75V$ and $V^- + 76V$, the op amp continues to operate, but in its Over-The-Top (OTT) region with degraded performance (see Over-The-Top Operation section of this data sheet for more detail).

The LT1997-2 will not operate correctly if the common-mode voltage at the inputs of the internal op amp (V_{CMOP}) is below V^-, but the part will not be damaged as long as V_{CMOP} is greater than $V^- – 25V$ and the junction temperature of the LT1997-2 does not exceed 150°C.

The voltage on LT1997-2's input pins should never be higher than $V^- + 270V$ or lower than $V^- – 270V$ under any circumstances.

The common-mode voltage at the inputs of the internal op amp (V_{CMOP}) is determined by the voltages on pins +INA, +INB, +INC and REF (see the Calculating Input Voltage Range section). This condition is true provided that the internal op amp's output is not clipped and feedback maintains the internal op amp's inputs at the same voltage.

In addition to the limits mentioned above, the common mode input voltage of the amplifier should be chosen so that the input resistors do not dissipate too much power. The power dissipated in a 250k resistor must be less than 1.8W. It must be less than 0.9W for the 125k resistor and less than 0.72W for the 100k resistor. For most applications, the pin voltage limitations will be reached before the resistor power limitation is reached.

Calculating Input Voltage Range

Figure 2 shows the LT1997-2 in the generalized case of a difference amplifier, with the inputs shorted for the common mode calculation. The values of R_F and R_G are dictated by how the positive inputs (+INA, +INB, +INC) and REF pin are connected.

By superposition we can write:

$$V_{CMOP} = V_{EXT} \bullet \frac{R_F}{R_F + R_G} + V_{REF} \bullet \frac{R_G}{R_F + R_G}$$

Or, solving for V_{EXT}:

$$V_{EXT} = V_{CMOP} \bullet \left(1 + \frac{R_G}{R_F}\right) - V_{REF} \bullet \frac{R_G}{R_F}$$

But valid V_{CMOP} voltages are limited to $V_S+ – 1.75V$ (or $V_S– + 76V$ for OTT) on the high side and $V_S–$ on the low side, so:

$$\text{MAX } V_{EXT} = \left(V_S+ – 1.75\right) \bullet \left(1 + \frac{R_G}{R_F}\right) - V_{REF} \bullet \frac{R_G}{R_F}$$

APPLICATIONS INFORMATION

and:

$$\text{MIN } V_{EXT} = (V_S-)\bullet\left(1+\frac{R_G}{R_F}\right)-V_{REF}\bullet\frac{R_G}{R_F}$$

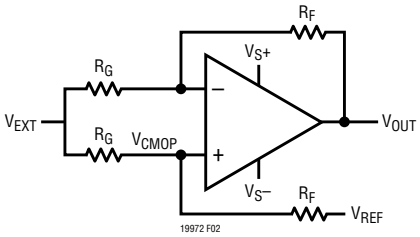


Figure 2. Calculating the Common Mode Input Voltage Range

Exceeding the MAX V_{EXT} limit will cause the amplifier to transition into the Over-The-Top region. The maximum input voltage for the Over-The-Top region is:

$$\text{MAX } V_{EXTOTT} = (V_S-+76)\bullet\left(1+\frac{R_G}{R_F}\right)-V_{REF}\bullet\frac{R_G}{R_F}$$

Keep in mind that the above MAX and MIN values for input voltage range should not exceed V⁻ ±270V, the ABSMAX voltage range specified earlier for LT1997-2's input pins.

The negative inputs (–INA, –INB, –INC) are not limited by the internal op amp common mode range (V_{CMOP}) because they do not affect it. They are limited by the output swing of the amplifier (and obviously by the allowed voltage range for the input pins).

Over-The-Top Operation

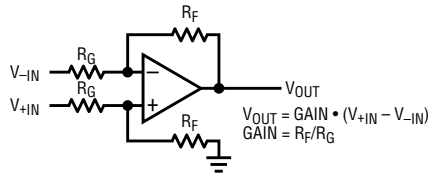
When the input common mode voltage of the internal op amp (V_{CMOP}) in the LT1997-2 is biased near or above the V⁺ supply, the op amp is operating in the Over-The-Top (OTT) region. The op amp continues to operate with an input common mode voltage of up to 76V above V⁻ (regardless of the positive power supply voltage V⁺), but its performance is degraded. The op amp's input bias currents change from under ±2nA to 14µA. The op amp's input offset current rises to ±50nA, which adds ±1.25mV to the output offset voltage.

In addition, when operating in the Over-The-Top region, the differential input impedance of the internal op amp decreases from 1MΩ in normal operation to approximately 3.7kΩ in Over-The-Top operation. This resistance appears across the summing nodes of the internal op amp and boosts noise and offset while decreasing speed. Noise and offset will increase by 80%. The bandwidth will be reduced by 45%. For more detail on Over-The-Top operation, consult the LT6015 data sheet.

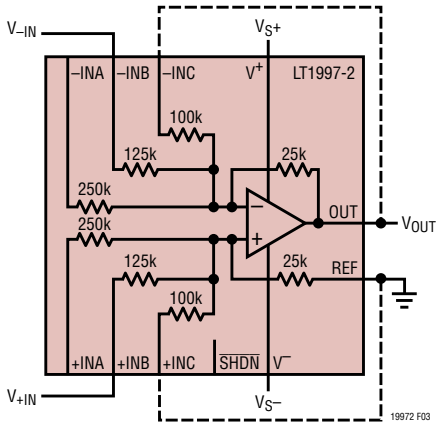
Difference Amplifiers

The LT1997-2 is ideally suited to be used as a difference amplifier. Figure 3 shows the basic 4-resistor difference amplifier and the LT1997-2. A difference gain of 0.2 (attenuation = 5) is shown, but can be altered by additional dashed connections. By connecting the 100k resistors in parallel with the 25k feedback resistors, the gain is reduced to 0.16 (attenuation = 6.25). Of course there are many possible gains and Figure 4 shows circuit schematics of some of those difference amplifier gains.

Note that the common mode voltage at the inputs of the internal op amp (V_{CMOP}) is set by the voltages at pins +INA, +INB, +INC and REF.



DIFFERENCE AMPLIFIER CONFIGURATION



DIFFERENCE AMPLIFIER CONFIGURATION
IMPLEMENTED WITH THE LT1997-2, R_F = 25k, R_G = 125k, GAIN = 0.2

ADDING THE DASHED CONNECTIONS CONNECT THE
100k RESISTOR IN PARALLEL WITH R_F, SO R_F IS REDUCED TO 20k.
THE GAIN BECOMES 20k/125k = 0.16

Figure 3. The LT1997-2 Configured as a Difference Amplifier. Gain Is Set by Connecting the Correct Resistors or Combinations of Resistors. Gain of 0.2 (Attenuation = 5) Is Shown, with Dashed Lines Modifying It to a Gain of 0.16 (Attenuation = 6.25)

Rev 0

APPLICATIONS INFORMATION

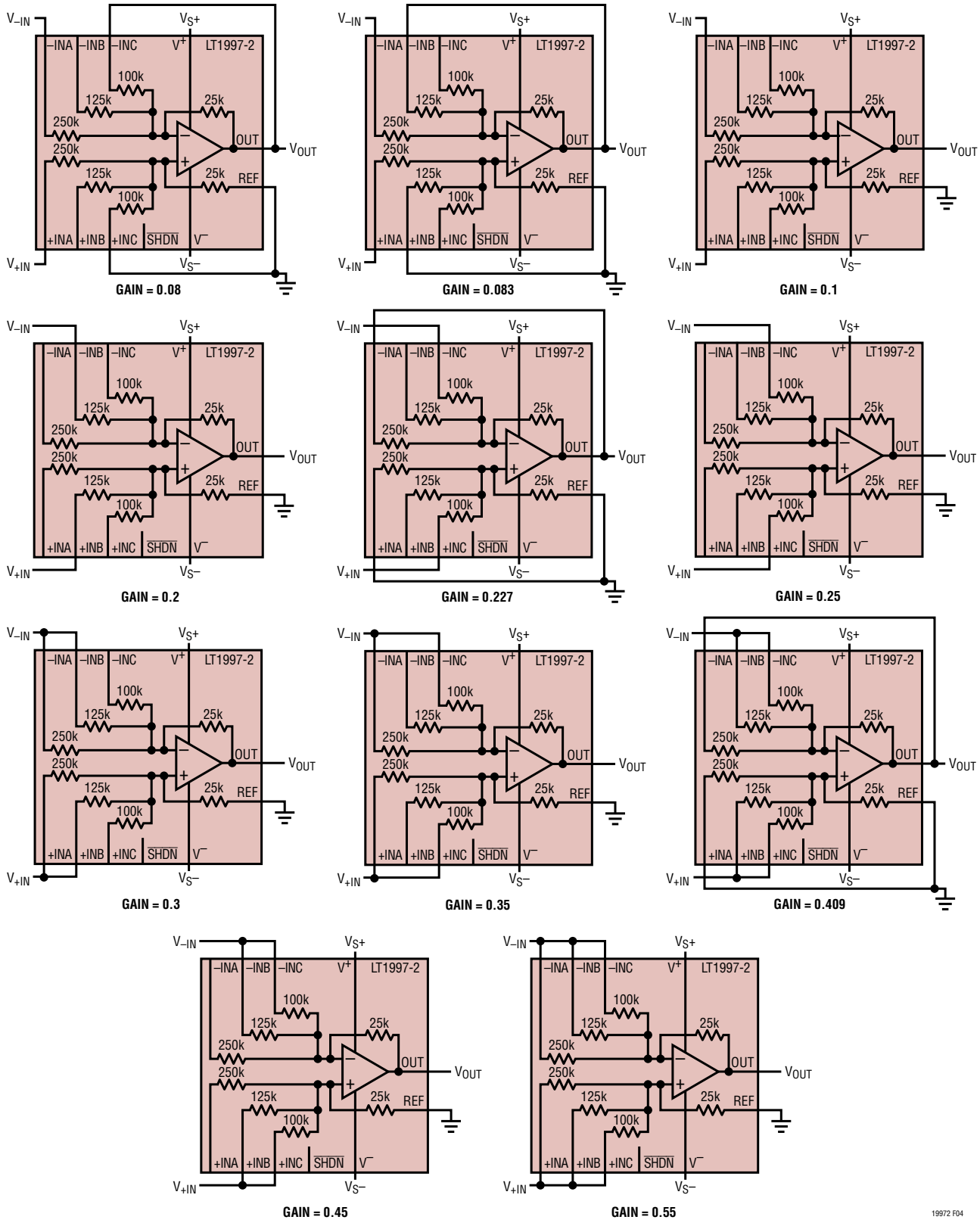
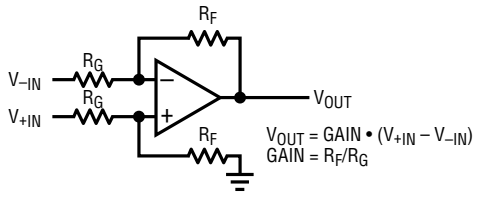


Figure 4. Many Difference Amplifier Gains Can Be Achieved by Strapping Pins

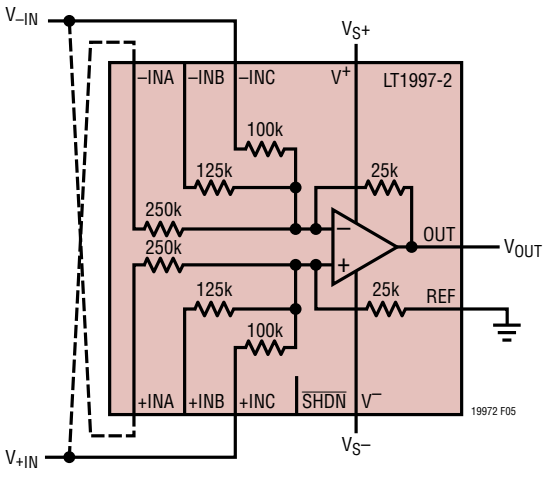
APPLICATIONS INFORMATION

Difference Amplifier: Additional Gains Using Cross-Coupling

Figure 5 shows the basic difference amplifier as well as the LT1997-2 with cross-coupled inputs. The additional dashed connections reduce the differential gain from 0.25 to 0.15. Using this method, additional gains are achievable and a few example schematics of the difference amplifiers using cross-coupling are shown in Figure 6. To summarize, Table 1 shows a complete list of all difference amplifier gains (attenuations) and how they are constructed using (both conventional or cross-coupling) pin strapping. Note that there are 38 unique gains ranging from 0.0455 to 0.55 (corresponding to attenuations from 1.8182 to 22) which can be achieved with the LT1997-2 using no external components.



DIFFERENCE AMPLIFIER CONFIGURATION



DIFFERENCE AMPLIFIER CONFIGURATION
IMPLEMENTED WITH THE LT1997-2, R_F = 25k, R_G = 100k, GAIN = 0.25

GAIN CAN BE ADJUSTED BY CROSS-COUPLING THE INPUTS.
MAKING THE DASHED CONNECTIONS REDUCES THE GAIN FROM 0.25 TO 0.15

Figure 5. Cross-Coupling of the LT1997-2 Allows Additional Gains to Be Constructed

Table 1. Difference Amplifier Gains (Attenuations)

GAIN	ATTENUATION	V_{+IN}	$V_{–IN}$	GND (REF)	OUT
0.0455	22	–INB, +INC	+INB, –INC	+INA	–INA
0.05	20	–INB, +INC	+INB, –INC		
0.0556	18	–INB, +INC	+INB, –INC	–INA	+INA
0.069	14.5	+INA	–INA	+INB, +INC	–INB, –INC
0.08	12.5	+INA	–INA	+INC	–INC
0.0833	12	+INA	–INA	+INB	–INB
0.0952	10.5	+INA	–INA	–INB, +INC	+INB, –INC
0.1	10	+INA	–INA		
0.1053	9.5	+INA	–INA	+INB, –INC	–INB, +INC
0.125	8	+INA	–INA	–INB	+INB
0.1333	7.5	+INA	–INA	–INC	+INC
0.1481	6.75	+INB	–INB	+INA, +INC	–INA, –INC
0.15	6.6667	–INA, +INC	+INA, –INC		
0.16	6.25	+INB	–INB	+INC	–INC
0.1739	5.75	+INB	–INB	–INA, +INC	+INA, –INC
0.1818	5.5	+INB	–INB	+INA	–INA
0.1875	5.3333	–INA, +INC	+INA, –INC	–INB	+INB
0.1923	5.2	+INC	–INC	+INA, +INB	–INA, –INB
0.2	5	+INB	–INB		
0.2083	4.8	+INC	–INC	+INB	–INB
0.2222	4.5	+INB	–INB	–INA	+INA
0.2273	4.4	+INC	–INC	+INA	–INA
0.24	4.1667	+INA, +INB	–INA, –INB	+INC	–INC
0.25	4	+INC	–INC		
0.2667	3.75	+INB	–INB	–INC	+INC
0.2778	3.6	+INC	–INC	–INA	+INA
0.2917	3.4286	+INA, +INC	–INA, –INC	+INB	–INB
0.3	3.3333	+INA, +INB	–INA, –INB		
0.3077	3.25	+INB	–INB	–INA, –INC	+INA, +INC
0.3125	3.2	+INC	–INC	–INB	+INB
0.35	2.8571	+INA, +INC	–INA, –INC		
0.3571	2.8	+INC	–INC	–INA, –INB	+INA, +INB
0.4	2.5	+INA, +INB	–INA, –INB	–INC	+INC
0.4091	2.4444	+INB, +INC	–INB, –INC	+INA	–INA
0.4375	2.2857	+INA, +INC	–INA, –INC	–INB	+INB
0.45	2.2222	+INB, +INC	–INB, –INC		
0.5	2	+INB, +INC	–INB, –INC	–INA	+INA
0.55	1.8182	+INA, +INB, +INC	–INA, –INB, –INC		

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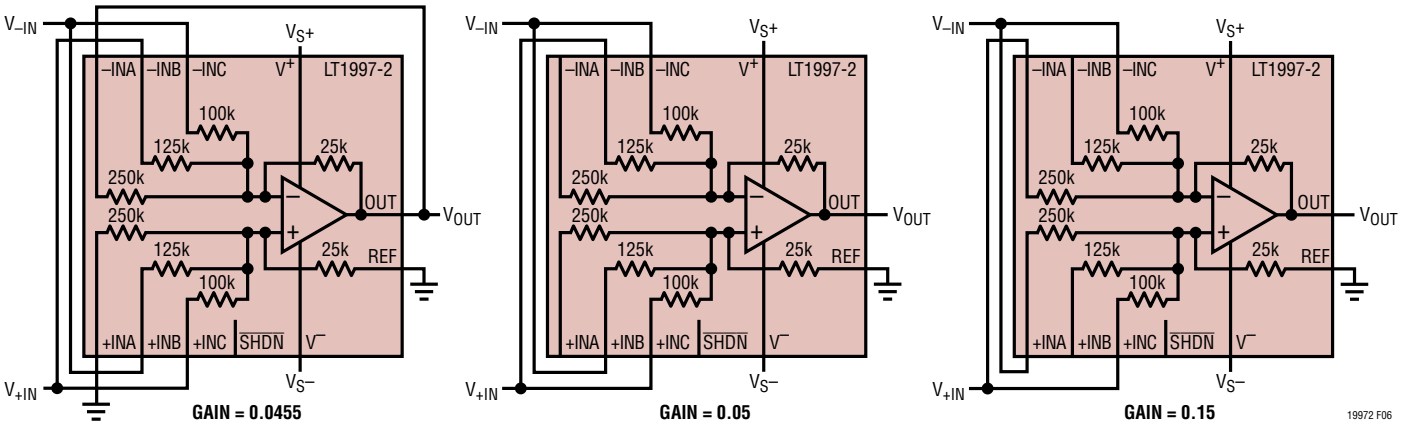

Figure 6. Examples of More Difference Amplifier Gains That Can Be Achieved

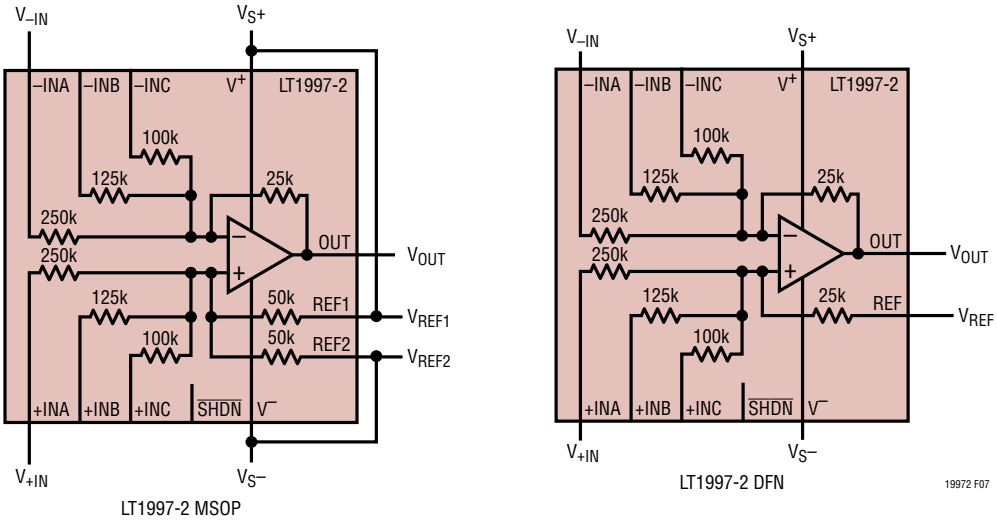

Figure 7. The LT1997-2 Reference Resistors: Split Resistors in the MSOP Package, Single Resistor in the DFN Package

Amplifiers for a Single-Ended Input

All of the difference amplifier configurations discussed in the preceding section can be used as noninverting or inverting amplifiers if the input is single-ended. For example, to achieve a positive attenuation for a single-ended input using the LT1997-2, simply ground $V_{–IN}$ and connect the input signal to V_{+IN}. Similarly, to achieve a negative attenuation for a single-ended input using the LT1997-2 , simply ground V_{+IN} and connect the input signal to $V_{–IN}$.

Reference Resistors

In the preceding discussions, the Reference resistor is shown as a single 25k resistor. This is true in the DFN package. In the MSOP package the reference resistor is split into two 50k resistors (Figure 7). Tying the REF1 and REF2 pins to the same voltage produces the same reference voltage as tying the V_{REF} pin in the DFN package to that voltage. Connecting REF1 and REF2 to different voltages produces an effective reference voltage that is the average of V_{REF1} and V_{REF2}. This feature is especially useful when the desired reference voltage is half way between the sup-

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plies. Tying REF1 to V_S+ and REF2 to V_S– produces the desired mid-supply voltage without the help of another external reference voltage (Figure 7). The ratio of R_{REF1} to R_{REF2} is very precise:

$$\frac{\Delta R}{R} = \left| \frac{R_{REF1} - R_{REF2}}{\left(\frac{R_{REF1} + R_{REF2}}{2} \right)} \right| < 90\text{ppm}$$

Shutdown

The LT1997-2 has a shutdown pin ($\overline{SHDN}$). Under normal operation this pin should be tied to V^+ or allowed to float. Tying this pin 2.5V or more below V^+ will cause the part to enter a low power state. The supply current is reduced to less than 25µA and the op amp output becomes high impedance. The voltages at the input pins can still be present even in shutdown mode.

Supply Voltage

The positive supply pin of the LT1997-2 should be bypassed with a small capacitor (typically 0.1µF) as close to the supply pins as possible. When driving heavy loads, an additional 4.7µF electrolytic capacitor should be added. When using split supplies, the same is true for the $V^–$ supply pin.

Output

The output of the LT1997-2 can typically swing to within 50mV of either rail with no load and is capable of sourcing and sinking approximately 30mA at 25°C. The LT1997-2 is internally compensated to drive at least 0.5nF of capacitance under any output loading conditions. For larger capacitive loads, a 0.22µF capacitor in series with a 150Ω resistor between the output and ground will compensate the amplifier to drive capacitive loads greater than 0.5nF.

Distortion

The LT1997-2 features excellent distortion performance when the internal op amp is operating in the normal operating region. Operating the LT1997-2 with the internal op amp in the over the top region will increase distortion due to the lower loop gain of the op amp. Operating the LT1997-2 with input common mode voltages that go from the normal to Over-The-Top operation will significantly degrade the LT1997-2's linearity as the op amp must transition between two different input stages. Driving resistive loads significantly smaller than the 25k internal feedback resistor will also degrade the amplifier's linearity performance.

High Voltage Pin Spacing

For applications with very high input voltages, the LT1997-2 pinout eases the printed circuit board (PCB) layout burden. Voltages at +INA, –INA, +INB, and –INB input pins are separated from other pins by virtue of unpopulated pin locations, as illustrated in the Pin Configuration section of this data sheet.

Power Dissipation Considerations

Because of the ability of the LT1997-2 to operate on power supplies up to ±25V, to withstand very high input voltages and to drive heavy loads, there is a need to ensure the die junction temperature does not exceed 150°C. The LT1997-2 is housed in DF14 (θ_{JA} = 45°C/W, θ_{JC} = 3°C/W) and MS16 (θ_{JA} = 130°C/W) packages.

In general, the die junction temperature (T_J) can be estimated from the ambient temperature (T_A), the device's power dissipation (P_D) and the thermal resistance of the device and board (θ_{JA}).

$$T_J = T_A + P_D \bullet \theta_{JA}$$

The thermal resistance from the junction to the ambient environment (θ_{JA}) is the sum of the thermal resistance from the junction to the exposed pad (θ_{JC}) and the thermal resistance from the exposed pad to the ambient environment (θ_{CA}). The θ_{CA} value depends on how much PCB metal is connected to the exposed pad in the board. The more PCB metal that is used, the lower θ_{CA} and θ_{JA} will be.

Power is dissipated by the amplifier's quiescent current, by the output current driving a resistive load, and by the input current driving the LT1997-2's internal resistor network.

$$P_D = \left(\left(V_S+ - V_S- \right) \bullet I_S \right) + P_{OD} + P_{RESD}$$

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For a given supply voltage, the worst-case output power dissipation $P_{OD(MAX)}$ occurs with the output voltage at half of either supply voltage. $P_{OD(MAX)}$ is given by:

$$P_{OD(MAX)} = \frac{(V_S/2)^2}{R_{LOAD}}$$

The power dissipated in the internal resistors (P_{RESD}) depends on the manner the input resistors have been configured as well as the input voltage, the output voltage and the voltage on the REF pin. The following equations and Figure 8 show the different components of P_{RESD} corresponding to the different groups of the LT1997-2's internal resistors, assuming that the LT1997-2 is used with a dual supply configuration with REF pin at ground (refer to Figure 3 for resistor terminologies used in equations below).

$$P_{RESDA} = \frac{(V_{+IN})^2}{R_G + R_F}$$

$$P_{RESDB} = \frac{\left(V_{-IN} - V_{+IN} \bullet \frac{R_F}{R_G + R_F}\right)^2}{R_G}$$

$$P_{RESDC} = \frac{\left(V_{+IN} \bullet \frac{R_F}{R_G + R_F} - V_{OUT}\right)^2}{R_F}$$

$$P_{RESD} = P_{RESDA} + P_{RESDB} + P_{RESDC}$$

In general, P_{RESD} increases with higher input voltage and lower output and REF pin voltages.

Example: For an LT1997-2 in a DFN package mounted on a PC board with a thermal resistance of 45°C/W, operating on ±25V supplies and driving a 2.5kΩ load to 12.5V with V_{+IN} = 255V and REF = 0V, the total power dissipation is given by:

$$P_D = (50 \bullet 0.6mA) + \frac{12.5^2}{2.5k} + \frac{255^2}{275k} + \frac{\left(130 - \frac{255}{11}\right)^2}{250k} + \frac{\left(\frac{255}{11} - 12.5\right)^2}{25k}$$

$$= 0.38W$$

Assuming a thermal resistance of 45°C/W, the die temperature will experience an 17°C rise above ambient. This implies that the maximum ambient temperature the LT1997-2 should operate under the above conditions is:

T_A = 150°C – 17°C = 133°C

It is recommended that the exposed pad of the DFN package have as much PCB metal connected to it as reasonably available. The more PCB metal connected to the exposed

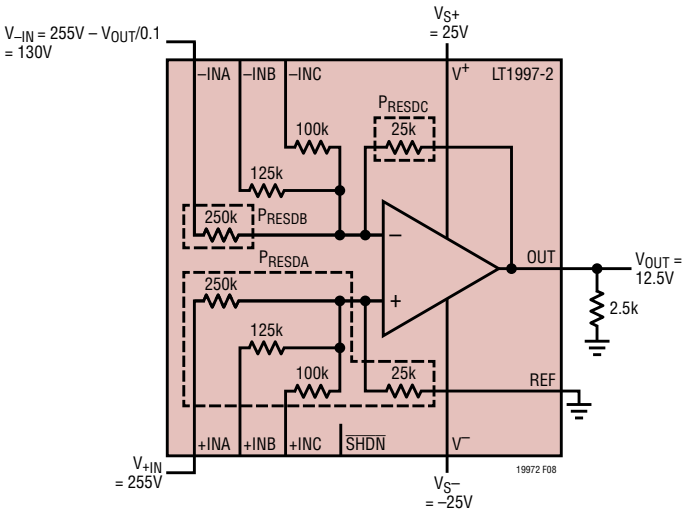

Figure 8. Power Dissipation Example

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pad, the lower the thermal resistance. Connecting a large amount of PCB metal to the exposed pad can reduce the θ_{JA} to even less than 45°C/W. Use multiple vias from the exposed pad to the V^- plane. The exposed pad is electrically connected to the V^- pin. In addition, a heat sink may be necessary if operating near maximum junction temperature.

The MSOP package has no exposed pad and a higher thermal resistance (θ_{JA} = 130°C/W). It should not be used in applications which have a high ambient temperature, require driving a heavy load, or require an extreme input voltage.

Thermal Shutdown

For safety, the LT1997-2 will enter shutdown mode when the die temperature rises to approximately 163°C. This thermal shutdown has approximately 9°C of hysteresis requiring the die temperature to cool 9°C before enabling the amplifier again.

ESD Protection

The LT1997-2 is protected by a number of ESD structures. The structures are shown in Figure 9.

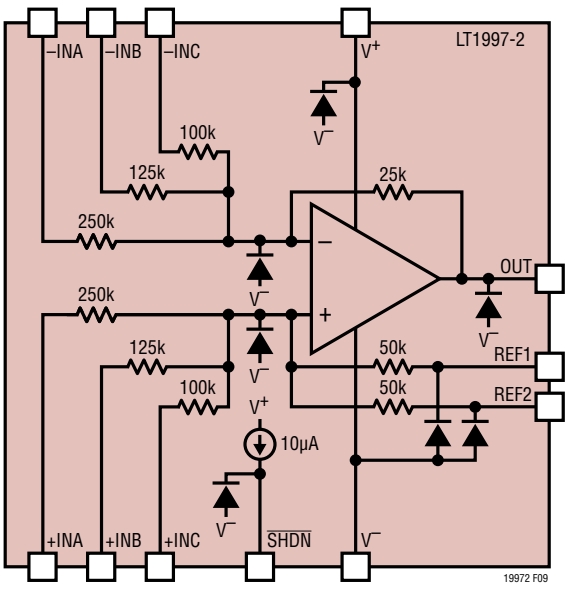


Figure 9. ESD Protection

The ESD structures serve to protect the internal circuitry but also limit signal swing on certain nodes. The structures on the internal op amp inputs limit the voltage on these nodes to 0.3V below V^- and 80V above V^-. The voltage on the REF (DFN), REF1 (MSOP) and REF2 (MSOP) pins are limited to 0.3V below V^- and 60V above V^-. The voltage on the $\overline{SHDN}$ pin is limited to 0.3V below V^- and 0.3V above V^+.

Direct Line Voltage Measurement

Since the LT1997-2 can withstand up to ±255V at its input pins, configurations with the highest attenuation factors allow for direct sensing of the 60Hz, 120VAC line voltage. The circuit shown in Figure 10 directly measures the line and neutral signals. The ground of the circuit can reasonably connect to earth ground. The neutral voltage level will typically hover near earth. The ability of the LT1997-2 to sense high voltages with varying common mode levels enables this extremely simple implementation.

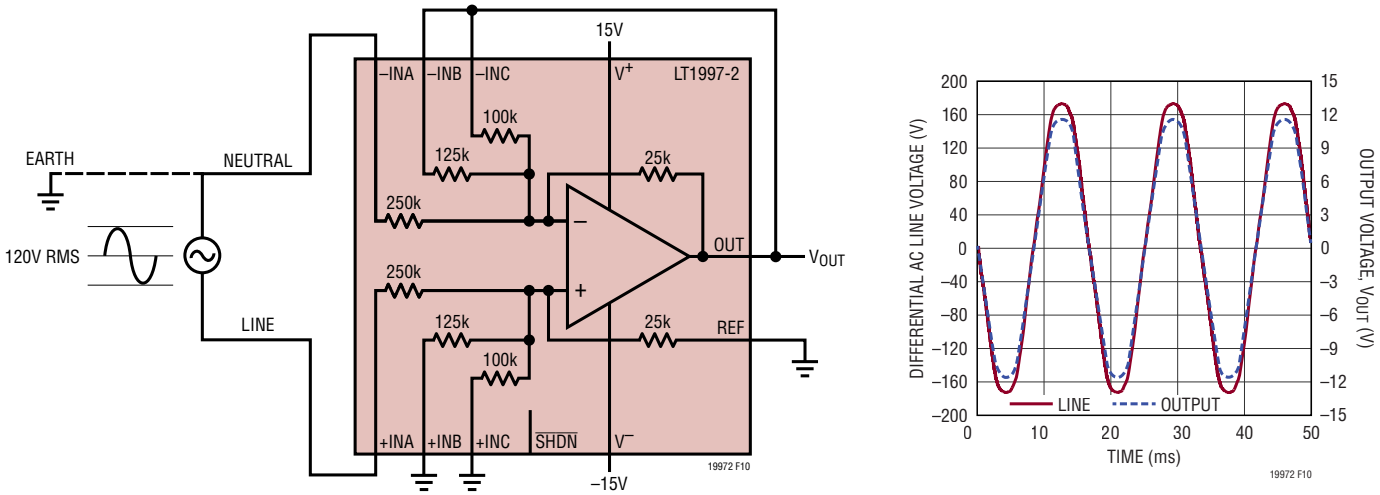
High Side Large Voltage Measurement

In some applications, an electrical potential develops relative to a high line voltage. As an example, some LED current control power conversion topologies place the LED at the high voltage. Even more interestingly, the high line may be moving. Off-line LED conversion such as in modern light bulbs sometimes use LEDs pegged to the rectified line voltage.

The circuit in Figure 11 uses the LT3590 to control LED current. A LT1997-2 configured for a gain of 0.08V/V can enable detection of an LED open circuit fault condition. With the LED open circuited, the voltage across the LED (which is being sensed by the LT1997-2) rises, and at 41.25V the LT1997-2 output rises above 3.3V, indicating a fault condition.

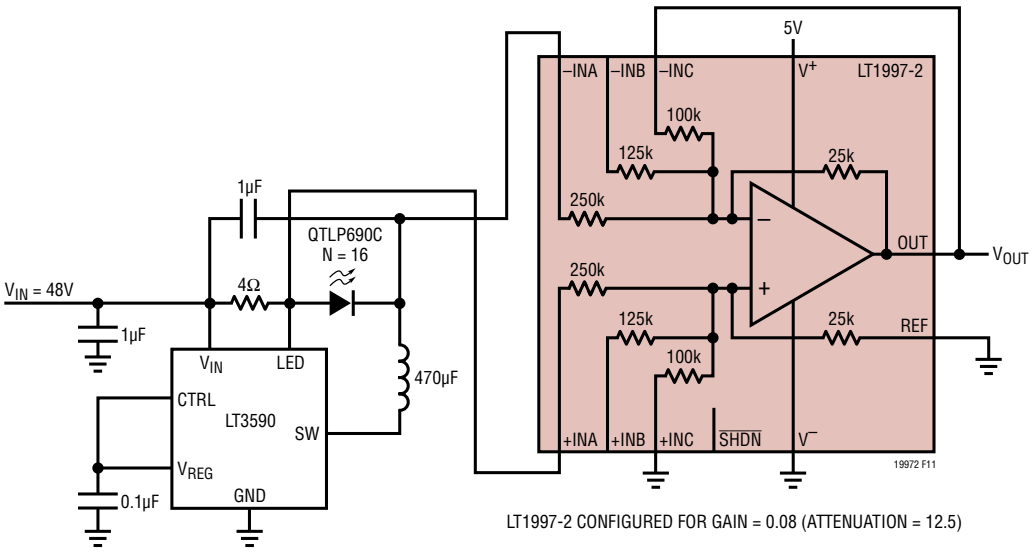
A large voltage referred to the rectified AC mains can be attenuated and shifted to a system's low voltage circuitry. Figure 12 shows this kind of function. Off-line LED lighting that employs nonisolated buck power conversion is one such example.

APPLICATIONS INFORMATION



LT1997-2 CONFIGURED FOR GAIN = 0.069 (ATTENUATION = 14.5)

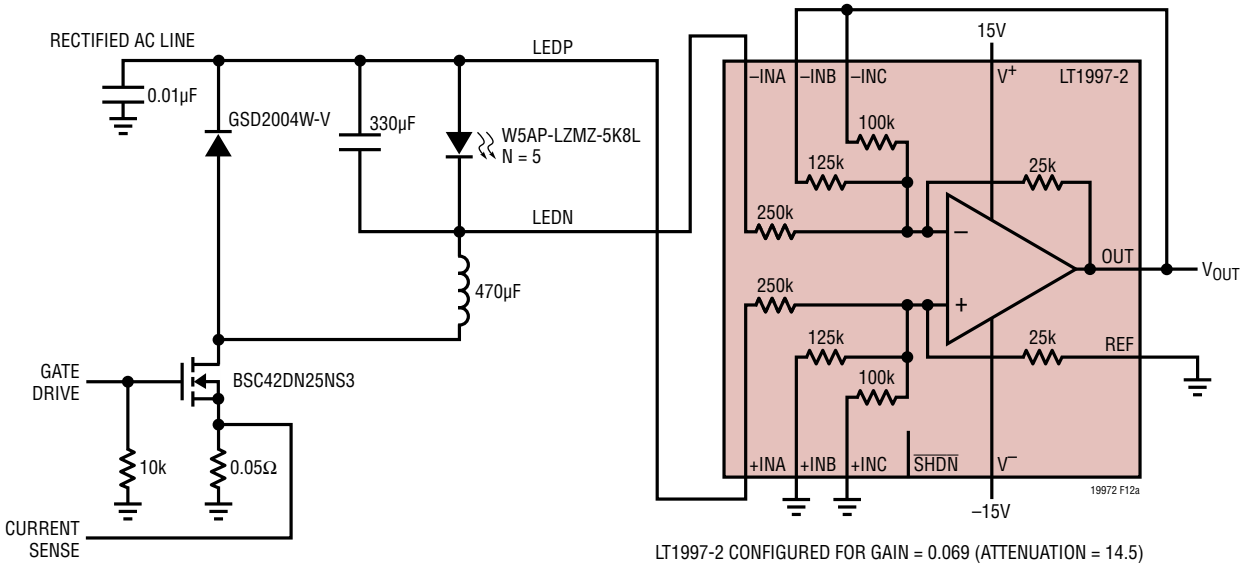
Figure 10. Direct Line Voltage (120VAC, 60Hz) Measurement



LT1997-2 CONFIGURED FOR GAIN = 0.08 (ATTENUATION = 12.5)

Figure 11. Detection of an LED Open Circuit Fault Condition

APPLICATIONS INFORMATION



LT1997-2 CONFIGURED FOR GAIN = 0.069 (ATTENUATION = 14.5)

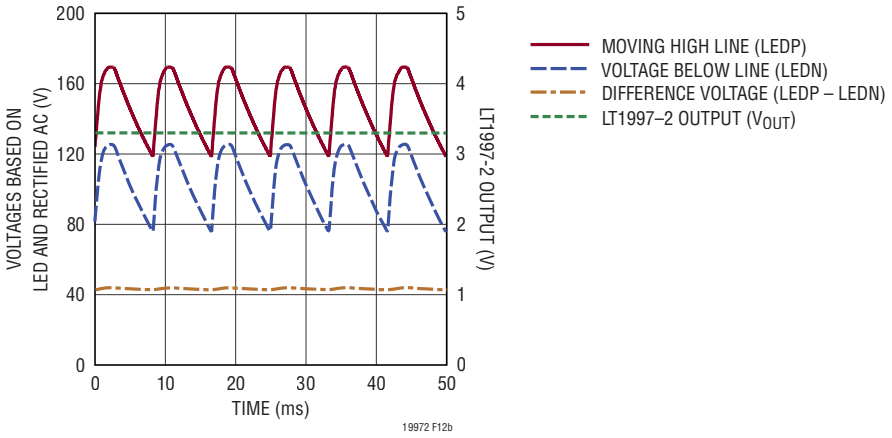
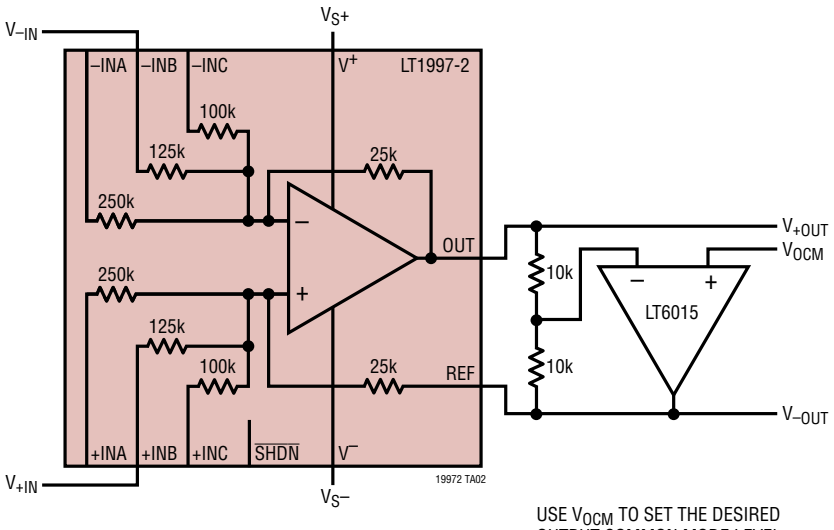


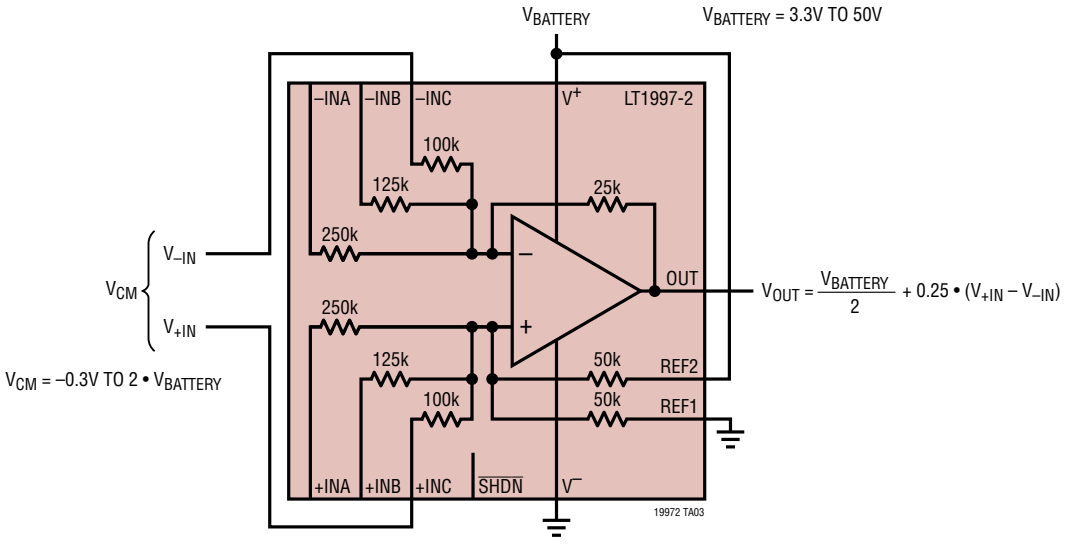
Figure 12. LED Common Mode Swings Relative to Rectified AC

TYPICAL APPLICATIONS

LT1997-2 Configured for Differential Output with Gain = 0.2

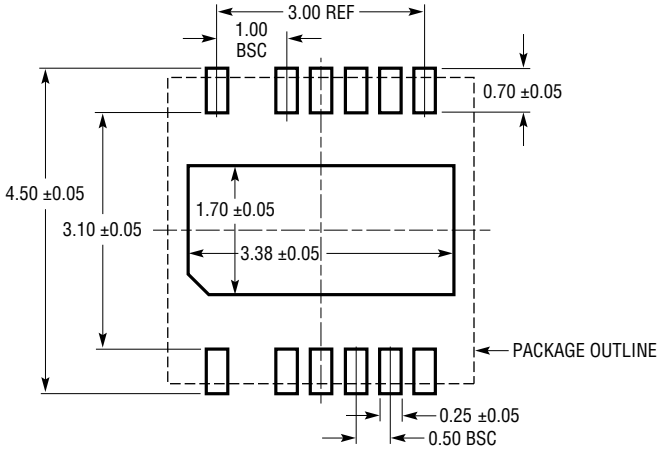


Precision Over-The-Top Single-Supply Funnel Amplifier

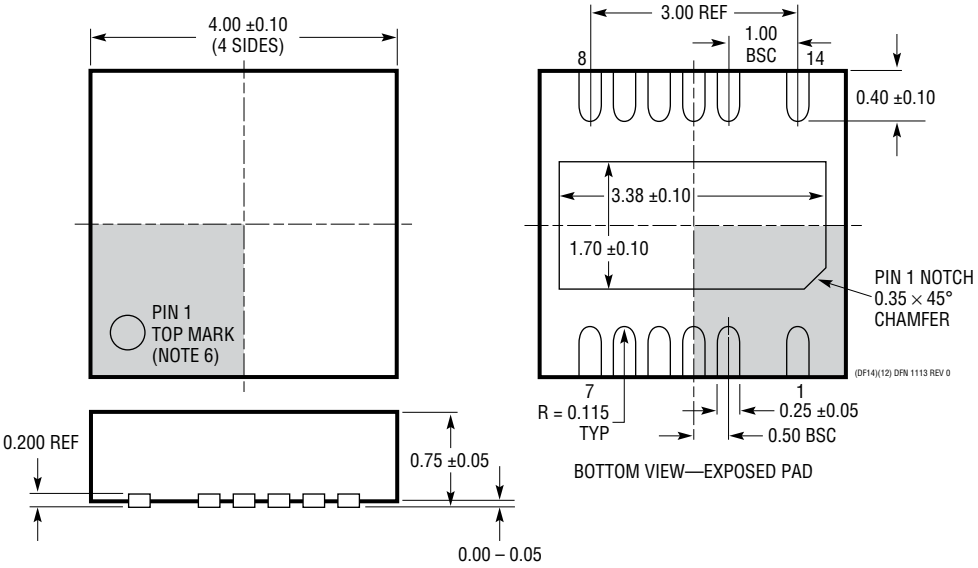


PACKAGE DESCRIPTION

DF Package
14(12)-Lead Plastic DFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1963 Rev Ø)



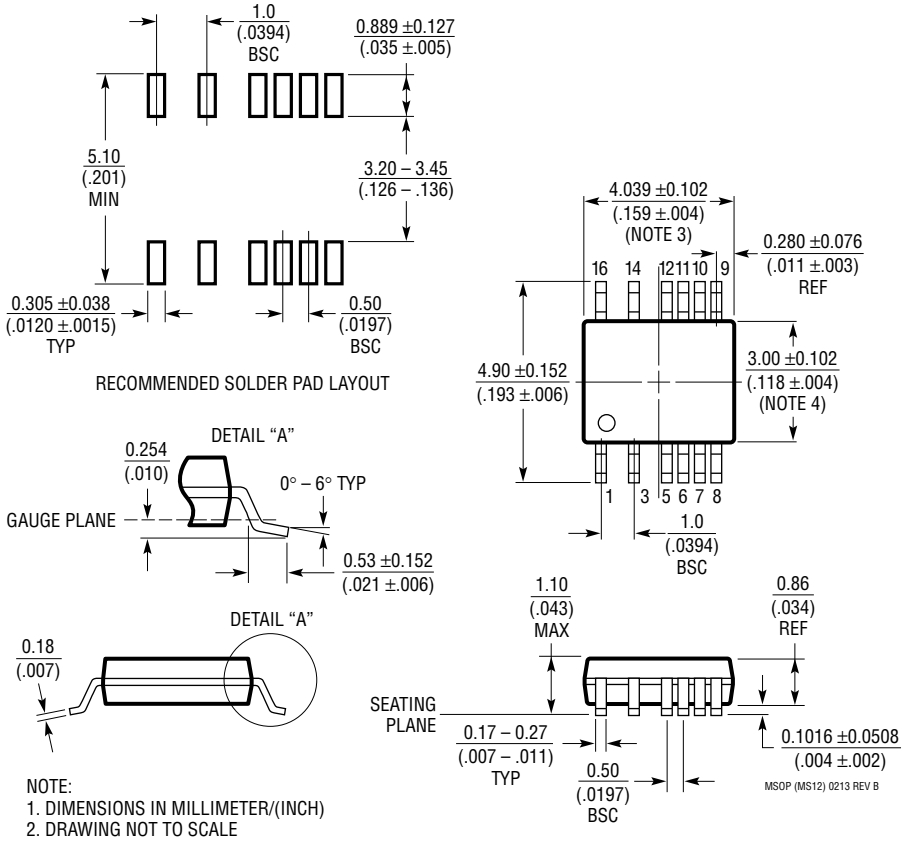
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. PACKAGE OUTLINE DOES NOT CONFORM TO JEDEC MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS Package
16 (12)-Lead Plastic MSOP with 4 Pins Removed
(Reference LTC DWG # 05-08-1847 Rev B)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX